THE DATASHEET OF

CA91L862A-50ILV

QSpan II™ Device Errata

8091862_ER001_04

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6024 Silver Creek Valley Road San Jose, California 95138

Telephone: (408) 284-8200 • FAX: (408) 284-3572

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About this Document

This document describes device errata for the QSpan II, part number CA91L862A.

Revision History

8091862_ER001_04, October 2009

This version of the document was rebranded as IDT. It does not include any technical changes.

8091862_ER001_03, February 2006

This document was revised to include a new device errata, “3. EEPROM contents corrupted during load under reset conditions” on page 5.

8091862_ER001_02, January 2004

8091862_ER001_01, April 2001

Device Errata

Errata
“1. Retry Counter (MAX_RTRY) during Configurations Writes” on page 4
“2. Incorrect Response During PCI Configuration Cycles with I2O_BAR” on page 4
“3. EEPROM contents corrupted during load under reset conditions” on page 5

1. Retry Counter (MAX_RTRY) during Configurations Writes

Description

When the QSpan II performs a configuration write on the PCI bus, if the MAX_RTRY bits of the MISC_CTL2 register (0x808) are set to 01, 10, or 11 (128 retries, 256 retries, and 384 retries, respectively), the QSpan II does not stop generating configuration write cycles at the programmed MAX_RTRY count limit. The QSpan II will continually re-issue the configuration cycle until the cycle is completed.

Work Around

Do not use MAX_RTRY while performing a configuration write on the PCI bus.

2. Incorrect Response During PCI Configuration Cycles with I2O_BAR

Description

If an external agent is performing PCI configuration cycles to another PCI device, and the base address programmed in the I2O Base Address Register (I2O_BAR) of the QSpan II matches the PCI configuration address (such as AD[31:16]), then the QSpan II incorrectly responds to that cycle.

The following conditions need to occur for the errata to be present:

- The QSpan II must be configured by either a EEPROM, or the PCI_DIS pin is sampled high upon the device coming out of reset.
- The QSpan II must be enabled for the use of the I2O Messaging Unit; that is, the I2O_EN bit must be set in the I2O Control and Status Register (offset 0x200).
- The BA field of the I2O Base Address Register (offset 0x10) is written where only 1 bit BA[31:16] is high.

For example, if the QSpan II IDSEL signal is connected to AD[31] of the PCI bus and the I2O_BAR is programmed as 0x1000_0000, then the QSpan II responds correctly to the configuration cycle when AD[31] is toggled high. However, the QSpan II will respond incorrectly to the configuration cycle when AD[28] is high, which corresponds to the address programmed in the I2O_BAR register.

Workaround

Ensure the value programmed in the I2O_BAR register does not match a valid PCI configuration address AD[31:16]. This is done by making sure that more than one bit in the I2O_BAR BA[31:16] field is programmed to a 1.

3. EEPROM contents corrupted during load under reset conditions

Description

When the QSpan II is reading from EEPROM at power-up and a reset occurs, an inadvertent write to the EEPROM could take place and corrupt its contents.

Workaround

This issue is not applicable to designs that will never have a reset condition occur during the initial EEPROM load. For designs that could have a reset condition during the EEPROM load, this problem can be avoided by using a write-protected EEPROM.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: EHBhelp@idt.com
phone: 408-360-1538
document: 8091862_ER001_04

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