THE DATASHEET OF

EVAL-ADN4650EBZ

ANALOG DEVICES

EVAL-ADN4650EB1Z User Guide
UG-933

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Evaluating the ADN4650 5 kV rms, 600 Mbps LVDS Isolator (SOIC_W)

FEATURES

Isolated ground planes (logic side and bus side)
Convenient connections through SMA terminals
- **3.3 V/2.5 V power on Side 1 (V_{IN1}/V_{DD1}) and Side 2 (V_{IN2}/V_{DD2})**
- **Ground on Side 1 (GND_1) and Side 2 (GND_2)**
- **LVDS input signals: D_{IN1+}, D_{IN1-}, D_{IN2+}, D_{IN2-}**
- **LVDS output signals: D_{OUT1+}, D_{OUT1-}, D_{OUT2+}, D_{OUT2-}**

Jumper-selectable supply power of 3.3 V or 2.5 V
Termination resistors on all LVDS drivers/receivers

EVALUATION KIT CONTENTS

EVAL-ADN4650EB1Z evaluation board

DOCUMENTS NEEDED

ADN4650 data sheet

EQUIPMENT NEEDED

Signal generator
Oscilloscope

GENERAL DESCRIPTION

The EVAL-ADN4650EB1Z allows quick and easy evaluation of the ADN4650 low-voltage differential signalling (LVDS) isolator without the need for external components. The ADN4650 employs Analog Devices, Inc., *i*Coupler® technology to combine a 2-channel isolator with an LVDS receiver and driver into a single, 20-lead wide body SOIC package. The ADN4650 is capable of running at data rates of up to 600 Mbps with very low jitter.

The evaluation board has separate ground and power planes for each side of the isolator. This separation enables the evaluation of the ADN4650 with galvanic isolation between both sides of the device. Jumper-selectable power supplies at 3.3 V or 2.5 V are required on each side of the ADN4650. An on-chip LDO can provide 2.5 V using an external 3.3 V power supply.

Complete information about the ADN4650 is available in the ADN4650 data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

EVAL-ADN4650EB1Z EVALUATION BOARD

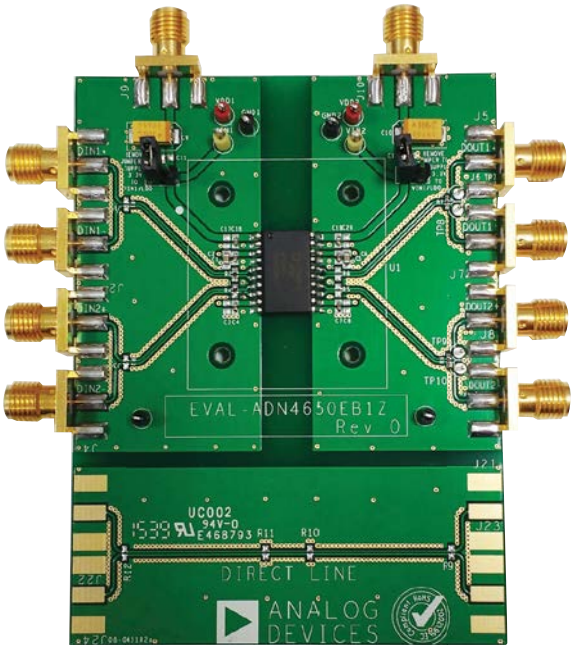

Figure 1.

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REVISION HISTORY

4/16—Revision 0: Initial Version

EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

On the EVAL-ADN4650EB1Z, the power supplies are configured using Jumpers P4 and P7 (see Table 1) and are connected to the J9 and J10 SMA connectors (see Table 2 and Table 3). A 3.3 V power supply can be applied to Side 1 and/or Side 2 of the ADN4650 by removing Jumpers P4 (Side 1) and P7 (Side 2). If a 2.5 V power supply is connected, insert the relevant jumper must (P4 for Side 1 and P7 for Side 2). At 300 MHz with a load resistance of 100 Ω, the maximum operating current from each power supply is 72 mA.

When using a 3.3 V power supply, V_{IN1} and V_{DD1} (Pin 1 and Pin 3 on the ADN4650) are bypassed to GND_1 on the board using 1 µF capacitors (C18 and C2, respectively). V_{IN2} and V_{DD2} (Pin 20 and Pin 18 on the ADN4650) are bypassed to GND_2 on the board using 1 µF capacitors (C19 and C6, respectively). When using a 2.5 V power supply, V_{IN1} or V_{IN2} connects directly to V_{DD1} or V_{DD2} by shorting Jumpers P4 or P7, respectively. Both V_{DD1} pins are also bypassed to GND_1 with 0.1 µF capacitors (C1 and C4). Both V_{DD2} pins are also bypassed to GND_2 with 0.1 µF capacitors (C5and C7).

Figure 4 shows an example operation of the EVAL-ADN4650EB1Z. SMA connectors expose all LVDS inputs and outputs (see Table 2 and Table 3). Connect a signal generator using the J1 and J2 connectors and set up a 300 MHz square wave clock with an amplitude of 350 mV and an offset of 1.2 V. Connect the oscilloscope directly to the J5 and J6 connectors to perform timing measurements including propagation delay and skew. Precision measurements, for example, jitter, using a differential probe requires attaching the probe at the TP7 and TP8 test points (or TP9 and TP10 for Isolator Channel 2) and potentially cutting the traces to the connectors to minimize reflections.

Figure 2 shows a plot of the oscilloscope connected via the J5 and J6 connectors. Oscilloscope Channel 3 (green) and Channel 4 (purple) show the J5 and J6 connectors separately (single-ended) with the differential signal (orange).

Figure 3 shows an operation of the second isolated LVDS channel. In contrast to Figure 2, the signal generator connects via the J3 and J4 connectors and the oscilloscope connects to the J7 and J8 connectors. Oscilloscope Channel 3 (green) and Channel 4 (purple) show the J7 and J8 connectors separately (single-ended) with the differential signal (orange).

Figure 2. D_{OUT1-} and D_{OUT1+} with a 300 MHz Clock, Single-Ended and Differential

Figure 3. D_{OUT2-} and D_{OUT2+} with a 300 MHz Clock, Single-Ended and Differential

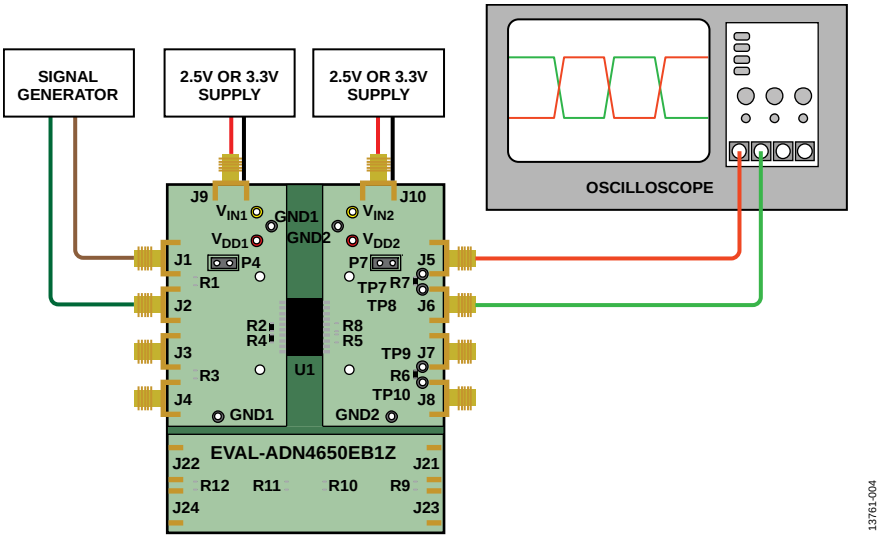

Figure 4. Basic LVDS Isolator Evaluation Board Operation

Table 1. Jumper Configuration

Jumper	Position	Description
P4	Open	3.3 V power supply connected to Connector J9 for V_{IN1}
	Closed	2.5 V power supply connected to Connector J9, V_{IN1} shorted to V_{DD1}
P7	Open	3.3 V power supply connected to Connector J9 for V_{IN2}
	Closed	2.5 V power supply connected to Connector J9, V_{IN2} shorted to V_{DD2}

Table 2. Side 1 Connector Descriptions

Connector	Description
J9	Power supply, 3.3 V (Jumper P4 open) or 2.5 V (Jumper P4 closed)
J1	D_{IN1+}, noninverted LVDS input for Isolator Channel 1
J2	D_{IN1-}, inverted LVDS input for Isolator Channel 1
J3	D_{IN2+}, noninverted LVDS input for Isolator Channel 2
J4	D_{IN2-}, inverted LVDS input for Isolator Channel 2
J22	Connects to Connector J21 (test trace for calibration)
J24	Connects to Connector J23 (test trace for calibration)

Table 3. Side 2 Connector Descriptions

Connector	Description
J10	Power supply, 3.3 V (Jumper P7 open) or 2.5 V (Jumper P7 closed)
J5	D_{OUT1+}, noninverted LVDS output for Isolator Channel 1
J6	D_{OUT1-}, inverted LVDS output for Isolator Channel 1
J7	D_{OUT2+}, noninverted LVDS output for Isolator Channel 2
J8	D_{OUT2-}, inverted LVDS output for Isolator Channel 2
J21	Connects to Connector J22 (test trace for calibration)
J23	Connects to Connector J24 (test trace for calibration)

RADIATED EMISSIONS TEST RESULTS (EN 55022)

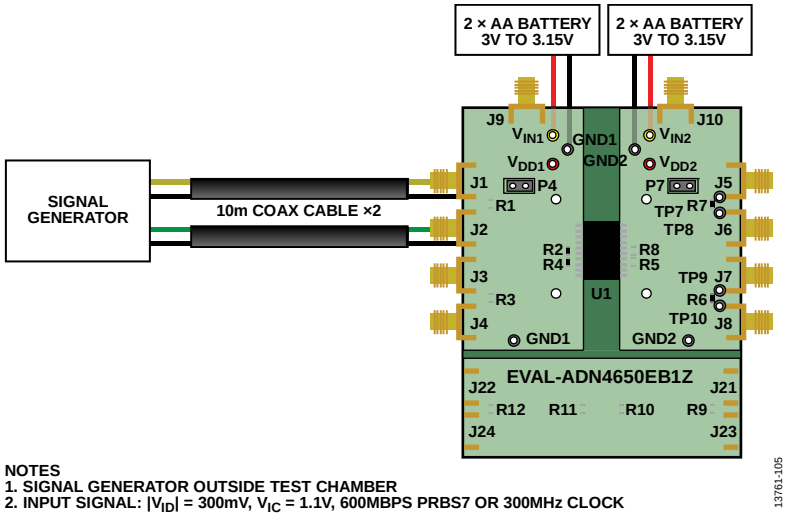

Figure 5. Test Setup for EN 55022 Radiated Emissions Testing

Radiated emissions testing is performed at an independent external test facility with the EVAL-ADN4650EB1Z. Evaluating the EVAL-ADN4650EB1Z to the EN 55022 standard is undertaken in a 10 m radiated emissions test chamber using the test setup shown in Figure 5. The setup comprises a battery-powered EVAL-ADN4650EB1Z connected to a signal generator located outside the chamber via coaxial cables. As specified by the EN 55022 standard, both horizontal and vertical peak scans are undertaken with any visible emissions peaks investigated using quasi-peak detector measurement. For each frequency measured using a quasi-peak detector, the device under test rotates through 360 degrees to find the worst case angle. The receiving antenna then elevates from 1 m to 4 m in height to find the worst case elevation. The worst case quasi-peak measurements are compared to the EN 55022 Class B and Class A limits.

The test results are shown in Table 4; a classification report is available on request (please contact Analog Devices or the component distributor for support). Radiated emissions are measured across 30 MHz to 1 GHz and from 1 GHz to 3 GHz.

With a 600 Mbps PRBS7 input, the EVAL-ADN4650EB1Z passes the EN 55022 Class B limits.

With a 300 MHz clock input, the EVAL-ADN4650EB1Z passes the EN 55022 Class A limits. To pass the Class B limits when isolating high frequency clocks, reduce the printed circuit board (PCB) clearance from the 8 mm implemented on EVAL-ADN4650EB1Z to, for example, 2 mm.

Table 4. EN 55022 Radiated Emissions Classification

Test Condition	Result
600 Mbps PRBS7	Passes EN 55022 Class B
300 MHz Clock	Passes EN 55022 Class A

EVALUATION BOARD SCHEMATIC AND ARTWORK

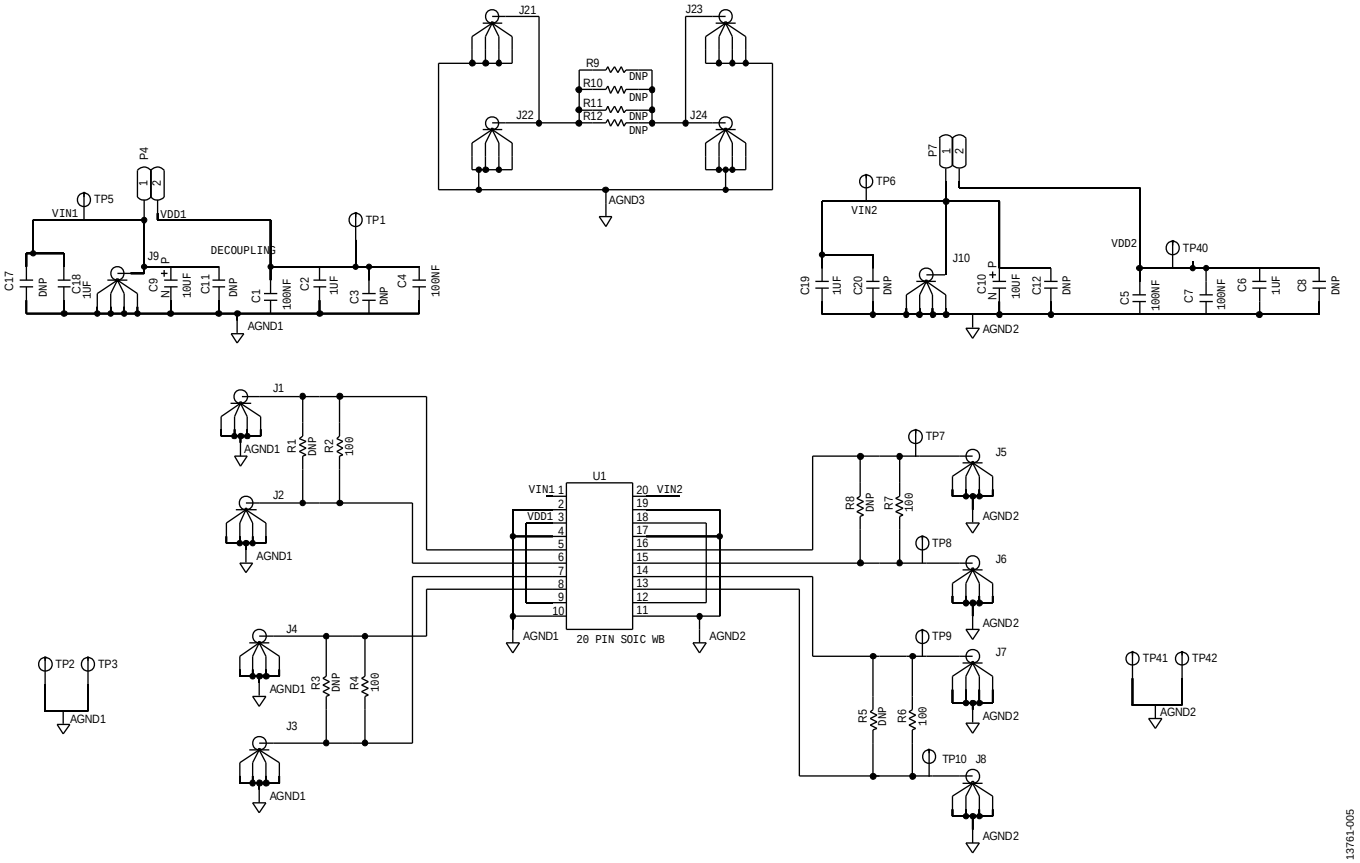

Figure 6. EVAL-ADN4650EB1Z Schematic

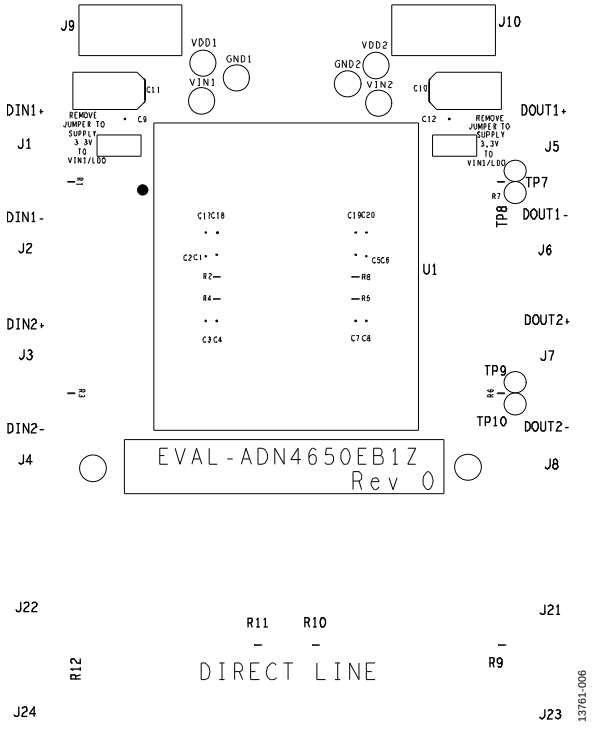

Figure 7. EVAL-ADN4650EB1Z Silkscreen

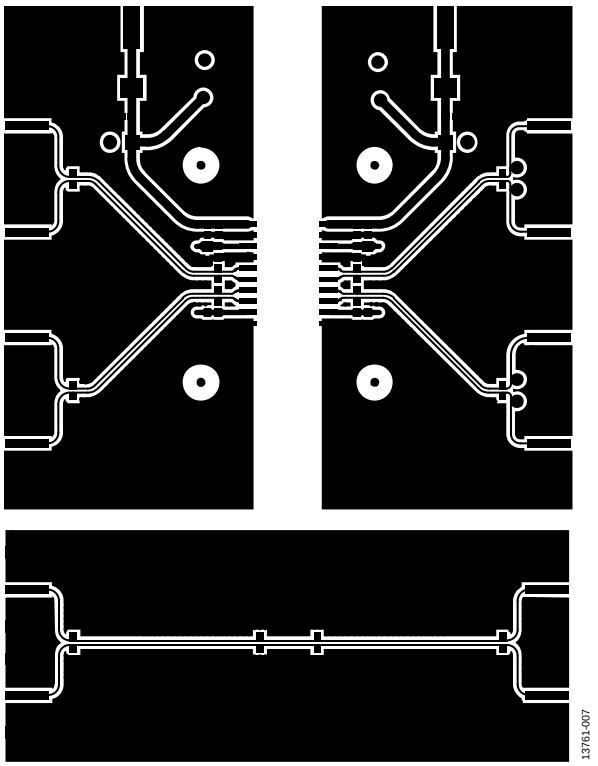

Figure 8. EVAL-ADN4650EB1Z Component Side

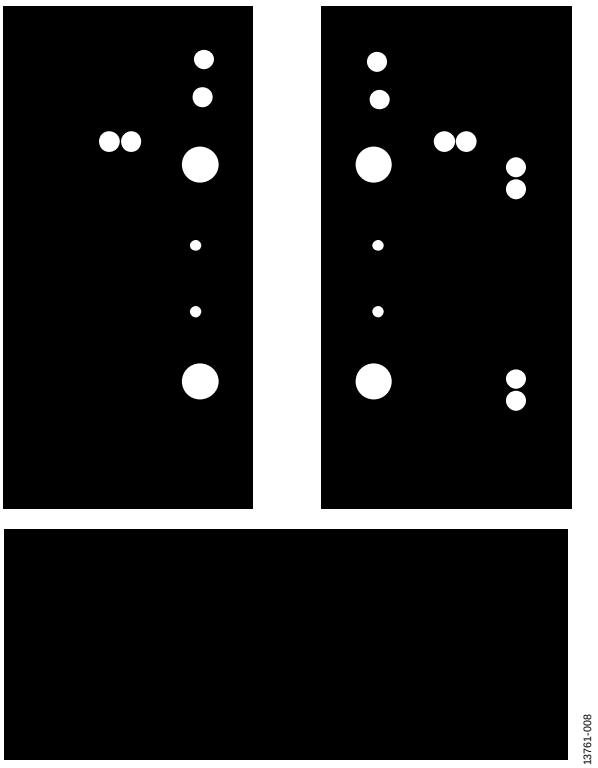

Figure 9. EVAL-ADN4650EB1Z Inner Layer 2, Ground

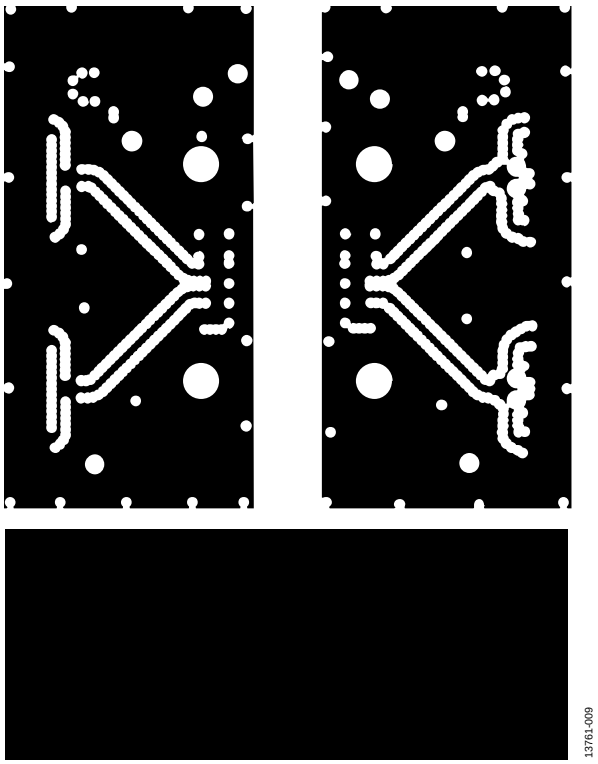

Figure 10. EVAL-ADN4650EB1Z Inner Layer 3, Power

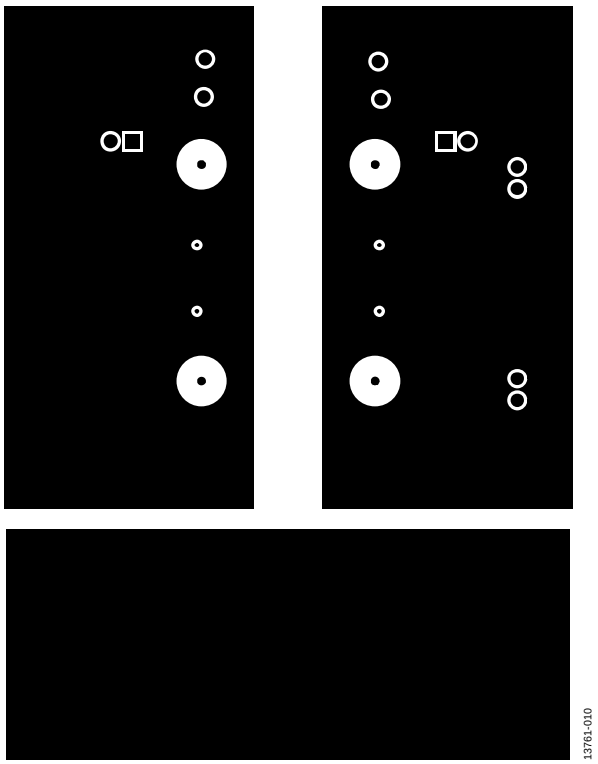

Figure 11. EVAL-ADN4650EB1Z Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 5.

Qty.	Reference Designator	Description	Manufacturer	Part Number
4	C1, C4, C5, C7	Capacitor, 100 nF, 0402	Multicomp	MC0402X104K100CT
2	C2, C6	Capacitor, 1 µF, 0603	Multicomp	MC0603X105K100CT
4	C3, C8, C11, C12, C17, C20	Capacitor, 0402	Not fitted	Not applicable
2	C9, C10	Capacitor, tantalum, 10 µF, Case C	AVX	TAJC106K016RNJ
2	C18, C19	Capacitor, 1 µF, 0402	Multicomp	MC0402X105K6R3CT
10	J1 to J10	Connector, SMA, edge	Johnson	142-0701-801
4	J21 to J24	Connector, SMA, edge	Not fitted	Not applicable
2	P4, P7	2-pin header and jumper	TE Connectivity	826926-2 and 3M/969102-0000-DA)
8	R1, R4, R6, R8 to R12	Resistor, 0402	Not fitted	Not applicable
4	R2, R3, R5, R7	Resistor, 100 Ω, 0402	Multicomp	MCMR04X1000FTL
2	TP1/VDD1, TP40/VDD2	Test point, yellow	Vero	20-313140
4	TP2, TP3, TP41, TP42	Test point, black	Vero	20-2137
2	TP5/VIN1, TP6/VIN2	Test point, red	Vero	20-313137
4	TP7, TP8, TP9, TP10	Test point, pin, silver	Oxley	028/30P/LA/KP2 SILVER
1	U1	ADN4650 5 kV rms, 600 Mbps, LVDS isolator	Analog Devices	ADN4650BRWZ

RELATED LINKS

Resource	Description
ADN4650	Product page, ADN4650, 5 kV rms, 600 Mbps, dual Tx or Rx channel, LVDS isolator

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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