THE DATASHEET OF

MT46H64M32L2JG-5:A

Mobile LPDDR

168-Ball Package-on-Package (PoP) TI OMAP™

MT46HxxxMxxLxJG

Features

- Vdd/Vddq = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; 2 data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- 4 internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths (BL): 2, 4, 8, or 16[1]
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- STATUS READ REGISTER (SRR) supported[2]
- Selectable output drive strength
- Clock stop capability
- 64ms refresh

Options	Marking
• Vdd/Vddq	
– 1.8V/1.8V	H
• Configuration	
– 128 Meg x 16 (32 Meg x 16 x 4 banks)	128M16
– 64 Meg x 32 (16 Meg x 32 x 4 banks)	64M32
– 64 Meg x 16 (16 Meg x 16 x 4 banks)	64M16
– 32 Meg x 32 (8 Meg x 32 x 4 banks)	32M32
• Device version	
– Single die, standard addressing	LF
– 2-die stack, standard addressing	L2
• Plastic “green” package	
– 168-ball VFBGA (12mm x 12mm)	JG
• Timing – cycle time	
– 5ns @ CL = 3	-5
– 5.4ns @ CL = 3	-54
– 6ns @ CL = 3	-6
• Operating temperature range	
– Commercial (0° to +70°C)	None
– Industrial (–40°C to +85°C)	IT

Notes: 1. Contact factory for availability.
2. Contact factory for remapped SRR output.

Table 1: Configuration Addressing

Architecture	128 Meg x 16	64 Meg x 32	64 Meg x 16	32 Meg x 32
Configuration	32 Meg x 16 x 4 banks	16 Meg x 32 x 4 banks	16 Meg x 16 x 4 banks	8 Meg x 32 x 4 banks
Refresh count	8K	8K	8K	8K
Row addressing	16K (A[13:0])	8K (A[12:0])	16K (A[13:0])	8K (A[12:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])

Part Numbering Information - 168-Ball PoP

Micron® 168-ball packaged LPDDR-SDRAM devices are available in several configurations.

Figure 1: 168-Ball Part Number Chart

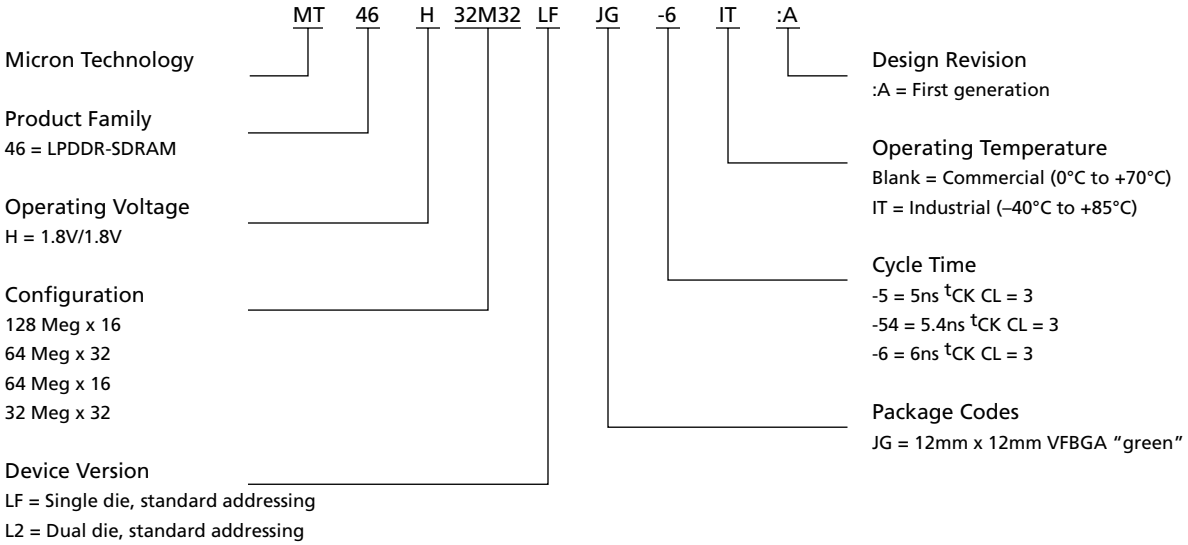


Table 2: 168-Ball Production Part Numbers

Part Numbers	LPDDR Product	Physical Part Marking
MT46H32M32LFJG-5:A	1Gb DDR, x32, 200 MHz	D9KFD
MT46H32M32LFJG-5 IT:A	1Gb DDR, x32, 200 MHz	D9KFC
MT46H32M32LFJG-54:A	1Gb DDR, x32, 185 MHz	D9KVC
MT46H32M32LFJG-54 IT:A	1Gb DDR, x32, 185 MHz	D9KVD
MT46H32M32LFJG-6:A	1Gb DDR, x32, 166 MHz	D9KNG
MT46H32M32LFJG-6 IT:A	1Gb DDR, x32, 166 MHz	D9KCK
MT46H64M32L2JG-5:A	2 x 1Gb DDR, x32, 200 MHz	D9KDK
MT46H64M32L2JG-5 IT:A	2 x 1Gb DDR, x32, 200 MHz	D9KDG
MT46H64M32L2JG-54:A	2 x 1Gb DDR, x32, 185 MHz	D9KDJ
MT46H64M32L2JG-54 IT:A	2 x 1Gb DDR, x32, 185 MHz	D9KVB
MT46H64M32L2JG-6:A	2 x 1Gb DDR, x32, 166 MHz	D9KCX
MT46H64M32L2JG-6 IT:A	2 x 1Gb DDR, x32, 166 MHz	D9KCW

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

General Description

The 1Gb Mobile LPDDR die contained within this package is a high-speed CMOS, dynamic random access memory containing 1,073,741,824 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 268,435,456-bit banks is organized as 16,384 rows by 1024 columns by 16 bits. Each of the x32's 268,435,456-bit banks is organized as 8192 rows by 1024 columns by 32 bits.

Figure 2: Functional Block Diagram (64 Meg x 16)

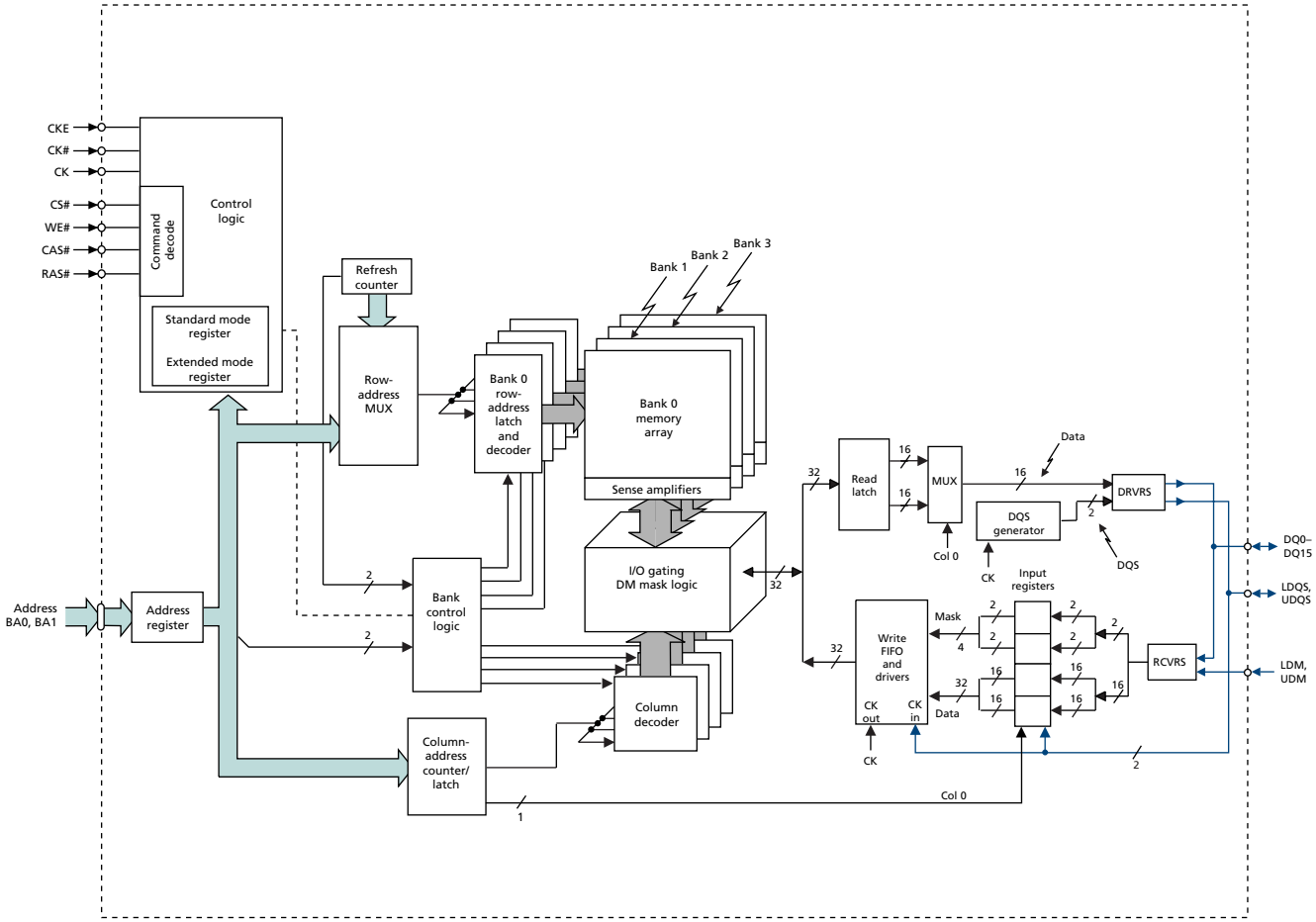
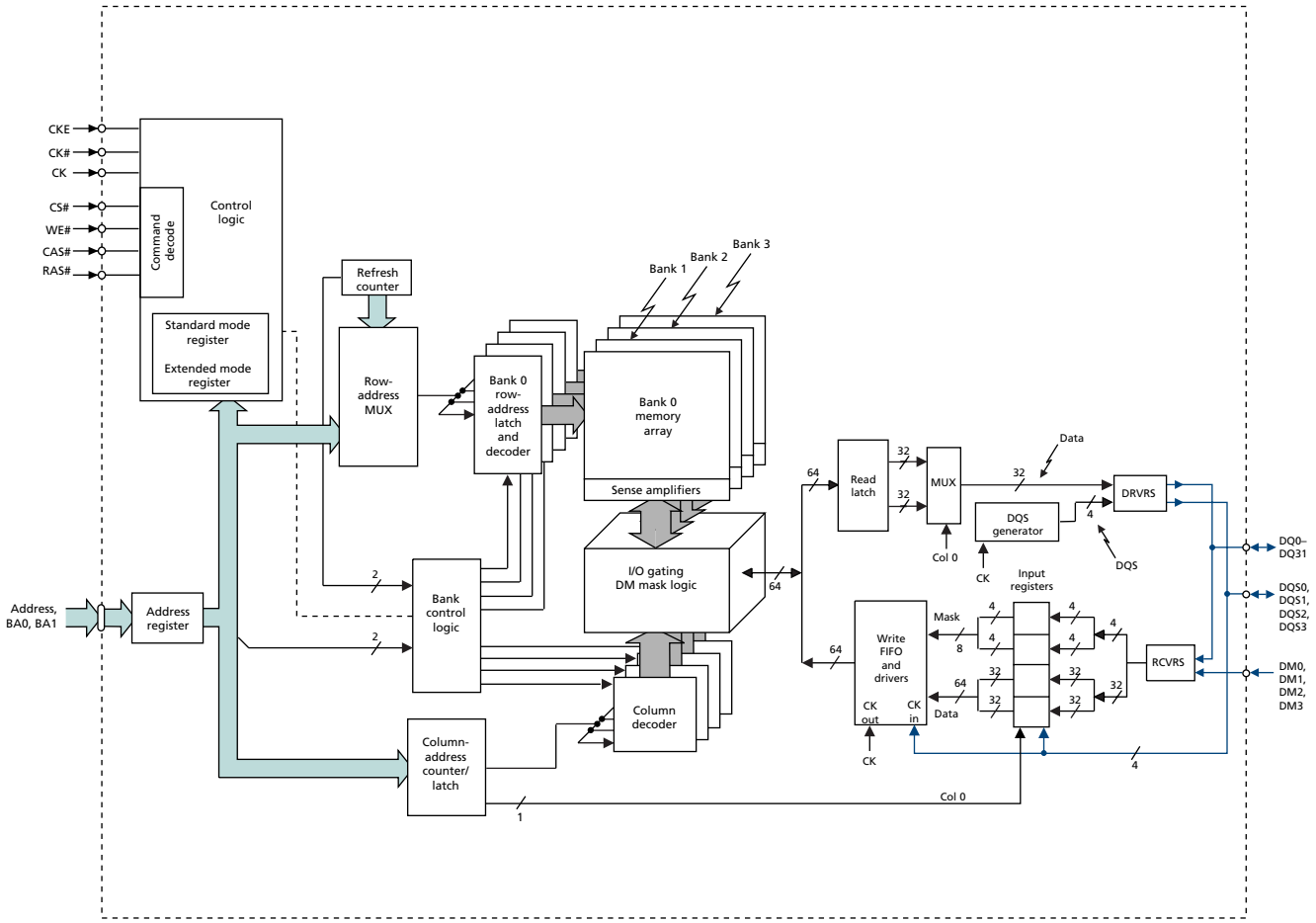
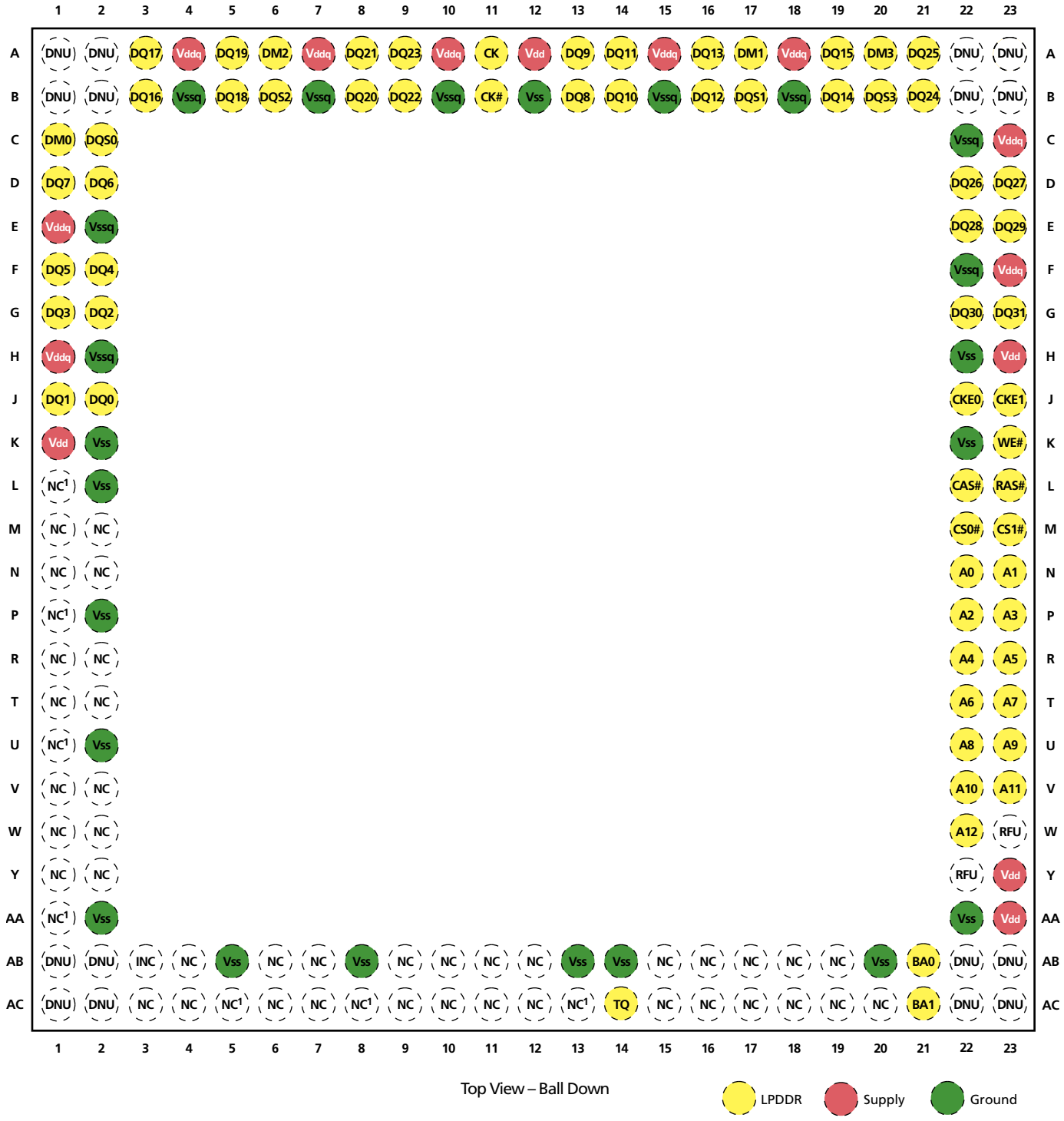


Figure 3: Functional Block Diagram (32 Meg x 32)



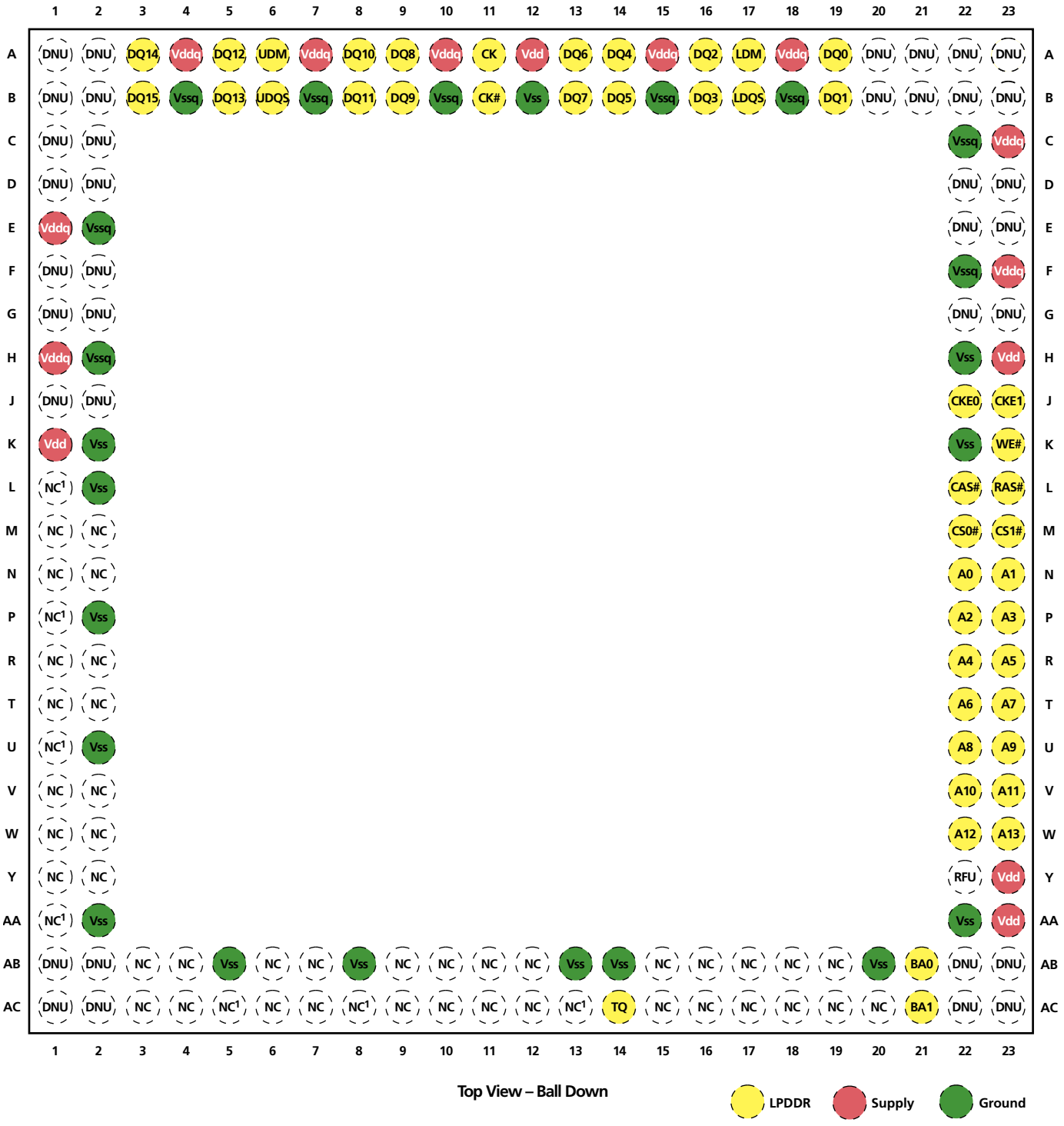
Ball Assignments and Descriptions

Figure 4: 168-Ball VFBGA (x32) Ball Assignments



Notes: 1. Although not bonded to the die, these pins may be connected on the package substrate.

Figure 5: 168-Ball VFBGA (x16) Ball Assignments



Notes: 1. Although not bonded to the die, these pins may be connected together on the package substrate.

Table 3: x16/x32 LPDDR Ball Descriptions

x16 Balls	x32 Balls	Symbol	Type	Description
W23, W22, V23, V22, U23, U22, T23, T22, R23, R22, P23, P22, N23, N22	W22, V23, V22, U23, U22, T23, T22, R23, R22, P23, P22, N23, N22	A[13:0] (x16) A[12:0] (x32)	Input	Address inputs: Specify row/column addresses. Also used to load the mode registers. The maximum address is determined by density and configuration. Consult the product data sheet for the maximum address for a given density and configuration. Unused address pins become RFU[1].
AB21, AC21	AB21, AC21	BA0, BA1	Input	Bank address inputs: Specifies one of the 4 banks.
L22	L22	CAS#	Input	Column select: Specifies the command to execute.
A11, B11	A11, B11	CK, CK#		CK is the system clock. CK and CK# are differential clock inputs. All address and control signals are sampled and referenced on the crossing of the rising edge of CK with the falling edge of CK#.
J22, J23	J22, J23	CKE0, CKE1	Input	Clock enable: CKE0 is used for a single LPDDR product. CKE1 is used for dual LPDDR products and is considered RFU for single products.
M22, M23	M22, M23	CS0#, CS1#	Input	Chip select: CS0# is used for a single LPDDR product. CS1# is used for dual LPDDR products and is considered RFU for single products
A17, A6	A20, A6, A17, C1	LDM, UDM (x16) DM[3:0] (x32)	Input	Data mask: Determines which bytes are written during WRITE operations. For x16 LPDDR, unused DM balls become DNU.
L23	L23	RAS#	Input	Row select: Specifies the command to execute.
K23	K23	WE#	Input	Write enable: Specifies the command to execute.
B3, A3, B5, A5, B8, A8, B9, A9, B13, A13, B14, A14, B16, A16, B19, A19	G23, G22, E23, E22, D23, D22, A21, B21, A9, B9, A8, B8, A5, B5, A3, B3, A19, B19, A16, B16, A14, B14, A13, B13, D1, D2, F1, F2, G1, G2, J1, J2	DQ[15:0] (x16) DQ[31:0] (x32)	Input/ output	Data bus: Data inputs/outputs. DQ[31:16] are DNU for x16 LPDDR devices. Note: For dual-die devices, the I/O capacitance will be twice the value shown in the packaged data sheet.
B17, B6	B20, B6, B17, C2	LDQS, UDQS (x16) DQS[3:0] (x32)	Input/ output	Data strobe: Coordinates read/write transfers of data; one DQS per DQ byte.
AC14	AC14	TQ	Output	Temperature sensor output: TQ HIGH when LPDDR T_J exceeds 85°C.
A12, H23, K1, Y23, AA23	A12, H23, K1, Y23, AA23	Vdd	Supply	Vdd: LPDDR power supply.
A4, A7, A10, A15, A18, C23, E1, F23, H1	A4, A7, A10, A15, A18, C23, E1, F23, H1	Vddq	Supply	Vddq: LPDDR I/O power supply.

Notes: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 4: Non-Device-Specific Ball Descriptions

Shared Balls				
x16	**x32**	**Symbol**	**Type**	**Description**
B12, H22, K2, K22, L2, P2, AA2, AA22, AB5, AB8, AB13, AB14, AB20	B12, H22, K2, K22, L2, P2, AA2, AA22, AB5, AB8, AB13, AB14, AB20	Vss	Supply	Vss: Shared ground.
Miscellaneous Balls				
x16	**x32**	**Symbol**	**Type**	**Description**
A20, A21, B20, B21, C1, C2, D1, D2, D22, D23, E22, E23, F1, F2, G1, G2, G22, G23, J1, J2, L1, M1, M2, N1, N2, P1, R1, R2, T1, T2, U1, V1, V2, W1, W2, Y1, Y2, AA1, AB3, AB4, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB15, AB16, AB17, AB18, AB19, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC15, AC16, AC17, AC18, AC19, AC20	L1, M1, M2, N1, N2, P1, R1, R2, T1, T2, U1, V1, V2, W1, W2, Y1, Y2, AA1, AB3, AB4, AB6, AB7, AB9, AB10, AB11, AB12, AB15, AB16, AB17, AB18, AB19, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC15, AC16, AC17, AC18, AC19, AC20	NC	–	No connect: Not internally connected.
A1, A2, A22, A23, B1, B2, B22, B23, AB1, AB2, AB22, AB23, AC1, AC2, AC22, AC23	A1, A2, A22, A23, B1, B2, B22, B23, AB1, AB2, AB22, AB23, AC1, AC2, AC22, AC23	DNU	–	Do not use: Must be grounded or left floating.
Y22	W23, Y22	RFU[1]	–	Reserved for future use.

Notes: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Electrical Specifications

Table 5: Absolute Maximum Ratings

Parameters/Conditions	Symbol	Min	Max	Unit
Vdd, Vddq supply voltage relative to Vss	Vdd, Vddq	–1.0	2.4	V
Voltage on any pin relative to Vss	Vin	–0.5	2.4 or (Vddq + 0.3V), whichever is less	V
Storage temperature range		–55	+150	°C

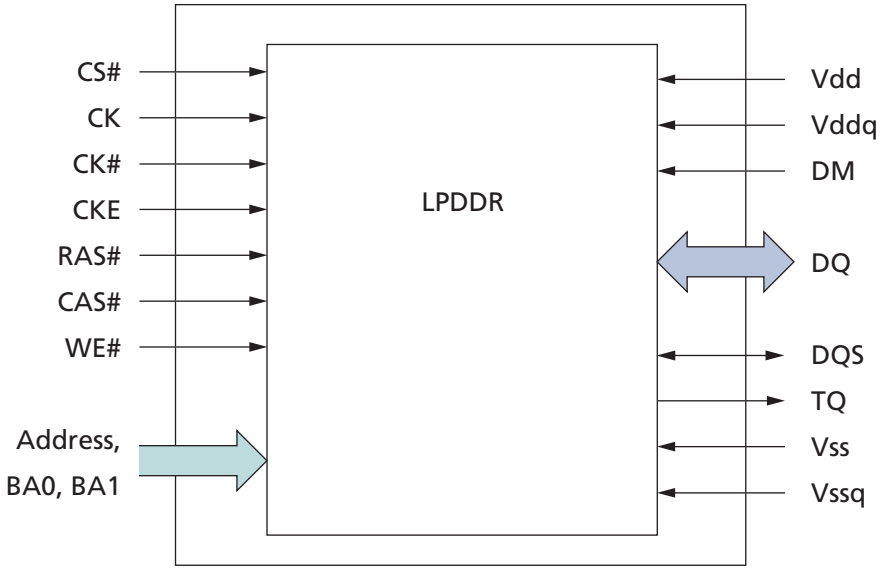
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage	Vdd	1.70	1.80	1.95	V
I/O supply voltage	Vddq	1.70	1.80	1.95	V
Operating temperature range		–40	–	+85	°C

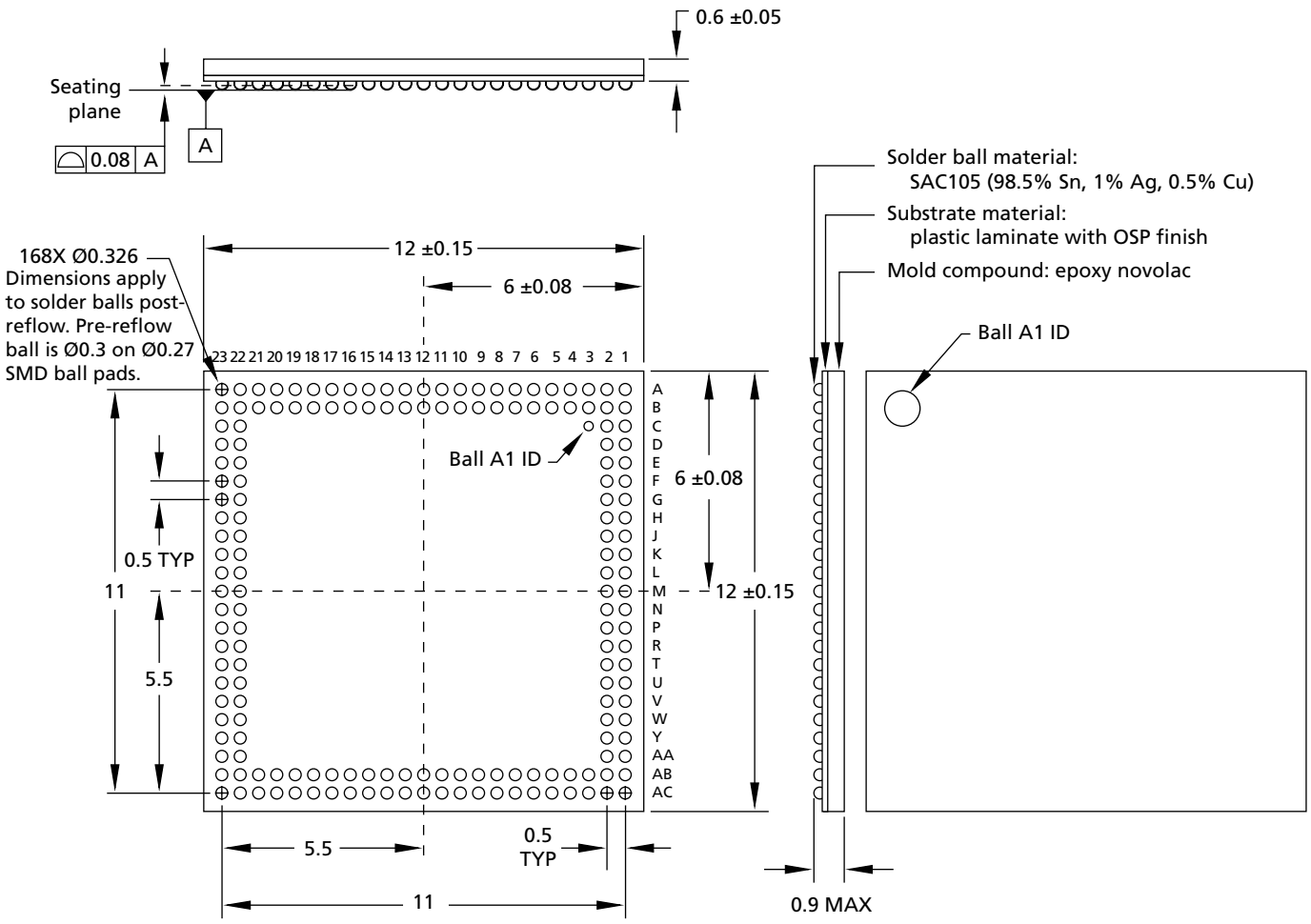
Device Diagram

Figure 6: 168-Ball VFBGA Functional Block Diagram



Package Dimensions

Figure 7: 168-Ball VFBGA



Notes: 1. All dimensions are in millimeters.

Revision History

Rev. B, Preliminary 1/09

- "Mobile LPDDR" on page 1: Changed title from "LPDDR-SDRAM" to "Mobile LPDDR."
- "General Description" on page 3: Deleted "SDRAM" from description.
- Table 4, "Non-Device-Specific Ball Descriptions," on page 8: Removed V2 from Vss x16 and x32 balls; divided table into shared balls and miscellaneous balls.

Rev. A, Preliminary 11/08

- Initial release.

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