THE DATASHEET OF

LTC2324HUKG-12#PBF

Quad, 12-Bit + Sign, 2Msps/Ch Simultaneous Sampling ADC

FEATURES

- **2Msps/Ch Throughput Rate**
- **Four Simultaneously Sampling Channels**
- **Guaranteed 12-Bit, No Missing Codes**
- **$8V_{P-P}$ Differential Inputs with Wide Input Common Mode Range**
- **78dB SNR (Typ) at f_{IN} = 500kHz**
- **–88dB THD (Typ) at f_{IN} = 500kHz**
- Guaranteed Operation to 125°C
- Single 3.3V or 5V Supply
- Low Drift (20ppm/°C Max) 2.048V or 4.096V Internal Reference
- 1.8V to 2.5V I/O Voltages
- CMOS or LVDS SPI-Compatible Serial I/O
- Power Dissipation 40mW/Ch (Typ)
- Small 52-Lead (7mm × 8mm) QFN Package

APPLICATIONS

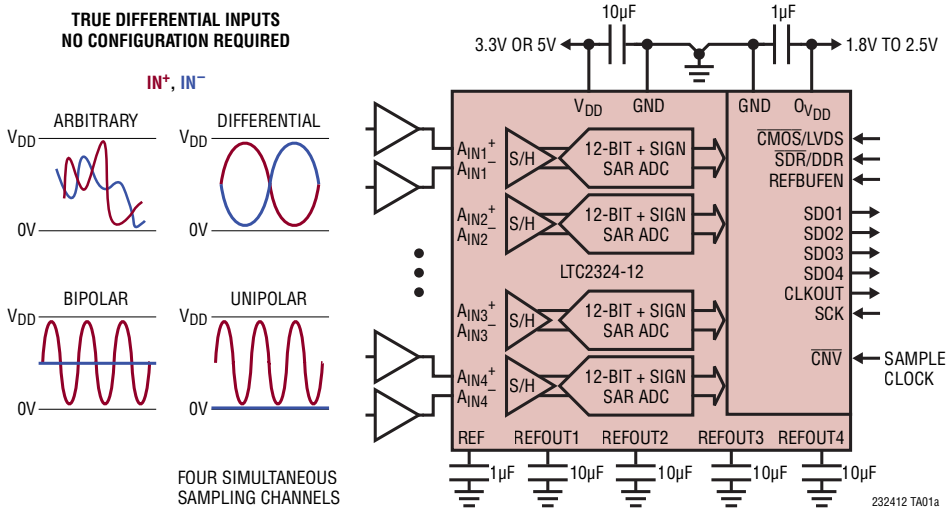
- High Speed Data Acquisition Systems
- Communications
- Optical Networking
- Multiphase Motor Control

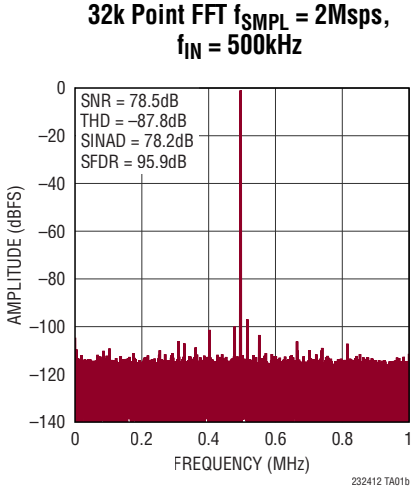
DESCRIPTION

The LTC®2324-12 is a low noise, high speed quad 12-bit + sign successive approximation register (SAR) ADC with differential inputs and wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2324-12 has an $8V_{P-P}$ differential input range, making it ideal for applications which require a wide dynamic range with high common mode rejection. The LTC2324-12 achieves ±0.5LSB INL typical, no missing codes at 12 bits and 78dB SNR.

The LTC2324-12 has an onboard low drift (20ppm/°C max) 2.048V or 4.096V temperature-compensated reference. The LTC2324-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 2Msps per channel throughput with no latency makes the LTC2324-12 ideally suited for a wide variety of high speed applications. The LTC2324-12 dissipates only 40mW per channel and offers nap and sleep modes to reduce the power consumption to 26µW for further power savings during inactive periods.

TYPICAL APPLICATION



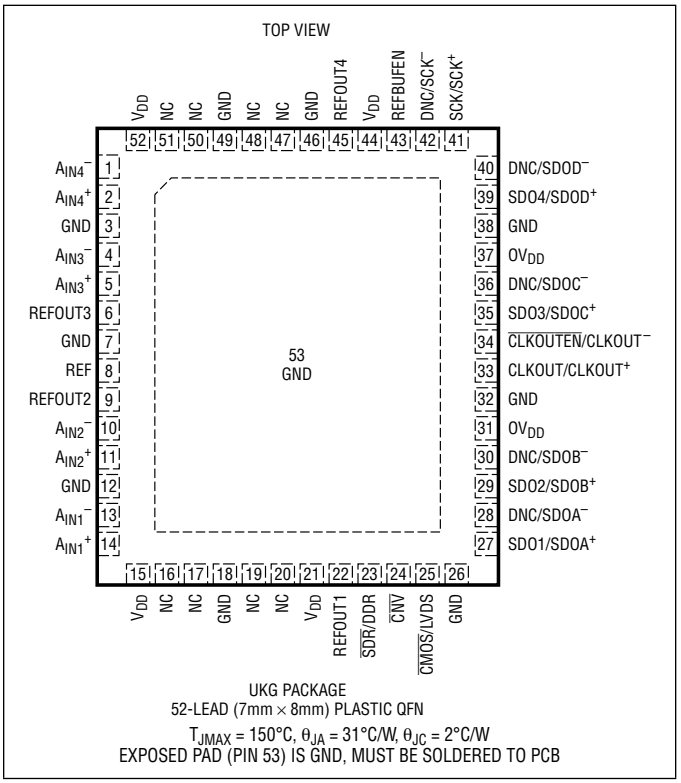


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Supply Voltage (OV_{DD}) 3V
Analog Input Voltage
  A_{IN}^+, A_{IN}^- (Note 3) ..... –0.3V to (V_{DD} + 0.3V)
  $\overline{REFOUT1,2,3,4}$ ..... –0.3V to (V_{DD} + 0.3V)
  $\overline{CNV}$ ..... –0.3V to (OV_{DD} + 0.3V)
Digital Input Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Operating Temperature Range
  LTC2324C ..... 0°C to 70°C
  LTC2324I ..... –40°C to 85°C
  LTC2324H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UKG PACKAGE
52-LEAD (7mm × 8mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 31°C/W, θ_{JC} = 2°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2324-12#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2324CUKG-12#PBF	LTC2324CUKG-12#TRPBF	LTC2324UKG-12	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2324IUKG-12#PBF	LTC2324IUKG-12#TRPBF	LTC2324UKG-12	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 85°C
LTC2324HUKG-12#PBF	LTC2324HUKG-12#TRPBF	LTC2324UKG-12	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (A_{IN}^+ to A_{IN}^-)	(Note 5)	●	0		V_{DD}	V
V_{IN}^-	Absolute Input Range (A_{IN}^+ to A_{IN}^-)	(Note 5)	●	0		V_{DD}	V
$V_{IN}^+ – V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ – V_{IN}^-$	●	–REFOUT1,2,3,4		REFOUT1,2,3,4	V
V_{CM}	Common Mode Input Range	$V_{CM} = (V_{IN}^+ – V_{IN}^-)/2$	●	0		V_{DD}	V
I_{IN}	Analog Input DC Leakage Current		●	–1		1	µA
C_{IN}	Analog Input Capacitance				10		pF
CMRR	Input Common Mode Rejection Ratio	f_{IN} = 500kHz			102		dB
V_{IHCNV}	$\overline{CNV}$ High Level Input Voltage		●	1.5			V
V_{ILCNV}	$\overline{CNV}$ Low Level Input Voltage		●			0.5	V
I_{INCNV}	$\overline{CNV}$ Input Current		●	–10		10	µA

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	12			Bits
	No Missing Codes		●	12			Bits
	Transition Noise				0.2		LSB_{RMS}
INL	Integral Linearity Error	(Note 6)	●	–1	0	1	LSB
DNL	Differential Linearity Error		●	–0.25	±0.1	0.25	LSB
BZE	Bipolar Zero-Scale Error	(Note 7)	●	–0.2	0	0.2	LSB
	Bipolar Zero-Scale Error Drift				0.01		LSB/°C
FSE	Bipolar Full-Scale Error	$V_{REFOUT1,2,3,4}$ = 4.096V (REFBUFEN Grounded) (Note 7)	●	–0.5	0	0.5	LSB
	Bipolar Full-Scale Error Drift	$V_{REFOUT1,2,3,4}$ = 4.096V (REFBUFEN Grounded)			15		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS (Notes 4, 8).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 500kHz, $V_{REFOUT1,2,3,4}$ = 4.096V, Internal Reference	●	74	78		dB
		f_{IN} = 500kHz, $V_{REFOUT1,2,3,4}$ = 5V, External Reference			78		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 500kHz, $V_{REFOUT1,2,3,4}$ = 4.096V, Internal Reference	●	75	78.5		dB
		f_{IN} = 500kHz, $V_{REFOUT1,2,3,4}$ = 5V, External Reference			78.5		dB
THD	Total Harmonic Distortion	f_{IN} = 500kHz, $V_{REFOUT1,2,3,4}$ = 4.096V, Internal Reference	●		–88	–77.5	dB
		f_{IN} = 500kHz, $V_{REFOUT1,2,3,4}$ = 5V, External Reference			–88		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 500kHz, $V_{REFOUT1,2,3,4}$ = 4.096V, Internal Reference	●	77.5	93		dB
		f_{IN} = 500kHz, $V_{REFOUT1,2,3,4}$ = 5V, External Reference			93		dB
	–3dB Input Bandwidth				55		MHz
	Aperture Delay				500		ps
	Aperture Delay Matching				500		ps
	Aperture Jitter				1		ps_{RMS}
	Transient Response	Full-Scale Step			3		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{REFOUT1,2,3,4}$	Internal Reference Output Voltage	4.75V < V_{DD} < 5.25V 3.13V < V_{DD} < 3.47V	● ●	4.078 2.034	4.096 2.048	4.115 2.064	V V
	V_{REF} Temperature Coefficient	(Note 14)	●		3	20	ppm/°C
	REFOUT1,2,3,4 Output Impedance				0.25		Ω
	$V_{REFOUT1,2,3,4}$ Line Regulation	4.75V < V_{DD} < 5.25V			0.3		mV/V
$I_{REFOUT1,2,3,4}$	External Reference Current	REFBUFEN = 0V REFOUT1,2,3,4 = 4.096V REFOUT1,2,3,4 = 2.048V (Notes 9, 10)			 385 204		 µA µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Digital Inputs and Outputs $\overline{CMOS}$/LVDS = GND							
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA
LVDS Digital Inputs and Outputs $\overline{CMOS}$/LVDS = OV_{DD}							
V_{ID}	LVDS Differential Input Voltage	100Ω Differential Termination OV_{DD} = 2.5V	●	240		600	mV
V_{IS}	LVDS Common Mode Input Voltage	100Ω Differential Termination OV_{DD} = 2.5V	●	1		1.45	V
V_{OD}	LVDS Differential Output Voltage	100Ω Differential Termination OV_{DD} = 2.5V	●	220	350	600	mV
V_{OS}	LVDS Common Mode Output Voltage	100Ω Differential Termination OV_{DD} = 2.5V	●	0.85	1.2	1.4	V
V_{OD_LP}	Low Power LVDS Differential Output Voltage	100Ω Differential Termination OV_{DD} = 2.5V	●	100	200	350	mV
V_{OS_LP}	Low Power LVDS Common Mode Output Voltage	100Ω Differential Termination OV_{DD} = 2.5V	●	0.85	1.2	1.4	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	5V Operation 3.3V Operation	● ●	4.75 3.13		5.25 3.47	V V
I_{VDD}	Supply Current	2Msps Sample Rate (AIN⁺ = AIN⁻ = 0V)	●		31	36.5	mA
CMOS I/O Mode $\overline{CMOS}$/LVDS = GND							
OV_{DD}	Supply Voltage		●	1.71		2.63	V
I_{OVDD}	Supply Current	2Msps Sample Rate (C_L = 5pF)	●		4.4	8	mA
I_{NAP}	Nap Mode Current	Conversion Done (I_{VDD})	●		5.3	6.4	mA
I_{SLEEP}	Sleep Mode Current	Sleep Mode (I_{VDD} + I_{OVDD})	●		20	90	µA
$P_{D\_3.3V}$	Power Dissipation	V_{DD} = 3.3V, 2Msps Sample Rate Nap Mode Sleep Mode	● ● ●		102 18 20	130 21 288	mW mW µW
P_{D_5V}	Power Dissipation	V_{DD} = 5V, 2Msps Sample Rate Nap Mode Sleep Mode	● ● ●		162 27 30	202 32 424	mW mW µW
LVDS I/O Mode $\overline{CMOS}$/LVDS = OV_{DD}, OV_{DD} = 2.5V							
OV_{DD}	Supply Voltage		●	2.37		2.63	V
I_{OVDD}	Supply Current	1.5Msps Sample Rate (C_L = 5pF, R_L = 100Ω)	●		26	31.5	mA
I_{NAP}	Nap Mode Current	Conversion Done (I_{VDD})	●		5.3	6.4	mA
I_{SLEEP}	Sleep Mode Current	Sleep Mode (I_{VDD} + I_{OVDD})	●		20	90	µA
$P_{D\_3.3V}$	Power Dissipation	V_{DD} = 3.3V, 2Msps Sample Rate Nap Mode Sleep Mode	● ● ●		151 52 80	185 56 288	mW mW µW
P_{D_5V}	Power Dissipation	V_{DD} = 5V, 2Msps Sample Rate Nap Mode Sleep Mode	● ● ●		214 52 30	262 66 424	mW mW µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			2	Msps
t_{CYC}	Time Between Conversions	(Note 11) t_{CYC} = t_{CNVH} + t_{CONV} + $t_{READOUT}$	●	0.5		1000	µs
t_{CONV}	Conversion Time		●	220			ns
t_{CNVH}	$\overline{CNV}$ High Time		●	30			ns
$t_{ACQUISITION}$	Sampling Aperture	(Note 11) $t_{ACQUISITION}$ = t_{CYC} – t_{CONV}			250		ns
t_{WAKE}	REFOUT1,2,3,4 Wake-Up Time	$C_{REFOUT1,2,3,4}$ = 10µF			50		ms
CMOS I/O Mode, SDR $\overline{CMOS}$/LVDS = GND, $\overline{SDR}$/ DDR = GND							
t_{SCK}	SCK Period	(Note 13)	●	9.1			ns
t_{SCKH}	SCK High Time		●	4.1			ns
t_{SCKL}	SCK Low Time		●	4.1			ns
t_{HSDO_SDR}	SDO Data Remains Valid Delay from CLKOUT↓	C_L = 5pF (Note 12)	●	0		1.5	ns
$t_{DSCKCLKOUT}$	SCK to CLKOUT Delay	(Note 12)	●	2		4.5	ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{DCNVSDOZ}$	Bus Relinquish Time After $\overline{CNV}$↑	(Note 11)	●			3	ns
$t_{DCNVSDOV}$	SDO Valid Delay from $\overline{CNV}$↓	(Note 11)	●			3	ns
$t_{DSCKHCNVH}$	SCK Delay Time to $\overline{CNV}$↑	(Note 11)	●	0			ns
CMOS I/O Mode, DDR $\overline{CMOS}$/LVDS = GND, $\overline{SDR}$/ DDR = OV_{DD}							
t_{SCK}	SCK Period		●	18.2			ns
t_{SCKH}	SCK High Time		●	8.2			ns
t_{SCKL}	SCK Low Time		●	8.2			ns
t_{HSDO_DDR}	SDO Data Remains Valid Delay from CLKOUT↓	C_L = 5pF (Note 12)	●	0		1.5	ns
$t_{DSCKCLKOUT}$	SCK to CLKOUT Delay	(Note 12)	●	2		4.5	ns
$t_{DCNVSDOZ}$	Bus Relinquish Time After $\overline{CNV}$↑	(Note 11)	●			3	ns
$t_{DCNVSDOV}$	SDO Valid Delay from $\overline{CNV}$↓	(Note 11)	●			3	ns
$t_{DSCKHCNVH}$	SCK Delay Time to $\overline{CNV}$↑	(Note 11)	●	0			ns
LVDS I/O Mode, SDR $\overline{CMOS}$/LVDS = OV_{DD}, $\overline{SDR}$/DDR = GND							
t_{SCK}	SCK Period		●	3.3			ns
t_{SCKH}	SCK High Time		●	1.5			ns
t_{SCKL}	SCK Low Time		●	1.5			ns
t_{HSDO_SDR}	SDO Data Remains Valid Delay from CLKOUT↓	C_L = 5pF (Note 12)	●	0		1.5	ns
$t_{DSCKCLKOUT}$	SCK to CLKOUT Delay	(Note 12)	●	2		4	ns
$t_{DSCKHCNVH}$	SCK Delay Time to $\overline{CNV}$↑	(Note 11)	●	0			ns
LVDS I/O Mode, DDR $\overline{CMOS}$/LVDS = OV_{DD}, $\overline{SDR}$/DDR = OV_{DD} = 2.5V							
t_{SCK}	SCK Period		●	6.6			ns
t_{SCKH}	SCK High Time		●	3			ns
t_{SCKL}	SCK Low Time		●	3			ns
t_{HSDO_DDR}	SDO Data Remains Valid Delay from CLKOUT↓	C_L = 5pF (Note 12)	●	0		1.5	ns
$t_{DSCKCLKOUT}$	SCK to CLKOUT Delay	(Note 12)	●	2		4	ns
$t_{DSCKHCNVH}$	SCK Delay Time to $\overline{CNV}$↑	(Note 11)	●	0			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground, or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground, or above V_{DD} or OV_{DD}, without latch-up.

Note 4: V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT1,2,3,4 = 4.096V, f_{SMPL} = 2MHz.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 0 0000 0000 0000 and 1 1111 1111 1111. Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale ±4.096V input with REF = 4.096V.

Note 9: When REFOUT1,2,3,4 is overdriven, the internal reference buffer must be turned off by setting REFBUFEN = 0V.

Note 10: f_{SMPL} = 2MHz, $I_{REFOUT1,2,3,4}$ varies proportionally with sample rate.

Note 11: Guaranteed by design, not subject to test.

Note 12: Parameter tested and guaranteed at OV_{DD} = 1.71V and OV_{DD} = 2.5V.

Note 13: t_{SCK} of 9.1ns allows a shift clock frequency up to 110MHz for rising edge capture.

Note 14: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 15: $\overline{CNV}$ is driven from a low jitter digital source, typically at OV_{DD} logic levels.

ADC TIMING CHARACTERISTICS

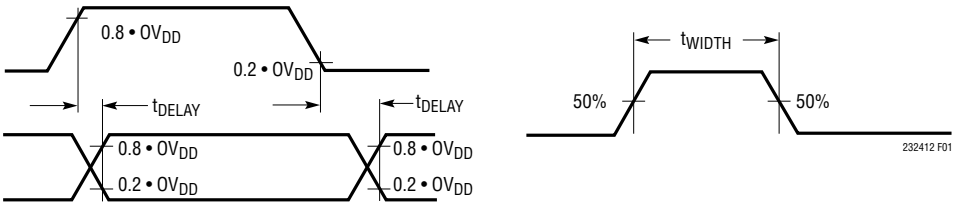
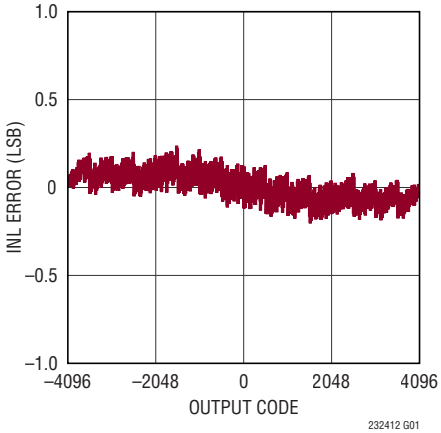


Figure 1. Voltage Levels for Timing Specifications

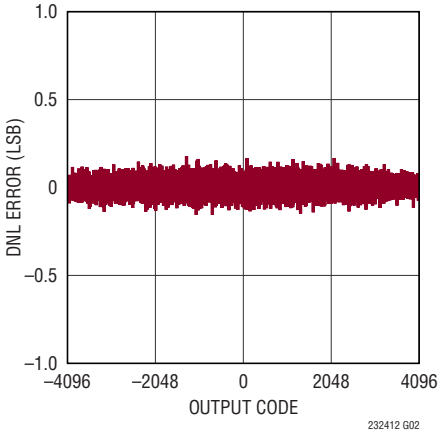
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT1,2,3,4 = 4.096V, f_{SMPL} = 2Msps, unless otherwise noted.

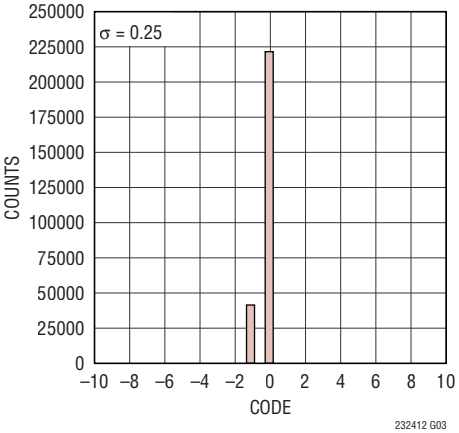
Integral Nonlinearity vs Output Code



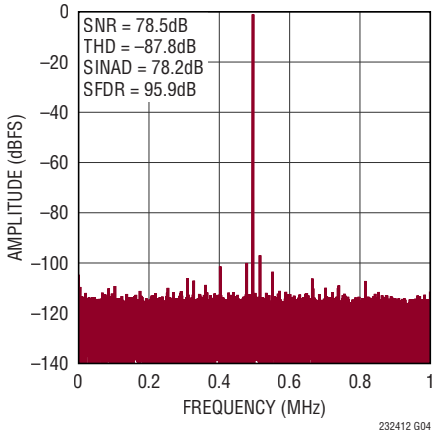
Differential Nonlinearity vs Output Code



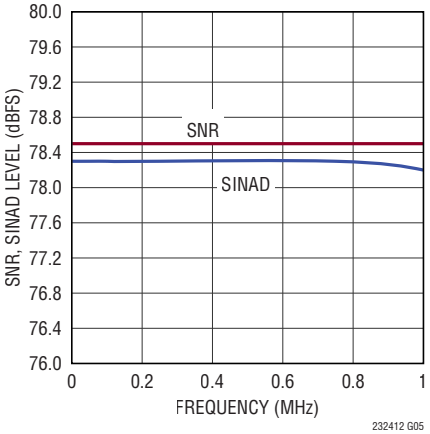
DC Histogram



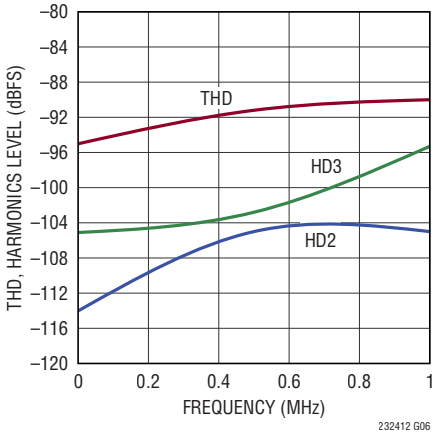
32k Point FFT, f_{SMPL} = 2Msps, f_{IN} = 500kHz



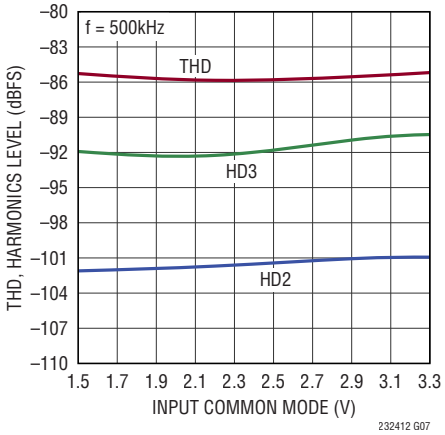
SNR, SINAD vs Input Frequency (1kHz to 1MHz)



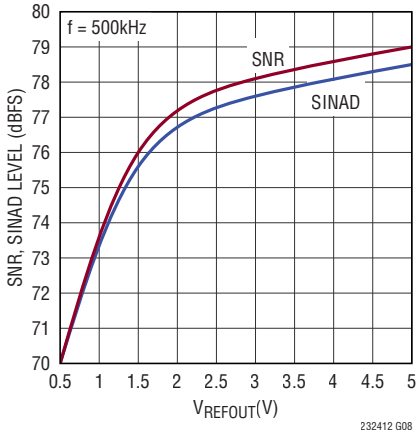
THD, Harmonics vs Input Frequency (1kHz to 1MHz)



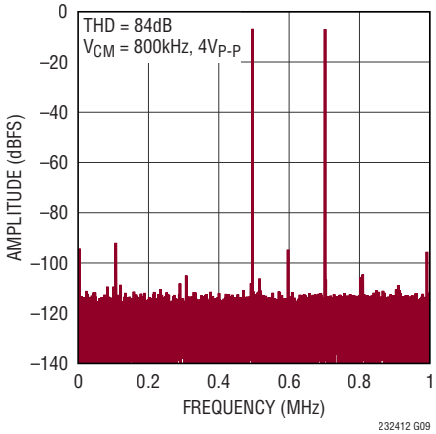
THD, Harmonics vs Input Common Mode



SNR, SINAD vs Reference Voltage, f_{IN} = 500kHz



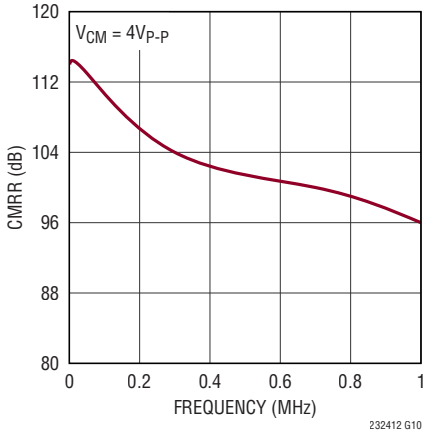
32k Point FFT, IMD, f_{SMPL} = 2Msps, A_{IN}^+ = 500kHz, A_{IN}^- = 1.3MHz



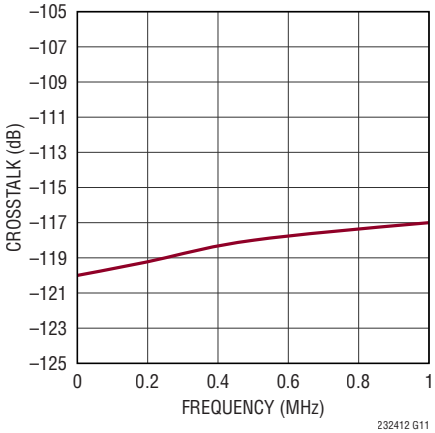
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFOUT1,2,3,4 = 4.096V, f_{SMPL} = 2Msps, unless otherwise noted.

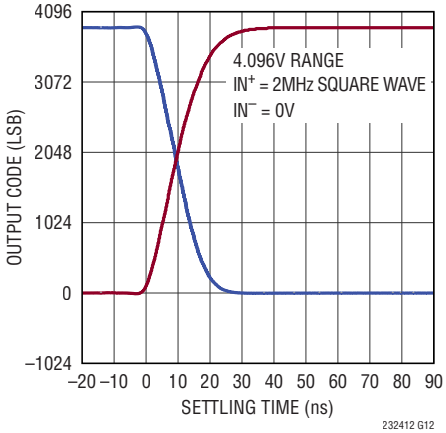
CMRR vs Input Frequency



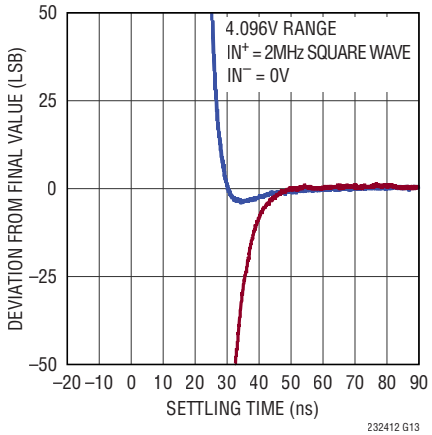
Crosstalk vs Input Frequency



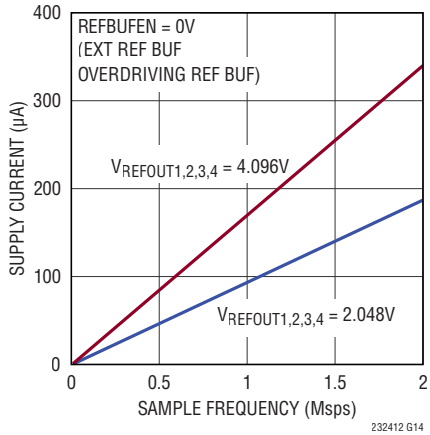
Step Response (Large Signal Settling)



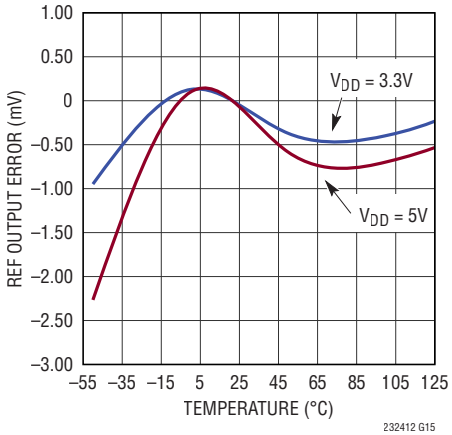
Step Response (Fine Settling)



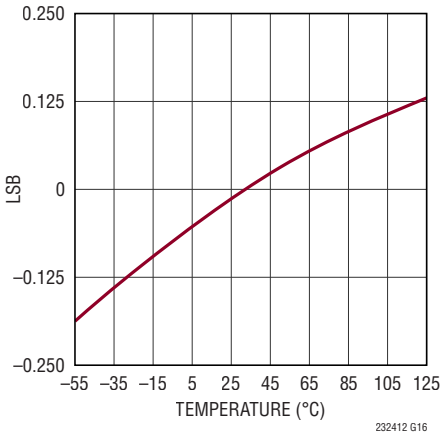
External Reference Supply Current vs Sample Frequency



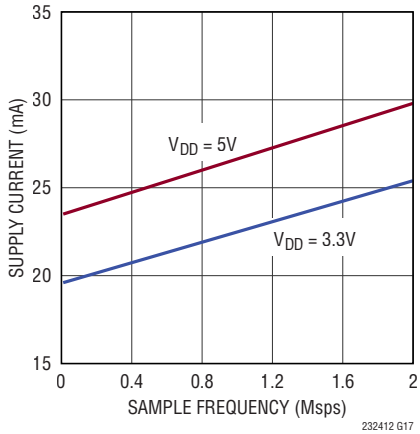
REF Output vs Temperature



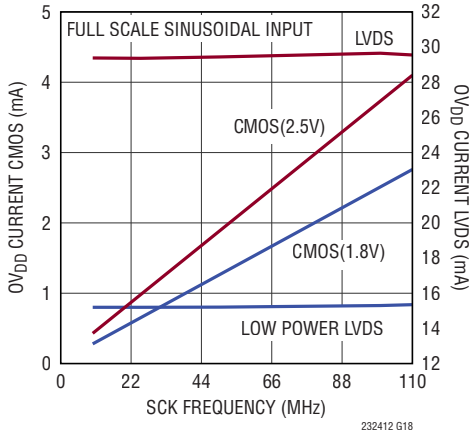
Offset Error vs Temperature



Supply Current vs Sample Frequency



OV_{DD} Current vs SCK Frequency, C_{LOAD} = 10pF



PIN FUNCTIONS

PINS THAT ARE THE SAME FOR ALL DIGITAL I/O MODES

AIN4$^+$, AIN4$^-$ (Pins 2, 1): Analog Differential Input Pins. Full-scale range (AIN4$^+$ – AIN4$^-$) is ±REFOUT4 voltage. These pins can be driven from V_{DD} to GND.

GND (Pins 3, 7, 12, 18, 26, 32, 38, 46, 49): Ground. These pins and exposed pad (Pin 53) must be tied directly to a solid ground plane.

AIN3$^+$, AIN3$^-$ (Pins 5, 4): Analog Differential Input Pins. Full-scale range (AIN3$^+$ – AIN3$^-$) is ±REFOUT3 voltage. These pins can be driven from V_{DD} to GND.

REFOUT3 (Pin 6): Reference Buffer 3 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

REF (Pin 8): Common 4.096V reference output. Decouple to GND with a 1µF low ESR ceramic capacitor. May be overdriven with a single external reference to establish a common reference for ADC cores 1 through 4.

REFOUT2 (Pin 9): Reference Buffer 2 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

AIN2$^+$, AIN2$^-$ (Pins 11, 10): Analog Differential Input Pins. Full-scale range (AIN2$^+$ – AIN2$^-$) is ±REFOUT2 voltage. These pins can be driven from V_{DD} to GND.

AIN1$^+$, AIN1$^-$ (Pins 14, 13): Analog Differential Input Pins. Full-scale range (AIN1$^+$ – AIN1$^-$) is ±REFOUT1 voltage. These pins can be driven from V_{DD} to GND.

V_{DD} (Pins 15, 21, 44, 52): Power Supply. Bypass V_{DD} to GND with a 10µF ceramic capacitor and a 0.1µF ceramic capacitor close to the part. The V_{DD} pins should be shorted together and driven from the same supply.

REFOUT1 (Pin 22): Reference Buffer 1 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

$\overline{\text{SDR}}$/DDR (Pin 23): Double Data Rate Input. Controls the frequency of SCK and CLKOUT. Tie to GND for the falling edge of SCK to shift each serial data output (Single Data Rate, SDR). Tie to OV_{DD} to shift serial data output on each edge of SCK (Double Data Rate, DDR). CLKOUT will be a delayed version of SCK for both pin states.

$\overline{\text{CNV}}$ (Pin 24): Convert Input. This pin, when high, defines the acquisition phase. When this pin is driven low, the conversion phase is initiated and output data is clocked out. This input must be driven at OV_{DD} levels with a low jitter pulse. This pin is unaffected by the $\overline{\text{CMOS}}$/LVDS pin.

$\overline{\text{CMOS}}$/LVDS (Pin 25): I/O Mode Select. Ground this pin to enable CMOS mode, tie to OV_{DD} to enable LVDS mode. Float this pin to enable low power LVDS mode.

OV_{DD} (Pins 31, 37): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 2.63V. This supply is nominally set to the same supply as the host interface (CMOS: 1.8V or 2.5V, LVDS: 2.5V). Bypass OV_{DD} to GND (Pins 32 and 38) with 0.1µF capacitors.

REFBUFEN (Pin 43): Reference Buffer Output Enable. Tie to V_{DD} when using the internal reference. Tie to ground to disable the internal REFOUT1–4 buffers for use with external voltage references. This pin has a 500k internal pull-up to V_{DD}.

REFOUT4 (Pin 45): Reference Buffer 4 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

Exposed Pad (Pin 53): Ground. Solder this pad to ground.

PIN FUNCTIONS

CMOS DATA OUTPUT OPTION ($\overline{CMOS}$/LVDS = LOW)

SDO1 (Pin 27): CMOS Serial Data Output for ADC Channel 1. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO1 in SDR mode, 13 SCK edges in DDR mode.

SDO2 (Pin 29): CMOS Serial Data Output for ADC Channel 2. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO2 in SDR mode, 13 SCK edges in DDR mode.

SDO3 (Pin 35): CMOS Serial Data Output for ADC Channel 3. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO3 in SDR mode, 13 SCK edges in DDR mode.

SDO4 (Pin 39): CMOS Serial Data Output for ADC Channel 4. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO4 in SDR mode, 13 SCK edges in DDR mode.

CLKOUT (Pin 33): Serial Data Clock Output. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver (FPGA). The logic level is determined by OV_{DD}. This pin echoes the input at SCK with a small delay.

$\overline{CLKOUTEN}$ (Pin 34): CLKOUT can be disabled by tying Pin 34 to OV_{DD} for a small power savings. If CLKOUT is used, ground this pin.

SCK (Pin 41): Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins in SDR mode (DDR = LOW). In DDR mode ($\overline{SDR}$/DDR = HIGH) each edge of this clock shifts the conversion result MSB first onto the SDO pins. The logic level is determined by OV_{DD}.

DNC (Pins 28, 30, 36, 40, 42): In CMOS mode, do not connect this pin.

LVDS DATA OUTPUT OPTION ($\overline{CMOS}$/LVDS = HIGH OR FLOAT)

SDOA$^+$, SDOA$^-$ (Pins 27, 28): LVDS Serial Data Output for ADC Channel 1. The conversion result is shifted CH1 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDOA in SDR mode, 13 SCK edges in DDR mode. Terminate with a 100Ω resistor at the receiver (FPGA).

SDOB$^+$, SDOB$^-$ (Pins 29, 30): LVDS Serial Data Output for ADC Channel 2. The conversion result is shifted CH2 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDOB in SDR mode, 13 SCK edges in DDR mode. Terminate with a 100Ω resistor at the receiver (FPGA).

CLKOUT$^+$, CLKOUT$^-$ (Pins 33, 34): Serial Data Clock Output. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. These pins echo the input at SCK with a small delay. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA).

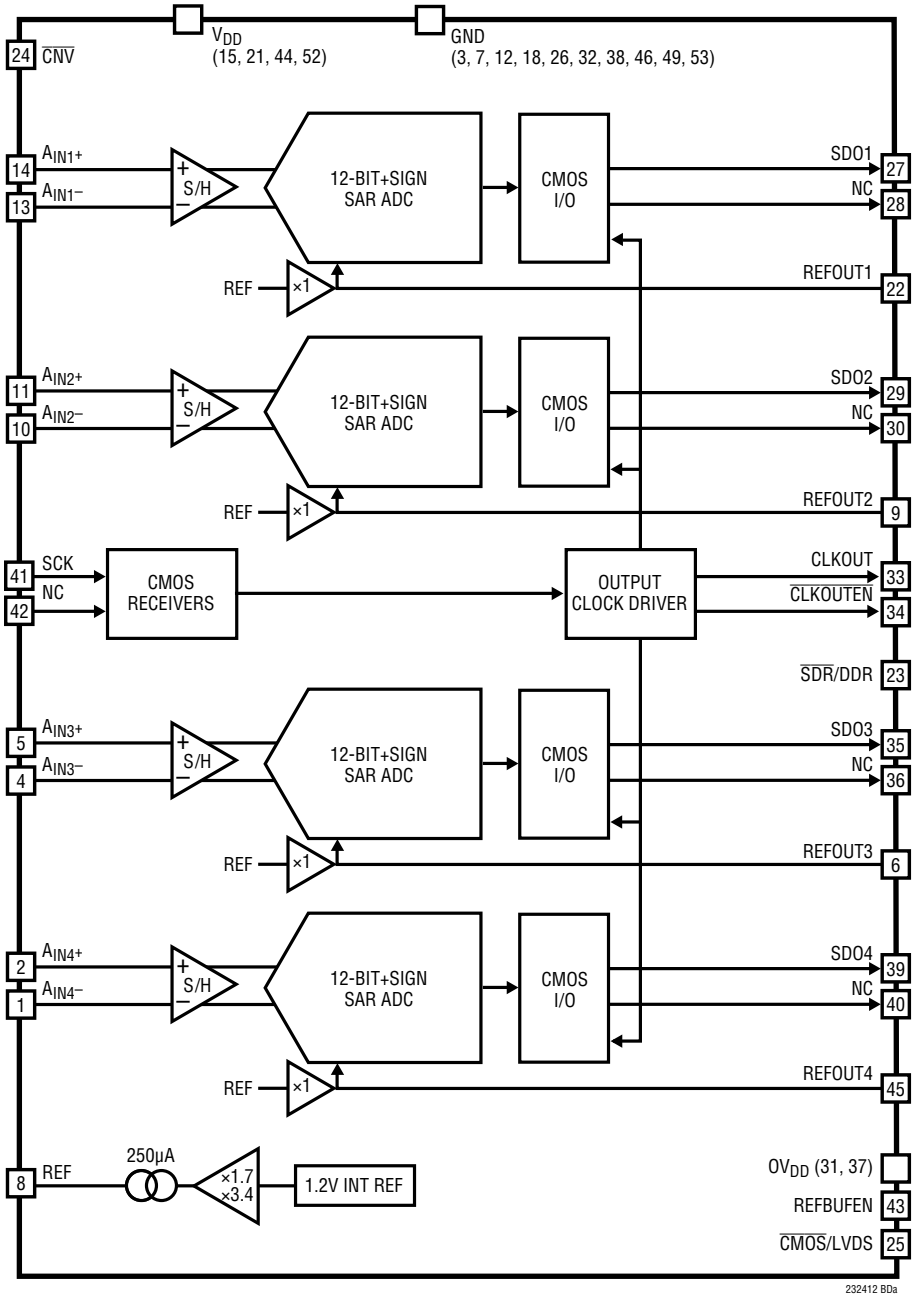
SDOC$^+$, SDOC$^-$ (Pins 35, 36): LVDS Serial Data Output for ADC channel 3. The conversion result is shifted CH3 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDOA in SDR mode, 13 SCK edges in DDR mode. Terminate with a 100Ω resistor at the receiver (FPGA).

SDOD$^+$, SDOD$^-$ (Pins 39, 40): LVDS Serial Data Output for ADC Channel 4. The conversion result is shifted CH4 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDOA in SDR mode, 13 SCK edges in DDR mode. Terminate with a 100Ω resistor at the receiver (FPGA).

SCK$^+$, SCK$^-$ (Pins 41, 42): Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins in SDR mode ($\overline{SDR}$/DDR = LOW). In DDR mode ($\overline{SDR}$/DDR = HIGH) each edge of this clock shifts the conversion result MSB first onto the SDO pins. These pins must be differentially terminated by an external 100Ω resistor at the receiver (ADC).

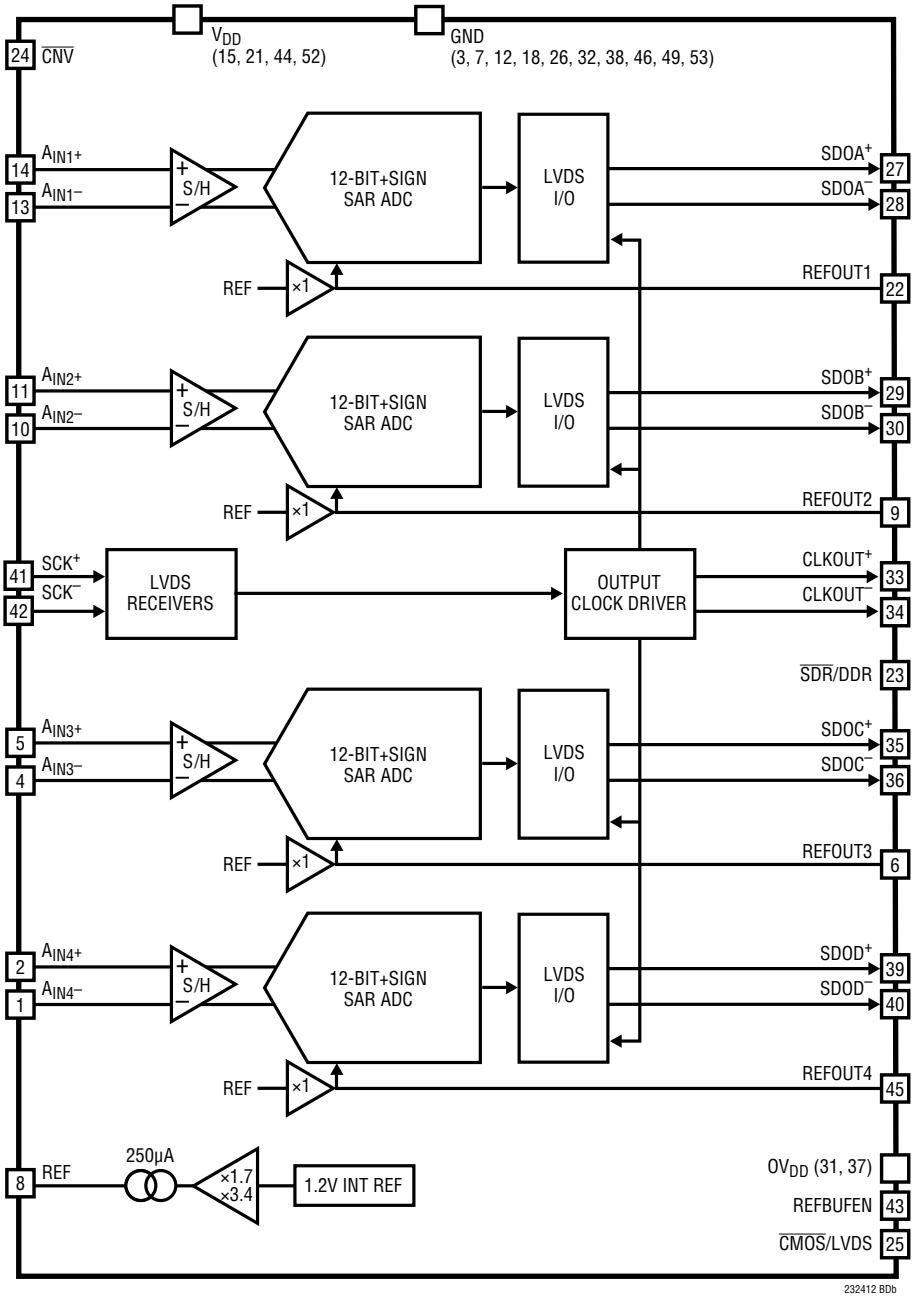
FUNCTIONAL BLOCK DIAGRAM

CMOS IO Mode



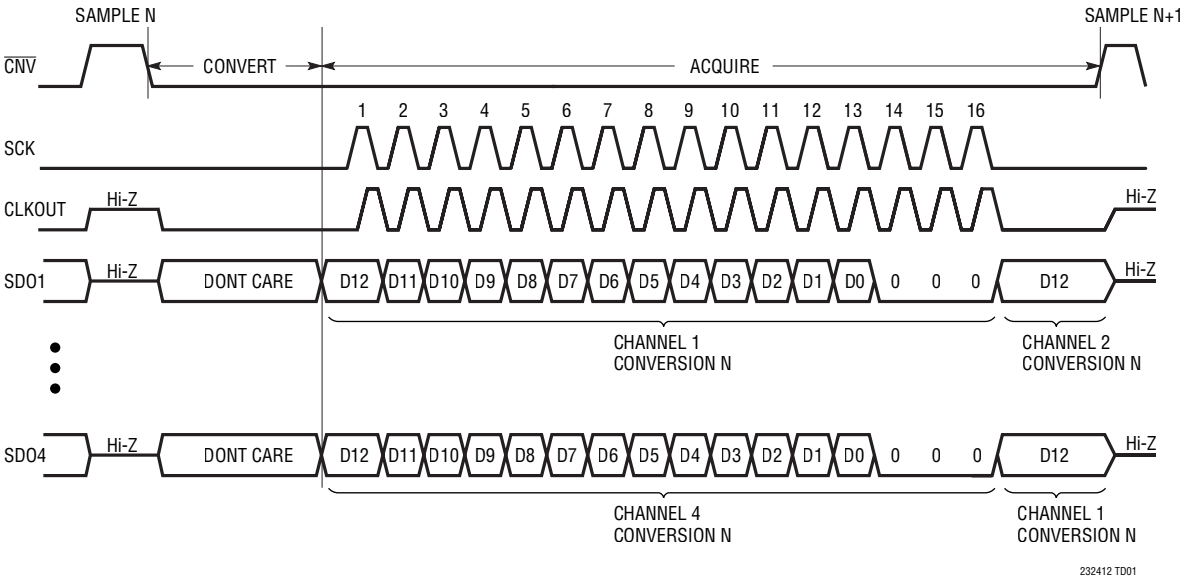
FUNCTIONAL BLOCK DIAGRAM

LVDS IO Mode

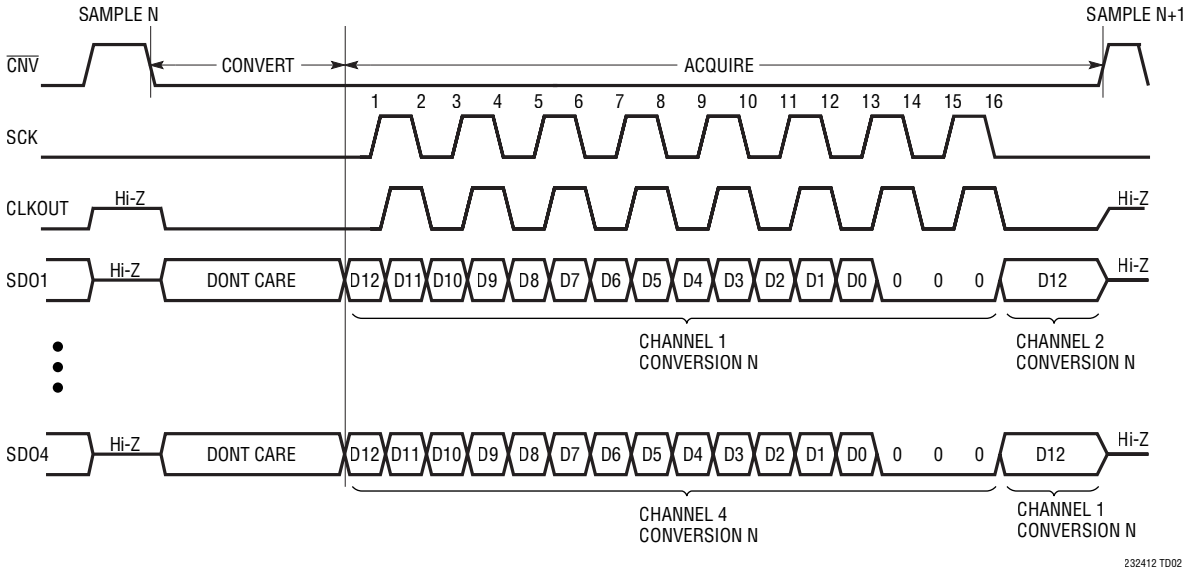


TIMING DIAGRAM

SDR Mode, CMOS (Reading 1 Channel per SDO)

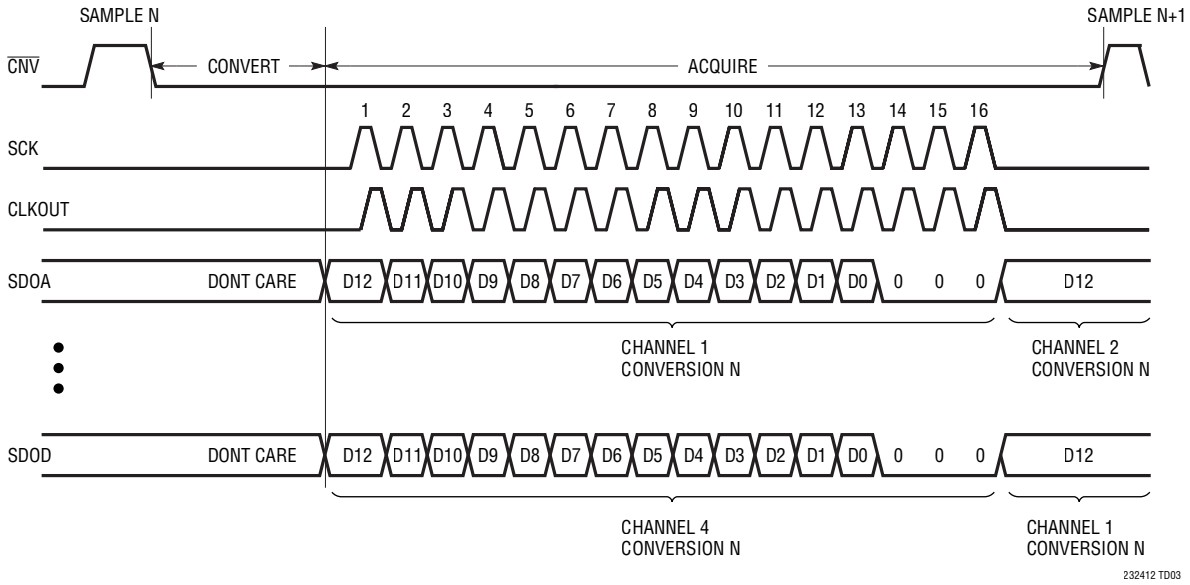


DDR Mode, CMOS (Reading 1 Channel per SDO)

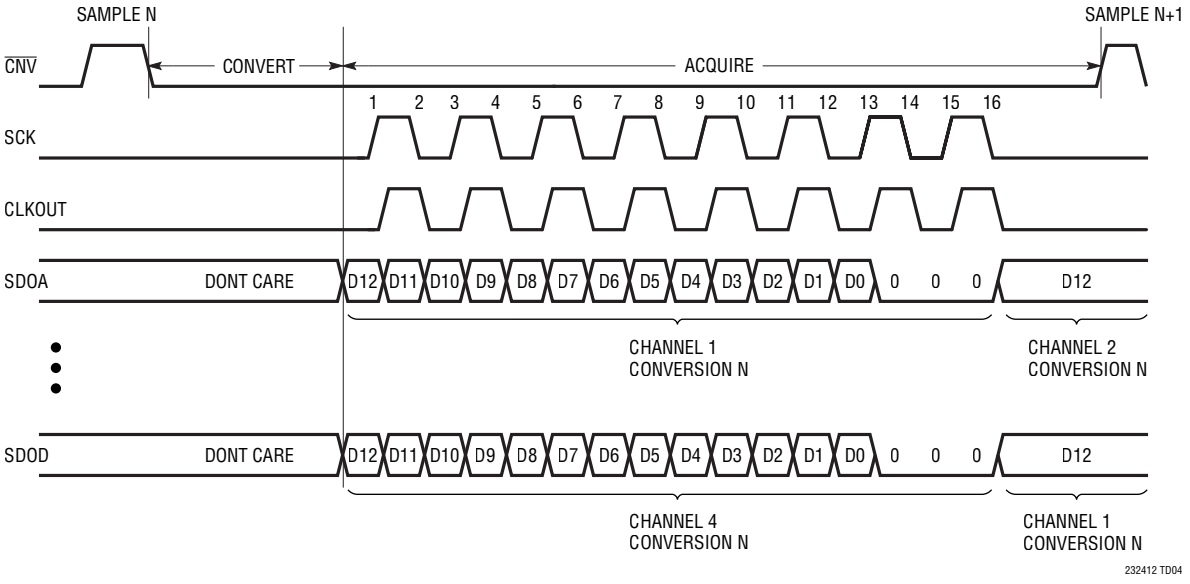


TIMING DIAGRAM

SDR Mode, LVDS (Reading 1 Channel per SDO Pair)



DDR Mode, LVDS (Reading 1 Channel per SDO Pair)



APPLICATIONS INFORMATION

OVERVIEW

The LTC2324-12 is a low noise, high speed 13-bit successive approximation register (SAR) ADC with differential inputs and a wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2324-12 has a $4V_{P-P}$ or $8V_{P-P}$ differential input range, making it ideal for applications which require a wide dynamic range. The LTC2324-12 achieves ±0.5LSB INL typical, no missing codes at 12 bits and 78dB SNR.

The LTC2324-12 has an onboard reference buffer and low drift (20ppm/°C max) 4.096V temperature-compensated reference. The LTC2324-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 2Msps per channel throughput with no-cycle latency makes the LTC2324-12 ideally suited for a wide variety of high speed applications. The LTC2324-12 dissipates only 40mW per channel. Nap and sleep modes are also provided to reduce the power consumption of the LTC2324-12 during inactive periods for further power savings.

CONVERTER OPERATION

The LTC2324-12 operates in two phases. During the acquisition phase, the sample capacitor is connected to the analog input pins A_{IN}^+ and A_{IN}^- to sample the differential analog input voltage, as shown in Figure 3. A falling edge on the $\overline{CNV}$ pin initiates a conversion. During the conversion phase, the 13-bit CDAC is sequenced through a successive approximation algorithm effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., $V_{REFOUT}/2$, $V_{REFOUT}/4$ … $V_{REFOUT}/32768$) using a differential comparator. At the end of conversion, a CDAC output approximates the sampled analog input. The ADC control logic then prepares the 12-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2324-12 digitizes the full-scale voltage of 2 × REFOUT1,2,3,4 into 2^{13} levels, resulting in an LSB size of 1mV with REF = 4.096V. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format.

Analog Input

The differential inputs of the LTC2324-12 provide great flexibility to convert a wide variety of analog signals with no configuration required. The LTC2324-12 digitizes the difference voltage between the A_{IN}^+ and A_{IN}^- pins while supporting a wide common mode input range. The analog input signals can have an arbitrary relationship to each other, provided that they remain between V_{DD} and GND. The LTC2324-12 can also digitize more limited classes of analog input signals such as pseudo-differential unipolar/bipolar and fully differential with no configuration required.

The analog inputs of the LTC2324-12 can be modeled by the equivalent circuit shown in Figure 3. The back-to-back diodes at the inputs form clamps that provide ESD protection. In the acquisition phase, 10pF (C_{IN}) from the sampling capacitor in series with approximately

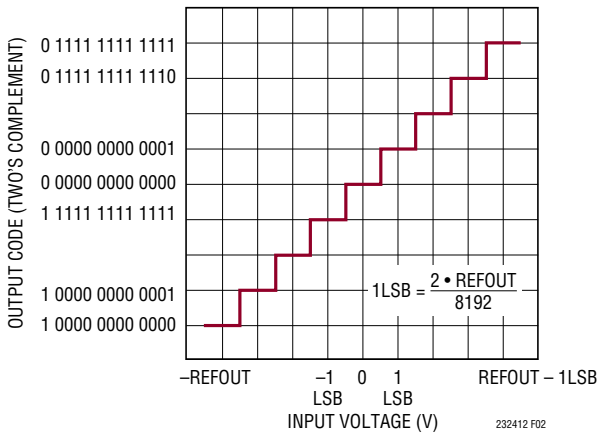


Figure 2. LTC2324-12 Transfer Function

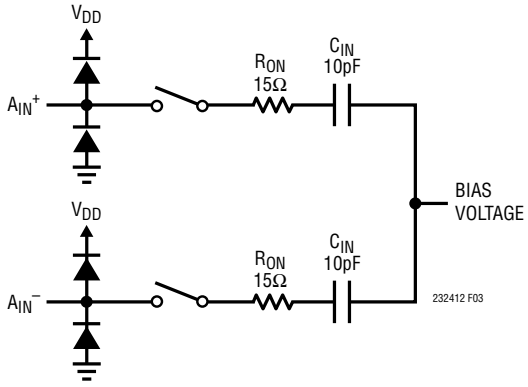


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2324-12

APPLICATIONS INFORMATION

15Ω (R_{ON}) from the on-resistance of the sampling switch is connected to the input. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC sampler. The inputs of the ADC core draw a small current spike while charging the C_{IN} capacitors during acquisition.

Single-Ended Signals

Single-ended signals can be directly digitized by the LTC2324-12. These signals should be sensed pseudo-differentially for improved common mode rejection. By connecting the reference signal (e.g., ground sense) of the main analog signal to the other A_{IN} pin, any noise or disturbance common to the two signals will be rejected by the high CMRR of the ADC. The LTC2324-12 flexibility handles both pseudo-differential unipolar and bipolar signals, with no configuration required. The wide common mode input range relaxes the accuracy requirements of any signal conditioning circuits prior to the analog inputs.

Pseudo-Differential Bipolar Input Range

The pseudo-differential bipolar configuration represents driving one of the analog inputs at a fixed voltage, typically $V_{REF}/2$, and applying a signal to the other A_{IN} pin. In this case the analog input swings symmetrically around the fixed input yielding bipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 4, and the corresponding transfer function in Figure 5. The fixed analog input pin need not be set at $V_{REF}/2$, but at some point within the V_{DD} rails allowing the alternate input to swing symmetrically around this voltage. If the input signal ($A_{IN}^+ - A_{IN}^-$) swings beyond ±REFOUT1,2,3,4/2, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

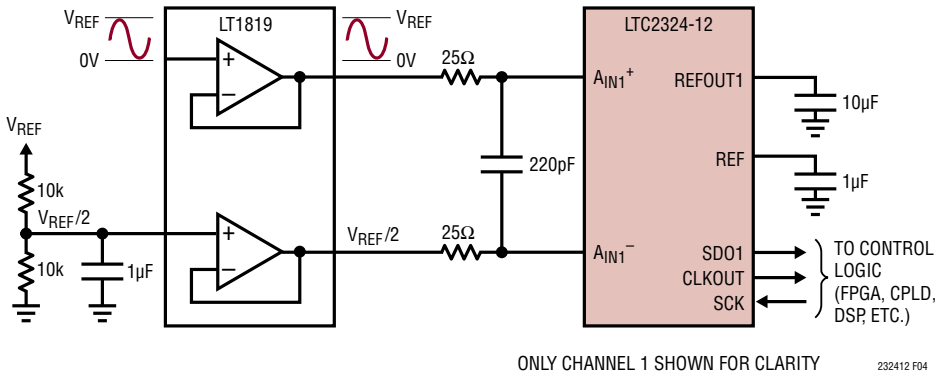


Figure 4. Pseudo-Differential Bipolar Application Circuit

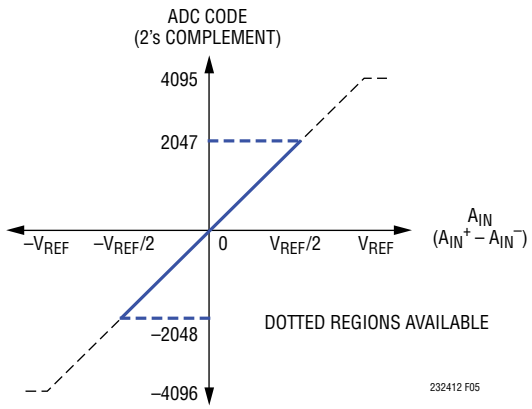


Figure 5. Pseudo-Differential Bipolar Transfer Function

APPLICATIONS INFORMATION

Pseudo-Differential Unipolar Input Range

The pseudo-differential unipolar configuration represents driving one of the analog inputs at ground and applying a signal to the other A_{IN} pin. In this case, the analog input swings between ground and V_{REF} yielding unipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 6, and the corresponding transfer function in Figure 7. If the input signal ($A_{IN}^+ - A_{IN}^-$) swings negative, valid codes will be generated by the ADC and must be clamped by the user, if necessary. A possible variant of this mode would be to tie A_{IN}^+ to ground and drive A_{IN}^- between ground and V_{REF} yielding a code span illustrated by the dotted line in Figure 7.

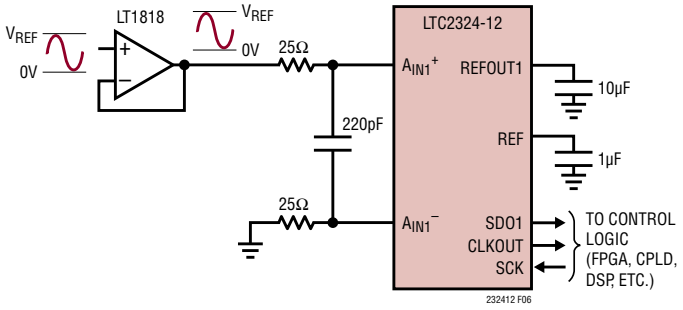


Figure 6. Pseudo-Differential Unipolar Application Circuit

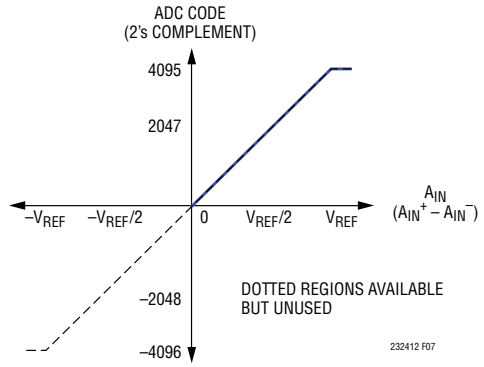


Figure 7. Pseudo-Differential Unipolar Transfer Function

Single-Ended-to-Differential Conversion

While single-ended signals can be directly digitized as previously discussed, single-ended to differential conversion circuits may also be used when higher dynamic range is desired. By producing a differential signal at the inputs of the LTC2324-12, the signal swing presented to the ADC is maximized, thus increasing the achievable SNR.

The LT®1819 high speed dual operational amplifier is recommended for performing single-ended-to-differential conversions, as shown in Figure 8. In this case, the first amplifier is configured as a unity-gain buffer and the single-ended input signal directly drives the high impedance input of this amplifier.

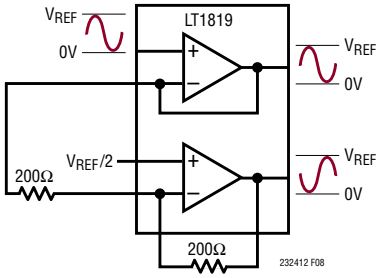


Figure 8. Single-Ended to Differential Driver

Fully-Differential Inputs

To achieve the best distortion performance of the LTC2324-12, we recommend driving a fully-differential signal through LT1819 amplifiers configured as two unity-gain buffers, as shown in Figure 9. This circuit achieves the full data sheet THD specification of –88dB at input frequencies up to 500kHz. A fully-differential input signal can span the maximum full-scale of the ADC, up to ±REFOUT1,2,3,4. The common mode input voltage can span the entire supply range up to V_{DD}, limited by the input signal swing. The fully-differential configuration is illustrated in Figure 10, with the corresponding transfer function illustrated in Figure 11.

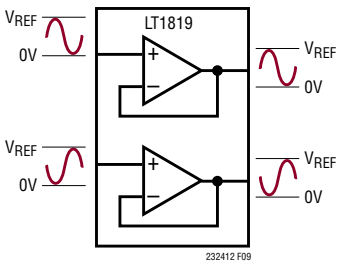


Figure 9. LT1819 Buffering a Fully-Differential Signal Source

APPLICATIONS INFORMATION

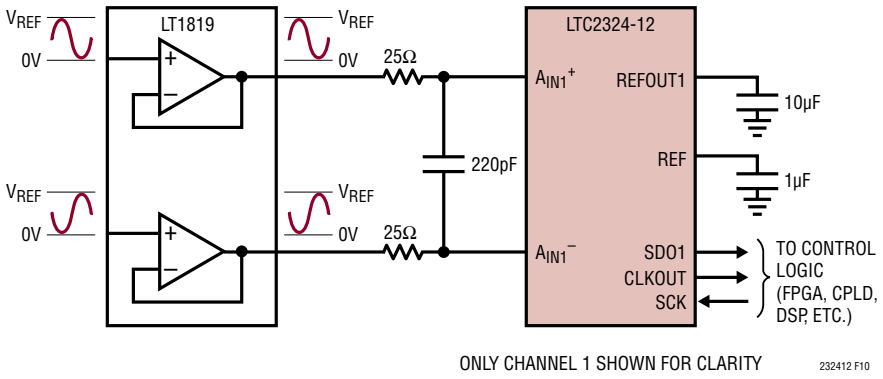


Figure 10. Fully-Differential Application Circuit

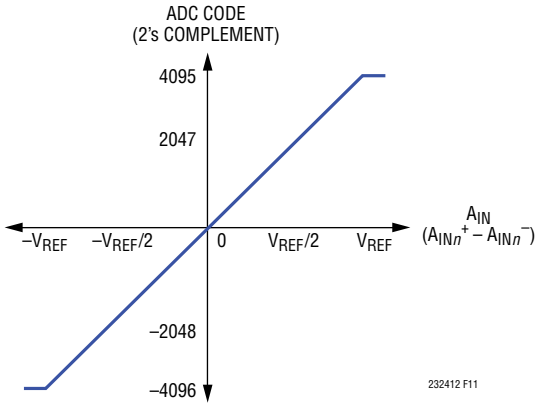


Figure 11. Fully-Differential Transfer Function

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2324-12 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC inputs draw a current spike when during acquisition.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2324-12. The amplifier provides low output impedance to minimize gain error and allows for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs, which draw a small current spike during acquisition.

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with a low bandwidth filter to minimize noise. The simple 1-pole RC lowpass filter shown in Figure 12 is sufficient for many applications.

APPLICATIONS INFORMATION

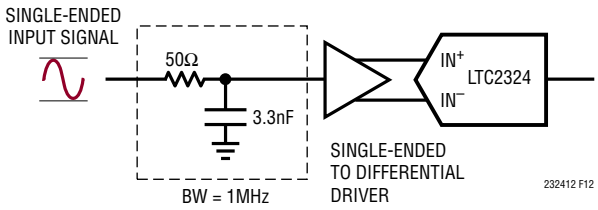


Figure 12. Input Signal Chain

The sampling switch on-resistance (R_{ON}) and the sample capacitor (C_{IN}) form a second lowpass filter that limits the input bandwidth to the ADC core to 110MHz. A buffer amplifier with a low noise density must be selected to minimize the degradation of the SNR over this bandwidth.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

ADC REFERENCE

Internal Reference

The LTC2324-12 has an on-chip, low noise, low drift (20ppm/°C max), temperature compensated bandgap reference. It is internally buffered and is available at REF (Pin 8). The reference buffer gains the internal reference voltage to 4.096V for supply voltages V_{DD} = 5V and to 2.048V for V_{DD} = 3.3V. The REF pin also drives the four internal reference buffers with a current limited output (250µA) so it may be easily overdriven with an external reference in the range of 1.25V to 5V. Bypass REF to GND with a 1µF (X5R, 0805 size) ceramic capacitor to compensate the reference buffer and minimize noise. The 1µF capacitor should be as close as possible to the LTC2324-12 package to minimize wiring inductance. The REFBUFEN pin does not affect the internal REF buffer. The voltage on the REF pin must be externally buffered if used for external circuitry.

Table 1. Reference Configurations and Ranges

REFERENCE CONFIGURATION	V_{DD}	REFBUFEN	REF PIN	REFOUT1,2,3,4 PIN	DIFFERENTIAL INPUT RANGE
Internal Reference with Internal Buffers	5V	5V	4.096V	4.096V	±4.096V
	3.3V	3.3V	2.048V	2.048V	±2.048V
Common External Reference with Internal Buffer (REF Pin Externally Overdriven)	5V	5V	1.25V to 5V	1.25V to 3.3V	±1.25V to ±5V
	3.3V	3.3V	1.25V to 5V	1.25V to 3.3V	±1.25V to ±3.3V
External Reference with REF Buffers Disabled	5V	0V	4.096V	1.25V to 5V	±1.25V to ±5V
	3.3V	0V	2.048V	1.25V to 3.3V	±1.25V to ±3.3V

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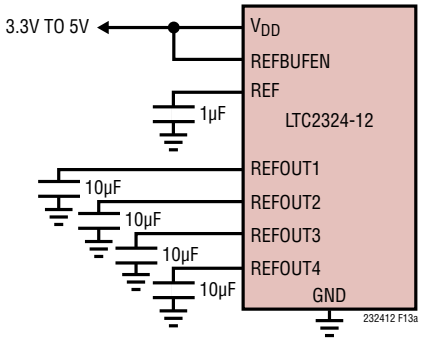
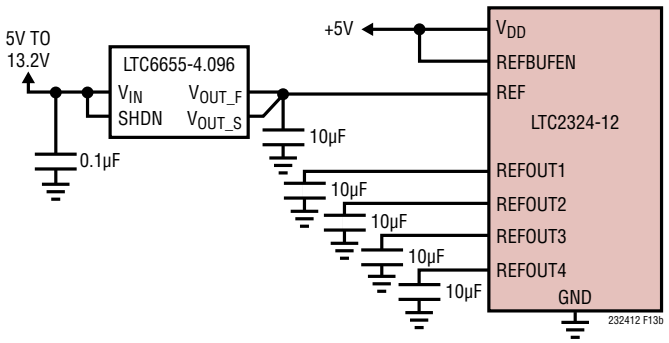
External Reference

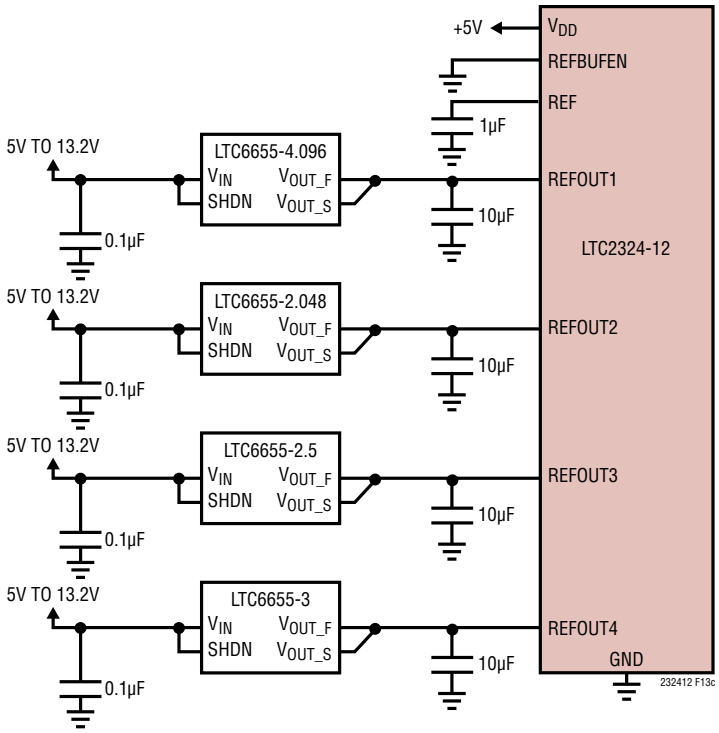
The internal REFOUT1,2,3,4 buffers can also be overdriven from 1.25V to 5V with an external reference at REFOUT1,2,3,4 as shown in Figure 13(c). To do so, REFBUFEN must be grounded to disable the REF buffers. A 55k internal resistance loads the REFOUT1,2,3,4 pins when the REF buffers are disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFOUT. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-4.096. By using a 5V reference, a higher SNR can be achieved. We recommend bypassing the LTC6655-5 with a 10µF ceramic capacitor (X5R, 0805 size) close to each of the REFOUT1,2,3,4 pins. If the REF pin voltage is used as a REFOUT reference when REFBUFEN is connected to GND, it should be buffered externally.



(13a) LTC2324-12 Internal Reference Circuit



(13b) LTC2324-12 with a Shared External Reference Circuit



(13c) LTC2324-12 with Different External Reference Voltages

Figure 13. Reference Connections

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Internal Reference Buffer Transient Response

The REFOUT1,2,3,4 pins of the LTC2324-12 draw charge (Q_{CONV}) from the external bypass capacitors during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to $I_{REF} = Q_{CONV}/t_{CYC}$. Thus, the DC current draw of $I_{REFOUT1,2,3,4}$ depends on the sampling rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 14 , I_{REFBUF} quickly goes from approximately ~75µA to a maximum of 500µA for REFOUT = 5V at 2Msps. This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFOUT will affect the accuracy of the output code. If an external reference is used to overdrive REFOUT1,2,3,4, the fast settling LTC6655 reference is recommended.

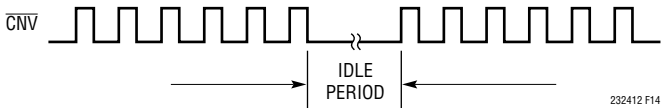

Figure 14. $\overline{CNV}$ Waveform Showing Burst Sampling

DYNAMIC PERFORMANCE

Fast Fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2324-12 provides guaranteed tested limits for both AC distortion and noise measurements. The typical large signal transient pulse response of the ADC is illustrated in Figure 15.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is bandlimited to frequencies from above DC and below half the sampling frequency. Figure 16 shows that the LTC2324-12 achieves a typical SINAD of 78dB at a 2MHz sampling rate with a 500kHz input.

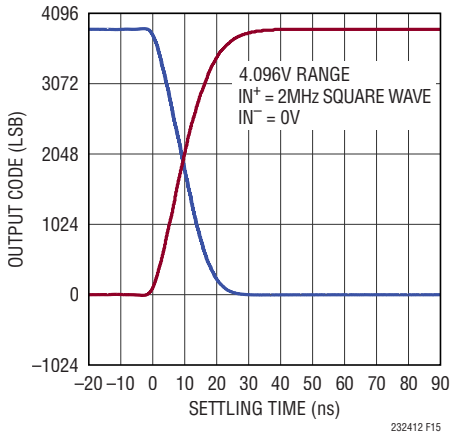

Figure 15. Transient Response of the LTC2324-12

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 16 shows that the LTC2324-12 achieves a typical SNR of 78dB at a 2MHz sampling rate with a 500kHz input.

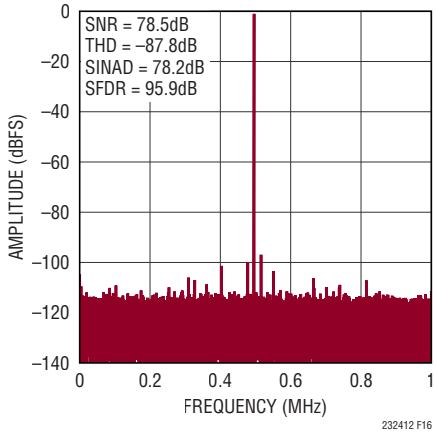

Figure 16. 32k Point FFT of the LTC2324-12

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N{}^2}}{V1}$$

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where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2324-12 requires two power supplies: the 3.3V to 5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2324-12 to communicate with any digital logic operating between 1.8V and 2.5V. When using LVDS I/O, the OV_{DD} supply must be set to 2.5V.

Power Supply Sequencing

The LTC2324-12 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2324-12 has a power-on-reset (POR) circuit that will reset the LTC2324-12 at initial power-up or whenever the power supply voltage drops below 2V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 10ms after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

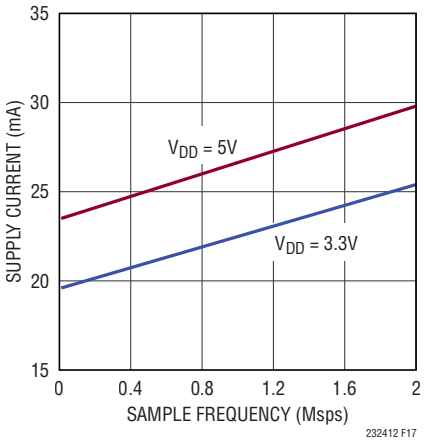

Figure 17. Power Supply Current of the LTC2324-12 vs Sampling Rate

TIMING AND CONTROL

$\overline{CNV}$ Timing

The LTC2324-12 sampling and conversion is controlled by $\overline{CNV}$. A rising edge on $\overline{CNV}$ will start sampling and the falling edge starts the conversion and readout process. The conversion process is timed by the SCK input clock. For optimum performance, $\overline{CNV}$ should be driven by a clean low jitter signal. The Typical Application at the back of the data sheet illustrates a recommended implementation to reduce the relatively large jitter from an FPGA $\overline{CNV}$ pulse source. Note the low jitter input clock times the falling edge of the $\overline{CNV}$ signal. The rising edge jitter of $\overline{CNV}$ is much less critical to performance. The typical pulse width of the $\overline{CNV}$ signal is 30ns with < 1.5ns rise and fall times at a 2Msps conversion rate.

SCK Serial Data Clock Input

In SDR mode ($\overline{SDR}$/DDR Pin 23 = GND), the falling edge of this clock shifts the conversion result MSB first onto the SDO pins. A 110MHz external clock must be applied at the SCK pin to achieve 2Msps throughput using all four SDO outputs. In DDR mode ($\overline{SDR}$/DDR Pin 23 = OV_{DD}), each input edge of SCK shifts the conversion result MSB first onto the SDO pins. A 55MHz external clock must be applied at the SCK pin to achieve 2Msps throughput using all four SDO1 through SDO4 outputs.

CLKOUT Serial Data Clock Output

The CLKOUT output provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver. For low throughput speed applications, CLKOUT can be disabled by tying Pin 34 to OV_{DD}.

Nap/Sleep Modes

Nap mode is a method to save power without sacrificing power-up delays for subsequent conversions. Sleep mode has substantial power savings, but a power-up delay is incurred to allow the reference and power systems to become valid. To enter nap mode on the LTC2324-12, the SCK signal must be held high or low and a series of

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two $\overline{CNV}$ pulses must be applied. This is the case for both CMOS and LVDS modes. The second rising edge of $\overline{CNV}$ initiates the nap state. The nap state will persist until either a single rising edge of SCK is applied, or further $\overline{CNV}$ pulses are applied. The SCK rising edge will put the LTC2324-12 back into the operational (full-power) state. When in nap mode, two additional pulses will put the LTC2324-12 in sleep mode. When configured for CMOS I/O operation, a single rising edge of SCK can return the LTC2324-12 into operational mode. A 10ms delay is necessary after exiting sleep mode to allow the reference buffer to recharge the external filter capacitor. In LVDS mode, exit sleep mode by supplying a fifth $\overline{CNV}$ pulse. The fifth pulse will return the LTC2324-12 to operational mode, and further SCK pulses will keep the part from re-entering nap and sleep modes. The fifth SCK pulse also works in CMOS mode as a method to exit sleep. In the absence of SCK pulses, repetitive $\overline{CNV}$ pulses will cycle the LTC2324-12 between operational, nap and sleep modes indefinitely.

Refer to the timing diagrams in Figure 18, Figure 19, Figure 20 and Figure 21 for more detailed timing information about sleep and nap modes.

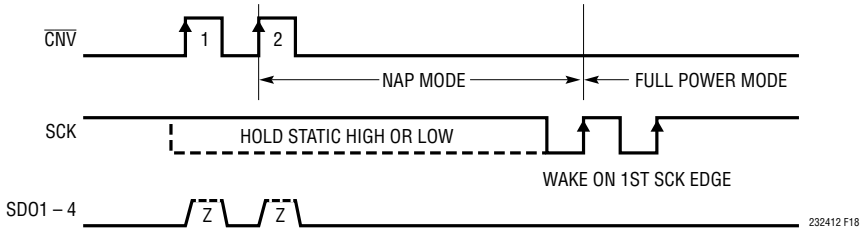

Figure 19. CMOS and LVDS Mode NAP and WAKE Using SCK

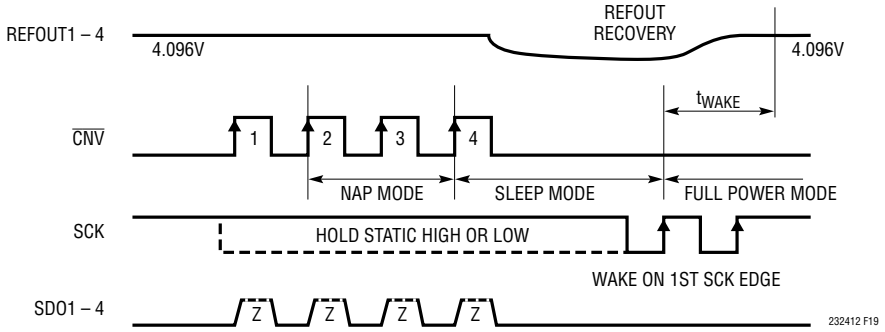

Figure 18. CMOS Mode SLEEP and WAKE Using SCK

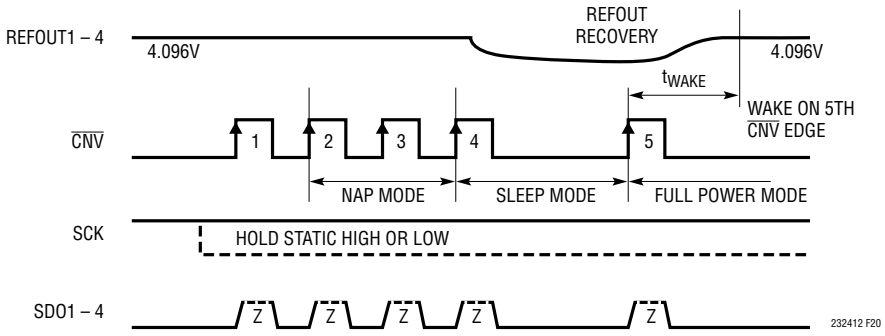

Figure 20. LVDS and CMOS Mode SLEEP and WAKE Using $\overline{CNV}$

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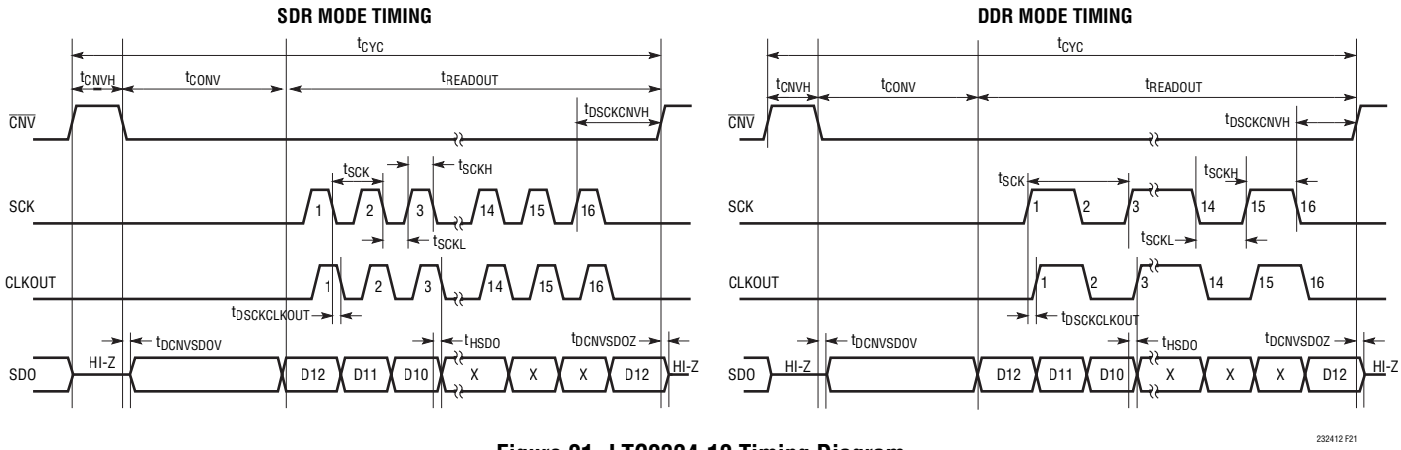

Figure 21. LTC2324-12 Timing Diagram

DIGITAL INTERFACE

The LTC2324-12 features a serial digital interface that is simple and straightforward to use. The flexible OV_{DD} supply allows the LTC2324-12 to communicate with any digital logic operating between 1.8V and 2.5V. In addition to a standard CMOS SPI interface, the LTC2324-12 provides an optional LVDS SPI interface to support low noise digital design. The $\overline{CMOS}$/LVDS pin is used to select the digital interface mode. The SCK input clock shifts the conversion result MSB first on the SDO pins. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver. In CMOS mode, use the SDO1 – SDO4, and CLKOUT pins as outputs. Use the SCK pin as an input. In LVDS mode, use the $SDOA^+$/$SDOA^-$ through $SDOD^+$/$SDOD^-$ and $CLKOUT^+$/$CLKOUT^-$ pins as differential outputs. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA). The SCK^+/SCK^- pins are differential inputs and must be terminated differentially by an external 100Ω resistor at the receiver(ADC).

SDR/DDR Modes

The LTC2324-12 has an SDR (single data rate) and DDR (double data rate) mode for reading conversion data from the SDO pins. In both modes, CLKOUT is a delayed version of SCK. In SDR mode, each negative edge of SCK shifts the conversion data out the SDO pins. In DDR mode, each edge of the SCK input shifts the conversion data out. In DDR mode, the required SCK frequency is half of what is required in SDR mode. Tie SDR/DDR to ground to configure for SDR mode and to OV_{DD} for DDR mode. The CLKOUT signal is a delayed version of the SCK input and is phase aligned with the SDO data. In SDR mode, the SDO transitions on the falling edge of CLKOUT as illustrated in Figure 21. We recommend using the rising edge of CLKOUT to latch the SDO data into the FPGA register in SDR mode. In DDR mode, the SDO transitions on each input edge of SCK. We recommend using the CLKOUT rising and falling edges to latch the SDO data into the FPGA registers in DDR mode. Since the CLKOUT and SDO data are phase aligned, we recommend digitally delaying the SDO data in the FPGA to provide adequate setup and hold timing margins in DDR mode.

Multiple Data Lanes

The LTC2324-12 has up to four SDO data lanes in CMOS mode and four SDO lanes in LVDS mode. In CMOS mode, the number of possible data lanes range from four (SDO1, SDO2, SDO3 and SDO4), two (SDO1 and SDO3) and one (SDO1). Generally, the more data lanes used, the lower the required SCK frequency. When using less than four lanes in CMOS mode, there is a limit on the maximum possible conversion frequency (see Table 2). Each SDO pin will hold the MSB of the conversion data. In DDR mode you can use a SCK frequency half of SDR mode. See Table 2 for examples of various possibilities and the resulting SCK frequency required.

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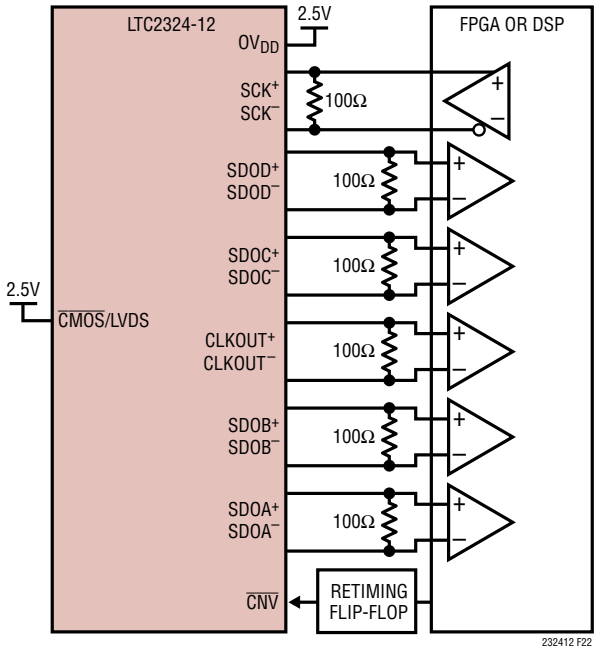

Figure 22. LTC2324-12 Using the LVDS Interface

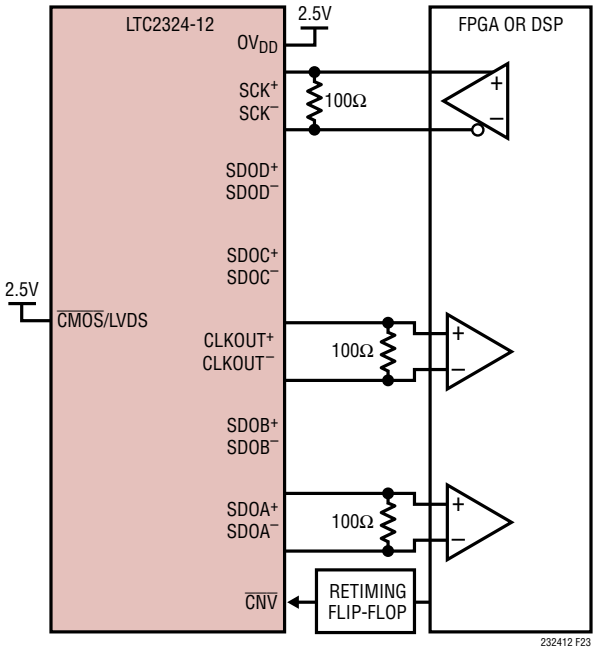

Figure 23. LTC2324-12 Using the LVDS Interface with One Lane

Table 2. Conversion Frequency for Various I/O Modes

I/O MODE	$\overline{CMOS}$/ LVDS PIN	$\overline{SDR}$/ DDR PIN	SDO1 – 4 LANES	SDOA – D LANES	SCK FREQ (MHz)	CLKOUT FREQ (MHz)	SCK CYCLES	OV_{DD}	CONVERSION FREQUENCY (Msps/CH)
CMOS	GND (CMOS)	GND (SDR)	SDO1 – SDO4		110	110	16	1.8V to 2.5V	2.0
		OV_{DD} (DDR)	SDO1 – SDO4		55	55	8		2.0
		OV_{DD} (DDR)	SDO1, SDO3		55	55	32		1.5
		GND (SDR)	SDO1		110	110	64		1.0
LVDS	OV_{DD} (LVDS)	GND (SDR)		SDOA – SDOD	300	300	16	2.5V	2.0
		OV_{DD} (DDR)		SDOA – SDOD	150	150	8		2.0
		OV_{DD} (DDR)		SDOA, SDOC	150	150	16		2.0
		GND (SDR)		SDOA	300	300	64		2.0

Notes: Conversion Period (SDR) = $t_{CNV\_MIN} + t_{CONV\_MAX} + (64/(Lanes \bullet f_{SCK}))$
Conversion Period (DDR) = $t_{CNV\_MIN} + t_{CONV\_MAX} + (32/(Lanes \bullet f_{SCK}))$
Conversion Frequency = 1/Conversion Period
SCK Cycles (SDR) = 64/Lanes
SCK Cycles (DDR) = 32/Lanes

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CMOS

In CMOS mode, the number of possible data lanes range from four (SDO1, SDO2, SDO3 and SDO4), two (SDO1 and SDO3) and one (SDO1). As suggested in the CMOS Timing Diagrams, each SDO lane outputs the conversion results for all analog input channels in a sequential circular manner. For example, the first conversion result on SDO1 corresponds to analog input channel 1, followed by the conversion results for channels 2 through 4. The data output on SDO1 then wraps back to channel 1 and this pattern repeats indefinitely. Other SDO lanes follow a similar circular pattern except the first conversion result presented on each lane corresponds to its associated analog input channel.

Applications that cannot accommodate the full four lanes of serial data may employ fewer lanes without reconfiguring the LTC2324-12. For example, capturing the first two conversion results (32 SCK cycles total in SDR mode and 32 SCK edges in DDR mode) from SDO1 and SDO3 provides data for analog input channels 1 and 2, 3 and 4, respectively, using two output lanes. Similarly, capturing the first four conversion results (64 SCK cycles total in SDR mode and 64 SCK edges in DDR mode) from SDO1 provides data for analog input channels 1 to 4, using one output lane. Generally, the more data lanes used, the lower the required SCK frequency. When using less than four lanes in CMOS mode, there is a limit on the maximum possible conversion frequency. See Table 2 for examples of various possibilities and the resulting SCK frequency required.

LVDS

In LVDS mode, the number of possible data lane pairs range from four (SDOA – SDOD), two (SDOA and SDOC) and one (SDOA). As suggested in the LVDS Timing Diagrams, each SDO lane pair outputs the conversion results for all analog input channels in a sequential circular manner. For example, the first conversion result on SDOA corresponds to analog input channel 1, followed by the conversion results for channels 2 through 4. The data output on SDOA then wraps back to channel 1 and this pattern repeats indefinitely. Other SDO lanes follow a similar circular pattern except the first conversion result presented on each lane corresponds to its associated analog input channel pairs (SDOA: analog input 1, SDOB: analog input 2, SDOC: analog input 3 and SDOD: analog input 4).

Applications that cannot accommodate the full four lanes of serial data may employ fewer lanes without reconfiguring the LTC2324-12. For example, capturing the first two conversion results (32 SCK cycles total in SDR mode and 32 SCK edges in DDR mode) from SDOA and SDOC provides data for analog input channels 1 through 4, respectively, using two output lanes. If only one lane can be accommodated, capturing the first four conversion results (64 SCK cycles total in SDR mode and 64 SCK edges in DDR mode) from SDOA provides data for all analog input channels. Generally, the more data lanes used, the lower the required SCK frequency. When using less than four lanes in LVDS mode, there is a limit on the maximum possible conversion frequency. See Table 2 for examples of various possibilities and the resulting SCK frequency required.

BOARD LAYOUT

To obtain the best performance from the LTC2324-12, a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals adjacent to analog signals or underneath the ADC.

Supply bypass capacitors should be placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. A single solid ground plane is recommended for this purpose. When possible, screen the analog input traces using ground.

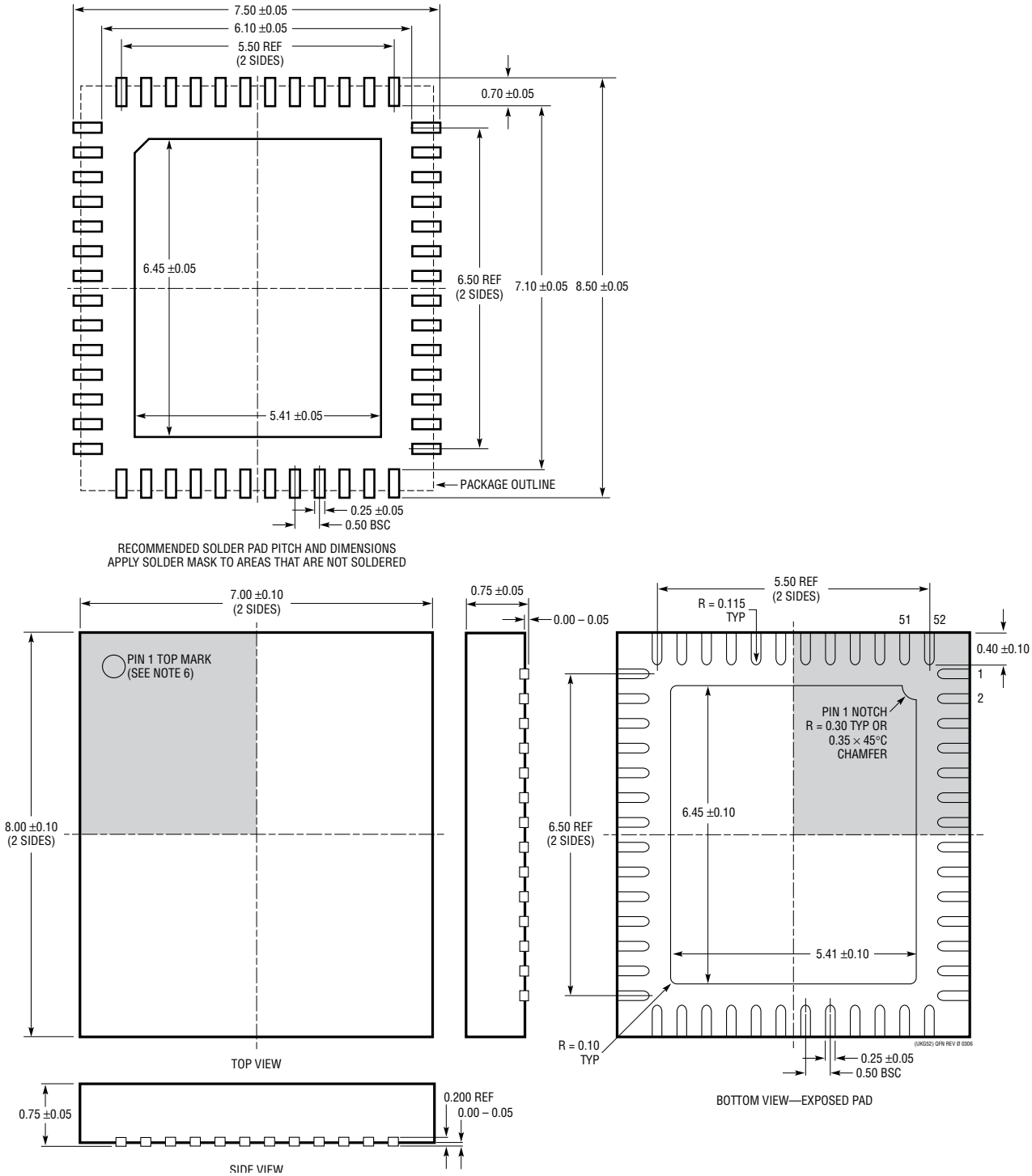
Recommended Layout

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to DC2395A, the evaluation kit for the LTC2324-12.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2324-12#packaging for the most recent package drawings.

UKG Package
52-Lead Plastic QFN (7mm × 8mm)
(Reference LTC DWG # 05-08-1729 Rev Ø)

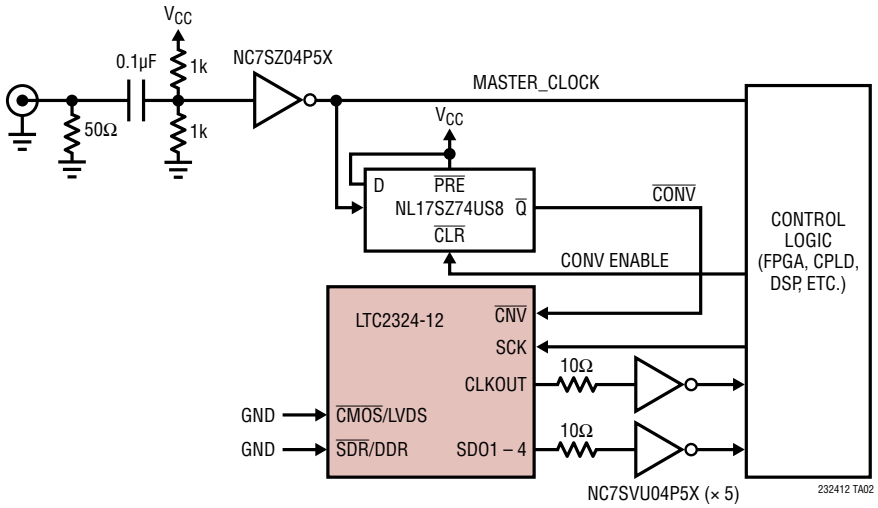


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/17	Corrected DNL typical value	3

TYPICAL APPLICATION

Low Jitter Clock Timing with RF Sine Generator Using Clock Squaring/Level-Shifting Circuit and Retiming Flip-Flop



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2311-16/LTC2311-14/ LTC2311-12	16-/14-/12-Bit, 5Msps Differential Input ADC	3.3V Supply, 1-Channel 40mW, 20ppm/°C Internal Reference, Flexible Inputs, 16-Lead MSOP Package
LTC2320-16/LTC2320-14/ LTC2320-12	16-/14-/12-Bit, Octal, 1.5Msps/Channel Simultaneous Sampling ADC	3.3V/5V Supply, 20mW/Channel, 20ppm/°C Internal Reference, Flexible Inputs, 7mm × 8mm QFN-52 Package
LTC2321-16/LTC2321-14/ LTC2321-12	16-/14-/12-Bit, Dual 2Msps, Simultaneous Sampling ADC	3.3V/5V Supply, 40mW/Channel, 20ppm/°C Max Internal Reference, Flexible Inputs, 4mm × 5mm QFN-28 Package
LTC2370-16/LTC2368-16/ LTC2367-16/LTC2364-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 94dB SNR, 5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16/ LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
DACs		
LTC2632	Dual 12-/10-/8-Bit, SPI V_{OUT} DACs with Internal Reference	2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, 8-Pin ThinSOT™ Package
LTC2602/LTC2612/ LTC2622	Dual 16-/14-/12-Bit SPI V_{OUT} DACs with External Reference	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, 8-Lead MSOP Package
References		
LTC6655	Precision Low Drift, Low Noise Buffered Reference	5V/4.096V/3.3V/3V/2.5V/2.048V/1.25V, 2ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift, Low Noise Buffered Reference	5V/4.096V/3.3V/3V/2.5V/2.048V/1.25V, 5ppm/°C, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LT1818/LT1819	400MHz, 2500V/µs, 9mA Single/Dual Operational Amplifiers	–85dBc Distortion at 5MHz, 6nV/√Hz Input Noise Voltage, 9mA Supply Current, Unity-Gain Stable
LT1806	325MHz, Single, Rail-to-Rail Input and Output, Low Distortion, Low Noise Precision Op Amps	–80dBc Distortion at 5MHz, 3.5nV/√Hz Input Noise Voltage, 9mA Supply Current, Unity-Gain Stable
LT6200	165MHz, Rail-to-Rail Input and Output, 0.95nV/√Hz Low Noise, Op Amp Family	Low Noise, Low Distortion, Unity-Gain Stable

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