



**THE DATASHEET OF
SI53360-B-GT**



Si53360/61/62/65 Data Sheet

Low-Jitter, LVCMOS Fanout Clock Buffers with up to 12 outputs and Frequency Range from dc to 200 MHz

The Si53360/61/62/65 family of LVCMOS fanout buffers is ideal for clock/data distribution and redundant clocking applications. The family utilizes Skyworks advanced CMOS technology to fanout clocks from dc to 200 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. Built-in LDOs deliver high PSRR performance and eliminates the need for external components simplifying low jitter clock distribution in noisy environments.

The CMOS buffers are available in multiple configurations with 8 outputs (Si53360/61/65), or dual banks of 6 outputs each (Si53362). These buffers can be paired with the Si534x clock generators and Si5xx oscillators to deliver end-to-end clock tree performance.

KEY FEATURES

- Low additive jitter: 120 fs rms
- Built-in LDOs for high PSRR performance
- Up to 12 LVCMOS Outputs from LVCMOS inputs
- Frequency range: dc to 200 MHz
- Multiple configuration options
 - Dual Bank option
 - 2:1 Input MUX option
- RoHS compliant, Pb-free
- Temperature range: -40 to +85 °C

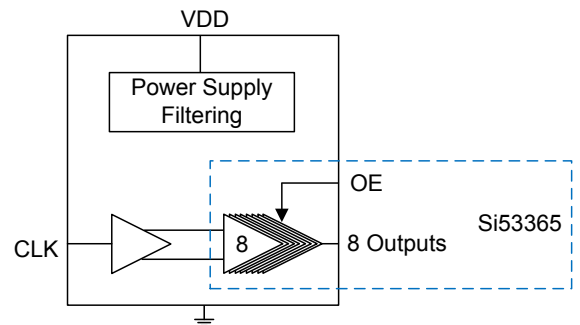
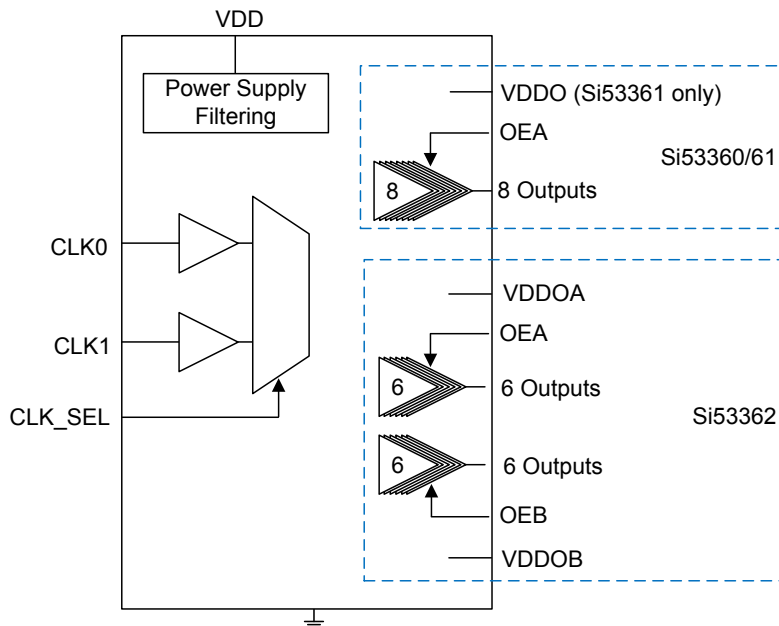


Table of Contents

| | |
|---|-----------|
| 1. Ordering Guide | 3 |
| 2. Functional Description | 4 |
| 2.1 LVCMOS Input Termination | 4 |
| 2.2 Input Mux | 4 |
| 2.3 Output Clock Termination Options | 5 |
| 2.4 AC Timing Waveforms | 6 |
| 2.5 Power Supply Noise Rejection | 6 |
| 2.6 Typical Phase Noise Performance: Single-Ended Input Clock | 7 |
| 2.7 Input Mux Noise Isolation | 8 |
| 3. Electrical Specifications | 9 |
| 4. Detailed Block Diagrams | 12 |
| 5. Si5336x Pin Descriptions | 15 |
| 5.1 Si53360 Pin Descriptions | .15 |
| 5.2 Si53361 Pin Descriptions | .17 |
| 5.3 Si53362 Pin Descriptions | .19 |
| 5.4 Si53365 Pin Descriptions | .21 |
| 6. Package Outline | 22 |
| 6.1 16-Pin TSSOP Package | .22 |
| 6.2 16-Pin QFN Package | .24 |
| 6.3 24-Pin QFN Package | .25 |
| 7. PCB Land Pattern | 26 |
| 7.1 16-Pin TSSOP Land Pattern | .26 |
| 7.2 16-Pin QFN Land Pattern | .27 |
| 7.3 24-Pin QFN Land Pattern | .29 |
| 8. Top Markings | 31 |
| 8.1 Si53360/65 Top Markings | .31 |
| 8.2 Si53361 Top Marking | .32 |
| 8.3 Si53362 Top Marking | .33 |
| 9. Revision History | 34 |

1. Ordering Guide

Table 1.1. Si5336x Ordering Guide

| Part Number | Input | LVC MOS Output | Output Enable | Frequency Range | Package |
|--------------|-------------------------------|---------------------------------------|---------------|-----------------|------------------|
| Si53360-B-GT | 2:1 selectable MUX LVC MOS | 1 bank / 8 Outputs | Single | dc to 200 MHz | 16-TSSOP |
| Si53361-B-GM | 2:1 selectable MUX LVC MOS | 1 bank / 8 Outputs (Settable VDDO) | Single | dc to 200 MHz | 16-QFN 3x3 mm |
| Si53362-B-GM | 2:1 selectable MUX LVC MOS | 2 banks / 6 Outputs | 1 per bank | dc to 200 MHz | 24-QFN 4x4 mm |
| Si53365-B-GT | 1 bank / 1 Input LVC MOS | 1 bank / 8 Outputs | Single | dc to 200 MHz | 16-TSSOP |

2. Functional Description

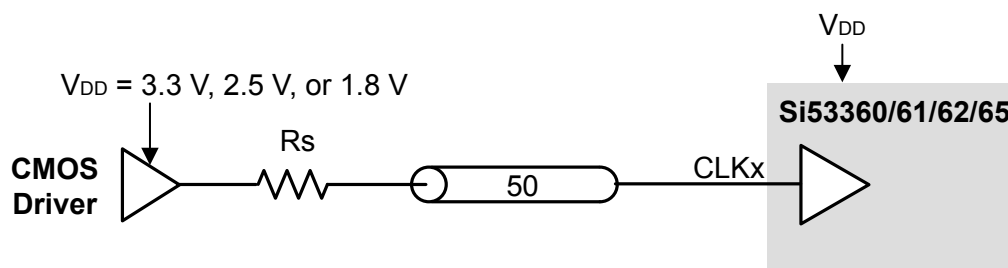
The Si53360/61/62/65 are a family of low-jitter, low skew, fixed format (LVCMOS) buffers. These devices are available in multiple configurations customized for the end application (refer to 1. [Ordering Guide](#) for more details on configurations).

2.1 LVCMOS Input Termination

The table below summarizes the various ac- and dc-coupling options supported by the LVCMOS device, and the figure shows the recommended input clock termination.

Table 2.1. LVCMOS Input Clock Options

| | LVCMOS | |
|-----------|------------|------------|
| | AC-Coupled | DC-Coupled |
| 1.8 V | No | Yes |
| 2.5/3.3 V | Yes | Yes |



Note: Value for R_s should be chosen so that the total source impedance matches the characteristic impedance of the PCB trace.

Figure 2.1. Recommended Input Clock Termination

2.2 Input Mux

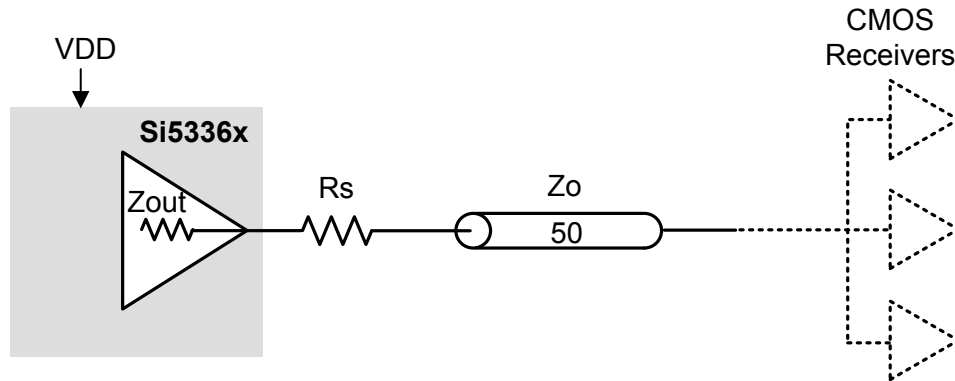
The Si53360-61/62 provide two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. The following table summarizes the input and output clock based on the input mux settings.

Table 2.2. Input Mux Logic

| CLK_SEL | CLK0 | CLK1 | Q |
|---------|------|------|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

2.3 Output Clock Termination Options

The recommended output clock termination options are shown below. Unused outputs should be left unconnected.



Note:

$R_s = 33$ ohm for 3.3 V and 2.5 V operation.

$R_s = 0$ ohm for 1.8 V operation.

Figure 2.2. LVC MOS Output Termination

2.4 AC Timing Waveforms

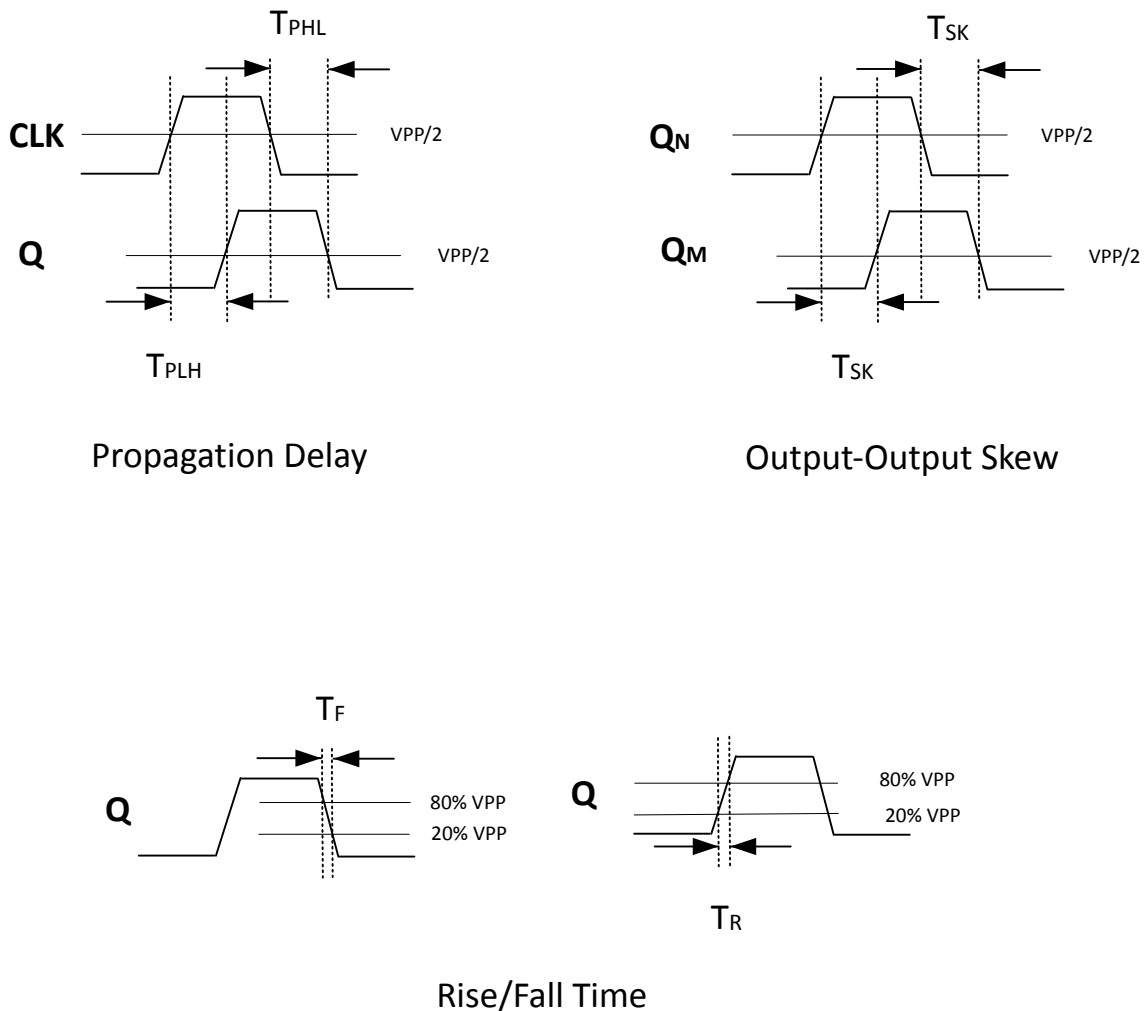


Figure 2.3. AC Timing Waveforms

2.5 Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject power supply noise and simplify low-jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for more information.

2.6 Typical Phase Noise Performance: Single-Ended Input Clock

Each of the phase noise plots superimposes Source Jitter and Total Jitter on the same diagram.

- Source Jitter - Reference clock phase noise (measured Single-ended to PNA).
- Total Jitter - Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. For more information, see 3. Electrical Specifications.

Note: To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

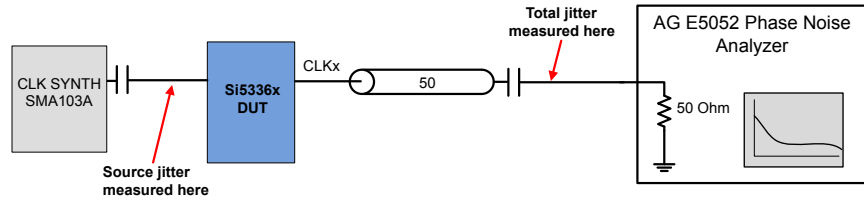


Figure 2.4. Single-ended Measurement Method

The following figure shows three phase noise plots superimposed on the same diagram.

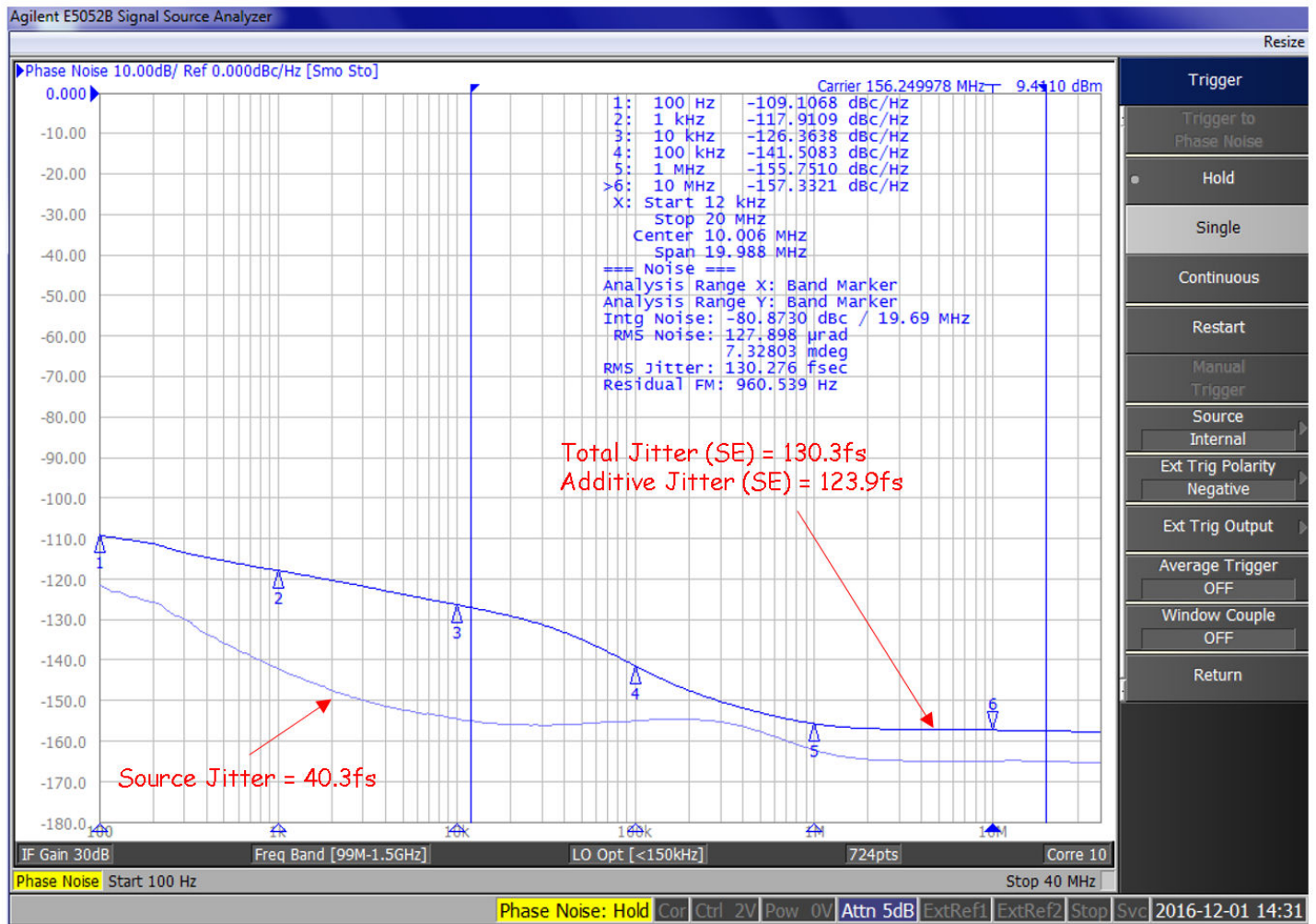


Figure 2.5. Total Jitter Single-Ended Input (156.25 MHz)

| Frequency (MHz) | Single-Ended Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) |
|-----------------|-------------------------------------|--------------------|------------------------|---------------------------|
| 156.25 | 1.0 | 40.3 | 130.28 | 123.89 |

2.7 Input Mux Noise Isolation

The input clock mux is designed to minimize crosstalk between the CLK0 and CLK1. This improves phase jitter performance when clocks are present at both the CLK0 and CLK1 inputs. The following figure shows a measurement of the input mux's noise isolation.

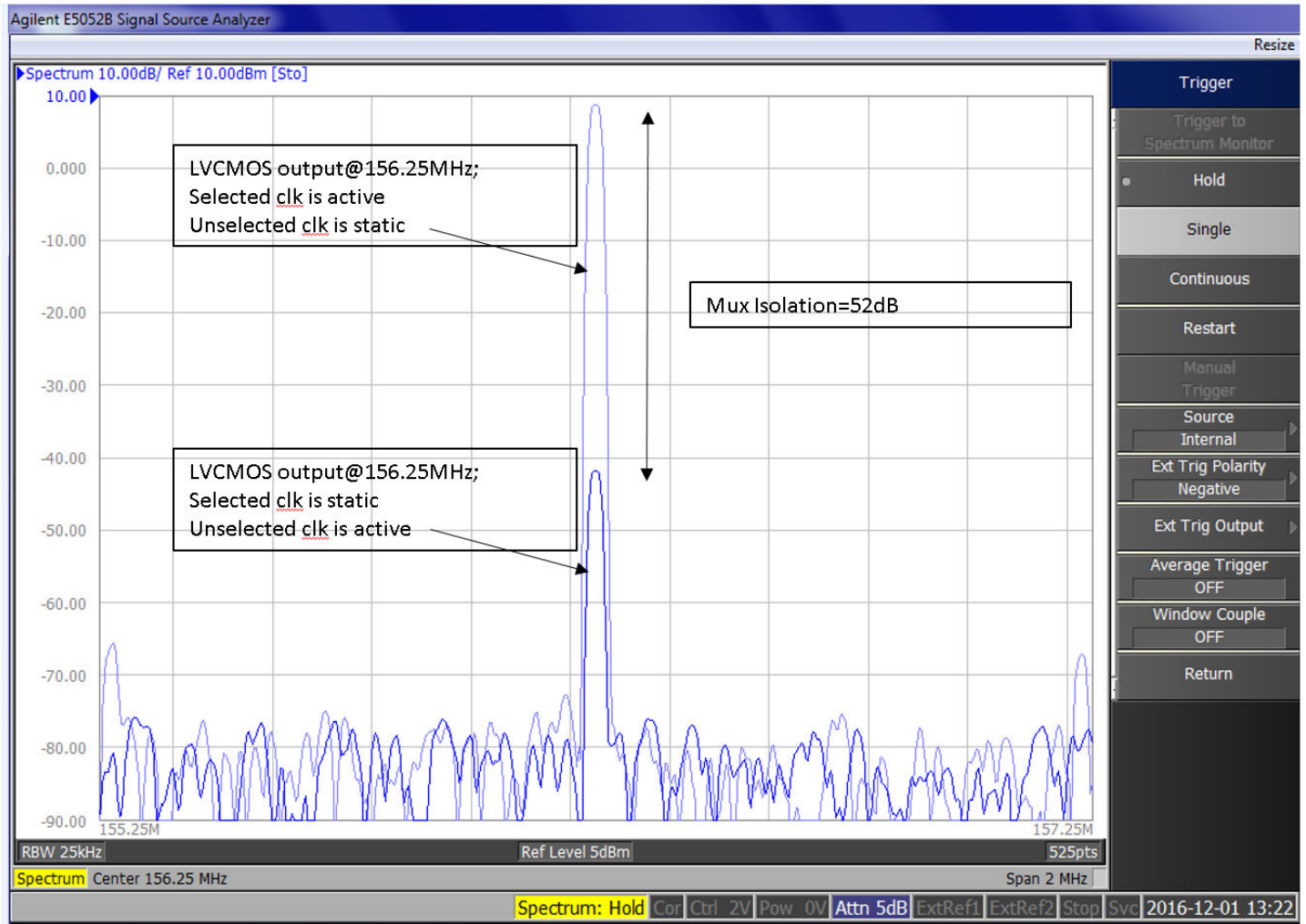


Figure 2.6. Input Mux Noise Isolation (Single-ended Input Clock, 16QFN Package)

3. Electrical Specifications

Table 3.1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|----------|----------------|------|-----|------|------|
| Ambient Operating Temperature | T_A | | -40 | — | 85 | °C |
| Supply Voltage Range | V_{DD} | LVCMOS | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |

Table 3.2. Input Clock Specifications
 $V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------|--|---------------------|-----|---------------------|------|
| LVCMOS Input High Voltage | V_{IH} | | $V_{DD} \times 0.7$ | — | — | V |
| LVCMOS Input Low Voltage | V_{IL} | | — | — | $V_{DD} \times 0.3$ | V |
| Input Capacitance | C_{IN} | CLK0 and CLK1 pins with respect to GND | — | 5 | — | pF |

Table 3.3. DC Common Characteristics (CLK_SEL, OEx)
 $V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------|--------------------------------------|---------------------|-----|---------------------|------------|
| Core Supply Current | I_{DD1} | $V_{DD} = 3.3\text{ V}$, Si53360/65 | — | 150 | — | mA |
| | | $V_{DD} = 3.3\text{ V}$, Si53361/62 | — | 35 | — | mA |
| Output Supply Current (per clock output, Si53361/62 only) | I_{DDO1} | $V_{DDOX} = 1.8\text{ V}$ | — | 7 | — | mA |
| | | $V_{DDOX} = 2.5\text{ V}$ | — | 10 | — | mA |
| | | $V_{DDOX} = 3.3\text{ V}$ | — | 13 | — | mA |
| Input High Voltage | V_{IH} | | $V_{DD} \times 0.8$ | — | — | V |
| Input Low Voltage | V_{IL} | | — | — | $V_{DD} \times 0.2$ | V |
| Internal Pull-up Resistor | R_{UP} | OEx, CLK_SEL | — | 25 | — | k Ω |

Note:

 1. Frequency = 200 MHz, $C_{load} = 0\text{ pF}$

Table 3.4. Output Characteristics (LVCMOS)
 $V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------|----------|--|---------------------|-----|---------------------|------|
| Output Voltage High | V_{OH} | $I_{OH} = -12\text{ mA}$, $V_{DD} = 3.3\text{ V}$ $I_{OH} = -9\text{ mA}$, $V_{DD} = 2.5\text{ V}$ $I_{OH} = -6\text{ mA}$, $V_{DD} = 1.8\text{ V}$ | $V_{DD} \times 0.8$ | — | — | V |
| Output Voltage Low | V_{OL} | $I_{OL} = 12\text{ mA}$, $V_{DD} = 3.3\text{ V}$ $I_{OL} = 9\text{ mA}$, $V_{DD} = 2.5\text{ V}$ $I_{OL} = 6\text{ mA}$, $V_{DD} = 1.8\text{ V}$ | — | — | $V_{DD} \times 0.2$ | V |

Table 3.5. AC Characteristics
 $V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------|-----------------------|---|------|-----|-----|------|
| Frequency | F | LVCMOS | dc | — | 200 | MHz |
| Duty Cycle (50% input duty cycle) | DC | 200 MHz, 2pF load TR/TF < 10% of period | 40 | 50 | 60 | % |
| Minimum Input Clock Slew Rate | SR | Required to meet prop delay and additive jitter specifications (20–80%) | 0.75 | — | — | V/ns |
| Output Rise/Fall Time | T_R/T_F | 200 MHz, 20/80%, 2 pF load | — | — | 850 | ps |
| Minimum Input Pulse Width | T_W | | 2 | — | — | ns |
| Propagation Delay | T_{PLH} , T_{PHL} | Low-to-high, high-to-low Single- ended, $C_L = 2\text{ pF}$ | 1.5 | 3.0 | 4.5 | ns |
| Output Enable Time | T_{EN} | F = 1 MHz | — | 10 | — | ns |
| | | F = 100 MHz | — | 10 | — | ns |
| Output Disable Time | T_{DIS} | F = 1 MHz | — | 20 | — | ns |
| | | F = 100 MHz | — | 20 | — | ns |
| Part-to-Part Skew | T_{SKPP} | $C_L = 2\text{ pF}$ | 0 | — | 300 | ps |
| Output-to-Output Skew | T_{SK} | $C_L = 2\text{ pF}$ | — | 40 | 125 | ps |

Table 3.6. Additive Jitter

| V_{DD} | Input ¹ | | | | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz) | |
|----------|--------------------|--------------|--|---|--------------|--|-----|
| | Freq (MHz) | Clock Format | Amplitude V_{IN} (Single-Ended, Peak-to-Peak) | Differential 20% to 80% Slew Rate (V/ns) | Clock Format | Typ | Max |
| 3.3 | 200 | SINGLE-ENDED | 0.15 | 0.637 | LVC MOS | 130 | 180 |
| 3.3 | 156.25 | SINGLE-ENDED | 0.5 | 0.458 | LVC MOS | 125 | 220 |
| 2.5 | 200 | SINGLE-ENDED | 0.15 | 0.637 | LVC MOS | 115 | 250 |
| 2.5 | 156.25 | SINGLE-ENDED | 0.5 | 0.458 | LVC MOS | 125 | 240 |

Note:

- For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.

Table 3.7. Thermal Conditions

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---------------|----------------|-------|------|
| 16- TSSOP Thermal Resistance, Junction to Ambient | θ_{JA} | Still air | 124.4 | °C/W |
| 16-QFN Thermal Resistance, Junction to Ambient | θ_{JA} | Still air | 57.6 | °C/W |
| 16- QFN Thermal Resistance, Junction to Case | θ_{JC} | Still air | 41.5 | °C/W |
| 24-QFN Thermal Resistance, Junction to Ambient | θ_{JA} | Still air | 37 | °C/W |
| 24- QFN Thermal Resistance, Junction to Case | θ_{JC} | Still air | 25 | °C/W |

Table 3.8. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|------------|--|------|-----|----------------|------|
| Storage Temperature | T_S | | -55 | — | 150 | °C |
| Supply Voltage | V_{DD} | | -0.5 | — | 3.8 | V |
| Input Voltage | V_{IN} | | -0.5 | — | $V_{DD} + 0.3$ | V |
| Output Voltage | V_{OUT} | | — | — | $V_{DD} + 0.3$ | V |
| ESD Sensitivity | HBM | HBM, 100 pF, 1.5 k Ω | — | — | 2000 | V |
| | CDM | | — | — | 500 | V |
| Peak Soldering Reflow Temperature | T_{PEAK} | Pb-Free; Solder reflow profile per JEDEC J-STD-020 | — | — | 260 | °C |
| Maximum Junction Temperature | T_J | | — | — | 125 | °C |

Note:

- Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

4. Detailed Block Diagrams

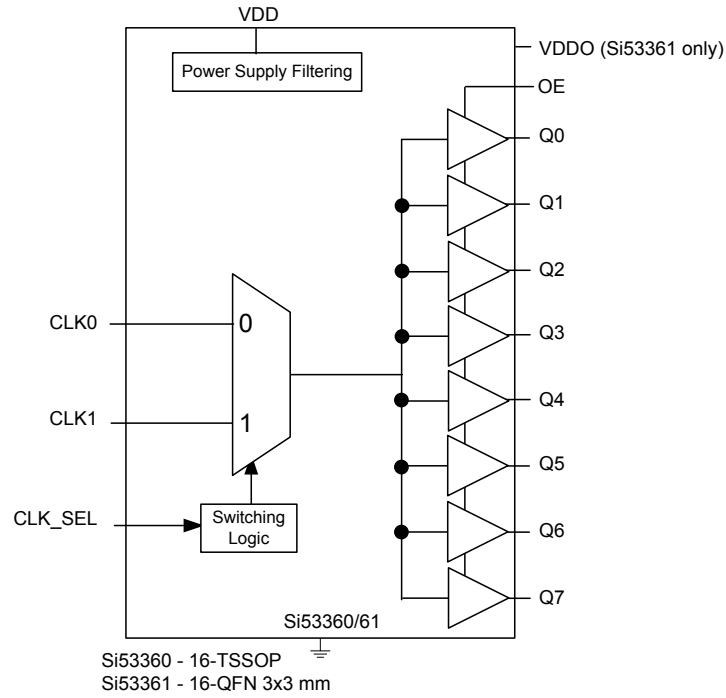


Figure 4.1. Si53360 and Si53361 Block Diagram

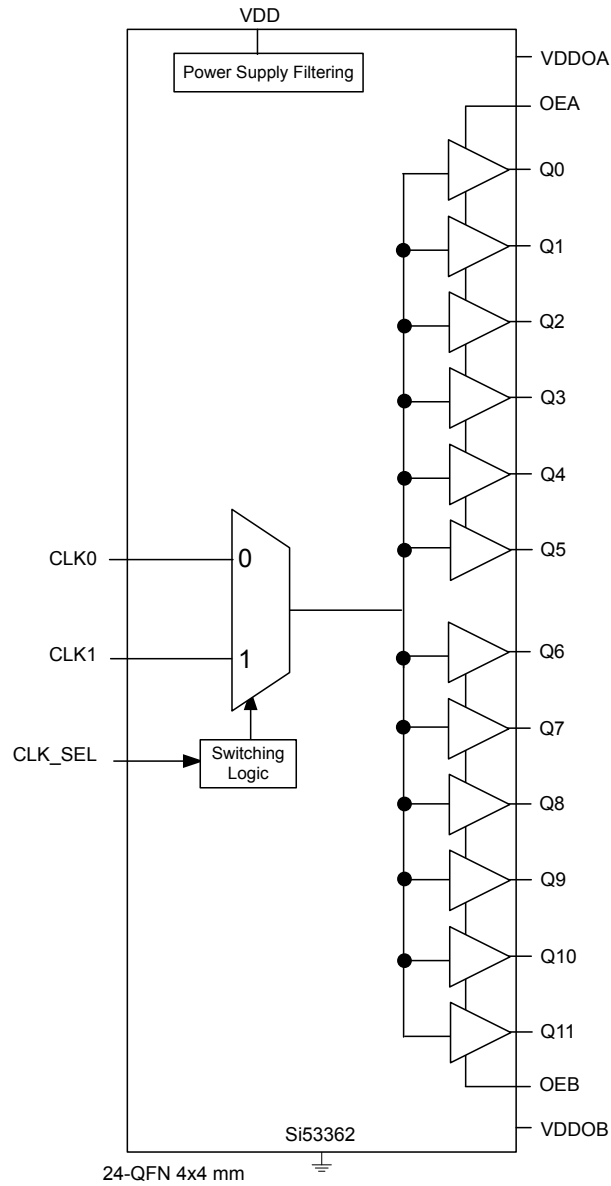


Figure 4.2. Si53362 Block Diagram

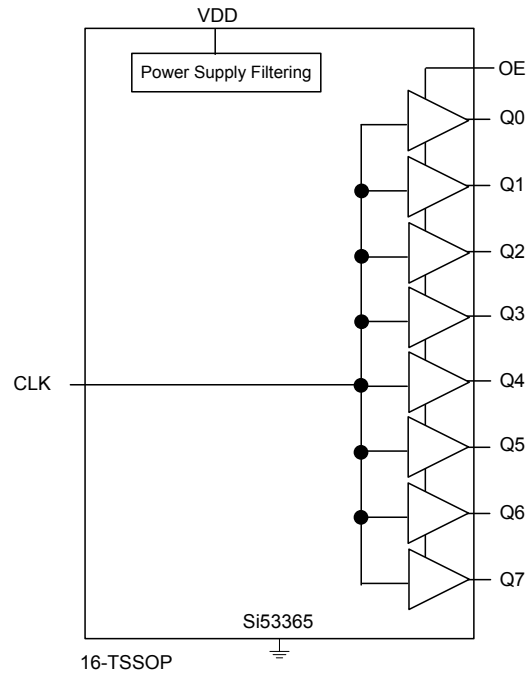


Figure 4.3. Si53365 Block Diagram

5. Si5336x Pin Descriptions

5.1 Si53360 Pin Descriptions

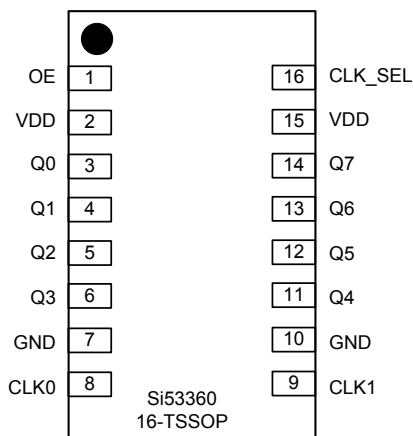


Figure 5.1. Si53360 Pin Descriptions

Table 5.1. Si53360 16-TSSOP Pin Descriptions

| Pin | Name | Type ¹ | Description |
|-----|---------|-------------------|---|
| 1 | OE | I | Output enable. When OE= high, the clock outputs are enabled. When OE= low, the clock outputs are tri-stated. OE features an internal pull-up resistor, and may be left unconnected. |
| 2 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 3 | Q0 | O | Output Clock 0. |
| 4 | Q1 | O | Output Clock 1. |
| 5 | Q2 | O | Output Clock 2. |
| 6 | Q3 | O | Output Clock 3. |
| 7 | GND | GND | Ground. |
| 8 | CLK0 | I | Input Clock 0. |
| 9 | CLK1 | I | Input Clock 1. |
| 10 | GND | GND | Ground. |
| 11 | Q4 | O | Output Clock 4. |
| 12 | Q5 | O | Output Clock 5. |
| 13 | Q6 | O | Output Clock 6. |
| 14 | Q7 | O | Output Clock 7. |
| 15 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 16 | CLK_SEL | I | Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-up resistor. |

| Pin | Name | Type ¹ | Description |
|--|------|-------------------|-------------|
| Note: 1. I = Input; O = Output; P = Power; GND = Ground. | | | |

5.2 Si53361 Pin Descriptions

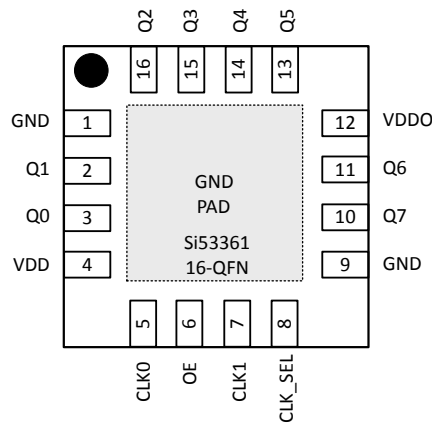


Figure 5.2. Si53361 Pin Descriptions

Table 5.2. Si53361 16-QFN Pin Descriptions

| Pin | Name | Type ¹ | Description |
|---------|--------------------|-------------------|--|
| 1 | GND | GND | Ground. |
| 2 | Q1 | O | Output Clock 1. |
| 3 | Q0 | O | Output Clock 0. |
| 4 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 5 | CLK0 | I | Input Clock 0. |
| 6 | OE | I | Output enable. When OE= high, the clock outputs are enabled. When OE= low, the clock outputs are tri-stated. OE features an internal pull-up resistor, and may be left unconnected. |
| 7 | CLK1 | I | Input Clock 1. |
| 8 | CLK_SEL | I | Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-up resistor. |
| 9 | GND | GND | Ground. |
| 10 | Q7 | O | Output Clock 7. |
| 11 | Q6 | O | Output Clock 6. |
| 12 | VDDO | P | Output voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDDO pin as possible. |
| 13 | Q5 | O | Output Clock 5. |
| 14 | Q4 | O | Output Clock 4. |
| 15 | Q3 | O | Output Clock 3. |
| 16 | Q2 | O | Output Clock 2. |
| GND Pad | Exposed Ground Pad | GND | Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met. |

| Pin | Name | Type ¹ | Description |
|--|------|-------------------|-------------|
| Note: 1. I = Input; O = Output; P = Power; GND = Ground. | | | |

5.3 Si53362 Pin Descriptions

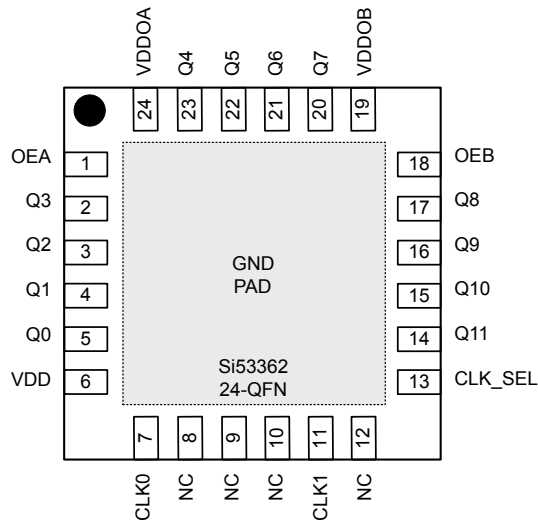


Figure 5.3. Si53362 Pin Descriptions

Table 5.3. Si53362 24-QFN Pin Descriptions

| Pin | Name | Type ¹ | Description |
|-----|---------|-------------------|---|
| 1 | OEA | I | Output Enable for Bank A (Q0-Q5). When OEA = HIGH, outputs Q0-Q5 are enabled. This pin contains an internal pull-up resistor, and leaving the pin disconnected enables the outputs. When OEA = LOW, Q0-Q5 are tri-stated. |
| 2 | Q3 | O | Output Clock 3. |
| 3 | Q2 | O | Output Clock 2. |
| 4 | Q1 | O | Output Clock 1. |
| 5 | Q0 | O | Output Clock 0. |
| 6 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 7 | CLK0 | I | Input Clock 0. |
| 8 | NC | — | No connect. Leave this pin unconnected. |
| 9 | NC | — | No connect. Leave this pin unconnected. |
| 10 | NC | — | No connect. Leave this pin unconnected. |
| 11 | CLK1 | I | Input Clock 1. |
| 12 | NC | — | No connect. Leave this pin unconnected. |
| 13 | CLK_SEL | I | Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-up resistor. |
| 14 | Q11 | O | Output Clock 11. |
| 15 | Q10 | O | Output Clock 10. |
| 16 | Q9 | O | Output Clock 9. |
| 17 | Q8 | O | Output Clock 8. |

| Pin | Name | Type ¹ | Description |
|---------|--------------------|-------------------|---|
| 18 | OEB | I | Output Enable for Bank B (Q6-Q11). When OEB = HIGH, outputs Q6-Q11 are enabled. This pin contains an internal pull-up resistor, and leaving the pin disconnected enables the outputs. When OEB = LOW, Q6-Q11 are tri-stated. |
| 19 | VDDOB | P | Output voltage supply—Bank B (Outputs: Q6 to Q11). Bypass with 1.0 μ F capacitor and place as close to the VDDOB pin as possible. |
| 20 | Q7 | O | Output Clock 7. |
| 21 | Q6 | O | Output Clock 6. |
| 22 | Q5 | O | Output Clock 5. |
| 23 | Q4 | O | Output Clock 4. |
| 24 | VDDOA | P | Output voltage supply—Bank A (Outputs: Q0 to Q5). Bypass with 1.0 μ F capacitor and place as close to the VDDOA pin as possible. |
| GND Pad | Exposed Ground Pad | GND | Ground Pad - Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met. |

Note:

1. I = Input; O = Output; P = Power; GND = Ground.

5.4 Si53365 Pin Descriptions

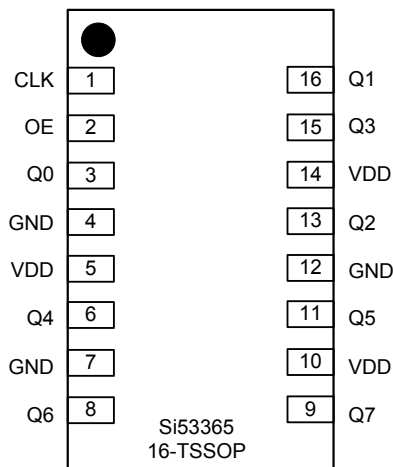


Figure 5.4. Si53365 Pin Descriptions

Table 5.4. Si53365 16-TSSOP Pin Descriptions

| Pin | Name | Type ¹ | Description |
|-----|------|-------------------|--|
| 1 | CLK | I | Input Clock. |
| 2 | OE | I | Output enable. When OE= high, the clock outputs are enabled. When OE= low, the clock outputs are low. OE features an internal pull-up resistor, and may be left unconnected. |
| 3 | Q0 | O | Output Clock 0. |
| 4 | GND | GND | Ground. |
| 5 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 6 | Q4 | O | Output Clock 4. |
| 7 | GND | GND | Ground. |
| 8 | Q6 | O | Output Clock 6. |
| 9 | Q7 | O | Output Clock 7. |
| 10 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 11 | Q5 | O | Output Clock 5. |
| 12 | GND | GND | Ground. |
| 13 | Q2 | O | Output Clock 2. |
| 14 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 15 | Q3 | O | Output Clock 3. |
| 16 | Q1 | O | Output Clock 1. |

Note:

1. I = Input; O = Output; P = Power; GND = Ground.

6. Package Outline

6.1 16-Pin TSSOP Package

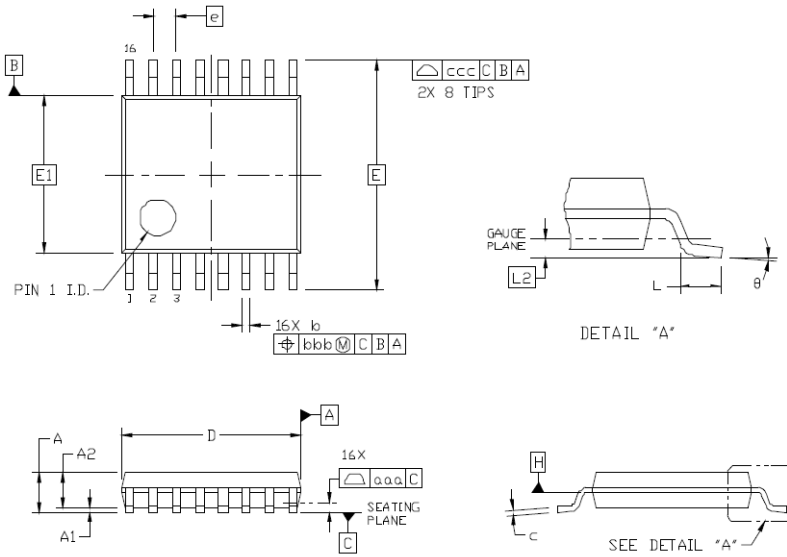


Figure 6.1. 16-Pin TSSOP Package

Table 6.1. 16-Pin TSSOP Package Dimensions

| Dimension | Min | Nom | Max |
|-----------|----------|------|------|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | — | 0.30 |
| c | 0.09 | — | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.40 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L2 | 0.25 BSC | | |
| θ | 0° | — | 8° |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.20 | | |

| Dimension | Min | Nom | Max |
|---|-----|-----|-----|
| <p>Note:</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.3. This drawing conforms to the JEDEC Solid State Outline MO-220.4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components. | | | |

6.2 16-Pin QFN Package

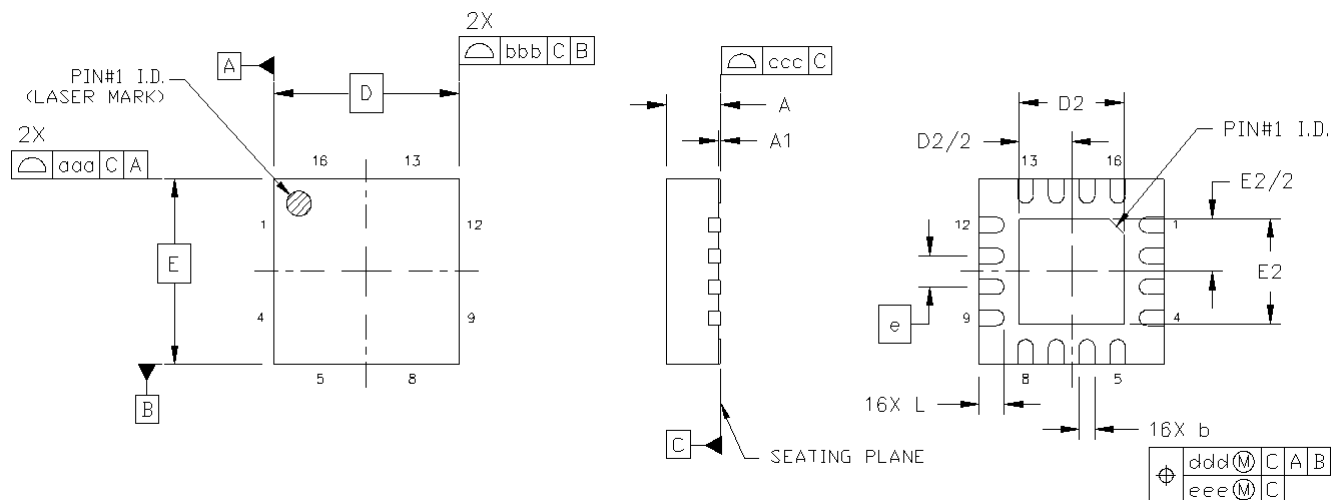


Figure 6.2. 16-Pin QFN Package

Table 6.2. 16-QFN Package Dimensions

| Dimension | Min | Nom | Max |
|-----------|-----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 3.00 BSC. | | |
| D2 | 1.65 | 1.70 | 1.75 |
| e | 0.50 BSC. | | |
| E | 3.00 BSC. | | |
| E2 | 1.65 | 1.70 | 1.75 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| eee | — | — | 0.05 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6.3 24-Pin QFN Package

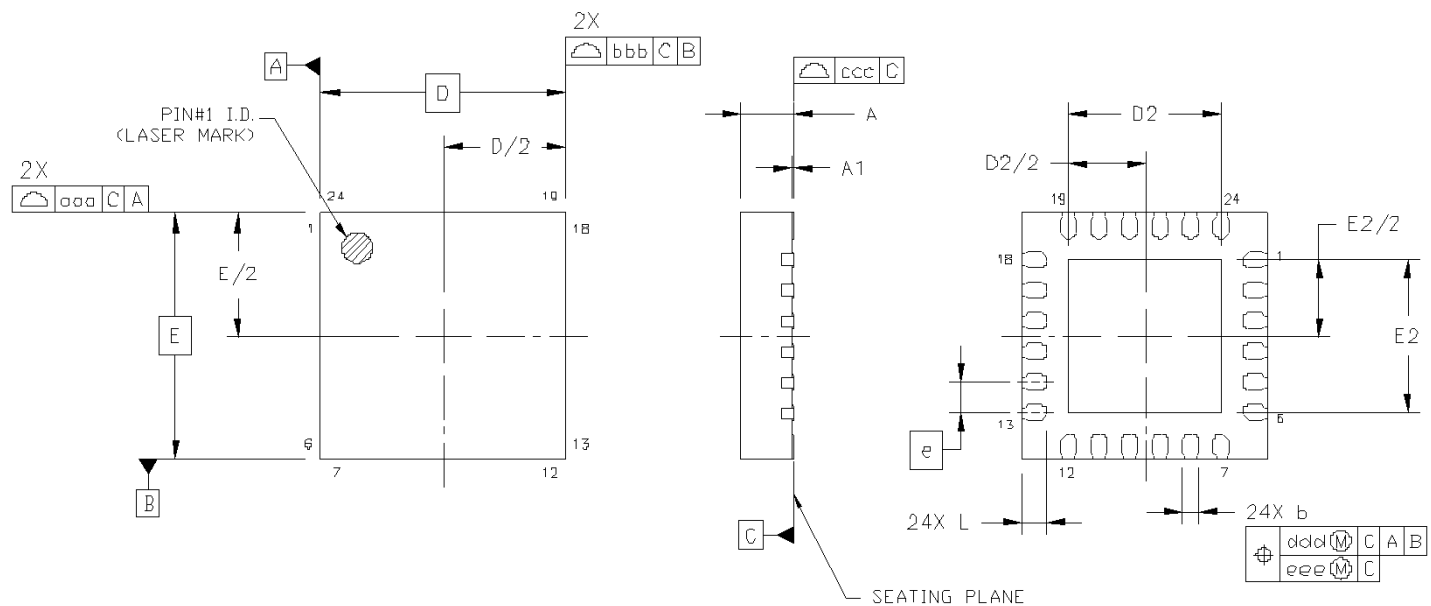


Figure 6.3. 24-Pin QFN Package

Table 6.3. 24-QFN Package Dimensions

| Dimension | Min | Nom | Max |
|-----------|-----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 4.00 BSC. | | |
| D2 | 2.35 | 2.50 | 2.65 |
| e | 0.50 BSC. | | |
| E | 4.00 BSC. | | |
| E2 | 2.35 | 2.50 | 2.65 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.08 | | |
| ddd | 0.10 | | |
| eee | 0.05 | | |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. PCB Land Pattern

7.1 16-Pin TSSOP Land Pattern

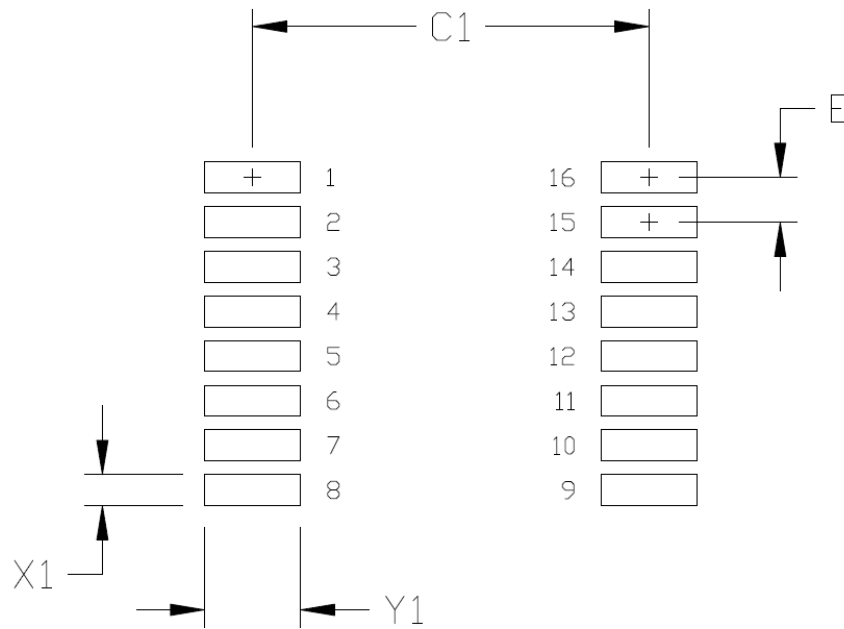


Figure 7.1. 16-Pin TSSOP Land Pattern

Table 7.1. 16-Pin TSSOP Land Pattern Dimensions

| Dimension | Feature | (mm) |
|-----------|--------------------|------|
| C1 | Pad Column Spacing | 5.80 |
| E | Pad Row Pitch | 0.65 |
| X1 | Pad Width | 0.45 |
| Y1 | Pad Length | 1.40 |

Notes:

1. This Land Pattern Design is based on IPC-7351 specifications for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.2 16-Pin QFN Land Pattern

Figure 7.2. 16-Pin QFN Land Pattern

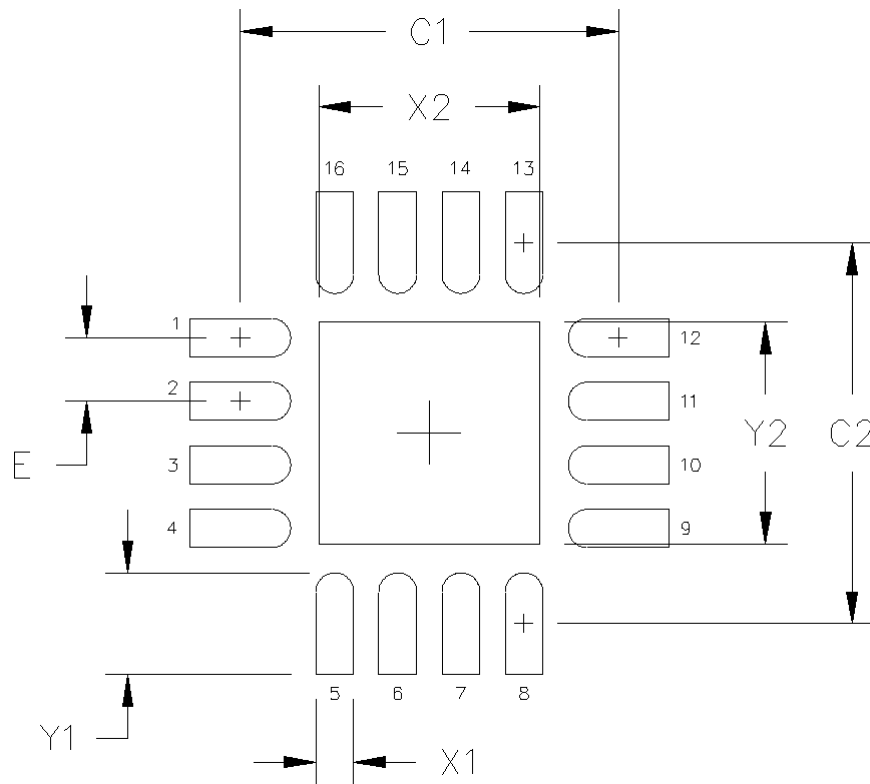


Table 7.2. 16-QFN Land Pattern Dimensions

| Dimension | mm |
|-----------|------|
| C1 | 3.00 |
| C2 | 3.00 |
| E | 0.50 |
| X1 | 0.30 |
| Y1 | 0.80 |
| X2 | 1.75 |
| Y2 | 1.75 |

| Dimension | mm |
|--|----|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm).2. This Land Pattern Design is based on the IPC-7351 guidelines.3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm. <p>Solder Mask Design</p> <ol style="list-style-type: none">1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none">1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.2. The stencil thickness should be 0.125 mm (5 mils).3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.4. A 2 x 2 array of 0.65 mm square openings on a 0.90 mm pitch should be used for the center ground pad. <p>Card Assembly</p> <ol style="list-style-type: none">1. A No-Clean, Type-3 solder paste is recommended.2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

7.3 24-Pin QFN Land Pattern

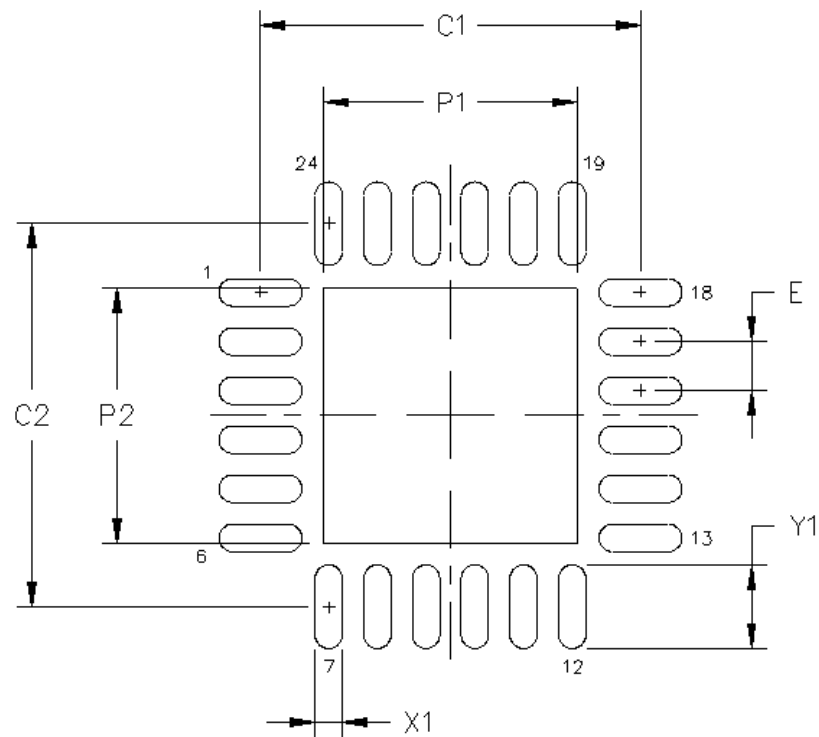


Figure 7.3. 24-Pin QFN Land Pattern

Table 7.3. 24-QFN Land Pattern Dimensions

| Dimension | mm |
|-----------|------|
| P1 | 2.55 |
| P2 | 2.55 |
| X1 | 0.25 |
| Y1 | 0.80 |
| C1 | 3.90 |
| C2 | 3.90 |
| E | 0.50 |

| Dimension | mm |
|--|----|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm).2. This Land Pattern Design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none">1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none">1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.2. The stencil thickness should be 0.125 mm (5 mils).3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.4. A 2 x 2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad. <p>Card Assembly</p> <ol style="list-style-type: none">1. A No-Clean, Type-3 solder paste is recommended.2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

8. Top Markings

8.1 Si53360/65 Top Markings

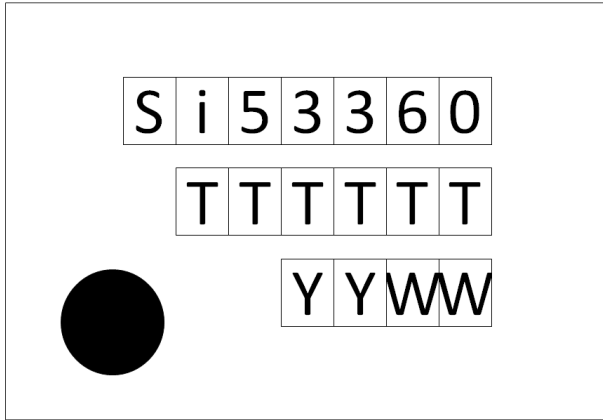


Figure 8.1. Si53360 Top Marking

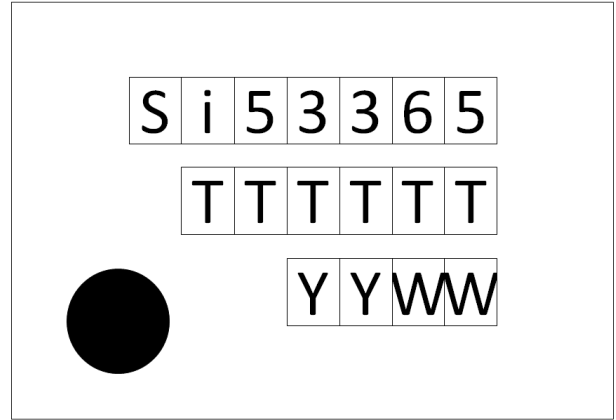


Figure 8.2. Si53365 Top Marking

Table 8.1. Si53360/65 Top Marking Explanation

| | | |
|------------------------|--|---|
| Mark Method: | Laser | |
| Font Size: | 2.0 Point (0.71 mm) Right-Justified | |
| Line 1 Marking: | Device Part Number | 53360 for Si53360, 53365 for Si53365 |
| Line 2 Marking: | TTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| Line 3 Marking | YY = Year, WW = Work Week | Corresponds to the year and work week of the mold date. |

8.2 Si53361 Top Marking

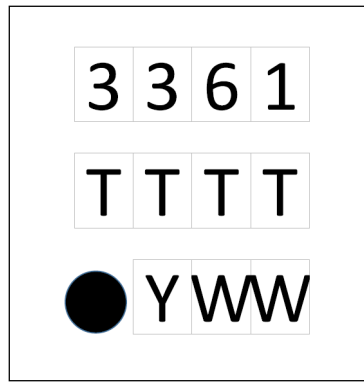


Figure 8.3. Si53361 Top Marking

Table 8.2. Si53361 Top Marking Explanation

| | | |
|------------------------|------------------------------------|---|
| Mark Method: | Laser | |
| Font Size: | 2.0 Point (0.71 mm) Center-aligned | |
| Line 1 Marking: | Device Part Number | 3361 for Si53361 |
| Line 2 Marking: | TTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| Line 3 Marking | YY = Year, WW = Work Week | Corresponds to the year and work week of the mold date. |

8.3 Si53362 Top Marking

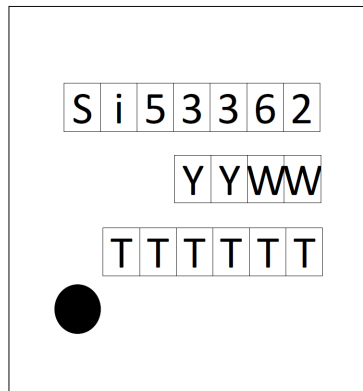


Figure 8.4. Si53362 Top Marking

Table 8.3. Si53362 Top Marking Explanation

| | | |
|------------------------|--|---|
| Mark Method: | Laser | |
| Font Size: | 2.0 Point (0.71 mm) Right-justified | |
| Line 1 Marking: | Device Part Number | 53362 for Si53362 |
| Line 2 Marking: | TTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| Line 3 Marking | YY = Year, WW = Work Week | Corresponds to the year and work week of the mold date. |

9. Revision History

Revision 1.3

December, 2018

- Changed CLK_SEL from pull-down resistor to pull-up resistor.
- Updated output state to low when OE pin is asserted low on Si53365.

Revision 1.2

December, 2016

- Introduced Si53361 and Si53362 new products.
- Merged Si53360/65 datasheets with the new products to create a single LVCMOS buffer datasheet.
- Added Core supply current spec at multiple supply voltages.
- Added “Internal pull-down resistor” typical spec.



SKYWORKS®

ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

www.skyworksinc.com/CBPro



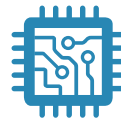
Portfolio

www.skyworksinc.com/ia/timing



SW/HW

www.skyworksinc.com/CBPro



Quality

www.skyworksinc.com/quality



Support & Resources

www.skyworksinc.com/support

Copyright © 2021 Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.


Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5®, SkyOne®, SkyBlue™, Skyworks Green™, Clockbuilder®, DSPLL®, ISOModem®, ProSLIC®, and SiPHY® are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at www.skyworksinc.com, are incorporated by reference.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View SI53360-B-GT on WIN SOURCE](#)
-  [Skyworks Solutions Inc. Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management