# THE DATASHEET OF

# Z8523316ASG

# Z85233

## EMSCC™ ENHANCED MONO SERIAL COMMUNICATION CONTROLLER

## GENERAL DESCRIPTION

The Zilog Enhanced Mono Serial Communication Controller, Z85233 EMSCC, is a software compatible CMOS member of the SCC family introduced by Zilog in 1981. The EMSCC is a full-duplex data communications controller capable of supporting a wide range of popular protocols. The Z85233 EMSCC is a single channel version (Channel A) of Zilog's Z85230 ESCC. Based on ZIlog's unique Superintegration™ Technology, the EMSCC is compatible with designs using Zilog's SCC and ESCC to receive and transmit data. It has many improvements that significantly reduce CPU overhead. The addition of a 4-byte transmit FIFO and an 8-byte receive FIFO significantly reduces the overhead required to provide data to, and get data from, the transmitter and receiver.

The EMSCC also has many features that improve packet handling in SDLC mode. The EMSCC will automatically: transmit a flag before the data, reset the Tx Underrun/EOM latch, force the TxD pin high at the appropriate time when using NRZI encoding, deassert the /RTS pin after the closing flag, and better handle ABORTed frames when using the 10x19 status FIFO. The combination of these features along with the deeper data FIFOs significantly simplifies SDLC driver software.

The CPU hardware interface has been simplified by relieving the databus setup time requirement and supporting the software generation of the interrupt acknowledge signal (/INTACK). These changes allow an interface with less external logic to many microprocessor families while maintaining compatibility with existing designs. I/O handling of the EMSCC is improved over the SCC with faster response of the /INT and /DTR//REQ pins.

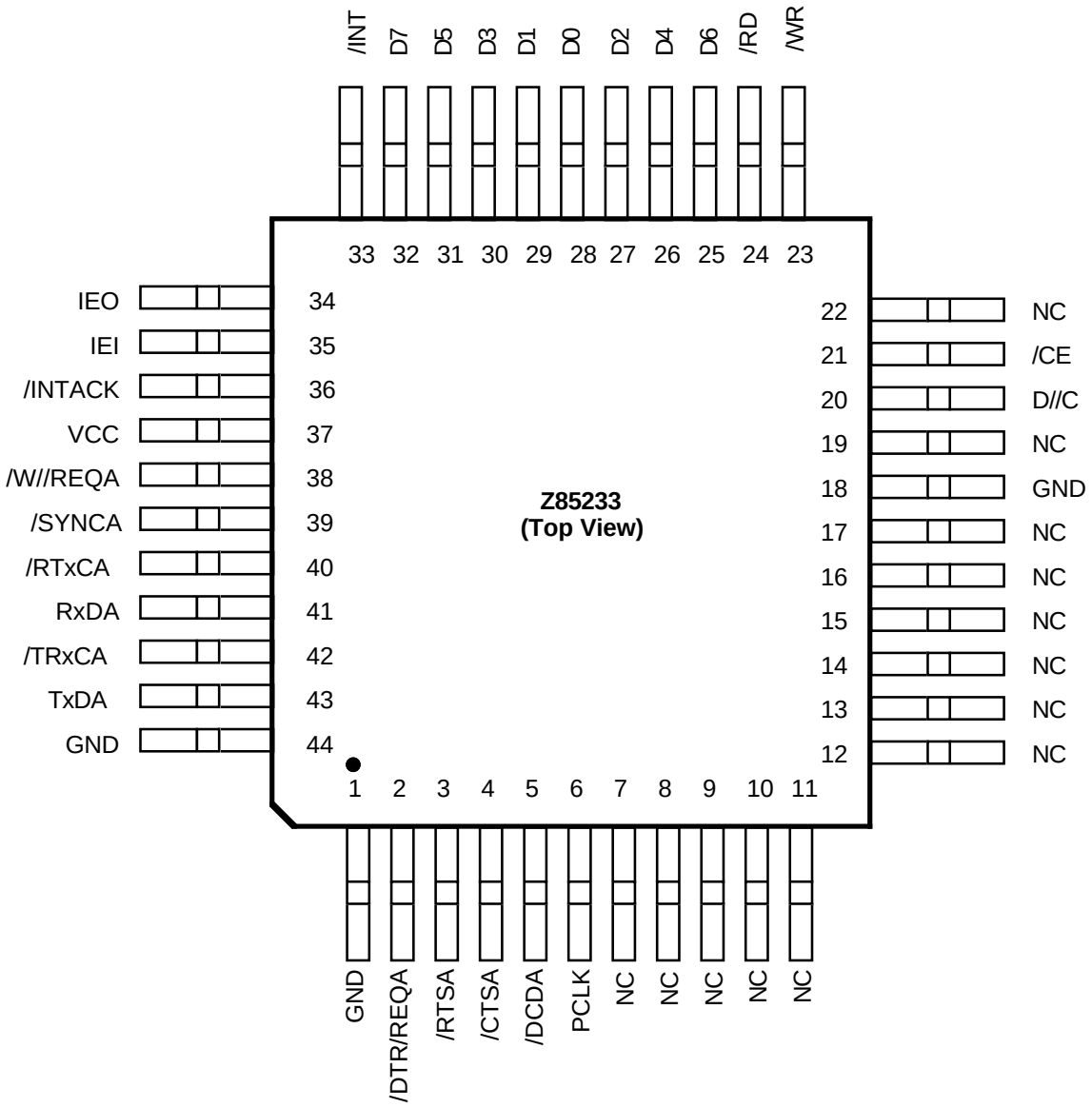
The many enhancements added to the EMSCC permits a system design that increases overall system performance with better data handling and less interface logic.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

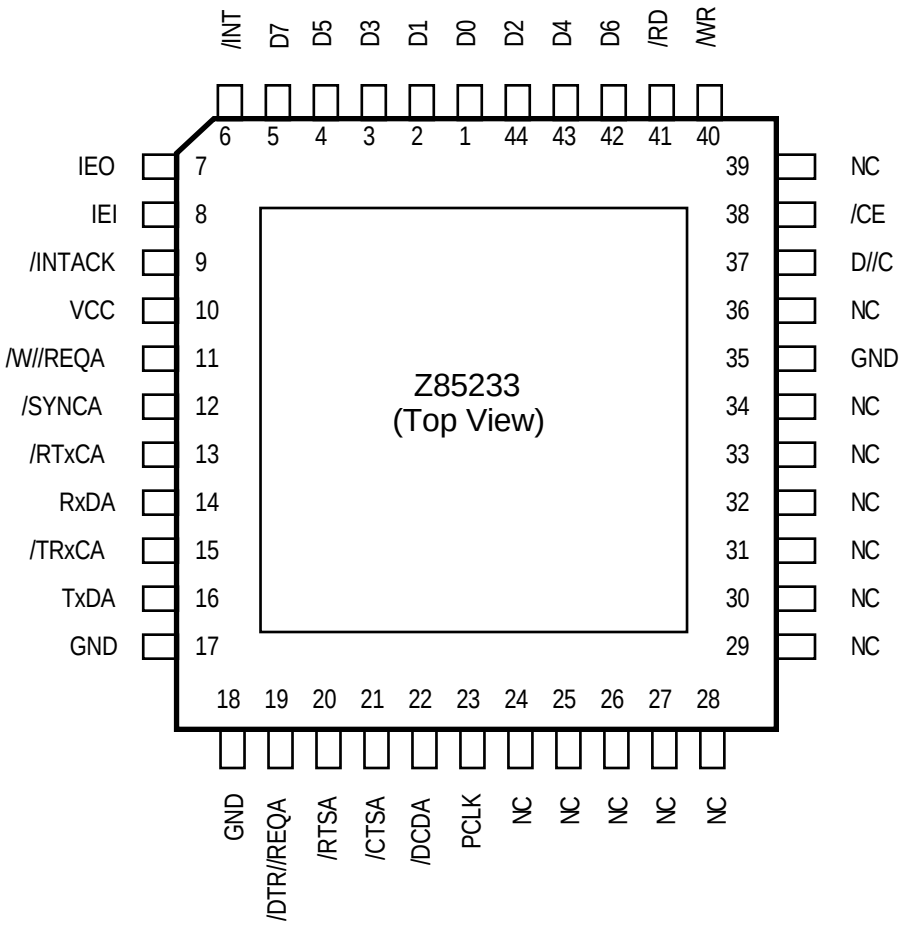
Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

## PIN DESCRIPTIONS




**Z85233 PQFP Pin Assignments**




**Z85233 PLCC Pin Assignments**

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ Supply Voltage range ..... -0.3V to +7.0V
Voltages on all pins
with respect to GND ..... -0.3V to $V_{CC}$ +0.3V
Operating Ambient
Temperature ..... See Ordering Information
Storage Temperature ..... -65°C to +150°C

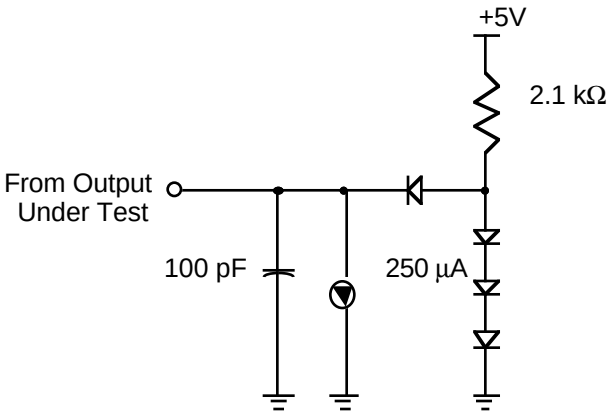
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

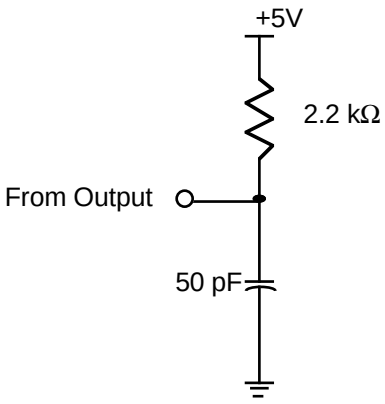
The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- +4.50 V ≤ $V_{CC}$ ≤ + 5.50 V
- GND = 0 V
- $T_A$ as specified in Ordering Information




**Standard Test Load**




**Open-Drain Test Load**

## CAPACITANCE

| Symbol | Parameter | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | 10 | pF | Unmeasured pins |
| $C_{OUT}$ | Output Capacitance | | 15 | pF | returned to ground. |
| $C_{I/O}$ | Bidirectional Capacitance | | 20 | pF | |

**Note:**
f = 1 MHz, over specified temperature range.

## MISCELLANEOUS

Gate Count - 7000

## DC CHARACTERISTICS

Z85233

| Symbol | Parameter | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.2 | | $V_{CC}$+0.3 | V | |
| $V_{IL}$ | Input Low Voltage | -0.3 | | 0.8 | V | |
| $V_{OH1}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = -1.6 mA |
| $V_{OH2}$ | Output High Voltage | $V_{CC}$-0.8 | | | V | $I_{OH}$ = -250 µA |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$= + 2.0 mA |
| $I_{IL}$ | Input Leakage | | | ±10.0 | µA | 0.4< $V_{IN}$<+2.4V |
| $I_{OL}$ | Output Leakage | | | ±10.0 | µA | 0.4< $V_{OUT}$ <+2.4V |
| $I_{CC1}$ | $V_{CC}$ Supply Current | | 4 | 8 (10 MHz) | mA | $V_{CC}$=5V $V_{IH}$=4.8 $V_{IL}$=0.2V |
| | | | 5 | 10 (16 MHz) | mA | Crystal Oscillators off |
| $I_{CC(OSC)}$ | Crystal OSC Current | | 6 | | mA | Current for each osc. in addition to $I_{CC1}$ |

**Notes:**

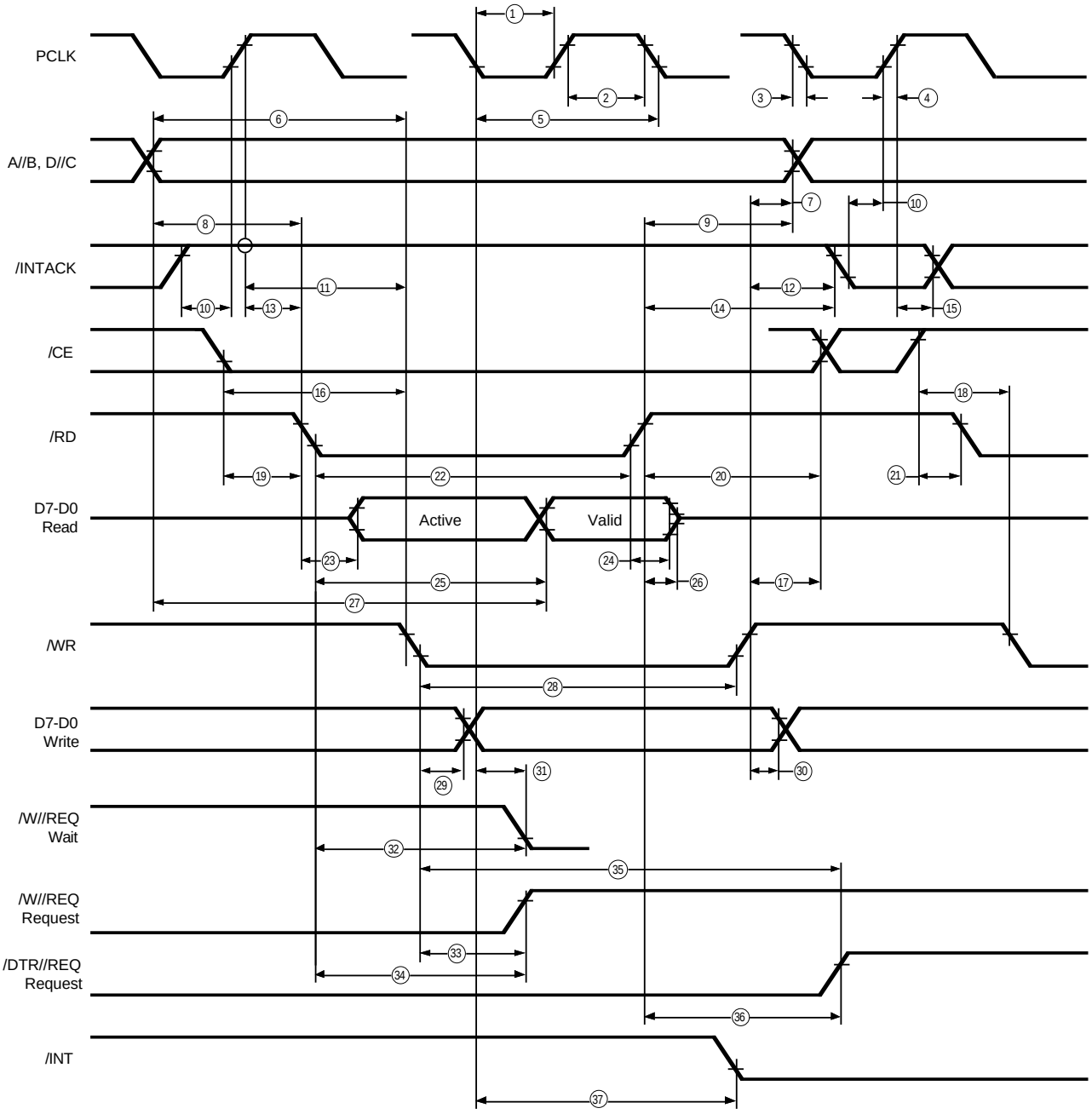
[1] $V_{CC}$ = 5V ± 10% unless otherwise specified, over specified temperature range.

[2] Typical $I_{CC}$ was measured with oscillator off.

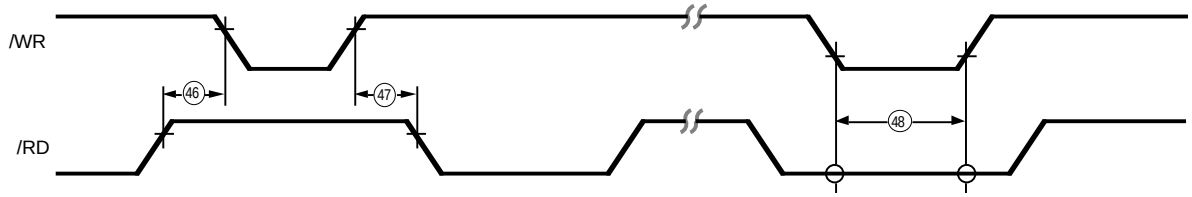
[3] No $I_{CC}$(osc) max is specified due to dependency on the external circuit.

## AC CHARACTERISTICS

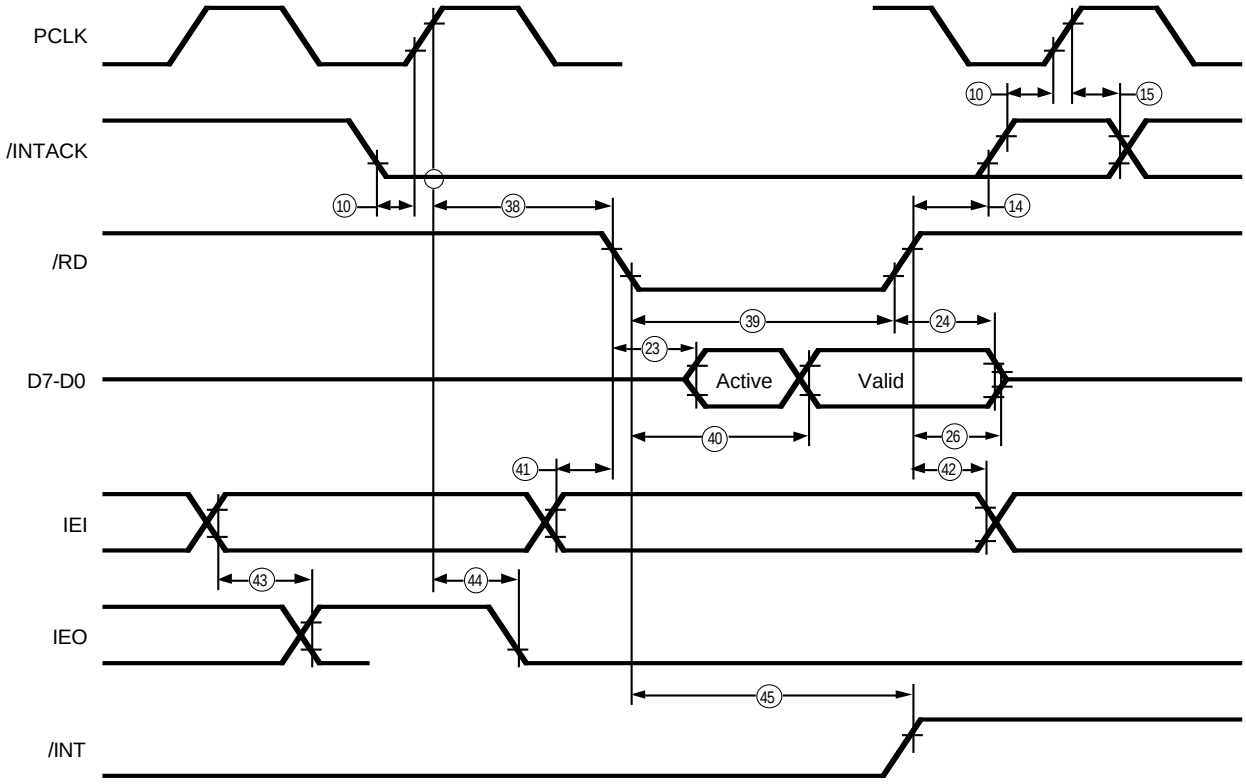
Z85233 Read and Write Timing Diagram



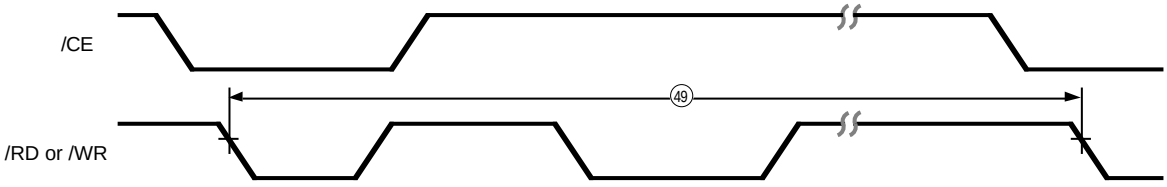

**Read and Write Timing Diagram**




**Reset Timing Diagram**




**Interrupt Acknowledge Timing Diagram**




**Cycle Timing Diagram**

## AC CHARACTERISTICS

Z85233 Read and Write Timing Table

| No | Symbol | Parameter | 10 MHz Min | 10 MHz Max | 16 MHz Min | 16 MHz Max | Notes |
|---|---|---|---|---|---|---|---|
| 1 | TwPCl | PCLK Low Width | 40 | 1000 | 26 | 1000 | |
| 2 | TwPCh | PCLK High Width | 40 | 1000 | 26 | 1000 | |
| 3 | TfPC | PCLK Fall Time | | 10 | | 5 | |
| 4 | TrPC | PCLK Rise Time | | 10 | | 5 | |
| 5 | TcPC | PCLK Cycle Time | 100 | 2000 | 61 | 2000 | |
| 6 | TsA(WR) | Address to /WR Fall Setup Time | 50 | | 35 | | |
| 7 | ThA(WR) | Address to /WR Rise Hold Time | 0 | | 0 | | |
| 8 | TsA(RD) | Address to /RD Fall Setup Time | 50 | | 35 | | |
| 9 | ThA(RD) | Address to /RD Rise Hold Time | 0 | | 0 | | |
| 10 | TsIA(PC) | /INTACK to PCLK Rise Setup Time | 20 | | 15 | | |

## AC CHARACTERISTICS

Z85233 Read and Write Timing Table

| No | Symbol | Parameter | 10 MHz Min | 10 MHz Max | 16 MHz Min | 16 MHz Max | Notes |
|---|---|---|---|---|---|---|---|
| 11 | TsIAi(WR) | /INTACK to /WR Fall Setup Time | 130 | | 70 | | [1] |
| 12 | ThIA(WR) | /INTACK to /WR Rise Hold Time | 0 | | 0 | | |
| 13 | TsIAi(RD) | /INTACK to /RD Fall Setup Time | 130 | | 70 | | [1] |
| 14 | ThIA(RD) | /INTACK to /RD Rise Hold Time | 0 | | 0 | | |
| 15 | ThIA(PC) | /INTACK to PCLK Rise Hold Time | 30 | | 15 | | |
| 16 | TsCEI(WR) | /CE Low to /WR Fall Setup Time | 0 | | 0 | | |
| 17 | ThCE(WR) | /CE to /WR Rise Hold Time | 0 | | 0 | | |
| 18 | TsCEh(WR) | /CE High to /WR Fall Setup Time | 50 | | 30 | | |
| 19 | TsCEI(RD) | /CE Low to /RD Fall Setup Time | 0 | | 0 | | [1] |
| 20 | ThCE(RD) | /CE to /RD Rise Hold Time | 0 | | 0 | | [1] |
| 21 | TsCEh(RD) | /CE High to /RD Fall Setup Time | 50 | | 30 | | [1] |
| 22 | TwRDI | /RD Low Width | 125 | 2TcPC | 70 | 2TcPC | [1] |
| 23 | TdRD(DRA) | /RD Fall to Read Data Active Delay | 0 | | 0 | | |
| 24 | TdRDr(DR) | /RD Rise to Data Not Valid Delay | 0 | | 0 | | |
| 25 | TdRDI(DR) | /RD Fall to Read Data Valid Delay | | 120 | | 70 | |
| 26 | TdRD(DRz) | /RD Rise to Read Data Float Delay | | 35 | | 30 | |
| 27 | TdA(DR) | Addr to Read Data Valid Delay | | 180 | | 100 | |
| 28 | TwWRI | /WR Low Width | 125 | | 75 | | |
| 29 | TdWR(DW) | /WR Fall to Write Data Valid Delay | | 20 | | 20 | |
| 30 | ThDW(WR) | Write Data to /WR Rise Hold Time | 0 | | 0 | | |
| 31 | TdWR(W) | /WR Fall to Wait Valid Delay | | 100 | | 50 | [4] |
| 32 | TdRD(W) | /RD Fall to Wait Valid Delay | | 100 | | 50 | [4] |
| 33 | TdWRf(REQ) | /WR Fall to /W//REQ Not Valid Delay | | 120 | | 70 | |
| 34 | TdRDf(REQ) | /RD Fall to /W//REQ Not Valid Delay | | 120 | | 70 | [6] |
| 35a | TdWRr(REQ) | /WR Fall to /DTR//REQ Not Valid | | 4TcPc | | 4TcPc | |
| 35b | TdWRr(REQ) | /WR Fall to /DTR//REQ Not Valid | | 100 | | 70 | [6] |
| 36 | TdRDr(REQ) | /RD Rise to /DTR//REQ Not Valid Delay | | NA | | NA | |
| 37 | TdPC(INT) | PCLK Fall to /INT Valid Delay | | 320 | | 175 | |
| 38 | TdIAi(RD) | /INTACK to /RD Fall (Ack) Delay | 90 | | 50 | | [5] |
| 39 | TwRDA | /RD (Acknowledge) Width | 125 | | 75 | | |
| 40 | TdRDA(DR) | /RD Fall(Ack) to Read Data Valid Delay | 120 | | 70 | | |
| 41 | TsIEI(RDA) | IEI to /RD Fall (Ack) Setup Time | 95 | | 50 | | |
| 42 | ThIEI(RDA) | IEI to /RD Rise (Ack) Hold Time | 0 | | 0 | | |
| 43 | TdIEI(IEO) | IEI to IEO Delay Time | | 90 | | 45 | |
| 44 | TdPC(IEO) | PCLK Rise to IEO Delay | | 175 | | 80 | |
| 45 | TdRDA(INT) | /RD Fall to /INT Inactive Delay | | 320 | | 200 | [4] |
| 46 | TdRD(WRQ) | /RD Rise to /WR Fall Delay for No Reset | 15 | | 10 | | |
| 47 | TdWRQ(RD) | /WR Rise to /RD Fall Delay for No Reset | 15 | | 10 | | |
| 48 | TwRES | /WR and /RD Low for Reset | 100 | | 75 | | |
| 49 | Trc | Valid Access Recovery Time | 4TcPc | | 4TcPc | | [3] |

**Notes:**

[1] Parameter does not apply to Interrupt Acknowledge transactions.

[3] Parameter applies only between transactions involving the EMSCC.

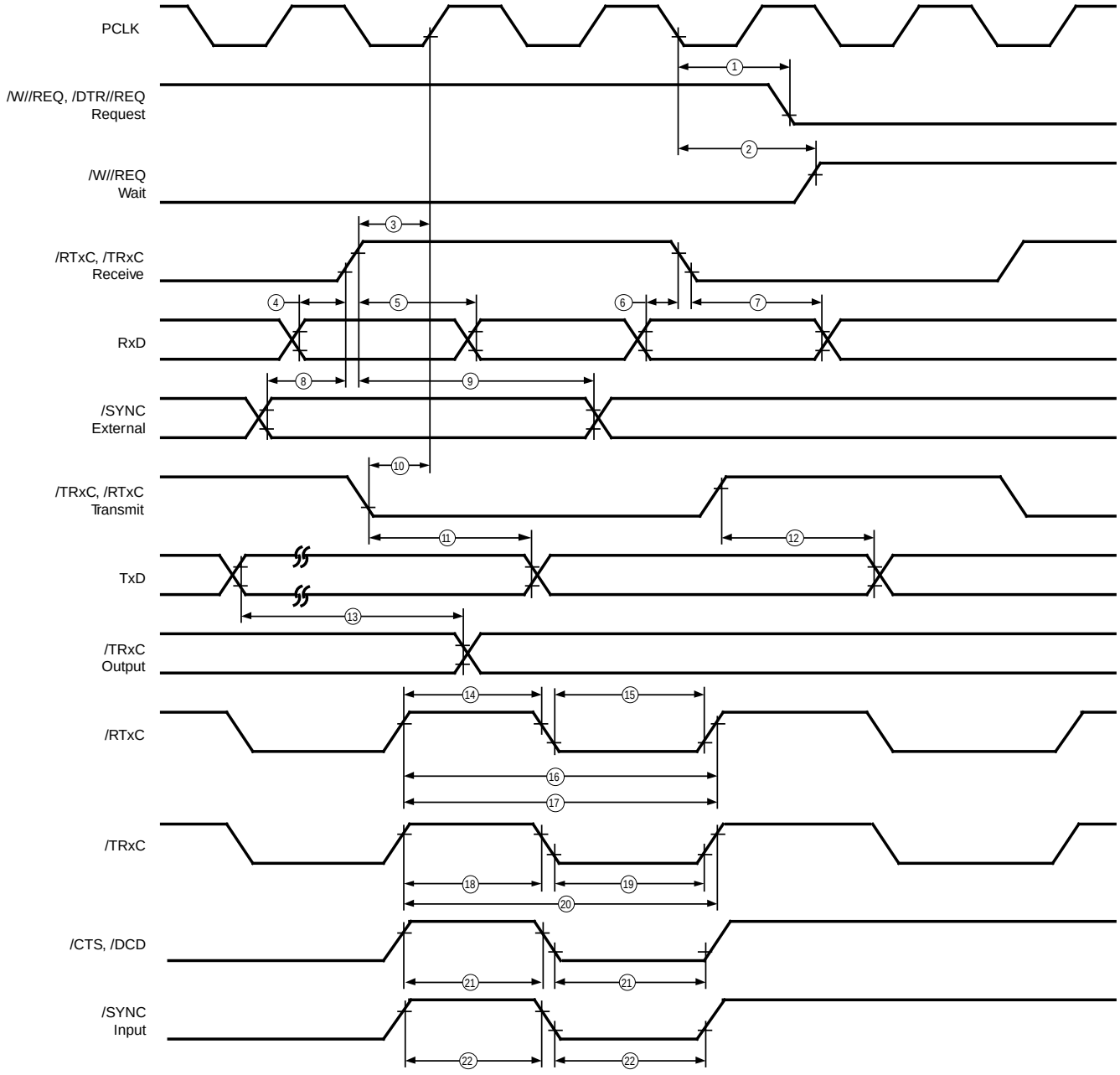
[4] Open-drain output, measured with open-drain test load.

[5] Parameter is system dependent. For any EMSCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain. TsIEI(RDA) for the EMSCC and TdIEI(IEO) for each device separating them in the daisy chain.

[6] Parameter applies to enhanced Request mode only (WR7' D4=1)

## AC CHARACTERISTICS

Z85233 General Timing Diagram




**General Timing Diagram**

## AC CHARACTERISTICS

Z85233 General Timing Table (Preliminary)

| No | Symbol | Parameter | 10 MHz Min | 10 MHz Max | 16 MHz Min | 16 MHz Max | Notes |
|---|---|---|---|---|---|---|---|
| 1a | TdPC(REQ) | /PCLK to W/REQ Valid | | 200 | | 80 | |
| 1b | TdPC(REQ) | /PCLK to DTR/ REQ Valid | | 200 | | 80 | [9] |
| 2 | TdPC(W) | /PCLK to Wait Inactive | | 300 | | 180 | |
| 3 | TsRXC(PC) | /RxC to /PCLK Setup Time | NA | NA | NA | NA | [1,4] |
| 4 | TsRXD(RXCr) | RxD to /RxC Setup Time | 0 | | 0 | | [1] |
| 5 | ThRXD(RxCr) | RxD to /RXC Hold Time | 125 | | 50 | | [1] |
| 6 | TsRXD(RXCf) | RxD to /RXC Setup Time | 0 | | 0 | | [1,5] |
| 7 | ThRXD(RXCf) | RXD to /RXC Hold Time | 125 | | 50 | | [1,5] |
| 8 | TsSY(RXC) | /SYNC to /RxC Setup Time | -150 | | -100 | | [1] |
| 9 | ThSY(RXC) | /SYNC to/RXC Hold Time | 5TcPc | | 5TcPc | | [1] |
| 10 | TsTXC(PC) | /TxC to /PCLK Setup Time | NA | | NA | | [2,4] |
| 11 | TdTXCf(TXD) | /TxC to TxD Delay | | 150 | | 80 | [2] |
| 12 | TdTxCr(TXD) | /TxC to TxD Delay | | 150 | | 80 | [2,5] |
| 13 | TdTXD(TRX) | TxD to TRxC Delay | | 140 | | 80 | |
| 14 | TwRTXh | RTxC High Width | 120 | | 80 | | [6] |
| 15 | TwRTXl | TRxC Low Width | 120 | | 80 | | [6] |
| 16a | TcRTX | RTxC Cycle Time | 400 | | 244 | | [6,7] |
| 16b | TxRX(DPLL) | DPLL Cycle Time Min | 50 | | 31 | | [7,8] |
| 17 | TcRTXX | Crystal Osc. Period | 100 | 1000 | 61 | 1000 | [3] |
| 18 | TwTRXh | TRxC High Width | 120 | | 80 | | [6] |
| 19 | TwTRXl | TRxC Low Width | 120 | | 80 | | [6] |
| 20 | TcTRX | TRxC Cycle Time | 400 | | 244 | | [6,7] |
| 21 | TwEXT | DCD or CTS Pulse Width | 120 | | 70 | | |
| 22 | TwSY | SYNC Pulse Width | 120 | | 70 | | |

**Notes:**

[1] RxC is /RTxC or /TRxC, whichever is supplying the receive clock.

[2] TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.

[3] Both /RTxC and /SYNC have 30 pF capacitors to ground connected to them.

[4] Synchronization of RxC to PCLK is eliminated in divide by four operation.

[5] Parameter applies only to FM encoding/decoding.

[6] Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.

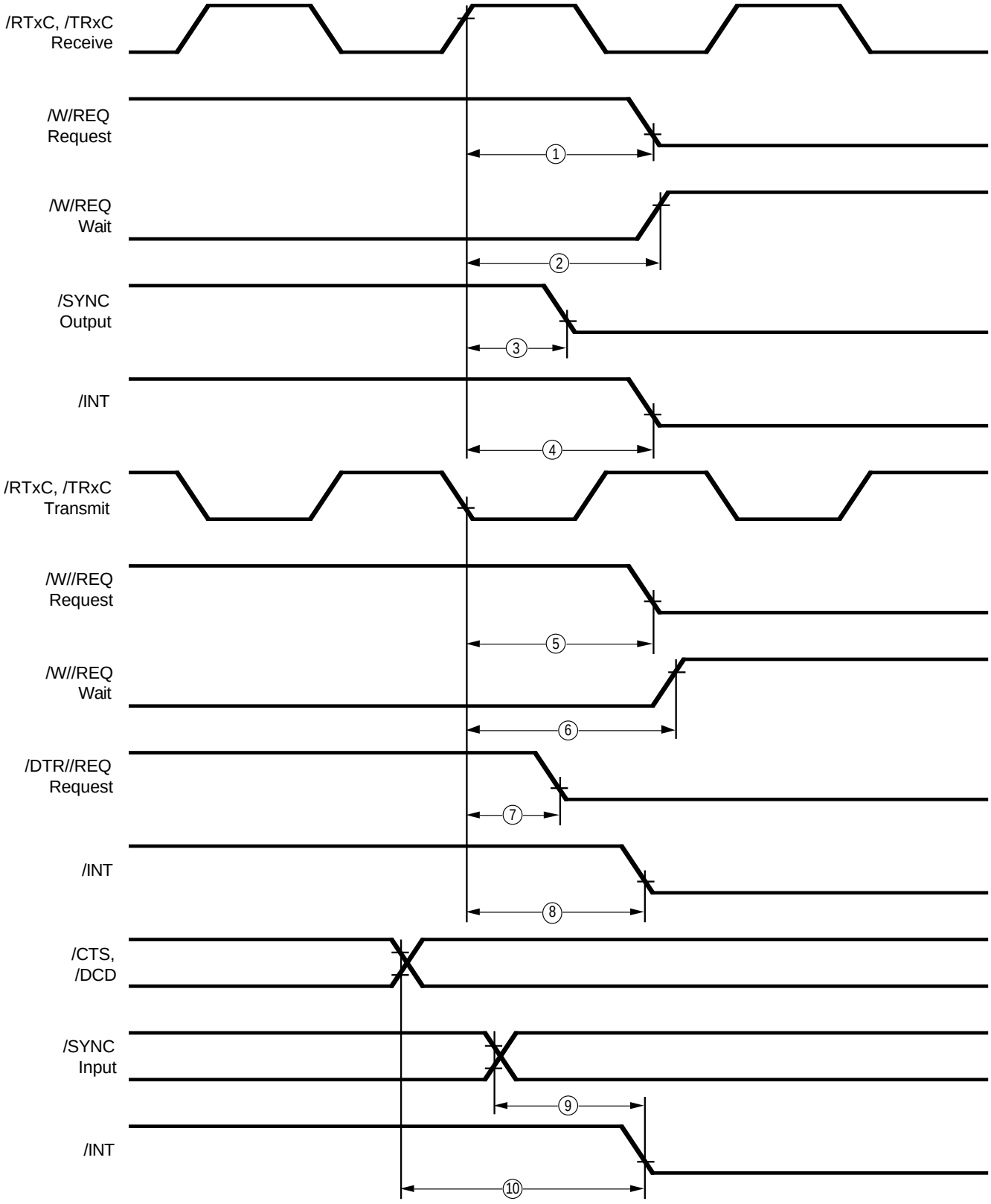
[7] The maximum receive or transmit data rate is 1/4 PCLK.

[8] Applies to DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock should have a 50% duty cycle.

[9] Parameter applies only when WR7' D4 is set to '1'.

## AC CHARACTERISTICS

Z85233 System Timing Diagram (Preliminary)




**System Timing**

## AC CHARACTERISTICS

Z85233 System Timing Table (Preliminary)

| No | Symbol | Parameter | 10 MHz Min | 10 MHz Max | 16 MHz Min | 16 MHz Max | Notes [4] |
|---|---|---|---|---|---|---|---|
| 1 | TdRXC(REQ) | /RXC to /W//REQ Valid | 13 | 17 | 13 | 17 | [2] |
| 2 | TdRXC(W) | /RxC to /Wait Inactive | 13 | 17 | 13 | 17 | [1,2] |
| 3 | TdRXC(SY) | /RxC to /SYNC Valid | 4 | 7 | 4 | 7 | [2] |
| 4 | TdRXC(INT) | /RxC to /INT Valid | 15 | 21 | 15 | 21 | [1,2] |
| 5 | TdTXC(REQ) | /TxC to /W//REQ Valid | 11 | 14 | 11 | 14 | [3] |
| 6 | TdTXC(W) | /TxC to /Wait Inactive | 8 | 14 | 8 | 14 | [1,3] |
| 7 | TdTXC(DRQ) | /TxC to /DTR//REQ Valid | 9 | 12 | 9 | 12 | [3] |
| 8 | TdTXC(INT) | /TxC to /INT Valid | 5 | 9 | 5 | 9 | [1,3] |
| 9 | TdSY(INT) | /SYNC to /INT Valid | 2 | 7 | 2 | 7 | [1] |
| 10 | TdEXT(INT) | /DCD or /CTS to /INT Valid | 3 | 8 | 3 | 8 | [1] |

**Notes:**

[1] Open-drain output, measured with open-drain test load.

[2] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.

[3] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.

[4] Units equal to TcPc

# Z85233 EMSCC ERRATA INFORMATION

The current revision of Zilog's Z85233 EMSCC has total of seven bugs. Suggested workarounds for some of the bugs are provided. The problem descriptions and the suggested workarounds are documented in the following pages.

1. IUS Problem

   (a) Problem Description

   The problem occurs under the following conditions:

   - SDLC 10x19 Status FIFO is enabled
   - Interrupts on Rx Special conditions only

   This mode is intended for an application where received characters are read by a DMA controller. EOF (End Of Frame) is treated differently from other special conditions, e.g. parity error, overrun error and CRC error in this mode.

   When EOF is detected:

   (a) Receive Character Available (RCA) interrupt is generated versus Special Conditions Interrupt in other operating mode.

   (b) The data FIFO is not locked versus locking the data FIFO in other operating mode. This is known as 'Anti-Lock' feature where:

      1. This allows the processor services the EOF interrupt with more latency. Immediate attention from the processor is not necessary because the data FIFO is not locked. Incoming data can still be securely delivered to the Receive FIFO and subsequent incoming data will not be lost.

         It also allows for an operation with no servicing at all of the interrupt.

      2. When the EOF interrupt (RCA interrupt) is serviced, the processor must use the Reset Highest IUS command to clear the EOF interrupt.

      3. If EOF interrupt happens when another lower priority interrupt is enabled, e.g. ext/status interrupt is being serviced, the Reset Highest IUS command issued by the lower priority interrupt service routine (to clear out the pending interrupt) can also accidentally clear the pending EOF interrupt.

      4. The Reset Highest IUS command clears the IP bit related to the EOF (in this mode, RCA IP bit) regardless of the priorities of the pending interrupts.

         This causes a problem when the following circumstances are gathered:

         - Another EMSCC interrupt is being serviced (e.g. Ext/Status interrupt for Transmitter Underrun in Full Duplex operation).
         - The DMA reads a byte marked with the EOF. The corresponding IP bit is set and the /INT line goes low (highest priority interrupt in the daisy chain).
         - The processor does not acknowledge this interrupt at that time, because it is servicing another interrupt.
         - The processor finishes servicing the other interrupt and uses the Reset Highest IUS command.
         - This resets the IP bit corresponding to the EOF, and the EOF interrupt is lost.

## Z85233 EMSCC ERRATA INFORMATION (Continued)

(b) Workarounds

Workarounds are identified and described below:

1. Alternate operating mode

   A very similar operating mode can be used to achieve the same functionality with minimum code modifications. The EMSCC should be operated in "receive interrupts on first character and special condition," instead of "receive interrupt on special condition only."

   In this mode, the anti-lock feature is not enabled. The FIFO is locked after the last character of a frame has been transferred, and the interrupt condition does not disappear until after a "Error Reset" command is issued to the EMSCC. No "Reset Highest IUS" command can clear any IP bit.

2. Use of the daisy chain
   This workaround uses the following two conditions:

   a) If only one channel is used, the EOF interrupt is the highest priority interrupt. As soon as it occurs the /INT pin goes Low, requesting an interrupt to the CPU.

   b) Channel A is the only channel issuing interrupts.

   If both conditions are satisfied, allowing nested interrupts can solve the problem.

   The processor servicing an interrupt on the daisy chain must be interruptible again from another interrupt of higher priority on that same daisy chain.

3. Use of RR7 register

   This workaround is applicable if EOF interrupt is only used to notify another part of the software that there has been another frame received:

   - After issuing the Reset IUS command, read RR7.

   - Check bit 6 of RR7. This bit indicates that the SDLC frame FIFO contains a valid frame. Although one interrupt may have been lost (IP reset) by the Reset IUS command, bit 6 of RR7 will always indicate that at least one frame is available in the frame FIFO.

   - If bit 6 of RR7 equals 1, notify the concerned part of the software that at least one frame is available in the frame FIFO.

(c) Conclusion

When the SDLC FIFO is enabled and 'Receive Interrupts on Special Conditions Only' is selected, software needs to check whether there is a Receive Character Available Interrupt, which is generated by DMA reading an EOF character, before issuing the 'Reset Highest IUS' command. Otherwise, the EOF interrupt conditions were cleared out by the command (Figure 1).

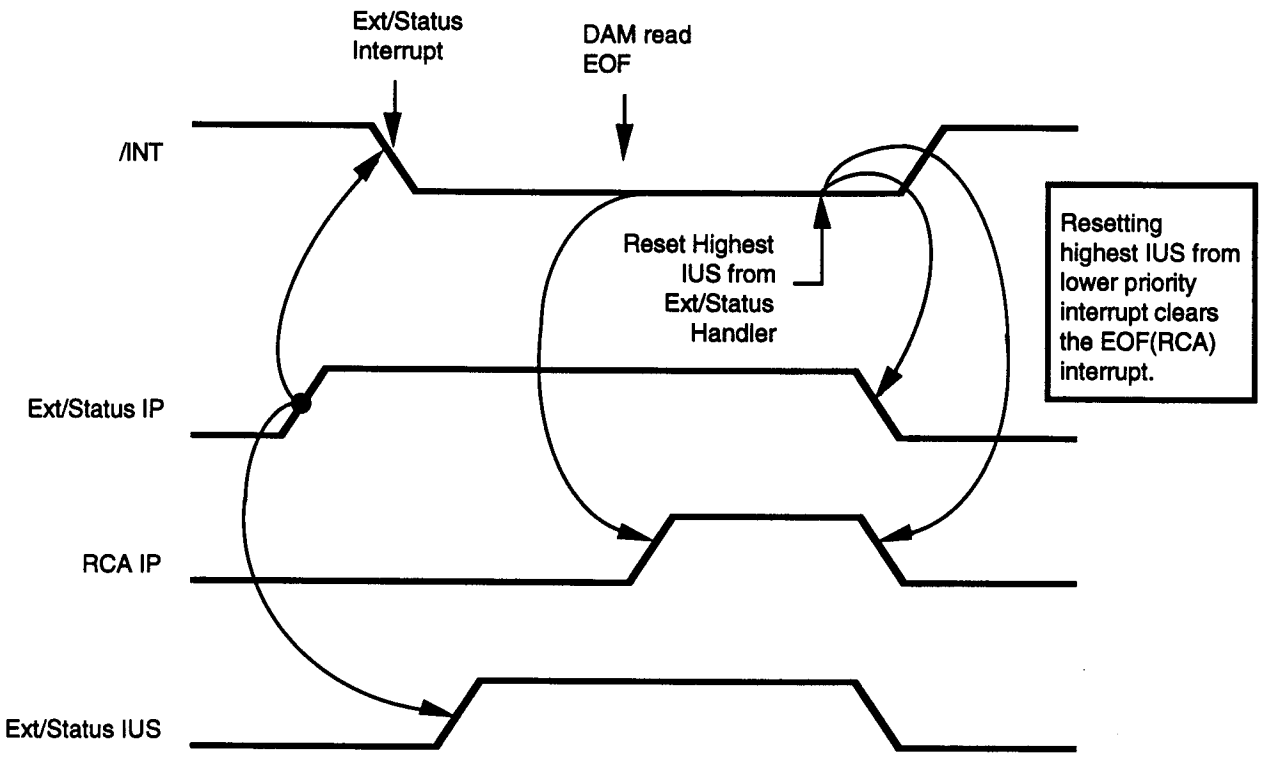



**Figure 1. Resetting Highest IUS From Lower Priority**

## Z85233 EMSCC ERRATA INFORMATION (Continued)

2. RTS Problem

(a) Problem Description

The Z85233 has identified a functional problem in 'Automatic RTS Deactivation' (Figure 2).

This mode is intended for SDLC applications where the /RTS signal from the ESCC is used to enable a line driver in multi-drop line communications.

Before the frame transmission, /RTS is asserted by 'Activate RTS' command (WR5 D1 = 0).

After the last data bit of a frame is sent, transmit underrun interrupt is generated. 'Deactivate RTS' command is issued (WR5 D1 = 1) to deactivate the /RTS signal for turning off the line driver after the multiple-frame packet is completely sent.

In SCC, the processor needs to monitor the data line to make sure that the frame is completely gone before the 'Deactivate RTS' command is issued.

In ESCC, /RTS can be programmed to deactivate automatically after the frame is completely sent without requiring additional monitoring if the following sequence is followed:

- Automatic /RTS Deactivation is enabled (WR7' D2 = 1)
- CRC/Flag on Underrun is enabled (WR10 D2 = 0)
- At transmit underrun interrupt service routine, issue 'Deactivate RTS' command.

  Consequently, the /RTS signal will be deactivated automatically after the closing flag is gone.

The 'Automatic RTS Deactivation' is working properly in single frame and two consecutive frames in back-to-back, but not in multiple back-to-back frames where more than two frames are in back-to-back.

In multiple back-to-back frames transmission, if the 'Deactivate RTS' command is issued at the beginning of the transmit underrun interrupt service routine, /RTS is deactivated after the CRC has gone, but before the closing flag is sent. Since the last frame is not correctly concluded, the frame will be corrupted.

(b) Workarounds

A workaround to the 'RTS Bug' is not to send back-to-back frames. Idle time is inserted in between frames.

Limitations of the workaround:

The system throughput is reduced by the idle time inserted between frames.

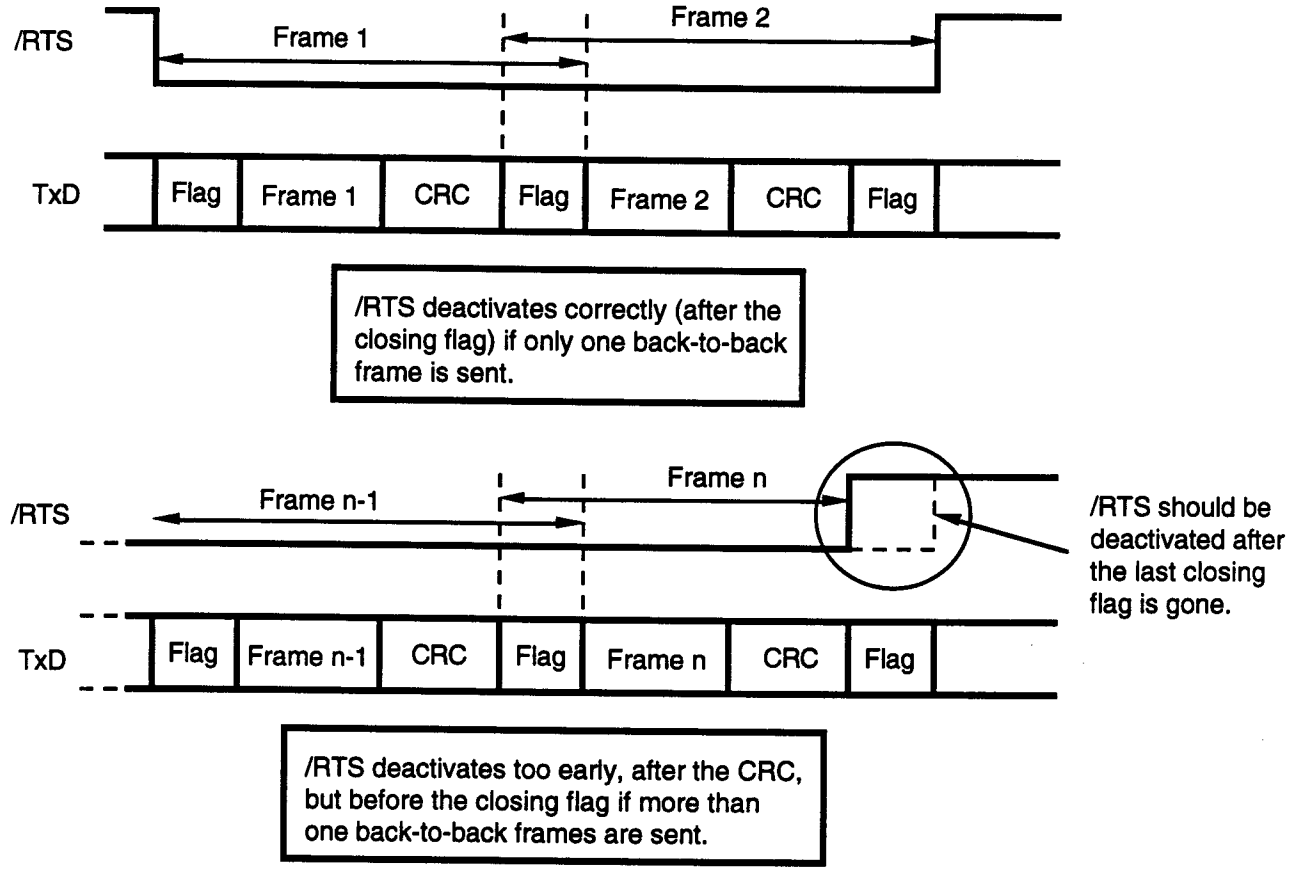



**Figure 2. Automatic RTS Deactivation Bug Illustration**

3. Automatic TxD Forced High in SDLC, NRZI, Mark Idle

   (a) Problem Description

   If WR10 is programmed wth D6, D5=01 (NRZI), D3=1 (Mark Idle) and WR4 D5,D4=10 (SDLC), TxD pin will be forced high after detecting the last bit of the closing flag at the falling edge of the TxC. This feature does not work properly if back to back frame is sent. The TxD output is automatically forced high for the duration of eight bit times and the first byte of the second frame is corrupted. In a multiple frame transmission, a zero bit was inserted before the opening flag of the second frame.

   (b) Workarounds

   Send back-to-back frames in Flag Idle:

   Since the 'Automatic TxD forced high' feature is having problems only if all the following conditions are gathered:

   - Back-to-back frame transmission
   - NRZI
   - Mark Idle

   Setting the system in Flag Idle mode (WR10 D3=0) in frame transmission allows back-to-back frames to be correctly sent without any data corruption.

## Z85233 EMSCC ERRATA INFORMATION (Continued)

4. SDLC FIFO Overflow

(a) Problem Description

In SDLC mode, D7 of RR7 (FIFO Overflow status bit) is set if the 11th frame is written to the 10X19 SDLC status FIFO while the FIFO is full, (i.e., 10 frames have been accumulated in the Status FIFO and have not yet been read by the Processor). Under this circumstance, the status FIFO is locked and no data can be written to the Status FIFO until D7 of RR7 is reset.

1. If the EMSCC is set up in Anti-Lock mode, i.e., the SDLC FIFO is used when 'Receive Interrupts on Special condition only' is enabled, the only way to reset D7 of RR7 (the FIFO Overflow bit), is to reset and set D2 (SDLC FIFO Enable Bit) of WR15. This causes the SDLC FIFO to be reset and all the SDLC frame information to be lost.

   With no Anti-Lock feature, the FIFO Overflow status bit is reset if SDLC FIFO is read.

2. If the EMSCC is setup in NRZI and Mark Idle in back-to-back frame transmission, once the FIFO Overflow bit (D7 of RR7) is set, the only way to reset the status is to reset and set D2 (SDLC FIFO Enable Bit) of WR15. This causes the SDLC FIFO to be reset and the unprocessed frame information stored in the SDLC FIFO to be lost.

(b) Workarounds

Do not use "Receive Interrupts on Special Conditions Only" and Mark Idle if there is a possibility of Status FIFO Overflow.

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5. Default RR0 Value

(a) Problem Description

D7 of RR0, Break/Abort status bit, is not consistently cleared after reset.

(b) Workarounds

Ignore the first D7 value read from RR0 after reset.

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6. Default RR10 Value

(a) Problem Description

D6 of RR10, Two Clock Missing bit, is sometimes erroneously set to indicate that the DPLL detects a clock edge in two successive tries after hardware reset.

(b) Workarounds

Ignore the first D6 value read from RR10 after hardware reset.

7. CRC Problem

(a) Problem Description

The CRC cannot be interpreted correctly from the Receive FIFO when one or two residue bits are sent. The CRC value is correctly received and checked but is not loaded to the Receive FIFO properly.

1. Two Residue Bits
   (Residue code = '000')

The last 3 bytes of the Receive FIFO will read:

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C5 | C4 | C3 | C2 | C1 | C0 | D9 | D8 |
| C15 | C14 | C13 | C12 | C11 | C10 | C9 | C8 |

Bit 6 and 7 of the CRC are lost.

2. One Residue Bit
   (Residue code = '111')

The last 3 bytes of the Receive FIFO will read:

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| C6 | C5 | C4 | C3 | C2 | C1 | C0 | D8 |
| C15 | C14 | C13 | C12 | C11 | C10 | C9 | C8 |

Bit 7 of the CRC is lost.

The CRC is received and loaded properly into the Receive FIFO in other situations, i.e., 0,3,4,5,6,7 residue bits.

The Residue Code (bit 3,2,1 of RR1) is reported correctly independent of the number of residue bits sent.

(b) Workaround

Ignore the CRC value read from the Receive FIFO if one or two residue bits are sent.



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