THE DATASHEET OF

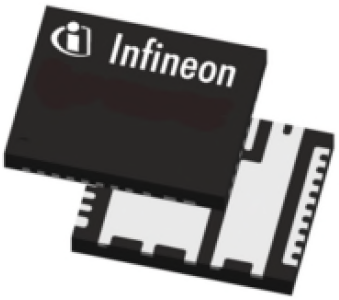
DHP1050N10N5AUMA1

100 V OptiMOS™ PowerStage

DHPx050N10N5

Features

- Symmetrical half-bridge 100V MOSFETs integrated with level-shift driver
- 100 V OptiMOS™ 5 Power MOSFET technology
- (DHP0050N10N5) Independently controlled high-side and low-side gate drivers
- (DHP1050N10N5) Differential input for superb robustness with inherent shoot-through protection
- Up to 20 A current handling capability
- 120 V On-chip bootstrap diode
- Maximum VDD Voltage 20 V
- Support operating frequency up to 1 MHz
- VDD/VHB under voltage lockout (UVLO)
- -10 V to 20 V input pin capability for increased robustness
- (DHP1050N10N5) -8 V to 15 V input pin common mode rejection
- -5 A output pin reverse current capability
- 8 V to 17 V supply voltage operating range
- Fast propagation delay
- < 6 ns delay matching between high- and low-side drivers
- Small 7.5 mm x 6.0 mm x 0.9 mm PQFN package
- Lead free RoHS compliant package



Potential applications

- Power modules and on-board converters for Telecom
- half-bridge and full-bridge converters
- Intermediate bus architecture
- Synchronous buck converter

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

DHPx050N10N5 is a 100 V half-bridge module designed for advanced DC/DC converter applications such as telecom bus converters. Technology offers an extremely compact, high performance half-bridge topology in an isolated package. This advanced device offers a combination of low $R_{DS(on)}$ and fast switching OptiMOS technology and the optimized half-bridge driver in a small PQFN package. At only 7.5 mm x 6 mm and featuring integrated bootstrap functionality, the compact footprint of this surface-mount package makes it suitable for applications that are space-constrained.

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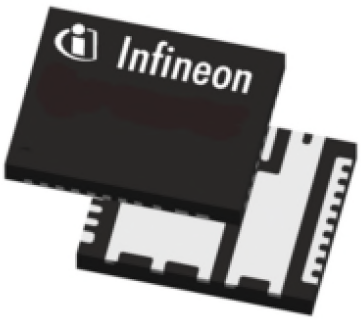
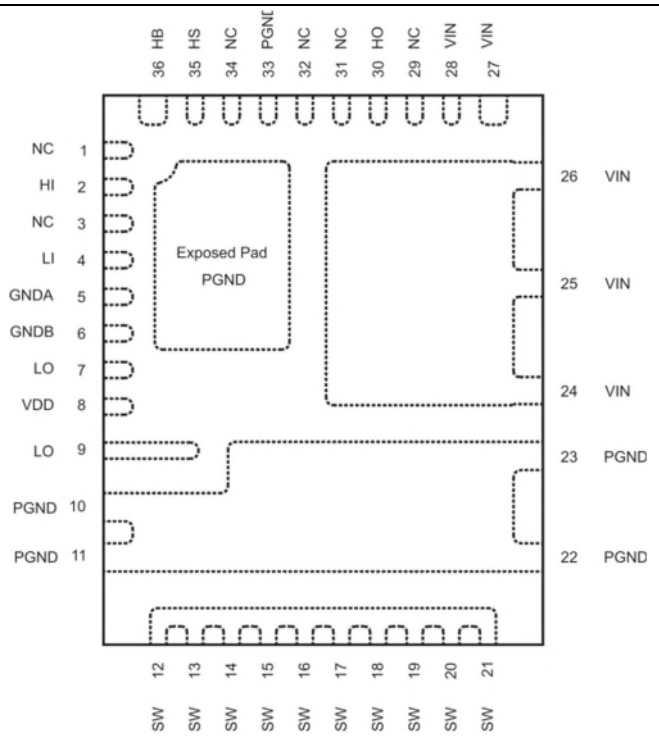
1 Package Information

PQFN-36	RoHS HAL	

1.1 Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
DHP0050N10N5	PQFN 7.5 mm x 6 mm	Tape and Reel	4000	DHP0050N10N5AUMA1
DHP1050N10N5	PQFN 7.5 mm x 6 mm	Tape and Reel	4000	DHP1050N10N5AUMA1

1.2 Module Pin-Out Description



(Top Transparent View)

Figure 1 Pin Configuration of PG-IQFN-36-1, Top Transparent View

Table 1 Pin Description

Pin #	Pin Name	Pin Description
1, 3, 29, 31, 32, 34	NC	Leave the pin unconnected or short neighboring VIN plane or ground.
2	HI	High side PWM input
4	LI	Low side PWM input
10, 11, 22, 23, 33	PGND	Power ground. It is also the power ground of the low-side MOSFET.
5	GNDA	Driver ground A. All driver power and signals are referenced to this pin.[1]
6	GNDB	Driver ground B. All driver power and signals are referenced to this pin.[1]
7, 9	LO	Low-side MOSFET driver output pin that can be connected to a test point in order to observe the waveform.
8	VDD	The supply of gate driver. Connect a 1uF cap between VDD and GNDA.
12-21	SW	Switching node of half bridge.
24-28	VIN	Up to 100V high current input voltage connection.
30	HO	High-side MOSFET driver output pin that can be connected to a test point in order to observe the waveform.
35	HS	Phase (switching) node. For Bootstrap capacitor connection only.
36	HB	High-side bootstrap. Connect a minimum 0.1µF capacitor from HB to HS pin. The bootstrap capacitor provides the charge to turn on the high-side MOSFET.

[1] Due to the benefit of differential input, the driver IC requires no separate ground between signal and power. Therefore, PGND, GNDA, and GNDB are connected internally.

2 Block Diagram

A simplified functional block diagram is given in the figure below

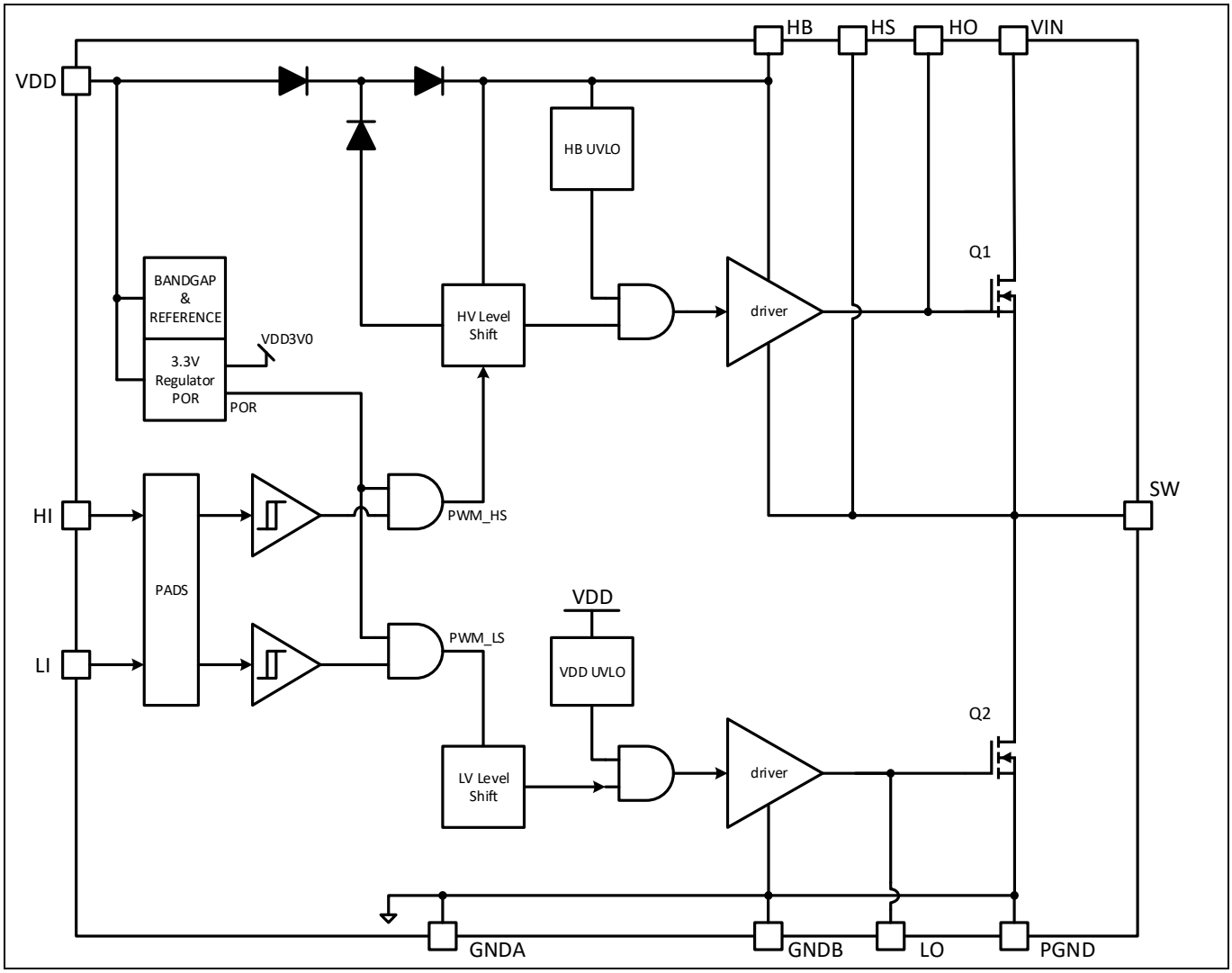


Figure 2 Block Diagram

3 Functional Description

The device is an integrated power stage designed to support advanced switching converters such as in telecom and datacom applications. The device pairs a level-shifted half-bridge driver with 100 V high-side and low-side symmetrical power MOSFETs. It features 4 A source current for both high-side and low-side and a strong 5 A high-side and 6 A low-side sink current driving capabilities to combat induced turn on.

DHP0050N10N5's input pins support TTL logic levels independently of supply voltage. They are capable to withstand voltages from -10 V to 20 V, allowing the device to interface with a broad range of analog and digital controllers. The input stage features built-in hysteresis for enhanced noise immunity. The low-side and high-side gate drivers are independently controlled and matched to typical 2 ns between the turn on and turn off of each other.

DHP1050N10N5's input pins support TTL logic levels independently of supply voltage. They are capable to withstand voltages from -10 V to 20 V and ground potential shifts from -8 V to 15 V, allowing the device to interface with a broad range of analog and digital controllers. The input stage features built-in hysteresis for enhanced noise immunity. The low-side and high-side gate drivers are differentially controlled and matched to typical 2 ns between the turn on and turn off of each other. The differential inputs provide inherent shoot-through protection and ensure high-side and low-side outputs are never on at the same time.

The switching node (HS pin) is able to handle negative voltages down to –(24 - V_{DD}) V which allows the high-side channel to be protected from inherent negative voltages caused by parasitic inductance and stray capacitance.

Under-voltage lockout circuits are provided for both high- and low-side drivers. UVLO protects the system by forcing the output low when the supply voltage is lower than the specified threshold.

The following sections describe key functionalities.

3.1 Supply Voltage

The absolute maximum supply voltage is 20 V. The minimum operating supply voltage is set by the under-voltage lockout function to a typical default value of 7.0 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

3.2 Input Control

DHP0050N10N5 device responds to the two inputs signals (HI and LI) independently according to the following truth table.

Table 2 DHP0050N10N5 Truth Table

LI	HI	LO	HO
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

The high-side and low-side outputs respond to high-side and low-side inputs independently.

DHP1050N10N5 device responds to the combination of two inputs signals (HI and LI) according to the following truth table.

Table 3 DHP1050N10N5 Truth Table

LI	HI	LO	HO
L	L	L	L
H	L	H	L
L	H	L	H
H	H	L	L

True differential input comes with inherent shoot through protection by preventing both low and high side to be on at the same time. It also provides noise immunity against ground bounce. The input stage is designed to operate reliably against –8 V / +15 V ground voltage drift. Input logic hysteresis also helps combat disturbances to the input signal.

3.3 Driver Outputs

The low output impedances allow fast transition of the load transistor. Specifically, the ultra-low impedance pull down resistances, typically 0.5 Ω for the high side and 0.35 Ω for the low side, keep the gate of the load transistor down during fast transient events – avoiding dv/dt induced re-turn-on.

3.4 Under-voltage Lockout (UVLO)

The under voltage lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO rising threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch on the device, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 7.0 V with 0.5 V hysteresis for supply voltage (V_{DD}) and 5.75 V with 0.25 V hysteresis for high side boot voltage (V_{HB}).

UVLO threshold trigger is synchronous. The clock gating ensures minimum pulse width set by the controller is obeyed at all times. This increases robustness of the integrated boot diode due to the controllability of the reverse recovery behavior.

3.5 Minimum Pulse Width

The device responds to input level according to the truth table in section Input Control as long as the logic signal complies with the minimum pulse width requirement. Signal pulse longer than the minimum allowable input pulse width yields valid output. Any output in response to shorter pulses or glitches should be disregarded and filtered out by the user. Under all allowable operation above input minimum pulse width of 40ns, the output behaves one to one to the input with minimal pulse width distortion.

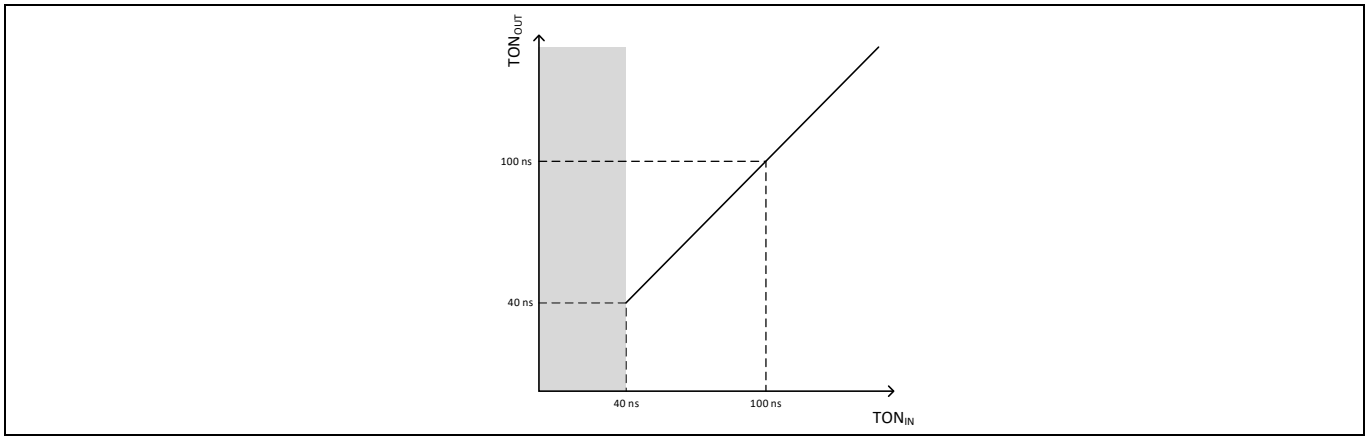


Figure 3 Minimum Pulse Width Input-output On-time Transfer Function

This is diagram is illustrative only with typical value. Actual value and pulse width distortion is subject to process variation. Output pulse width could in some case be shortened or extended to prevent retoggling. See transient detector section below.

3.6 Transient Detector

The transient detector block is designed to prevent re-toggling of the HO output in case of potential instability of the level shifter caused by phase node movement. For example, a fast-rising phase node voltage could pull the power ground (PGND) down. This could result in potential between HI and PGND higher than the rising threshold of the high-side signal. Such a glitch or noise can be picked up by the driver and propagate through which can lead to a shoot-through event, transformer volt-second imbalance, and potential device destruction.

The following describes the basic operation of the block.

- The transient detector monitors the phase node and tracks its movement, and the rate of change over time for both rising and falling edge.
- Whenever the rate of change is larger than a certain dv/dt threshold[1], the transient detector is active and blocks the HO output from changing state.
- A High-side Input (HI) toggle triggers a decision to change the state, but HO waits until the transient detector's active state is removed, then the decision is propagated through.

Additional propagation delay caused by the transient detector is limited to one-half of the oscillation period, as the signal always propagates through whenever the transient detector sees a peak or valley where dv/dt approaches zero. See link to *Understanding the transient detector* [1] for more information.

[1] Reference slew rate threshold versus temperature under Section 6 Typical Characteristics

4 Characteristics

4.1 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Symbol	Description	Min	Max	Unit
V_{IN}	Input Supply Voltage[1]	---	100	V
V_{DD}	Driver Supply Voltage	-0.3	20	V
V_{SW},V_{HS}	Phase Voltage[1,2]	-(24 - V_{DD})	V_{HB} + 0.3	V
V_{HB}	High Side Bootstrap Voltage[1,2]	-0.3	120	V
V_{HI}, V_{LI}	LI and HI Input Voltage	-10	20	V
T_J	Operating Junction Temperature	-40	150	°C
V_{LO}	Output voltage on LO	-0.3	V_{DD} + 0.3	V
V_{HO}	Output voltage on HO	V_{HS} – 0.3	V_{HB} + 0.3	V
I_{OR}	LO and HO Peak Reverse Current[3]	---	5	A
T_S	Storage Temperature	-55	150	°C

4.2 ESD Ratings

Symbol	Description	Value	Unit
ESD_{HBM}	Human Body Model sensitivity as per ANSI/ESDA/JEDEC JS-001 (HBM Class 1C)	1000 to < 2000	V
ESD_{CDM}	Charged Device Model sensitivity as per ANSI/ESDA/JEDEC JS-002 (CDM Class C3)	≥ 1000	V

4.3 Recommended Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All parameters specified in the subsequent tables refer to these operating conditions.

Symbol	Description	Min	Typ	Max	Unit
V_{IN}	PowerStage Input Voltage	---	---	80	V
V_{SW},V_{HS}	Phase Voltage to PGND	-(24 - V_{DD})	---	80	V
V_{DD}	Driver Supply Voltage	8	10	17	V
V_{HB}	High Side Bootstrap Voltage	-0.3	---	90	V
T_J	Junction Temperature	-40	---	125	°C
dv/dt	HS Slew Rate	---	---	50	V/ns

[1] All voltage ratings in this section referenced to ground and for Tc = 25 °C.

[2] Not subject to production test. Verified by design/characterization.

[3] For <500ns pulses

V_I	Differential Input Voltage[1] (DHP1050N10N5)	0	3.3	5	V
V_{ICMR}	Input Signal Common Mode Rejection (DHP1050N10N5)	-8 + V_I/2	---	15 – V_I/2	V

4.4 Static Electrical Characteristics

V_{DD} = (V_{HB}-V_{HS}) = 12 V. T_C = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to ground. The V_{DDR} parameters are referenced to ground. The V_{HBR} parameters are referenced to V_{HS}.

Symbol	Description	Min	Typ	Max	Units	Conditions
$R_{DS(on)}$	Drain-Source On-resistance[5]	---	4.3	5.0	mΩ	
V_{DDR}	V_{DD} UVLO Rising Threshold	6.6	7.0	7.4	V	
V_{DDH}	V_{DD} UVLO Threshold Hysteresis	---	0.5	---	V	
V_{HBR}	V_{HB} UVLO Rising Threshold[7]	5.5	5.75	6.0	V	
V_{HBH}	V_{HB} UVLO Threshold Hysteresis	---	0.275	---	V	
I_{HB}	Boot Voltage Quiescent Current	---	0.55	0.7	mA	V_{LI}=V_{HI}=0V
I_{HBO}	Boot Voltage Operating Current	---	30	---	mA	f=500kHz, Q_g=50nC
I_{DD}	V_{DD} Quiescent Current	---	0.55	0.7	mA	V_{LI}=V_{HI}=0V
I_{DDO}	V_{DD} Operating Current	---	30	---	mA	f=500kHz, Q_g=50nC
R_{IN}	Input Pulldown Resistance	54	68	82	kΩ	
V_{IR}	Rising Input Voltage Threshold	---	2.25	2.9	V	
V_{IF}	Falling Input Voltage Threshold	1.0	1.65	---	V	
V_{IH}	Input Logic Voltage Hysteresis	---	0.6	---	V	
R_{PUH}	High Side Pull Up Resistance	---	1.0	---	Ω	
R_{PDH}	High Side Pull Down Resistance	---	0.5	---	Ω	
R_{PUL}	Low Side Pull Up Resistance	---	1.0	---	Ω	
R_{PDL}	Low Side Pull Down Resistance	---	0.35	---	Ω	

4.5 Dynamic Electrical Characteristics

V_{DD} = (V_{HB}-V_{HS}) = 12 V, T_J=25°C, unless otherwise specified. Timing parameters are for driver portion only.

Symbol	Description	Min	Typ	Max	Units	Conditions
I_{PUH}	High Side Peak Pull Up Current[8]	---	4	---	A	V_{HO} = 0 V
I_{PDH}	High Side Peak Pull Down Current[8]	---	5	---	A	V_{HO} = 12 V
I_{PUL}	Low Side Peak Pull Up Current[8]	---	4	---	A	V_{LO} = 0 V
I_{PDL}	Low Side Peak Pull Down Current[8]	---	6	---	A	V_{LO} = 12 V

[1] Absolute voltage difference between HI And LI (|V_{HI}-V_{LI}|)

[5] Not subject to production test. Refer to BSC050N10NS5 datasheet for other MOSFET parameters.

[7] HB (high side bootstrap) related ratings referenced to V_{HS}.

[8] Not subject to production test.

T_{DR}	Rising Propagation Delay [1,2]	---	45	54	ns	
T_{DF}	Falling Propagation Delay[2,3]	---	45	54	ns	
T_{DM}	Delay Matching[4]	---	2	6	ns	
T_{PW}	Minimum Input Pulse Width[5]	---	---	40	ns	
T_{DRR}	Bootstrap Diode Turn off Time[6]	---	10	---	ns	I_F = 20 mA, I_{PRR} = 0.5 A

4.6 Thermal and Mechanical Characteristics

Symbol	Description	Min	Typ	Max	Units	Conditions
R_{thJC}	Junction to Case Thermal Resistance	---	0.32	---	°C/W	Bottom
		---	12.3	---		Top
R_{thJA}	Device on PCB	---	36	---	°C/W	6 cm^2 cooling area[7]

[1] Rising propagation delay from LI to LO and from HI to HO.

[2] A transient detector blocks the toggling of the high side output when it detects moving phase node (due to transition and/or oscillation). It prevents unwanted retoggling but may increase propogation delay. See transient detector activation in Figure 6.

[3] Falling propagation delay from LI to LO and from HI to HO.

[4] Delay matching between (1) LO Rising and HO Failing and (2) LO Falling and HO Rising, where LO and HO are measured when they reach MOSFET's typical gate threshold votlage

[5] Minimum input pulse width that produces valid output signal.

[6] External schottky boot diode in parallel recommended for high dv/dt application

[7] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thick) copper area for drain connection. PCB vertical in still air.

5 Descriptive Illustration

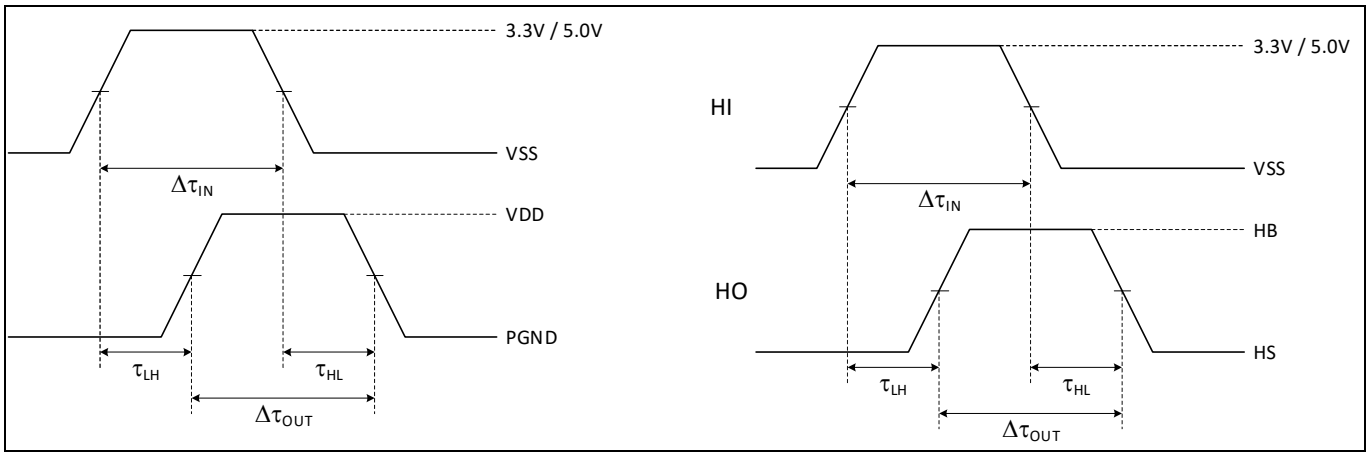


Figure 4 Propagation delay

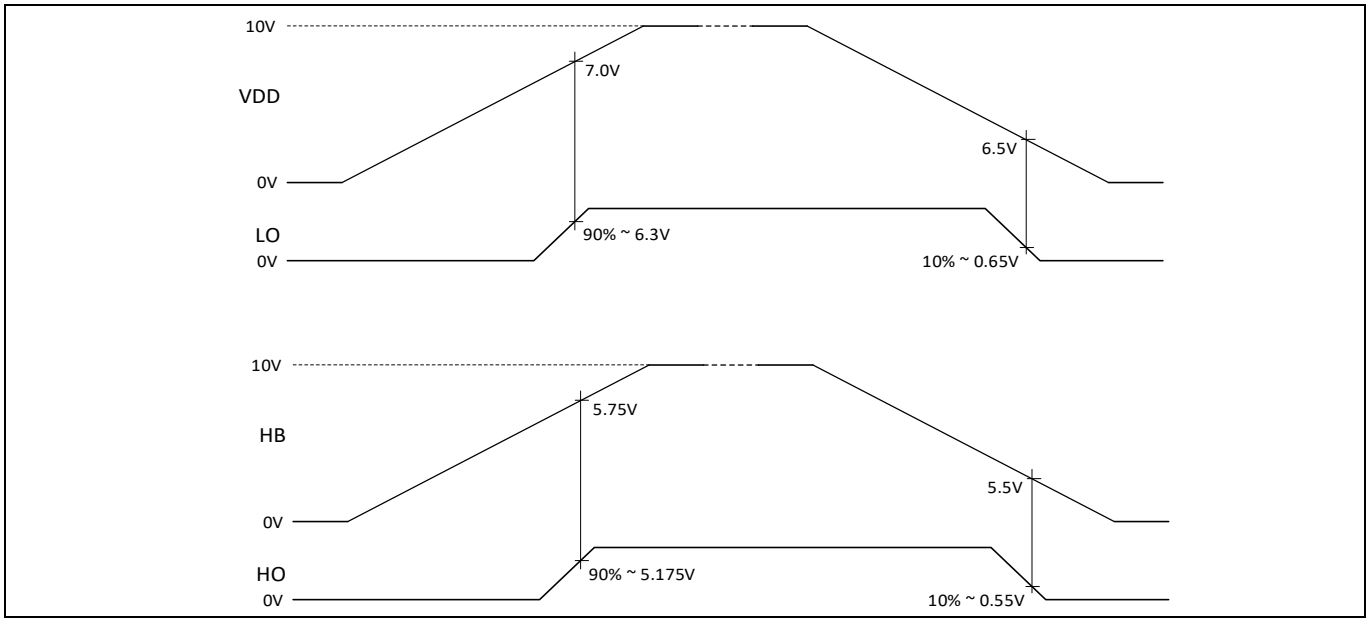


Figure 5 UVLO behavior

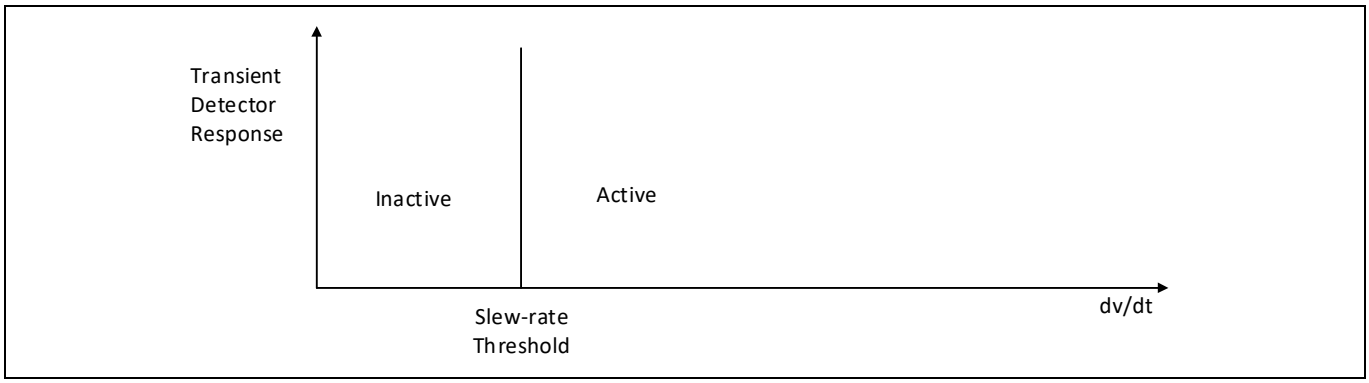
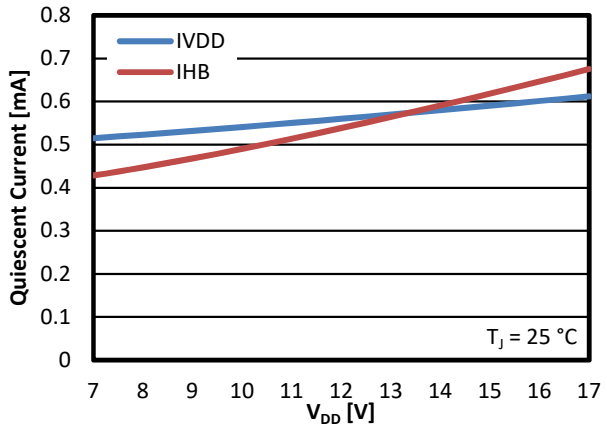


Figure 6 Transient Detector Response[1]

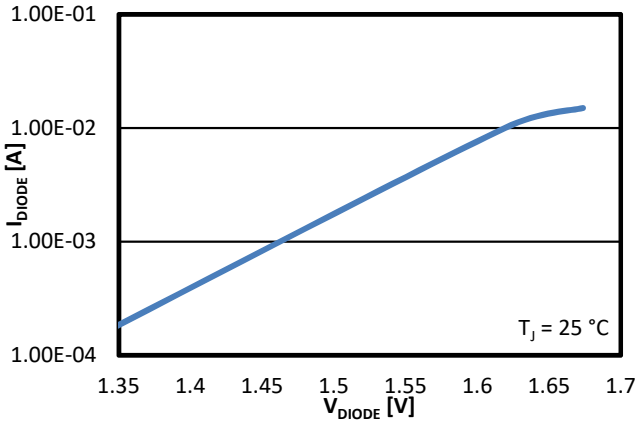
[1] Reference slew rate threshold versus temperature under Section 6 Typical Characteristics.

6 Typical Characteristics

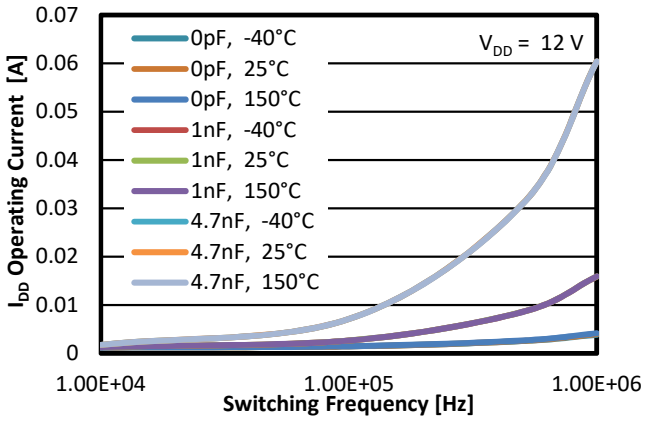
Quiescent Current vs. V_{DD}



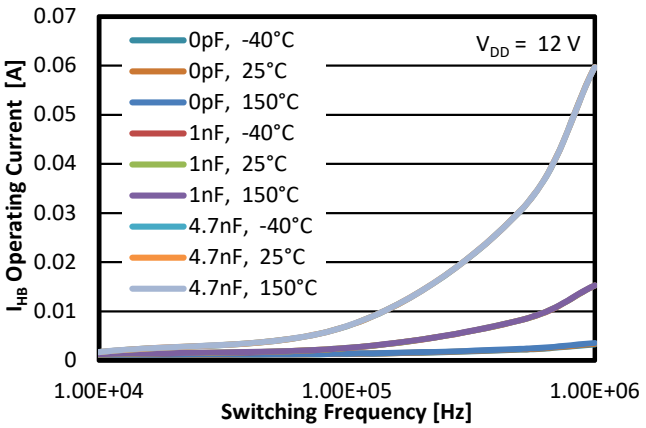
Diode Current vs. Voltage



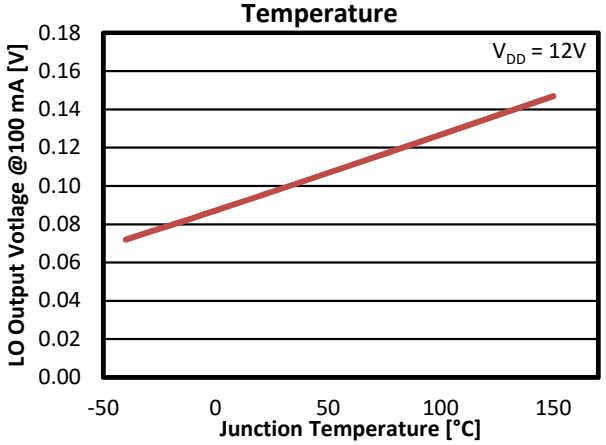
I_{DD} Operating Current vs. Temperature



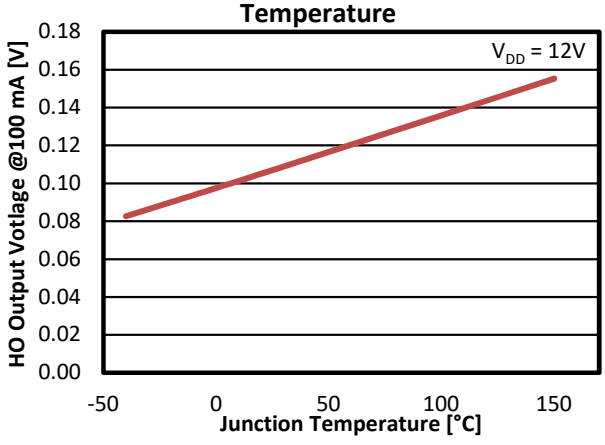
I_{HB} Operating Current vs. Temperature



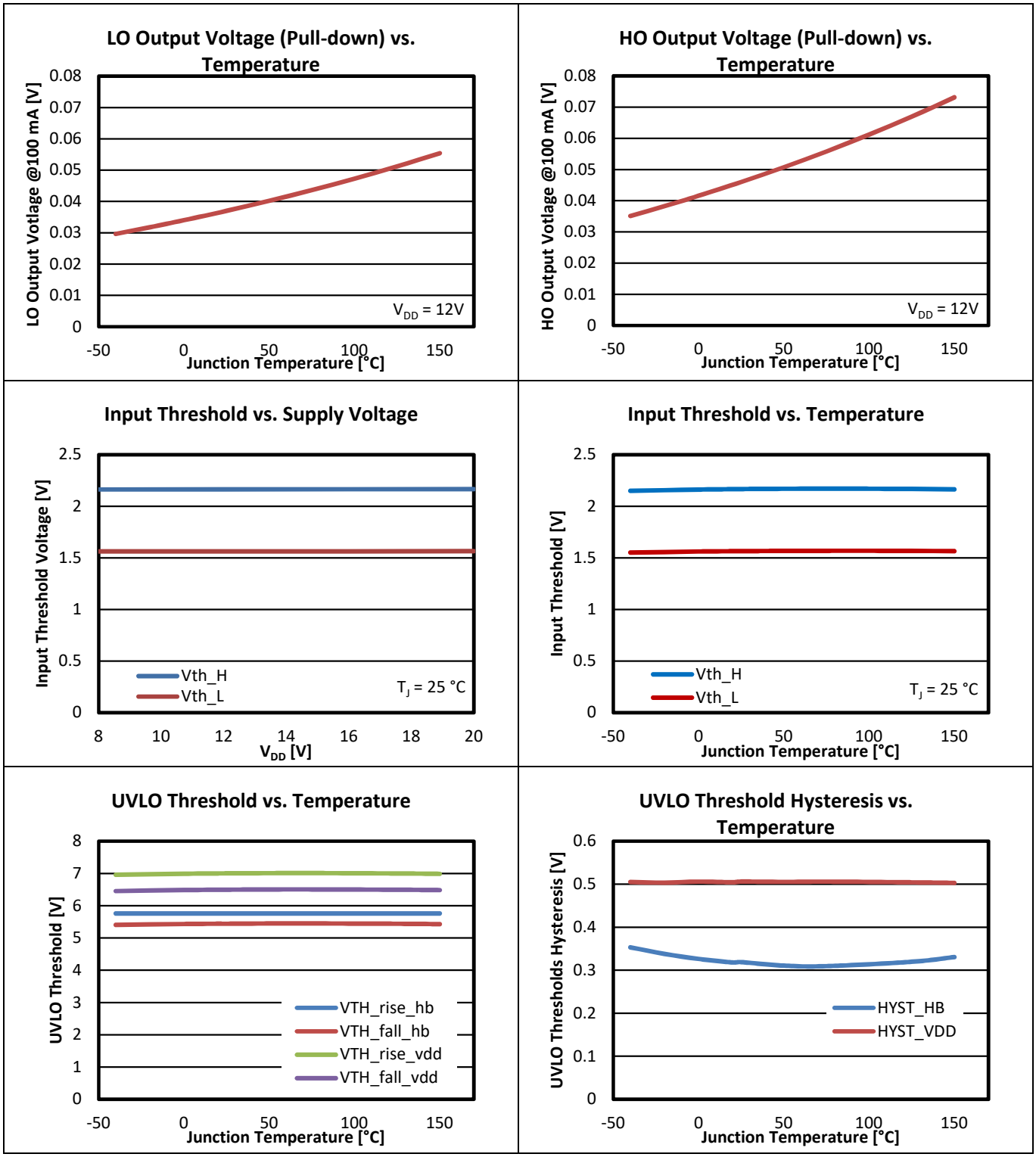
LO Output Voltage (Pull-up) vs. Temperature



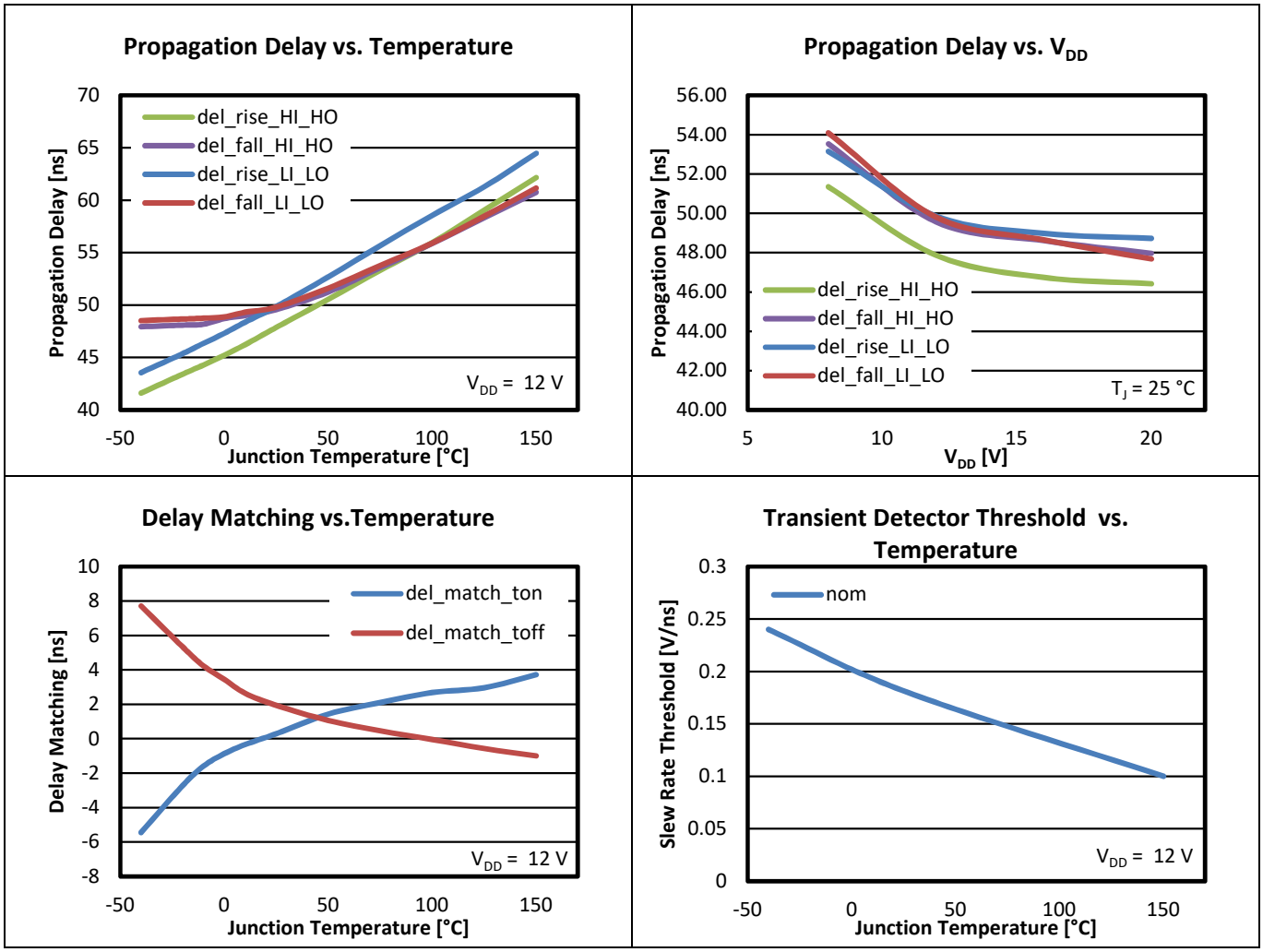
HO Output Voltage (Pull-up) vs. Temperature



Typical Characteristics



Typical Characteristics



7 Application and Guidelines

7.1 Typical Application Diagram

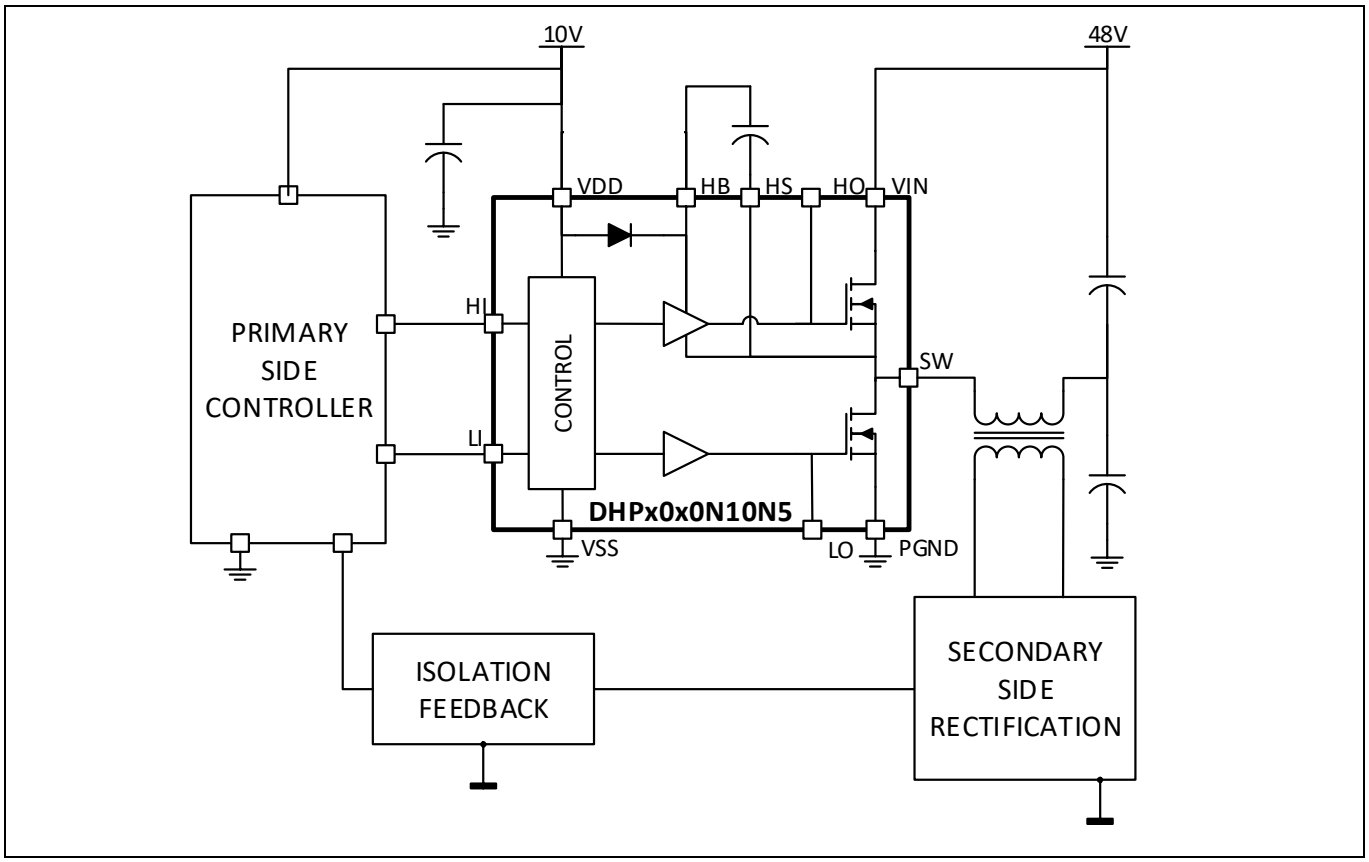


Figure 7 Typical Application 1 – Primary Side Half-bridge

7.2 Design Guidelines

In a half-bridge configurations, a high-side bias which is referenced to the switch node is needed in order to drive the gate of the high-side mosfet. One of the most common solutions due to its simplicity and low cost is the usage of a bootstrap circuit consisting of an internal boot diode and a capacitor as seen in **Figure 8**. However, this method imposes limitation on the power converter's duty cycle due to the requirement of recharging the bootstrap capacitor. This limitation can be mitigated through the proper selection of the bootstrap components.

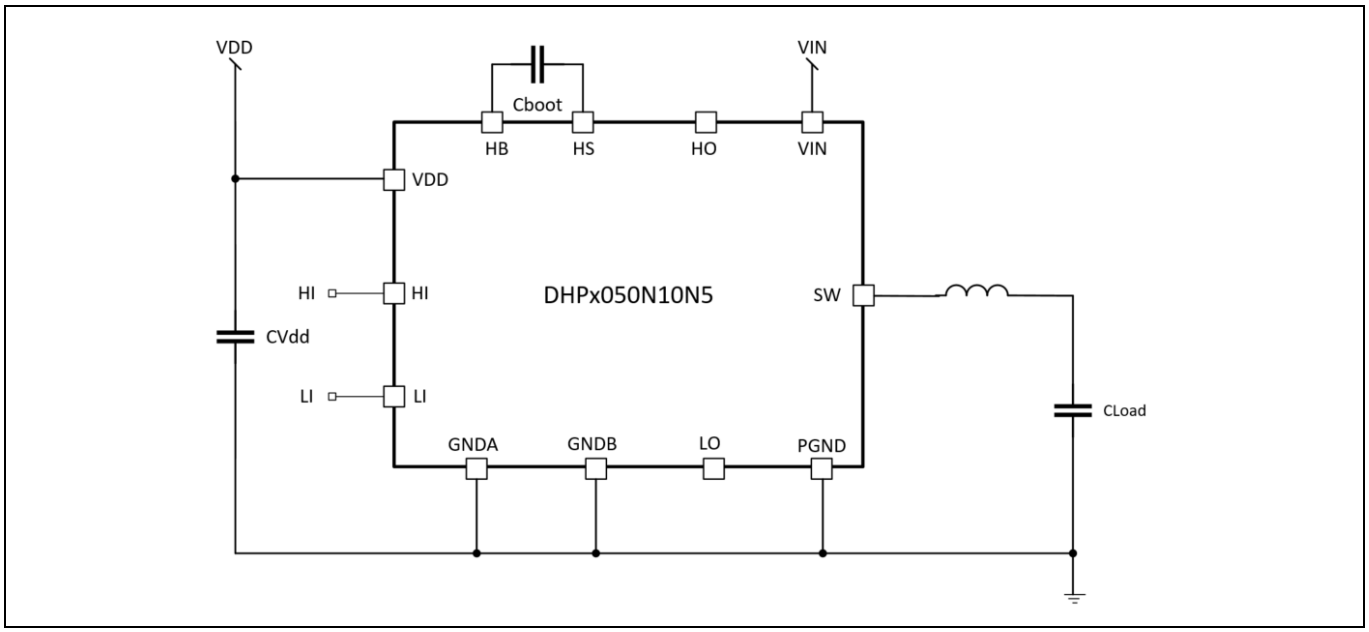


Figure 8 Gate drive circuitry

The bootstrap circuit operation is defined by two main periods:

Charging period: When the low-side mosfet (Q2) is ON and the high-side mosfet (Q1) is OFF, the switch node (SW) pin is pulled to ground creating a charging path for the bootstrap capacitor (C_{boot}) through the Vdd bypass capacitor (C_{Vdd}) and the internal bootstrap diode. For high dV/dt application, it is recommended to use an extrenal bootstrap diode.

Discharging period: When the low-side mosfet (Q2) is turned OFF and the high-side mosfet (Q1) starts conducting, the switch node (SW) pin is pulled to the high voltage V_{in} thus the internal bootstrap diode gets reverse biased. The bootstrap capacitor (C_{boot}) will then discharge some of its stored charges to the gate of the high-side mosfet as well as to other contributing factors such as the mosfet's gate-source leakage current, floating section quiescent current, floating section leakage current and the internal bootstrap diode reverse bias leakage current.

Typical waveform for the voltage across C_{boot} as a function of time is shown in **Figure 9** where the various contributions have been distinguished. The voltage across C_{boot} increases during the charging period and then it drops with a high negative dV/dt as it charges the gate of the high-side mosfet (Q1). After which, the C_{boot} voltage continues to drop but with a much lower slope because only the high-side bias current and some leakage current is discharing the C_{boot} during this phase.

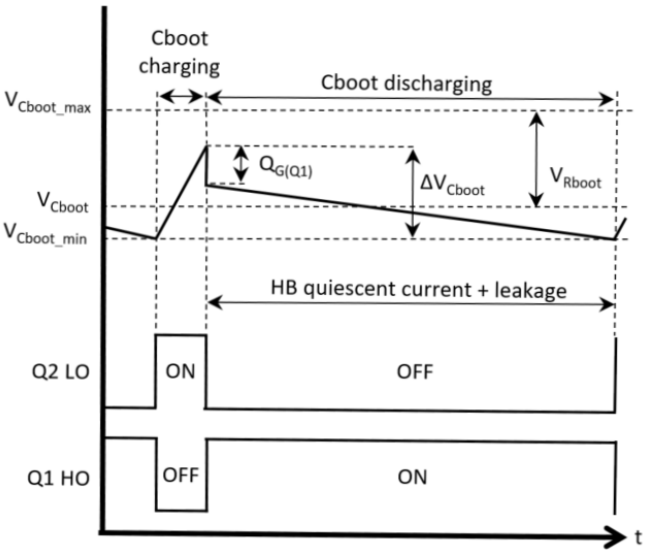


Figure 9 Typical C_{boot} waveform

7.2.1 Bootstrap Capacitor Selection

The bootstrap capacitor provides the necessary charge to drive the high-side mosfet and thus it needs to be sized in such a way that the maximum voltage drop across this capacitor will not fall below the high-side UVLO threshold during transient and normal operations. First, determine the maximum allowable voltage drop (ΔV_{Cboot_max}) when the high-side mosfet (Q1) is on which is given by the following formula:

$$\Delta V_{Cboot\_max} = V_{dd} - V_F - V_{HBR} - V_{HBH} \quad (1)$$

Where:

V_{dd} = Gate driver supply voltage

V_F = Bootstrap diode forward voltage drop with typical value of 1.25V at

I_F=100uA and 2.15V at I_F=100mA , T_J=25°C

V_{HBR} = HB UVLO rising threshold

V_{HBH} = HB UVLO threshold hysteresis

Next, determine the total charge (Q_T) that must be delivered by the bootstrap capacitor at maximum duty cycle. As mentioned, there are several factors that contribute to the discharge of the bootstrap capacitor such as the Q1's total gate charge, Q1's gate-source leakage current, HB quiescent current, HB leakage current, bootstrap diode reverse bias leakage current and bootstrap capacitor leakage current (if using an electrolytic capacitor). For sake of simplicity, only Q1's total gate charge and HB quiescent and leakage current are considered as the other sources of leakage are negligible in comparison.

$$Q_T = Q_G + \frac{I_{HB}}{F_{sw}} + I_{HBS} \times \frac{D_{max}}{F_{sw}} \quad (2)$$

Where:

Q_G = high-side mosfet (Q1) total gate charge

I_{HB} = HB maximum quiescent current

I_{HBS} = HB to VSS leakage current with a typical value of 1.25mA at 90V HB voltage and T_J=25°C

D_{max} = maximum duty cycle

F_{sw} = switching frequency

The minimum bootstrap capacitor value can then be calculated using the formula:

$$C_{boot\_min} \geq \frac{Q_T}{\Delta V_{Cboot\_max}} \quad (3)$$

7.2.2 VDD Bypass Capacitor Selection

The Vdd bypass capacitor provides the charge for the bootstrap capacitor during the charging period. As a rule of thumb, the Vdd bypass capacitor should be sized to be atleast 10~20 times larger than the bootstrap capacitor. This equates to a voltage ripple of 5~10% in the Vdd capacitor.

$$C_{Vdd} \geq 10\sim20 \times C_{boot} \quad (4)$$

7.2.3 Bootstrap Resistor Selection

The bootstrap resistor limits the current in the bootstrap diode during start-up when the bootstrap capacitor is initially completely discharged. The peak current through this resistor is given by:

$$I_{Pk\_Rboot} = \frac{V_{DD} - V_F}{R_{boot}} \quad (5)$$

The bootstrap resistor together with the bootstrap capacitor introduces a time constant and should be sized appropriately to achieve the desired start-up time. For this calculation, it is assumed that the bootstrap capacitor is fully charged after 4 time constant. With this, R_{boot} can be calculated using the following formula:

$$R_{boot} \leq \frac{t_{min}}{4 \times C_{boot}} \quad (6)$$

Where:

t_{min} = minimum on time of the low-side mosfet (Q2)

7.2.4 External Bootstrap Diode Selection

For high dV/dT applications, an external bootstrap diode is recommended to be in parallel with the internal bootstrap diode. A fast recovery or schottky diode with low forward voltage drop is recommended in order to minimize the losses and leakage current. It should be chosen such that it can handle the peak transient current from Equation (5) during start-up conditions and the blocking voltage rating should be higher than the maximum input voltage (V_{in}) with enough derating.

7.3 PCB Layout Guidelines

In order to maximize the performance of DHPx050N10N5, below are some guidelines/recommendations on how to optimize the PCB layout. Actual layout in a 600W quarter brick FB-FB module will be shown as an example.

- Input ceramic bypass capacitors should be placed as close as possible to the VIN and PGND pins to bypass the high frequency noise.
- Decoupling capacitors on VDD and Boot capacitor should be placed as close as possible to the VDD-GNDA/GNDB and HB-HS pins and their traces should be wide and short as possible to minimize the parasitics.
- If possible, VIN and PGND pins should be directly connected to the board's VIN and PGND copper plane since these traces handle large current transients. Also, use of multiple vias with adequate size is recommended not just to interconnect to different layers but also to distribute heat conduction evenly.
- It is recommended to have external boot diode placement for high dV/dt application.
- It is recommended to have an option for a series boot resistor to control the high side mosfet slew rate and therefore the low side mosfet overshoot. The boot loop path including the VDD capacitor, boot diode, boot series resistor and boot capacitor should be as small as possible.
- Exposed PGND pads and pins (PGND, GNDA and GNDB) should be connected together by a copper plane and then it should connect to the board's GND copper plane via multiple vias. With the source down configuration of the low-side mosfet, usage of multiple vias under the die results in a much better heat dissipation into the PCB.
- If a snubber is needed, it should be placed close to the SW and PGND pins.
- Copper trace between SW pad and the transformer windings should be as short and wide as possible to minimize losses and noise emission as this trace carries high frequency content and has high dV/dt. This SW copper trace also serve as a heatsink for the low-side mosfet so a balance between cooling and noise emission should be considered.

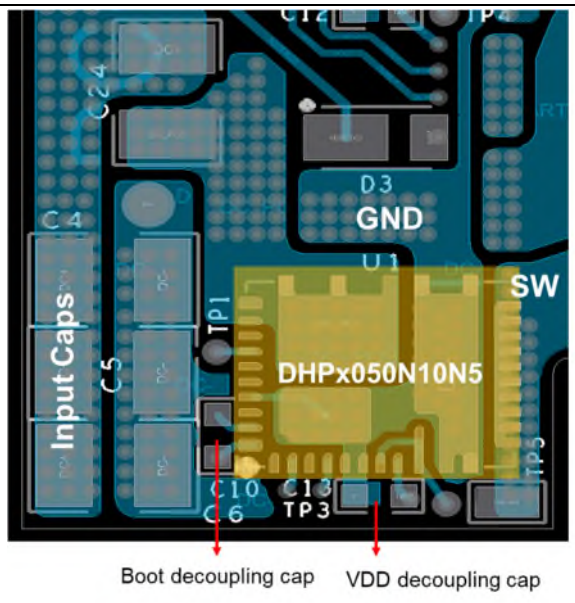


Figure 10 Example layout of DHPx050N10N5 in the primary side of a FB-FB ¼ brick board - Top Layer

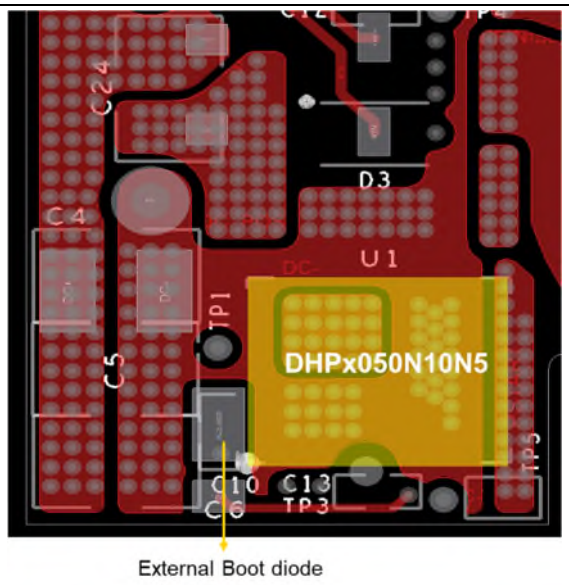


Figure 11 **Example layout of DHPx050N10N5 in the primary side of a FB-FB ¼ brick board – Bottom Layer**

8 Outline Dimensions

8.1 PG-IQFN-36-1 Package Outline, 1 of 2

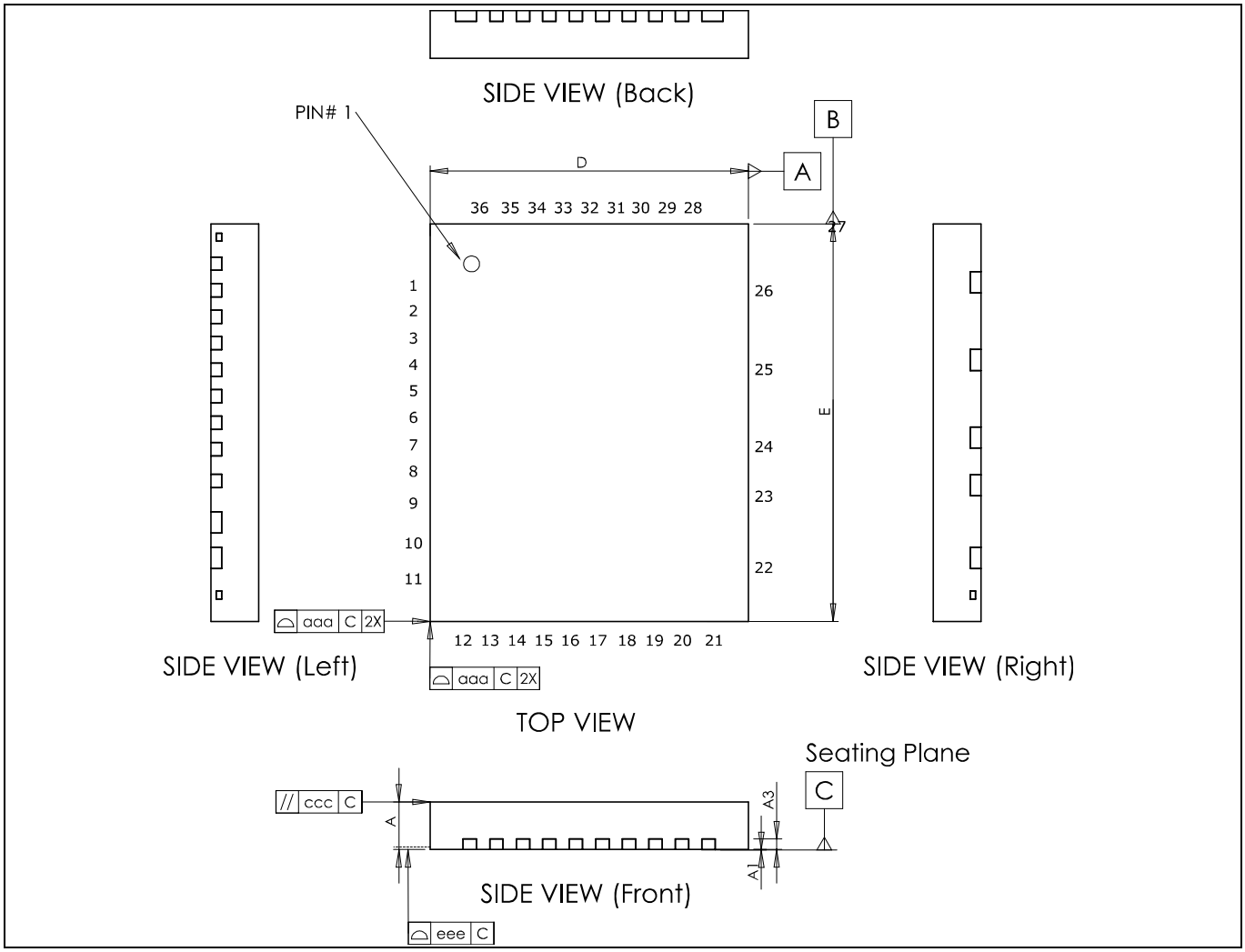
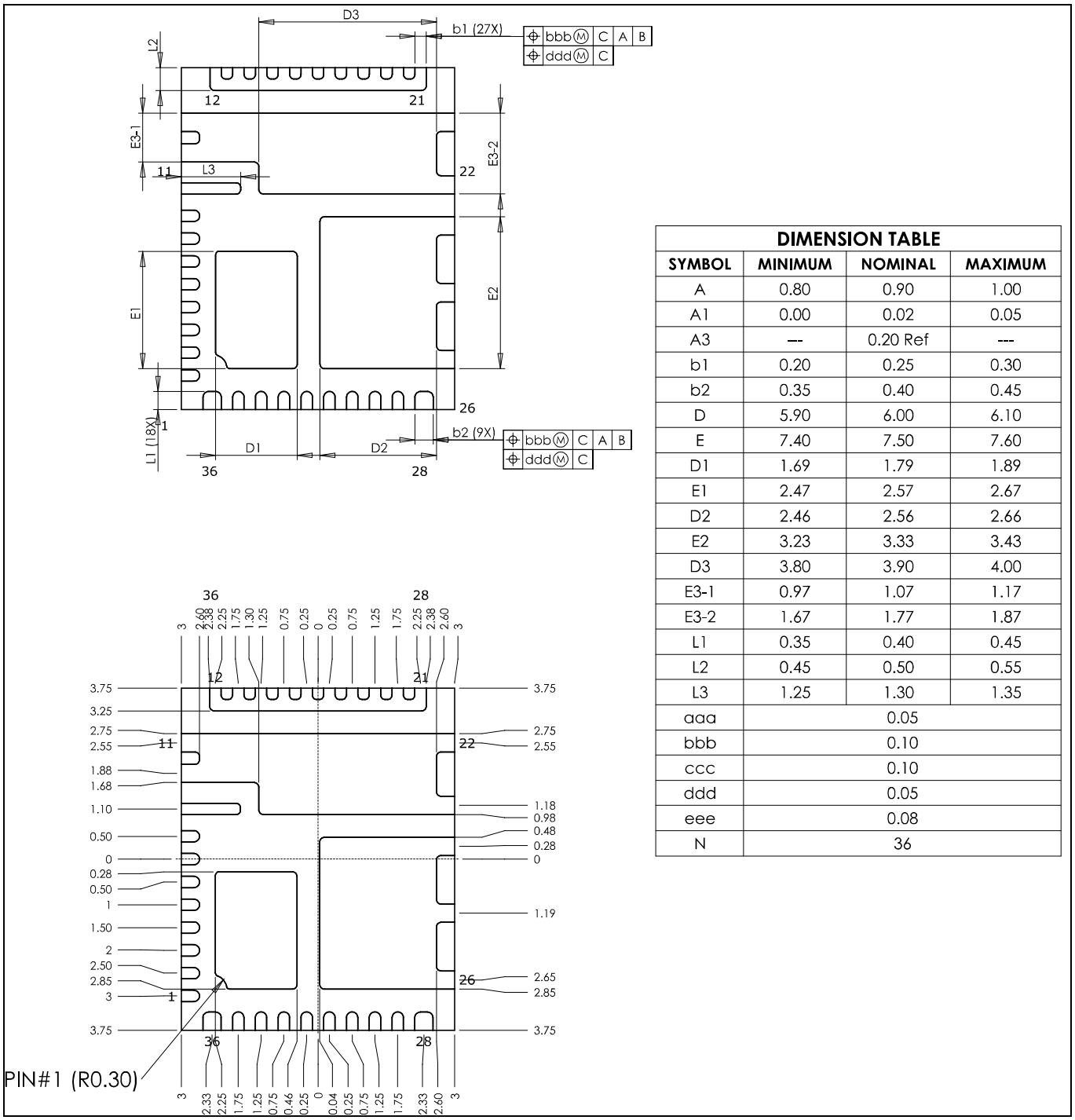


Figure 12 PG-IQFN-36-1 Outline Dimensions, 1 of 2

8.2 PG-IQFN-36-1 Package Outline, 2 of 2



DIMENSION TABLE			
SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.20 Ref	---
b1	0.20	0.25	0.30
b2	0.35	0.40	0.45
D	5.90	6.00	6.10
E	7.40	7.50	7.60
D1	1.69	1.79	1.89
E1	2.47	2.57	2.67
D2	2.46	2.56	2.66
E2	3.23	3.33	3.43
D3	3.80	3.90	4.00
E3-1	0.97	1.07	1.17
E3-2	1.67	1.77	1.87
L1	0.35	0.40	0.45
L2	0.45	0.50	0.55
L3	1.25	1.30	1.35
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	36		

Figure 13 PG-IQFN-36-1 Outline Dimensions, 2 of 2

8.3 PG-IQFN-36-1 Footprint Dimensions

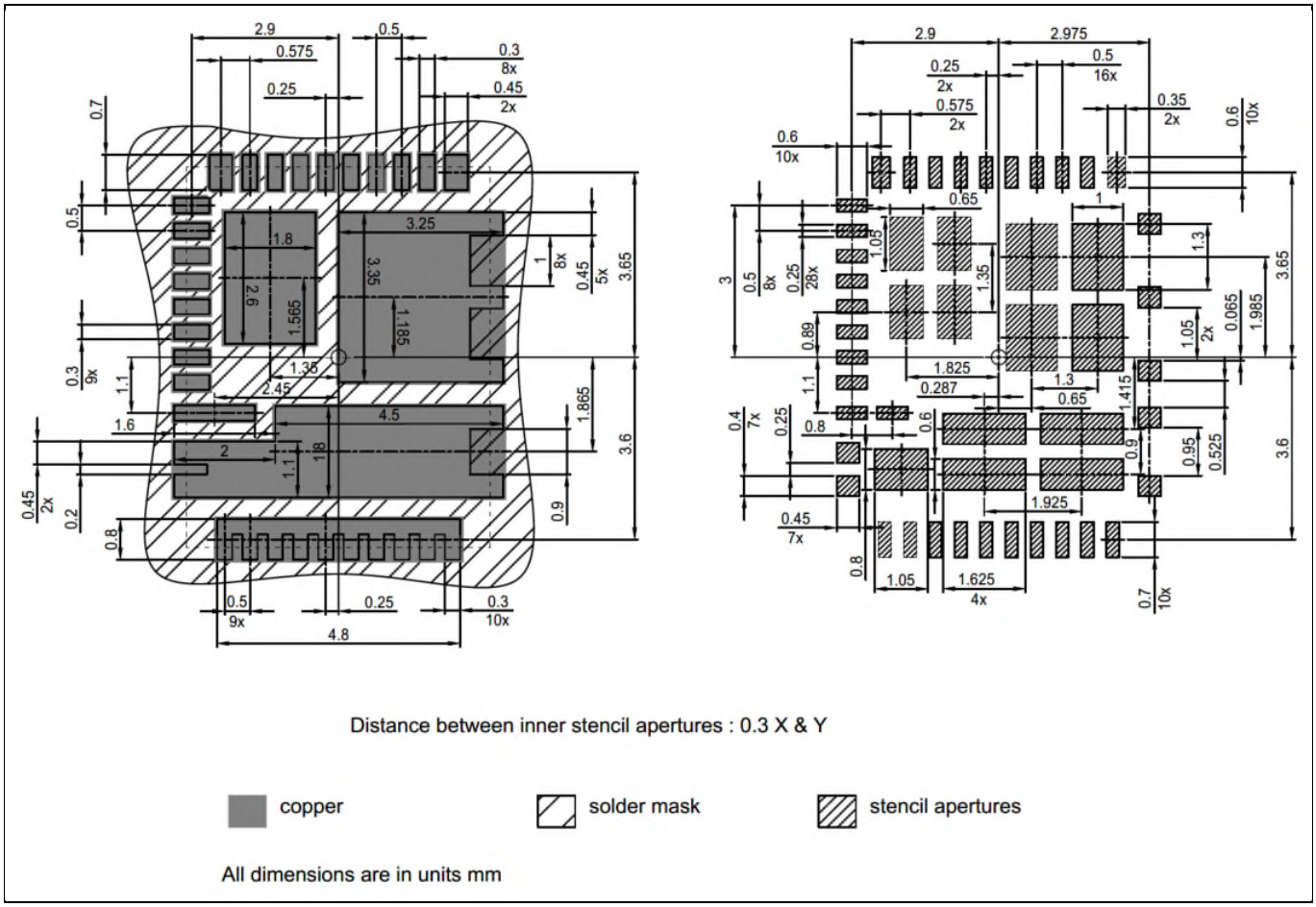
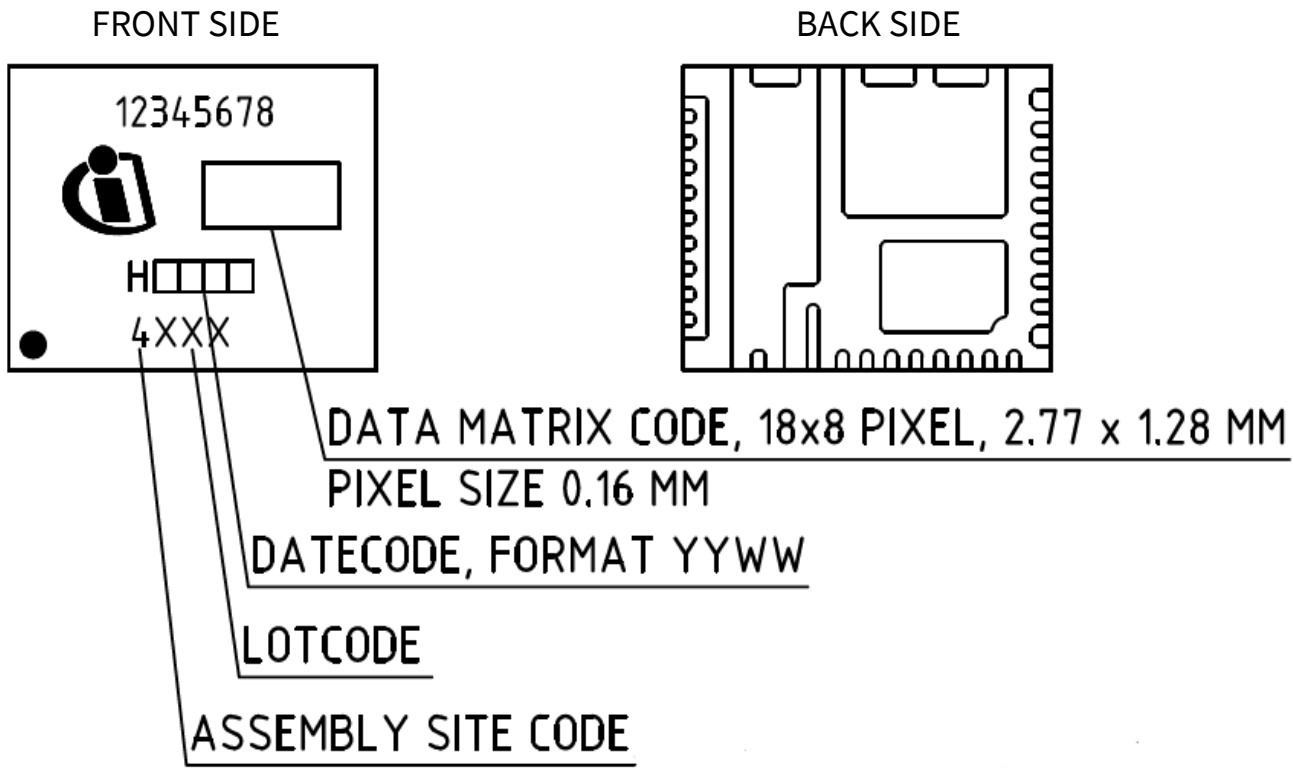


Figure 14 PG-IQFN-36-1 Footprint Dimensions

8.4 Top Marking



DHPx050N10N5

Marking Code	P = Pb Free; Y = Engineering Samples
Date Code	YWW format, where Y = least significant digit of the production year , WW = two digits representing the week of the production year

Revision history

Document version	Date of release	Description of changes
1.1	2020.03.12	Absolute maximum rating for V_{IN} and V_{HB} specified at Tc=25°C Removed DHPx070N10N5 parameters in the datasheet Added footnote for the rising/falling propagation delay
1.2	2020.07.30	Added ESD Ratings. Added Design and PCB layout Guidelines. Added footnote on V_{HS} and V_{HB} under Absolute Maximum Ratings. Added Transient Detector description under Functional Description.

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