THE DATASHEET OF

LPC1767FBD100K

LPC1769/68/67/66/65/64/63

32-bit Arm Cortex®-M3 microcontroller; up to 512 kB flash and 64 kB SRAM with Ethernet, USB 2.0 Host/Device/OTG, CAN

Rev. 9.10 — 8 September 2020 Product data sheet

1. General description

The LPC1769/68/67/66/65/64/63 are ARM Cortex-M3 based microcontrollers for embedded applications featuring a high level of integration and low power consumption. The Arm Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration.

The LPC1768/67/66/65/64/63 operate at CPU frequencies of up to 100 MHz. The LPC1769 operates at CPU frequencies of up to 120 MHz. The Arm Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The Arm Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

The peripheral complement of the LPC1769/68/67/66/65/64/63 includes up to 512 kB of flash memory, up to 64 kB of data memory, Ethernet MAC, USB Device/Host/OTG interface, 8-channel general purpose DMA controller, 4 UARTs, 2 CAN channels, 2 SSP controllers, SPI interface, 3 I^2C-bus interfaces, 2-input plus 2-output I^2S-bus interface, 8-channel 12-bit ADC, 10-bit DAC, motor control PWM, Quadrature Encoder interface, four general purpose timers, 6-output general purpose PWM, ultra-low power Real-Time Clock (RTC) with separate battery supply, and up to 70 general purpose I/O pins.

The LPC1769/68/67/66/65/64/63 are pin-compatible to the 100-pin LPC236x Arm7-based microcontroller series.

For additional documentation, see Section 19 “References”.

2. Features and benefits

- Arm Cortex-M3 processor, running at frequencies of up to 100 MHz (LPC1768/67/66/65/64/63) or of up to 120 MHz (LPC1769). A Memory Protection Unit (MPU) supporting eight regions is included.
- Arm Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
- Up to 512 kB on-chip flash programming memory. Enhanced flash memory accelerator enables high-speed 120 MHz operation with zero wait states.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- On-chip SRAM includes:
  - 32/16 kB of SRAM on the CPU with local code/data bus for high-performance CPU access.

- Two/one 16 kB SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for Ethernet, USB, and DMA memory, as well as for general purpose CPU instruction and data storage.

- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with SSP, I^2S-bus, UART, Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, and for memory-to-memory transfers.
- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, General Purpose DMA controller, Ethernet MAC, and the USB interface. This interconnect provides communication with no arbitration delays.
- Split APB bus allows high throughput with few stalls between the CPU and DMA.
- Serial interfaces:
  - Ethernet MAC with RMII interface and dedicated DMA controller. (Not available on all parts, see Table 2.)
  - USB 2.0 full-speed device/Host/OTG controller with dedicated DMA controller and on-chip PHY for device, Host, and OTG functions. (Not available on all parts, see Table 2.)
  - Four UARTs with fractional baud rate generation, internal FIFO, and DMA support. One UART has modem control I/O and RS-485/EIA-485 support, and one UART has IrDA support.
  - CAN 2.0B controller with two channels. (Not available on all parts, see Table 2.)
  - SPI controller with synchronous, serial, full duplex communication and programmable data length.
  - Two SSP controllers with FIFO and multi-protocol capabilities. The SSP interfaces can be used with the GPDMA controller.
  - Three enhanced I^2C bus interfaces, one with an open-drain output supporting full I^2C specification and Fast mode plus with data rates of 1 Mbit/s, two with standard port pins. Enhancements include multiple address recognition and monitor mode.
  - I^2S (Inter-IC Sound) interface for digital audio input or output, with fractional rate control. The I^2S-bus interface can be used with the GPDMA. The I^2S-bus interface supports 3-wire and 4-wire data transmit and receive as well as master clock input/output. (Not available on all parts, see Table 2.)
- Other peripherals:
  - 70 (100 pin package) General Purpose I/O (GPIO) pins with configurable pull-up/down resistors. All GPIOs support a new, configurable open-drain operating mode. The GPIO block is accessed through the AHB multilayer bus for fast access and located in memory such that it supports Cortex-M3 bit banding and use by the General Purpose DMA Controller.
  - 12-bit Analog-to-Digital Converter (ADC) with input multiplexing among eight pins, conversion rates up to 200 kHz, and multiple result registers. The 12-bit ADC can be used with the GPDMA controller.
  - 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support. (Not available on all parts, see Table 2)
  - Four general purpose timers/counters, with a total of eight capture inputs and ten compare outputs. Each timer block has an external count input. Specific timer events can be selected to generate DMA requests.
  - One motor control PWM with support for three-phase motor control.

- Quadrature encoder interface that can monitor one external quadrature encoder.
- One standard PWM/timer block with external count input.
- RTC with a separate power domain and dedicated RTC oscillator. The RTC block includes 20 bytes of battery-powered backup registers.
- WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- Arm Cortex-M3 system tick timer, including an external clock input option.
- Repetitive interrupt timer provides programmable and repeating timed interrupts.
- Each peripheral has its own clock divider for further power savings.

- Standard JTAG debug interface for compatibility with existing tools. Serial Wire Debug and Serial Wire Trace Port options. Boundary Scan Description Language (BSDL) is not available for this device.
- Emulation trace module enables non-intrusive, high-speed real-time tracing of instruction execution.
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.
- Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- Single 3.3 V power supply (2.4 V to 3.6 V).
- Four external interrupt inputs configurable as edge/level sensitive. All pins on Port 0 and Port 2 can be used as edge sensitive interrupt sources.
- Non-maskable Interrupt (NMI) input.
- Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, and the USB clock.
- The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in deep sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt, CAN bus activity, Port 0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- Power-On Reset (POR).
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- USB PLL for added flexibility.
- Code Read Protection (CRP) with different security levels.
- Unique device serial number for identification purposes.
- Available as LQFP100 (14 mm × 14 mm × 1.4 mm), TFBGA100[1] (9 mm × 9 mm × 0.7 mm), and WLCSP100 (5.07 × 5.07 × 0.53 mm) package.

1. LPC1768/65 only.

3. Applications

- eMetering
- Lighting
- Industrial networking
- Alarm systems
- White goods
- Motor control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1769FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1768FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1768FET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1768UK	WLCSP100	wafer level chip-scale package; 100 balls; 5.07 × 5.07 × 0.53 mm	-
LPC1767FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1766FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1765FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1765FET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC1764FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1763FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4.1 Ordering options

Table 2. Ordering options

Type number	Device order part number	Flash (kB)	SRAM in kB				Ethernet	USB	CAN	I^2S	DAC	GPIO	Maximum CPU operating frequency (MHz)
			CPU	AHB SRAM0	AHB SRAM1	Total							
LPC1769FBD100	LPC1769FBD100,551	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	120
LPC1768FBD100	LPC1768FBD100/CP32	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1768FET100	LPC1768FET100Z	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1768UK	LPC1768UKZ	512	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1767FBD100	LPC1767FBD100,551	512	32	16	16	64	yes	no	no	yes	yes	70	100
LPC1766FBD100	LPC1766FBD100,551	256	32	16	16	64	yes	Device/Host/OTG	2	yes	yes	70	100
LPC1765FBD100	LPC1765FBD100/3271	256	32	16	16	64	no	Device/Host/OTG	2	yes	yes	70	100
LPC1765FET100	LPC1765FET100,551	256	32	16	16	64	no	Device/Host/OTG	2	yes	yes	70	100
LPC1764FBD100	LPC1764FBD100,551	128	16	16	-	32	yes	Device only	2	no	no	70	100
LPC1763FBD100	LPC1763FBD100K	256	32	16	16	64	no	no	no	yes	yes	70	100

5. Marking

The LPC176x devices typically have the following top-side marking:

LPC176xxxx

xxxxxxx

xxYYWWR[x]

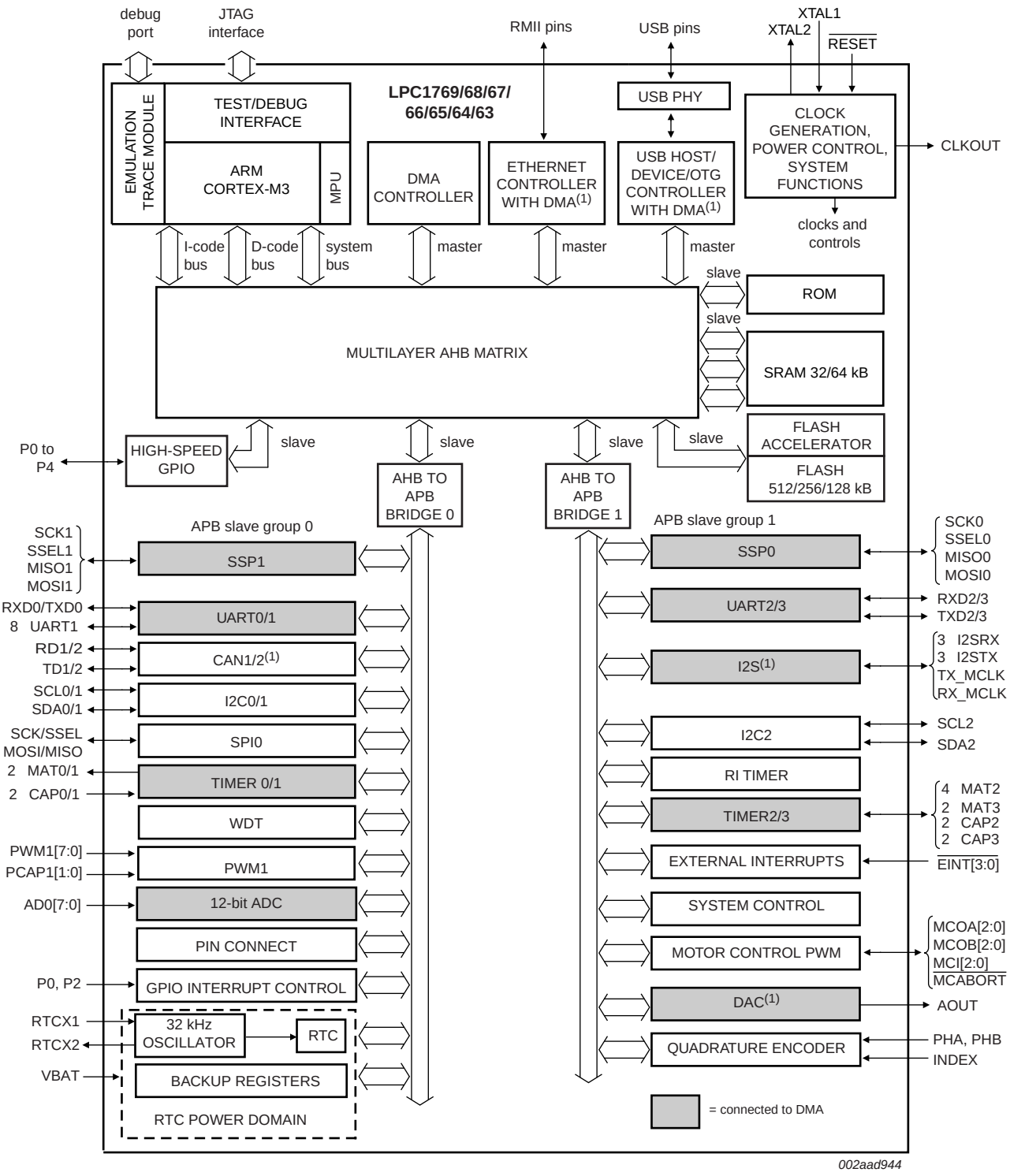
The last/second to last letter in the third line (field 'R') will identify the device revision. This data sheet covers the following revisions of the LPC176x:

Table 3. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision
'A'	Second device revision
'C'	Third device revision (LQFP100, TFBGA100 ONLY)

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

6. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. Block diagram

7. Pinning information

7.1 Pinning

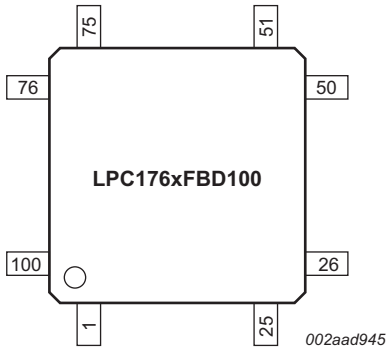


Fig 2. Pin configuration LQFP100 package

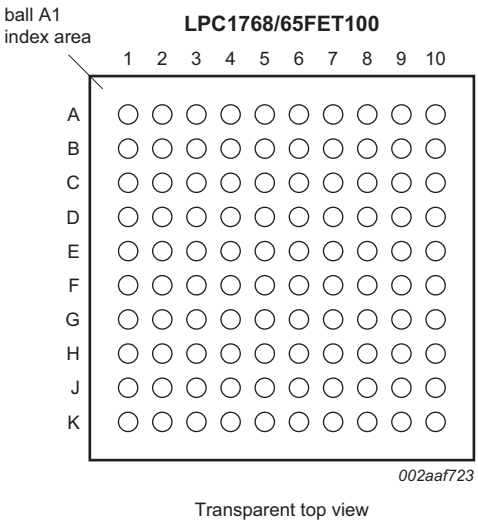


Fig 3. Pin configuration TFBGA100 package

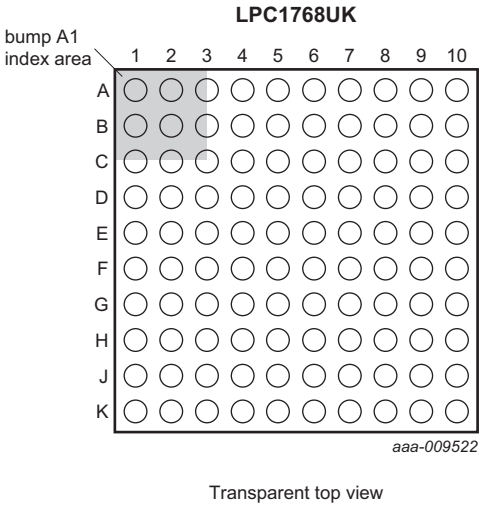


Fig 4. Pin configuration WLCSP100 package

Table 4. Pin allocation table TFBGA100

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	TDO/SWO	2	P0[3]/RXD0/AD0[6]	3	$V_{DD(3V3)}$	4	P1[4]/ENET_TX_EN
5	P1[10]/ENET_RXD1	6	P1[16]/ENET_MDC	7	$V_{DD(REG)(3V3)}$	8	P0[4]/I2SRX_CLK/ RD2/CAP2[0]
9	P0[7]/I2STX_CLK/ SCK1/MAT2[1]	10	P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	11	-	12	-
Row B							
1	TMS/SWDIO	2	RTCK	3	V_{SS}	4	P1[1]/ENET_TXD1
5	P1[9]/ENET_RXD0	6	P1[17]/ ENET_MDIO	7	V_{SS}	8	P0[6]/I2SRX_SDA/ SSEL1/MAT2[0]
9	P2[0]/PWM1[1]/TXD1	10	P2[1]/PWM1[2]/RXD1	11	-	12	-
Row C							
1	TCK/SWDCLK	2	$\overline{TRST}$	3	TDI	4	P0[2]/TXD0/AD0[7]
5	P1[8]/ENET_CRS	6	P1[15]/ ENET_REF_CLK	7	P4[28]/RX_MCLK/ MAT2[0]/TXD3	8	P0[8]/I2STX_WS/ MISO1/MAT2[2]
9	V_{SS}	10	$V_{DD(3V3)}$	11	-	12	-
Row D							
1	P0[24]/AD0[1]/ I2SRX_WS/CAP3[1]	2	P0[25]/AD0[2]/ I2SRX_SDA/TXD3	3	P0[26]/AD0[3]/ AOUT/RXD3	4	n.c.
5	P1[0]/ENET_TXD0	6	P1[14]/ENET_RX_ER	7	P0[5]/I2SRX_WS/ TD2/CAP2[1]	8	P2[2]/PWM1[3]/ CTS1/TRACEDATA[3]
9	P2[4]/PWM1[5]/ DSR1/TRACEDATA[1]	10	P2[5]/PWM1[6]/ DTR1/TRACEDATA[0]	11	-	12	-
Row E							
1	V_{SSA}	2	V_{DDA}	3	VREFP	4	n.c.
5	P0[23]/AD0[0]/ I2SRX_CLK/CAP3[0]	6	P4[29]/TX_MCLK/ MAT2[1]/RXD3	7	P2[3]/PWM1[4]/ DCD1/TRACEDATA[2]	8	P2[6]/PCAP1[0]/ RI1/TRACECLK

Table 4. Pin allocation table TFBGA100 *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
9	P2[7]/RD2/RTS1	10	P2[8]/TD2/TXD2	11	-	12	-
Row F							
1	VREFN	2	RTCX1	3	$\overline{\text{RESET}}$	4	P1[31]/SCK1/ AD0[5]
5	P1[21]/$\overline{\text{MCABORT}}$/ PWM1[3]/SSEL0	6	P0[18]/DCD1/ MOSI0/MOSI	7	P2[9]/USB_CONNECT/ RXD2	8	P0[16]/RXD1/ SSEL0/SSEL
9	P0[17]/CTS1/ MISO0/MISO	10	P0[15]/TXD1/ SCK0/SCK	11	-	12	-
Row G							
1	RTCX2	2	VBAT	3	XTAL2	4	P0[30]/USB_D−
5	P1[25]/MCOA1/ MAT1[1]	6	P1[29]/MCOB2/ PCAP1[1]/MAT0[1]	7	V_{SS}	8	P0[21]/RI1/RD1
9	P0[20]/DTR1/SCL1	10	P0[19]/DSR1/SDA1	11	-	12	-
Row H							
1	P1[30]/V_{BUS}/ AD0[4]	2	XTAL1	3	P3[25]/MAT0[0]/ PWM1[2]	4	P1[18]/USB_UP_LED/ PWM1[1]/CAP1[0]
5	P1[24]/MCI2/ PWM1[5]/MOSI0	6	$V_{DD(REG)(3V3)}$	7	P0[10]/TXD2/ SDA2/MAT3[0]	8	P2[11]/$\overline{\text{EINT1}}$/ I2STX_CLK
9	$V_{DD(3V3)}$	10	P0[22]/RTS1/TD1	11	-	12	-

Table 4. Pin allocation table TFBGA100 *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row J							
1	P0[28]/SCL0/ USB_SCL	2	P0[27]/SDA0/ USB_SDA	3	P0[29]/USB_D+	4	P1[19]/MCOA0/ USB_PPWR/ CAP1[1]
5	P1[22]/MCOB0/ USB_PWRD/ MAT1[0]	6	V_{SS}	7	P1[28]/MCOA2/ PCAP1[0]/ MAT0[0]	8	P0[1]/TD1/RXD3/SCL1
9	P2[13]/EINT3/ I2STX_SDA	10	P2[10]/EINT0/NMI	11	-	12	-
Row K							
1	P3[26]/STCLK/ MAT0[1]/PWM1[3]	2	$V_{DD(3V3)}$	3	V_{SS}	4	P1[20]/MCI0/ PWM1[2]/SCK0
5	P1[23]/MCI1/ PWM1[4]/MISO0	6	P1[26]/MCOB1/ PWM1[6]/CAP0[0]	7	P1[27]/CLKOUT /USB_OVRCR/ CAP0[1]	8	P0[0]/RD1/TXD3/SDA1
9	P0[11]/RXD2/ SCL2/MAT3[1]	10	P2[12]/EINT2/ I2STX_WS	11	-	12	-

7.2 Pin description

Table 5. Pin description

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[0] to P0[31]					I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins 12, 13, 14, and 31 of this port are not available.
P0[0]/RD1/TXD3/ SDA1	46	K8	H10	[1]	I/O	**P0[0] —** General purpose digital input/output pin.
					I	**RD1 —** CAN1 receiver input. (LPC1769/68/66/65/64 only).
					O	**TXD3 —** Transmitter output for UART3.
					I/O	**SDA1 —** I^2C1 data input/output. (This is not an I^2C-bus compliant open-drain pin).
P0[1]/TD1/RXD3/ SCL1	47	J8	H9	[1]	I/O	**P0[1] —** General purpose digital input/output pin.
					O	**TD1 —** CAN1 transmitter output. (LPC1769/68/66/65/64 only).
					I	**RXD3 —** Receiver input for UART3.
					I/O	**SCL1 —** I^2C1 clock input/output. (This is not an I^2C-bus compliant open-drain pin).
P0[2]/TXD0/AD0[7]	98	C4	B1	[2]	I/O	**P0[2] —** General purpose digital input/output pin.
					O	**TXD0 —** Transmitter output for UART0.
					I	**AD0[7] —** A/D converter 0, input 7.
P0[3]/RXD0/AD0[6]	99	A2	C3	[2]	I/O	**P0[3] —** General purpose digital input/output pin.
					I	**RXD0 —** Receiver input for UART0.
					I	**AD0[6] —** A/D converter 0, input 6.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[4]/ I2SRX_CLK/ RD2/CAP2[0]	81	A8	G2	[1]	I/O	**P0[4] —** General purpose digital input/output pin.
					I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**RD2 —** CAN2 receiver input. (LPC1769/68/66/65/64 only).
					I	**CAP2[0] —** Capture input for Timer 2, channel 0.
P0[5]/ I2SRX_WS/ TD2/CAP2[1]	80	D7	H1	[1]	I/O	**P0[5] —** General purpose digital input/output pin.
					I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					O	**TD2 —** CAN2 transmitter output. (LPC1769/68/66/65/64 only).
					I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/ I2SRX_SDA/ SSEL1/MAT2[0]	79	B8	G3	[1]	I/O	**P0[6] —** General purpose digital input/output pin.
					I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**SSEL1 —** Slave Select for SSP1.
					O	**MAT2[0] —** Match output for Timer 2, channel 0.
P0[7]/ I2STX_CLK/ SCK1/MAT2[1]	78	A9	J1	[1]	I/O	**P0[7] —** General purpose digital input/output pin.
					I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**SCK1 —** Serial Clock for SSP1.
					O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/ I2STX_WS/ MISO1/MAT2[2]	77	C8	H2	[1]	I/O	**P0[8] —** General purpose digital input/output pin.
					I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**MISO1 —** Master In Slave Out for SSP1.
					O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/ I2STX_SDA/ MOSI1/MAT2[3]	76	A10	H3	[1]	I/O	**P0[9] —** General purpose digital input/output pin.
					I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I/O	**MOSI1 —** Master Out Slave In for SSP1.
					O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	48	H7	H8	[1]	I/O	**P0[10] —** General purpose digital input/output pin.
					O	**TXD2 —** Transmitter output for UART2.
					I/O	**SDA2 —** I²C2 data input/output (this is not an open-drain pin).
					O	**MAT3[0] —** Match output for Timer 3, channel 0.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[11]/RXD2/ SCL2/MAT3[1]	49	K9	J10	[1]	I/O	**P0[11] —** General purpose digital input/output pin.
					I	**RXD2 —** Receiver input for UART2.
					I/O	**SCL2 —** I^2C2 clock input/output (this is not an open-drain pin).
					O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[15]/TXD1/ SCK0/SCK	62	F10	H6	[1]	I/O	**P0[15] —** General purpose digital input/output pin.
					O	**TXD1 —** Transmitter output for UART1.
					I/O	**SCK0 —** Serial clock for SSP0.
					I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	63	F8	J5	[1]	I/O	**P0[16] —** General purpose digital input/output pin.
					I	**RXD1 —** Receiver input for UART1.
					I/O	**SSEL0 —** Slave Select for SSP0.
					I/O	**SSEL —** Slave Select for SPI.
P0[17]/CTS1/ MISO0/MISO	61	F9	K6	[1]	I/O	**P0[17] —** General purpose digital input/output pin.
					I	**CTS1 —** Clear to Send input for UART1.
					I/O	**MISO0 —** Master In Slave Out for SSP0.
					I/O	**MISO —** Master In Slave Out for SPI.
P0[18]/DCD1/ MOSI0/MOSI	60	F6	J6	[1]	I/O	**P0[18] —** General purpose digital input/output pin.
					I	**DCD1 —** Data Carrier Detect input for UART1.
					I/O	**MOSI0 —** Master Out Slave In for SSP0.
					I/O	**MOSI —** Master Out Slave In for SPI.
P0[19]/DSR1/ SDA1	59	G10	K7	[1]	I/O	**P0[19] —** General purpose digital input/output pin.
					I	**DSR1 —** Data Set Ready input for UART1.
					I/O	**SDA1 —** I^2C1 data input/output (this is not an I^2C-bus compliant open-drain pin).
P0[20]/DTR1/SCL1	58	G9	J7	[1]	I/O	**P0[20] —** General purpose digital input/output pin.
					O	**DTR1 —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
					I/O	**SCL1 —** I^2C1 clock input/output (this is not an I^2C-bus compliant open-drain pin).
P0[21]/RI1/RD1	57	G8	H7	[1]	I/O	**P0[21] —** General purpose digital input/output pin.
					I	**RI1 —** Ring Indicator input for UART1.
					I	**RD1 —** CAN1 receiver input. (LPC1769/68/66/65/64 only).
P0[22]/RTS1/TD1	56	H10	K8	[1]	I/O	**P0[22] —** General purpose digital input/output pin.
					O	**RTS1 —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
					O	**TD1 —** CAN1 transmitter output. (LPC1769/68/66/65/64 only).

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P0[23]/AD0[0]/ I2SRX_CLK/ CAP3[0]	9	E5	D5	[2]	I/O	**P0[23] —** General purpose digital input/output pin.
					I	**AD0[0] —** A/D converter 0, input 0.
					I/O	**I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**CAP3[0] —** Capture input for Timer 3, channel 0.
P0[24]/AD0[1]/ I2SRX_WS/ CAP3[1]	8	D1	B4	[2]	I/O	**P0[24] —** General purpose digital input/output pin.
					I	**AD0[1] —** A/D converter 0, input 1.
					I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					I	**CAP3[1] —** Capture input for Timer 3, channel 1.
P0[25]/AD0[2]/ I2SRX_SDA/ TXD3	7	D2	A3	[2]	I/O	**P0[25] —** General purpose digital input/output pin.
					I	**AD0[2] —** A/D converter 0, input 2.
					I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. (LPC1769/68/67/66/65/63 only).
					O	**TXD3 —** Transmitter output for UART3.
P0[26]/AD0[3]/ AOUT/RXD3	6	D3	C5	[3]	I/O	**P0[26] —** General purpose digital input/output pin.
					I	**AD0[3] —** A/D converter 0, input 3.
					O	**AOUT —** DAC output (LPC1769/68/67/66/65/63 only).
					I	**RXD3 —** Receiver input for UART3.
P0[27]/SDA0/ USB_SDA	25	J2	C8	[4]	I/O	**P0[27] —** General purpose digital input/output pin. Output is open-drain.
					I/O	**SDA0 —** I²C0 data input/output. Open-drain output (for I²C-bus compliance).
					I/O	**USB_SDA —** USB port I²C serial data (OTG transceiver, LPC1769/68/66/65 only).
P0[28]/SCL0/ USB_SCL	24	J1	B9	[4]	I/O	**P0[28] —** General purpose digital input/output pin. Output is open-drain.
					I/O	**SCL0 —** I²C0 clock input/output. Open-drain output (for I²C-bus compliance).
					I/O	**USB_SCL —** USB port I²C serial clock (OTG transceiver, LPC1769/68/66/65 only).
P0[29]/USB_D+	29	J3	B10	[5]	I/O	**P0[29] —** General purpose digital input/output pin.
					I/O	**USB_D+ —** USB bidirectional D+ line. (LPC1769/68/66/65/64 only).
P0[30]/USB_D−	30	G4	C9	[5]	I/O	**P0[30] —** General purpose digital input/output pin.
					I/O	**USB_D− —** USB bidirectional D− line. (LPC1769/68/66/65/64 only).

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P1[0] to P1[31]					I/O	**Port 1:** Port 1 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 2, 3, 5, 6, 7, 11, 12, and 13 of this port are not available.
P1[0]/ ENET_TXD0	95	D5	C1	[1]	I/O	**P1[0] —** General purpose digital input/output pin.
					O	**ENET_TXD0 —** Ethernet transmit data 0. (LPC1769/68/67/66/64 only).
P1[1]/ ENET_TXD1	94	B4	C2	[1]	I/O	**P1[1] —** General purpose digital input/output pin.
					O	**ENET_TXD1 —** Ethernet transmit data 1. (LPC1769/68/67/66/64 only).
P1[4]/ ENET_TX_EN	93	A4	D2	[1]	I/O	**P1[4] —** General purpose digital input/output pin.
					O	**ENET_TX_EN —** Ethernet transmit data enable. (LPC1769/68/67/66/64 only).
P1[8]/ ENET_CRS	92	C5	D1	[1]	I/O	**P1[8] —** General purpose digital input/output pin.
					I	**ENET_CRS —** Ethernet carrier sense. (LPC1769/68/67/66/64 only).
P1[9]/ ENET_RXD0	91	B5	D3	[1]	I/O	**P1[9] —** General purpose digital input/output pin.
					I	**ENET_RXD0 —** Ethernet receive data. (LPC1769/68/67/66/64 only).
P1[10]/ ENET_RXD1	90	A5	E3	[1]	I/O	**P1[10] —** General purpose digital input/output pin.
					I	**ENET_RXD1 —** Ethernet receive data. (LPC1769/68/67/66/64 only).
P1[14]/ ENET_RX_ER	89	D6	E2	[1]	I/O	**P1[14] —** General purpose digital input/output pin.
					I	**ENET_RX_ER —** Ethernet receive error. (LPC1769/68/67/66/64 only).
P1[15]/ ENET_REF_CLK	88	C6	E1	[1]	I/O	**P1[15] —** General purpose digital input/output pin.
					I	**ENET_REF_CLK —** Ethernet reference clock. (LPC1769/68/67/66/64 only).
P1[16]/ ENET_MDC	87	A6	F3	[1]	I/O	**P1[16] —** General purpose digital input/output pin.
					O	**ENET_MDC —** Ethernet MIIM clock (LPC1769/68/67/66/64 only).
P1[17]/ ENET_MDIO	86	B6	F2	[1]	I/O	**P1[17] —** General purpose digital input/output pin.
					I/O	**ENET_MDIO —** Ethernet MIIM data input and output. (LPC1769/68/67/66/64 only).

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P1[18]/ USB_UP_LED/ PWM1[1]/ CAP1[0]	32	H4	D9	[1]	I/O	**P1[18] —** General purpose digital input/output pin.
					O	**USB_UP_LED —** USB GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus. (LPC1769/68/66/65/64 only).
					O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
					I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P1[19]/MCOA0/ $\overline{\text{USB\_PPWR}}$/ CAP1[1]	33	J4	C10	[1]	I/O	**P1[19] —** General purpose digital input/output pin.
					O	**MCOA0 —** Motor control PWM channel 0, output A.
					O	**$\overline{\text{USB\_PPWR}}$ —** Port Power enable signal for USB port. (LPC1769/68/66/65 only).
					I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P1[20]/MCI0/ PWM1[2]/SCK0	34	K4	E8	[1]	I/O	**P1[20] —** General purpose digital input/output pin.
					I	**MCI0 —** Motor control PWM channel 0, input. Also Quadrature Encoder Interface PHA input.
					O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
					I/O	**SCK0 —** Serial clock for SSP0.
P1[21]/$\overline{\text{MCABORT}}$/ PWM1[3]/ SSEL0	35	F5	E9	[1]	I/O	**P1[21] —** General purpose digital input/output pin.
					O	**$\overline{\text{MCABORT}}$ —** Motor control PWM, LOW-active fast abort.
					O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
					I/O	**SSEL0 —** Slave Select for SSP0.
P1[22]/MCOB0/ USB_PWRD/ MAT1[0]	36	J5	D10	[1]	I/O	**P1[22] —** General purpose digital input/output pin.
					O	**MCOB0 —** Motor control PWM channel 0, output B.
					I	**USB_PWRD —** Power Status for USB port (host power switch, LPC1769/68/66/65 only).
					O	**MAT1[0] —** Match output for Timer 1, channel 0.
P1[23]/MCI1/ PWM1[4]/MISO0	37	K5	E7	[1]	I/O	**P1[23] —** General purpose digital input/output pin.
					I	**MCI1 —** Motor control PWM channel 1, input. Also Quadrature Encoder Interface PHB input.
					O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
					I/O	**MISO0 —** Master In Slave Out for SSP0.
P1[24]/MCI2/ PWM1[5]/MOSI0	38	H5	F8	[1]	I/O	**P1[24] —** General purpose digital input/output pin.
					I	**MCI2 —** Motor control PWM channel 2, input. Also Quadrature Encoder Interface INDEX input.
					O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
					I/O	**MOSI0 —** Master Out Slave in for SSP0.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P1[25]/MCOA1/ MAT1[1]	39	G5	F9	[1]	I/O	**P1[25] —** General purpose digital input/output pin.
					O	**MCOA1 —** Motor control PWM channel 1, output A.
					O	**MAT1[1] —** Match output for Timer 1, channel 1.
P1[26]/MCOB1/ PWM1[6]/CAP0[0]	40	K6	E10	[1]	I/O	**P1[26] —** General purpose digital input/output pin.
					O	**MCOB1 —** Motor control PWM channel 1, output B.
					O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
					I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/CLKOUT /$\overline{\text{USB\_OVRCR}}$/ CAP0[1]	43	K7	G9	[1]	I/O	**P1[27] —** General purpose digital input/output pin.
					O	**CLKOUT —** Clock output pin.
					I	**$\overline{\text{USB\_OVRCR}}$ —** USB port Over-Current status. (LPC1769/68/66/65 only).
					I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/MCOA2/ PCAP1[0]/ MAT0[0]	44	J7	G10	[1]	I/O	**P1[28] —** General purpose digital input/output pin.
					O	**MCOA2 —** Motor control PWM channel 2, output A.
					I	**PCAP1[0] —** Capture input for PWM1, channel 0.
					O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/MCOB2/ PCAP1[1]/ MAT0[1]	45	G6	G8	[1]	I/O	**P1[29] —** General purpose digital input/output pin.
					O	**MCOB2 —** Motor control PWM channel 2, output B.
					I	**PCAP1[1] —** Capture input for PWM1, channel 1.
					O	**MAT0[1] —** Match output for Timer 0, channel 1.
P1[30]/V_{BUS}/ AD0[4]	21	H1	B8	[2]	I/O	**P1[30] —** General purpose digital input/output pin.
					I	**V_{BUS} —** Monitors the presence of USB bus power. (LPC1769/68/66/65/64 only). **Note:** This signal must be HIGH for USB reset to occur.
					I	**AD0[4] —** A/D converter 0, input 4.
P1[31]/SCK1/ AD0[5]	20	F4	C7	[2]	I/O	**P1[31] —** General purpose digital input/output pin.
					I/O	**SCK1 —** Serial Clock for SSP1.
					I	**AD0[5] —** A/D converter 0, input 5.
P2[0] to P2[31]					I/O	**Port 2:** Port 2 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the pin connect block. Pins 14 through 31 of this port are not available.
P2[0]/PWM1[1]/ TXD1	75	B9	K1	[1]	I/O	**P2[0] —** General purpose digital input/output pin.
					O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
					O	**TXD1 —** Transmitter output for UART1.
P2[1]/PWM1[2]/ RXD1	74	B10	J2	[1]	I/O	**P2[1] —** General purpose digital input/output pin.
					O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
					I	**RXD1 —** Receiver input for UART1.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P2[2]/PWM1[3]/ CTS1/ TRACEDATA[3]	73	D8	K2	[1]	I/O	**P2[2] —** General purpose digital input/output pin.
					O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
					I	**CTS1 —** Clear to Send input for UART1.
					O	**TRACEDATA[3] —** Trace data, bit 3.
P2[3]/PWM1[4]/ DCD1/ TRACEDATA[2]	70	E7	K3	[1]	I/O	**P2[3] —** General purpose digital input/output pin.
					O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
					I	**DCD1 —** Data Carrier Detect input for UART1.
					O	**TRACEDATA[2] —** Trace data, bit 2.
P2[4]/PWM1[5]/ DSR1/ TRACEDATA[1]	69	D9	J3	[1]	I/O	**P2[4] —** General purpose digital input/output pin.
					O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
					I	**DSR1 —** Data Set Ready input for UART1.
					O	**TRACEDATA[1] —** Trace data, bit 1.
P2[5]/PWM1[6]/ DTR1/ TRACEDATA[0]	68	D10	H4	[1]	I/O	**P2[5] —** General purpose digital input/output pin.
					O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
					O	**DTR1 —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
					O	**TRACEDATA[0] —** Trace data, bit 0.
P2[6]/PCAP1[0]/ RI1/TRACECLK	67	E8	K4	[1]	I/O	**P2[6] —** General purpose digital input/output pin.
					I	**PCAP1[0] —** Capture input for PWM1, channel 0.
					I	**RI1 —** Ring Indicator input for UART1.
					O	**TRACECLK —** Trace Clock.
P2[7]/RD2/ RTS1	66	E9	J4	[1]	I/O	**P2[7] —** General purpose digital input/output pin.
					I	**RD2 —** CAN2 receiver input. (LPC1769/68/66/65/64 only).
					O	**RTS1 —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal.
P2[8]/TD2/ TXD2	65	E10	H5	[1]	I/O	**P2[8] —** General purpose digital input/output pin.
					O	**TD2 —** CAN2 transmitter output. (LPC1769/68/66/65/64 only).
					O	**TXD2 —** Transmitter output for UART2.
P2[9]/ USB_CONNECT/ RXD2	64	F7	K5	[1]	I/O	**P2[9] —** General purpose digital input/output pin.
					O	**USB_CONNECT —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature. (LPC1769/68/66/65/64 only).
					I	**RXD2 —** Receiver input for UART2.
P2[10]/$\overline{\text{EINT0}}$/NMI	53	J10	K9	[6]	I/O	**P2[10] —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
					I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
					I	**NMI —** Non-maskable interrupt input.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
P2[11]/$\overline{\text{EINT1}}$/ I2STX_CLK	52	H8	J8	[6]	I/O	**P2[11] —** General purpose digital input/output pin.
					I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
					I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
P2[12]/$\overline{\text{EINT2}}$/ I2STX_WS	51	K10	K10	[6]	I/O	**P2[12] —** General purpose digital input/output pin.
					I	**$\overline{\text{EINT2}}$ —** External interrupt 2 input.
					I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
P2[13]/$\overline{\text{EINT3}}$/ I2STX_SDA	50	J9	J9	[6]	I/O	**P2[13] —** General purpose digital input/output pin.
					I	**$\overline{\text{EINT3}}$ —** External interrupt 3 input.
					I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*. (LPC1769/68/67/66/65/63 only).
P3[0] to P3[31]					I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available.
P3[25]/MAT0[0]/ PWM1[2]	27	H3	D8	[1]	I/O	**P3[25] —** General purpose digital input/output pin.
					O	**MAT0[0] —** Match output for Timer 0, channel 0.
					O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
P3[26]/STCLK/ MAT0[1]/PWM1[3]	26	K1	A10	[1]	I/O	**P3[26] —** General purpose digital input/output pin.
					I	**STCLK —** System tick timer clock input. The maximum STCLK frequency is 1/4 of the Arm processor clock frequency CCLK.
					O	**MAT0[1] —** Match output for Timer 0, channel 1.
					O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
P4[0] to P4[31]					I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available.
P4[28]/RX_MCLK/ MAT2[0]/TXD3	82	C7	G1	[1]	I/O	**P4[28] —** General purpose digital input/output pin.
					O	**RX_MCLK —** I^2S receive master clock. (LPC1769/68/67/66/65 only).
					O	**MAT2[0] —** Match output for Timer 2, channel 0.
					O	**TXD3 —** Transmitter output for UART3.
P4[29]/TX_MCLK/ MAT2[1]/RXD3	85	E6	F1	[1]	I/O	**P4[29] —** General purpose digital input/output pin.
					O	**TX_MCLK —** I^2S transmit master clock. (LPC1769/68/67/66/65 only).
					O	**MAT2[1] —** Match output for Timer 2, channel 1.
					I	**RXD3 —** Receiver input for UART3.

Table 5. Pin description *...continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
TDO/SWO	1	A1	A1	[7]	O	**TDO —** Test Data out for JTAG interface.
					O	**SWO —** Serial wire trace output.
TDI	2	C3	C4	[1][8]	I	**TDI —** Test Data in for JTAG interface.
TMS/SWDIO	3	B1	B3	[1][8]	I	**TMS —** Test Mode Select for JTAG interface.
					I/O	**SWDIO —** Serial wire debug data input/output.
$\overline{\text{TRST}}$	4	C2	A2	[1][8]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
TCK/SWDCLK	5	C1	D4	[7]	I	**TCK —** Test Clock for JTAG interface.
					I	**SWDCLK —** Serial wire clock.
RTCK	100	B2	B2	[7]	O	**RTCK —** JTAG interface control signal.
$\overline{\text{RSTOUT}}$	14	-	-	-	O	**$\overline{\text{RSTOUT}}$ —** This is a 3.3 V pin. LOW on this pin indicates the microcontroller being in Reset state.
$\overline{\text{RESET}}$	17	F3	C6	[9]	I	**External reset input:** A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	22	H2	D7	[10][11]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	23	G3	A9	[10][11]	O	Output from the oscillator amplifier.
RTCX1	16	F2	A7	[10][11]	I	Input to the RTC oscillator circuit.
RTCX2	18	G1	B7	[10]	O	Output from the RTC oscillator circuit.
V_{SS}	31, 41, 55, 72, 83, 97	B3, B7, C9, G7, J6, K3	E5, F5, F6, G5, G6, G7	[10]	I	**ground:** 0 V reference.
V_{SSA}	11	E1	B5	[10]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	28, 54, 71, 96	K2, H9, C10, A3	E4, E6, F7, G4	[10]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(REG)(3V3)}$	42, 84	H6, A7	F4, F10	[10]	I	**3.3 V voltage regulator supply voltage:** This is the supply voltage for the on-chip voltage regulator only.
V_{DDA}	10	E2	A4	[10]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.
VREFP	12	E3	A5	[10]	I	**ADC positive reference voltage:** This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC. This pin should be tied to 3.3 V if the ADC and DAC are not used.

Table 5. Pin description *…continued*

Symbol	Pin/ball				Type	Description
	LQFP100	TFBGA100	WLCSP100			
VREFN	15	F1	A6		I	**ADC negative reference voltage:** This should be nominally the same voltage as V_{SS} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC.
VBAT	19	G2	A8	[10][12]	I	**RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral.
n.c.	13	D4, E4	B6, D6		-	not connected.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[4] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V.

[7] 5 V tolerant pad with TTL levels and hysteresis. Internal pull-up and pull-down resistors disabled.

[8] 5 V tolerant pad with TTL levels and hysteresis and internal pull-up resistor.

[9] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[10] Pad provides special analog functionality. A 32 kHz crystal oscillator must be used with the RTC.

[11] When the system oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

[12] When the RTC is not used, connect VBAT to $V_{DD(REG)(3V3)}$ and leave RTCX1 floating.

8. Functional description

8.1 Architectural overview

Remark: In the following, the notation LPC17xx refers to all parts: LPC1769/68/67/66/65/64/63.

The Arm Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus (see Figure 1). The I-code and D-code core buses are faster than the system bus and are used similarly to TCM interfaces: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

The LPC17xx use a multi-layer AHB matrix to connect the Arm Cortex-M3 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

8.2 Arm Cortex-M3 processor

The Arm Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The Arm Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware divide, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The Arm Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual* that can be found on official Arm website.

8.3 On-chip flash program memory

The LPC17xx contain up to 512 kB of on-chip flash memory. A new two-port flash accelerator maximizes performance for use with the two fast AHB-Lite buses.

8.4 On-chip SRAM

The LPC17xx contain a total of 64 kB on-chip static RAM memory. This includes the main 32 kB SRAM, accessible by the CPU and DMA controller on a higher-speed bus, and two additional 16 kB each SRAM blocks situated on a separate slave port on the AHB multilayer matrix.

This architecture allows CPU and DMA accesses to be spread over three separate RAMs that can be accessed simultaneously.

8.5 Memory Protection Unit (MPU)

The LPC17xx have a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

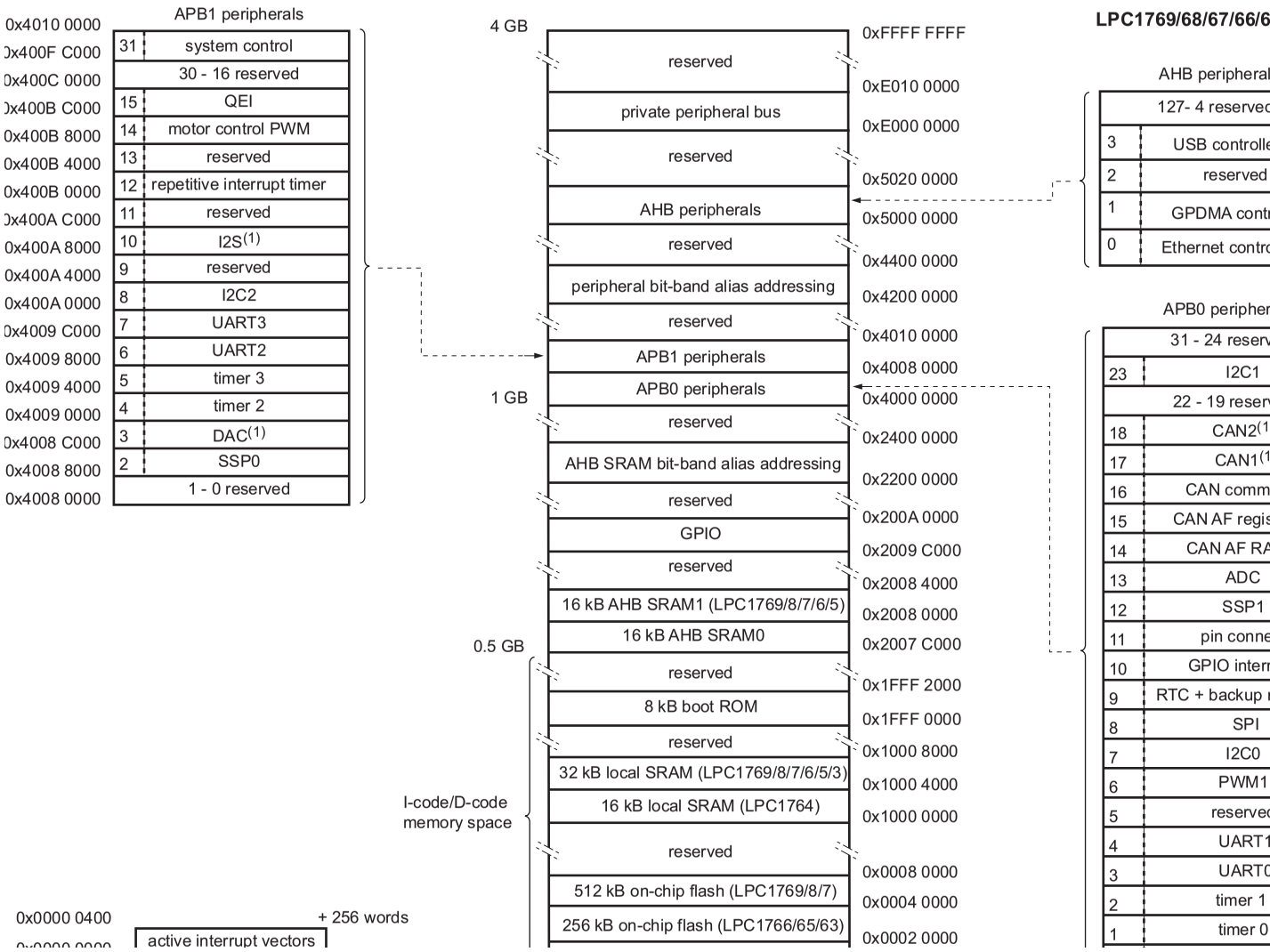
The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to 8 regions each of which can be divided into 8 subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

8.6 Memory map

The LPC17xx incorporates several distinct memory regions, shown in the following figures. Figure 5 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.



(1) Not available on all parts. See Table 2.

Fig 5. LPC17xx memory map

8.7 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Controls system exceptions and peripheral interrupts
- In the LPC17xx, the NVIC supports 33 vectored interrupts
- 32 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-Maskable Interrupt (NMI)
- Software interrupt generation

8.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any pin on Port 0 and Port 2 (total of 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a rising edge, a falling edge, or both.

8.8 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

Most pins can also be configured as open-drain outputs or to have a pull-up, pull-down, or no resistor enabled.

8.9 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the AHB master. The GPDMA controller allows data transfers between the USB and Ethernet controllers and the various on-chip SRAM areas. The supported APB peripherals are SSP0/1, all UARTs, the I^2S-bus interface, the ADC, and the DAC. Two match signals for each timer can be used to trigger DMA transfers.

Remark: The Ethernet controller is available on parts LPC1769/68/67/66/64. The USB controller is available on parts LPC1769/68/66/65/64. The I^2S-bus interface is available on parts LPC1769/68/67/66/65. The DAC is available on parts LPC1769/68/67/66/65/63.

8.9.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB bus master for transferring data. The interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

8.10 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC17xx use accelerated GPIO functions:

- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.
- Support for Cortex-M3 bit banding.
- Support for use with the GPDMA controller.

Additionally, any pin on Port 0 and Port 2 (total of 42 pins) providing a digital function can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake up the chip from Power-down mode.

8.10.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Pull-up/pull-down resistor configuration and open-drain configuration can be programmed through the pin connect block for each GPIO pin.

8.11 Ethernet

Remark: The Ethernet controller is available on parts LPC1769/68/67/66/64. The Ethernet block supports bus clock rates of up to 100 MHz (LPC1768/67/66/64) or 120 MHz (LPC1769). See Table 2.

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share the Arm Cortex-M3 D-code and system bus through the AHB-multilayer matrix to access the various on-chip SRAM blocks for Ethernet data, control, and status information.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

8.11.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with *IEEE standard 802.3*.
  - Fully compliant with 802.3x full duplex flow control and half duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.

- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Cyclic Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.
- Physical interface:
  - Attachment of external PHY chip through standard RMII interface.
  - PHY register access is available via the MIIM interface.

8.12 USB interface

Remark: The USB controller is available as device/Host/OTG controller on parts LPC1769/68/66/65 and as device-only controller on part LPC1764.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The USB interface includes a device, Host, and OTG controller with on-chip PHY for device and Host functions. The OTG switching protocol is supported through the use of an external controller. Details on typical USB interfacing solutions can be found in Section 15.1.

8.12.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the on-chip SRAM.

8.12.1.1 Features

- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.

- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the part can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled slave and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

8.12.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of a register interface, a serial interface engine, and a DMA controller. The register interface complies with the OHCI specification.

8.12.2.1 Features

- OHCI compliant.
- One downstream port.
- Supports port power switching.

8.12.3 USB OTG controller

USB OTG is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the host controller, device controller, and a master-only I^2C-bus interface to implement OTG dual-role device functionality. The dedicated I^2C-bus interface controls an external OTG transceiver.

8.12.3.1 Features

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

8.13 CAN controller and acceptance filters

Remark: The CAN controllers are available on parts LPC1769/68/66/65/64. See Table 2.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router among a number of CAN buses in industrial or automotive applications.

8.13.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes standard (11-bit) and extended-frame (29-bit) receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

8.14 12-bit ADC

The LPC17xx contain a single 12-bit successive approximation ADC with eight channels and DMA support.

8.14.1 Features

- 12-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range VREFN to VREFP.
- 12-bit conversion rate: 200 kHz.
- Individual channels can be selected for conversion.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.
- DMA support.

8.15 10-bit DAC

The DAC allows to generate a variable analog output. The maximum output value of the DAC is VREFP.

Remark: The DAC is available on parts LPC1769/68/67/66/65/63. See Table 2.

8.15.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive
- Dedicated conversion timer
- DMA support

8.16 UARTs

The LPC17xx each contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.16.1 Features

- Maximum UART data bit rate of 6.25 Mbit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- UART3 includes an IrDA mode to support infrared communication.
- All UARTs have DMA support.

8.17 SPI serial I/O controller

The LPC17xx contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

8.17.1 Features

- Maximum SPI data bit rate of 12.5 Mbit/s
- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

8.18 SSP serial I/O controller

The LPC17xx contain two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given

data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

8.18.1 Features

- Maximum SSP speed of 33 Mbit/s (master) or 8 Mbit/s (slave)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- DMA transfers supported by GPDMA

8.19 I^2C-bus serial I/O controllers

The LPC17xx each contain three I^2C-bus controllers.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

8.19.1 Features

- I^2C0 is a standard I^2C compliant bus interface with open-drain pins. I^2C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I^2C1 and I^2C2 use standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.
- All I^2C-bus controllers support multiple address recognition and a bus monitor mode.

8.20 I²S-bus serial I/O controllers

Remark: The I²S-bus interface is available on parts LPC1769/68/67/66/65/63. See Table 2.

The I²S-bus provides a standard communication interface for digital audio applications.

The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S-bus connection has one master, which is always the master, and one slave. The I²S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

8.20.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 96 kHz (16, 22.05, 32, 44.1, 48, 96) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I²S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S-bus input and I²S-bus output.

8.21 General purpose 32-bit timers/external event counters

The LPC17xx include four 32-bit timer/counters. The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.21.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.

- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

8.22 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC17xx. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

8.22.1 Features

- One PWM block with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.

- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must 'release' new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

8.23 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the PWM to immediately release all motor drive outputs. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

8.24 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.24.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with "less than" interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.

- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).
- Connected to APB.

8.25 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

8.25.1 Features

- 32-bit counter running from PCLK. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.

8.26 Arm Cortex-M3 system tick timer

The Arm Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval. In the LPC17xx, this timer can be clocked from the internal AHB clock or from a device pin.

8.27 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

8.27.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC (IRC) oscillator, the RTC oscillator, or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction

conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

- Includes lock/safe feature.

8.28 RTC and backup registers

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. The RTC on the LPC17xx is designed to have extremely low power consumption, i.e. less than 1 μA. The RTC will typically run from the main chip power supply, conserving battery power while the rest of the device is powered up. When operating from a battery, the RTC will continue working down to 2.1 V. Battery power can be provided from a standard 3 V Lithium button cell.

An ultra-low power 32 kHz oscillator will provide a 1 Hz clock to the time counting portion of the RTC, moving most of the power consumption out of the time counting function.

The RTC includes a calibration mechanism to allow fine-tuning the count rate in a way that will provide less than 1 second per day error when operated at a constant voltage and temperature. A clock output function (see Section 8.29.4) makes measuring the oscillator rate easy and accurate.

The RTC contains a small set of backup registers (20 bytes) for holding data while the main part of the LPC17xx is powered off.

The RTC includes an alarm function that can wake up the LPC17xx from all reduced power modes with a time resolution of 1 s.

8.28.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Backup registers (20 bytes) powered by VBAT.
- RTC power supply is isolated from the rest of the chip.

8.29 Clocking and power control

8.29.1 Crystal oscillators

The LPC17xx include three independent oscillators. These are the main oscillator, the IRC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the main PLL and ultimately the CPU.

Following reset, the LPC17xx will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 6 for an overview of the LPC17xx clock generation.

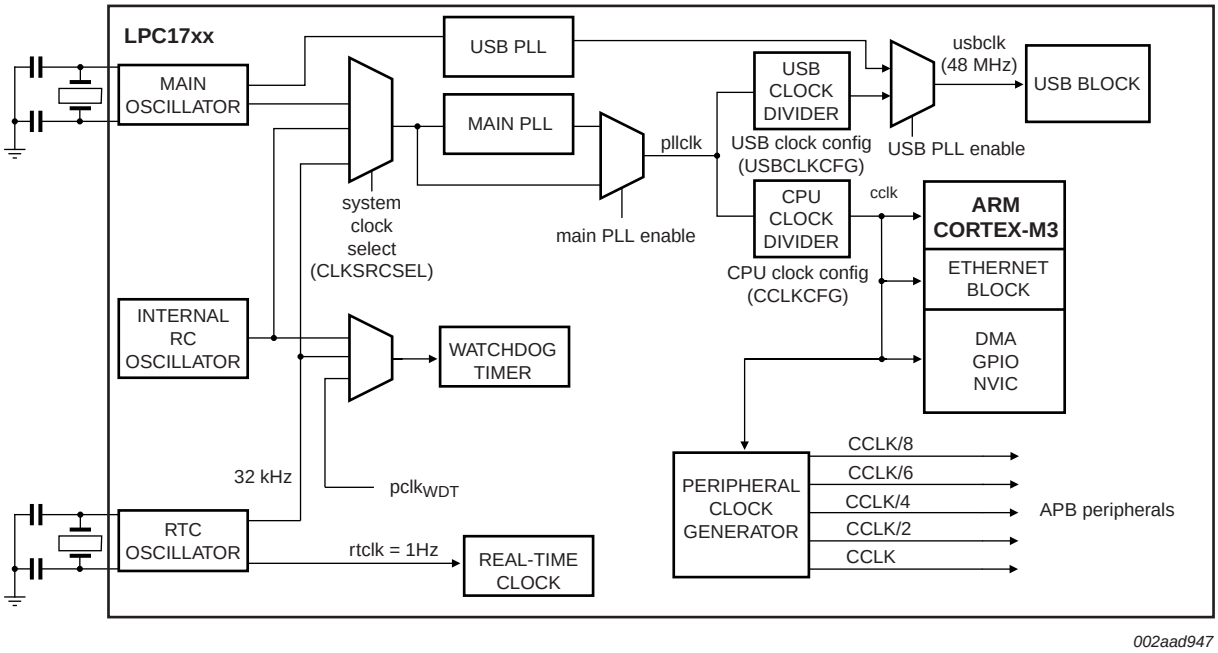


Fig 6. LPC17xx clocking generation block diagram

8.29.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC17xx use the IRC as the clock source. Software may later switch to one of the other available clock sources.

8.29.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator also provides the clock source for the dedicated USB PLL.

The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the main PLL. The clock selected as the PLL input is PLLCLKIN. The Arm processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 8.29.2 for additional information.

8.29.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC block, the main PLL, and/or the CPU.

8.29.2 Main PLL (PLL0)

The PLL0 accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and/or the USB block.

The PLL0 input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL0 input divider is the PLL0 multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value ‘M’, in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL0 is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL0 is enabled by software only. The program must configure and activate the PLL0, wait for the PLL0 to lock, and then connect to the PLL0 as a clock source.

8.29.3 USB PLL (PLL1)

The LPC17xx contain a second, dedicated USB PLL1 to provide clocking for the USB interface.

The PLL1 receives its clock input from the main oscillator only and provides a fixed 48 MHz clock to the USB block only. The PLL1 is disabled and powered off on reset. If the PLL1 is left disabled, the USB clock will be supplied by the 48 MHz clock from the main PLL0.

The PLL1 accepts an input clock frequency in the range of 10 MHz to 25 MHz only. The input frequency is multiplied up the range of 48 MHz for the USB clock using a Current Controlled Oscillators (CCO). It is insured that the PLL1 output has a 50 % duty cycle.

8.29.4 RTC clock output

The LPC17xx feature a clock output function intended for synchronizing with external devices and for use during system development to allow checking the internal clocks CCLK, IRC clock, main crystal, RTC clock, and USB clock in the outside world. The RTC clock output allows tuning the RTC frequency without probing the pin, which would distort the results.

8.29.5 Wake-up timer

The LPC17xx begin operation at power-up and when awakened from Power-down mode by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of Reset, and

whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The Wake-up Timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

8.29.6 Power control

The LPC17xx support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

Integrated PMU (Power Management Unit) automatically adjust internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.

The LPC17xx also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

8.29.6.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.29.6.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after 4 cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

8.29.6.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does, but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 4 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

8.29.6.4 Deep power-down mode

The Deep power-down mode can only be entered from the RTC block. In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

The LPC17xx can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

8.29.6.5 Wake-up interrupt controller

The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC.This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

8.29.7 Peripheral power control

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

8.29.8 Power domains

The LPC17xx provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup Registers.

On the LPC17xx, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(REG)(3V3)}$ pin powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC17xx application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. Therefore, there is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is available.

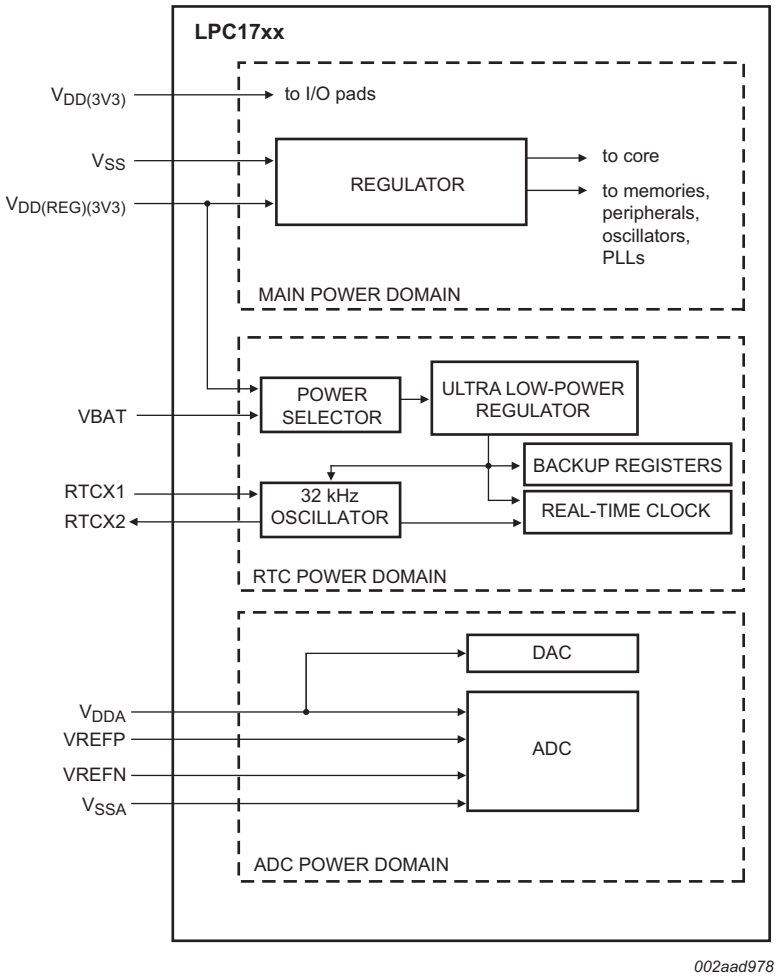


Fig 7. Power distribution

8.30 System control

8.30.1 Reset

Reset has four sources on the LPC17xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, causes the $\overline{\text{RSTOUT}}$ pin to go LOW and starts the wake-up timer (see description in Section 8.29.5). The wake-up timer ensures that reset remains asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization. Once reset is de-asserted, or, in case of a BOD-triggered reset, once the voltage rises above the BOD threshold, the $\overline{\text{RSTOUT}}$ pin goes HIGH.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the Boot Block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

8.30.2 Brownout detection

The LPC17xx include 2-stage monitoring of the voltage on the $V_{DD(REG)(3V3)}$ pins. If this voltage falls below 2.2 V, the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register.

The second stage of low-voltage detection asserts reset to inactivate the LPC17xx when the voltage on the $V_{DD(REG)(3V3)}$ pins falls below 1.85 V. This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the power-on reset circuitry maintains the overall reset.

Both the 2.2 V and 1.85 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.2 V detection to reliably interrupt, or a regularly executed event loop to sense the condition.

8.30.3 Code security (Code Read Protection - CRP)

This feature of the LPC17xx allows user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P2[10] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

8.30.4 APB interface

The APB peripherals are split into two separate APB buses in order to distribute the bus bandwidth and thereby reducing stalls caused by contention between the CPU and the GPDMA controller.

8.30.5 AHB multilayer matrix

The LPC17xx use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the Arm Cortex-M3 to the flash memory, the main (32 kB) static RAM, and the Boot ROM. The GPDMA can also access all of these memories. The peripheral DMA controllers, Ethernet, and USB can access all SRAM blocks. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

8.30.6 External interrupt inputs

The LPC17xx include up to 46 edge sensitive interrupt inputs combined with up to four level sensitive external interrupt inputs as selectable pin functions. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

8.30.7 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC17xx is configured for 128 total interrupts.

8.31 Emulation and debugging

Debug and trace functions are integrated into the Arm Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The Arm Cortex-M3 is configured to support up to eight breakpoints and four watch points.

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	–0.5	+4.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	–0.5	+4.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[2]	–0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC	[2]	–0.5	+4.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[2]	–0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins	[2][3]	–0.5	+5.1	V
V_I	input voltage	5 V tolerant digital I/O pins; $V_{DD} \geq 2.4$ V	[2][4]	–0.5	+5.5	V_I
		$V_{DD} = 0$ V		–0.5	+3.6	
		5 V tolerant open-drain pins PIO0_27 and PIO0_28	[2][5]	–0.5	+5.5	
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[6]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature				150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[7]	–4000	+4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended, and proper operation is not guaranteed. The conditions for functional operation are specified in Table 8.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 8) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] See Table 19 for maximum operating voltage.

[4] Including voltage on outputs in 3-state mode.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[7] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C)
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 7. Thermal resistance (±15 %)

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP100				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	38.01	°C/W
		Single-layer (4.5 in × 3 in); still air	55.09	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		9.065	°C/W
TFBGA100				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	55.2	°C/W
		Single-layer (4.5 in × 3 in); still air	45.6	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		9.5	°C/W

11. Static characteristics

Table 8. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3][4]	2.5	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[5]	2.1	3.3	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.5	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled; PCLK = $^{CCLK}/_{8}$					
		CCLK = 12 MHz; PLL disabled	[6][7]	-	7	-	mA
		CCLK = 100 MHz; PLL enabled	[6][7]	-	42	-	mA
		CCLK = 100 MHz; PLL enabled (LPC1769)	[6][8]	-	50	-	mA
		CCLK = 120 MHz; PLL enabled (LPC1769)	[6][8]	-	67	-	mA
		sleep mode	[6][9]	-	2	-	mA
		deep sleep mode	[6][10]	-	240	-	µA
		power-down mode	[6][10]	-	31	-	µA
		deep power-down mode; RTC running	[11]	-	630	-	nA
I_{BAT}	battery supply current	deep power-down mode; RTC running					
		$V_{DD(REG)(3V3)}$ present	[12]	-	530	-	nA
		$V_{DD(REG)(3V3)}$ not present	[13]	-	1.1	-	µA
$I_{DD(IO)}$	I/O supply current	deep sleep mode	[14][15]	-	40	-	nA
		power-down mode	[14][15]	-	40	-	nA
		deep power-down mode	[14]	-	10	-	nA

Table 8. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(ADC)}$	ADC supply current	active mode; ADC powered	[16][17]	-	1.95	-	mA
		ADC in Power-down mode	[16][18]	-	<0.2	-	µA
		deep sleep mode	[16]	-	38	-	nA
		power-down mode	[16]	-	38	-	nA
		deep power-down mode	[16]	-	24	-	nA
$I_{I(ADC)}$	ADC input current	on pin VREFP					
		deep sleep mode	[19]	-	100	-	nA
		power-down mode	[19]	-	100	-	nA
		deep power-down mode	[19]	-	100	-	nA
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[20][21][22]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[23]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[23]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	µA

Table 8. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I²C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[24]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	-	3.6	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	-	3.6	V
USB pins (LPC1769/68/66/65/64 only)							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[2]	-	-	±10	µA
V_{BUS}	bus supply voltage		[2]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[2]	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	[2]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[2]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V	[2]	-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND	[2]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[2]	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[2][25]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ $V_{DD((3V3)}$ ≤ 3.6 V. Guaranteed by design.

[3] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[4] V_{DDA} for DAC specs are from 2.7 V to 3.6 V.

[5] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[6] $V_{DD(REG)(3V3)}$ = 3.3 V; T_{amb} = 25 °C for all power consumption measurements.

[7] Applies to LPC1768/67/66/65/64/63.

[8] Applies to LPC1769 only.

[9] IRC running at 4 MHz; main oscillator and PLL disabled; PCLK = $^{CCLK}/_{8}$.

[10] BOD disabled.

[11] On pin $V_{DD(REG)(3V3)}$. I_{BAT} = 530 nA. $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[12] On pin VBAT; $I_{DD(REG)(3V3)}$ = 630 nA; $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[13] On pin VBAT; V_{BAT} = 3.0 V; T_{amb} = 25 °C.

[14] All internal pull-ups disabled. All pins configured as output and driven LOW. $V_{DD(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[15] TCK/SWDCLK pin needs to be externally pulled LOW.

[16] On pin V_{DDA}; V_{DDA} = 3.3 V; T_{amb} = 25 °C. The ADC is powered if the PDN bit in the AD0CR register is set to 1 and in Power-down mode of the PDN bit is set to 0.

[17] The ADC is powered if the PDN bit in the AD0CR register is set to 1. See *LPC17xx user manual UM10360_1*.

[18] The ADC is in Power-down mode if the PDN bit in the AD0CR register is set to 0. See *LPC17xx user manual UM10360_1*.

[19] $V_{i(VREFP)}$ = 3.3 V; T_{amb} = 25 °C.

[20] Including voltage on outputs in 3-state mode.

[21] $V_{DD(3V3)}$ supply voltages must be present.

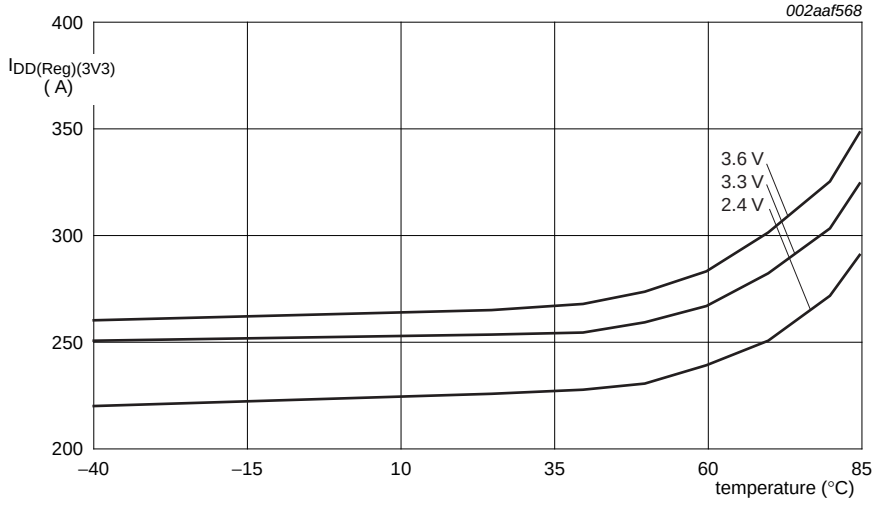
[22] 3-state outputs go into 3-state mode in Deep power-down mode.

[23] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[24] To V_{SS}.

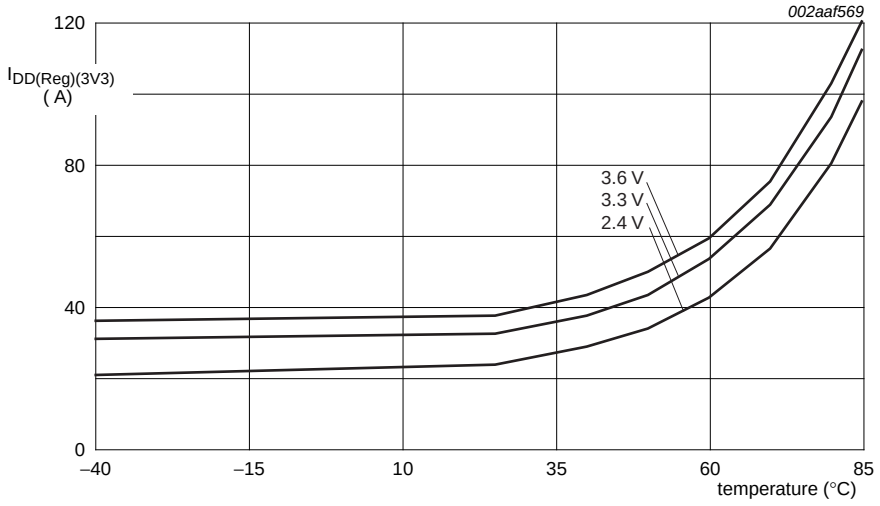
[25] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

11.1 Power consumption



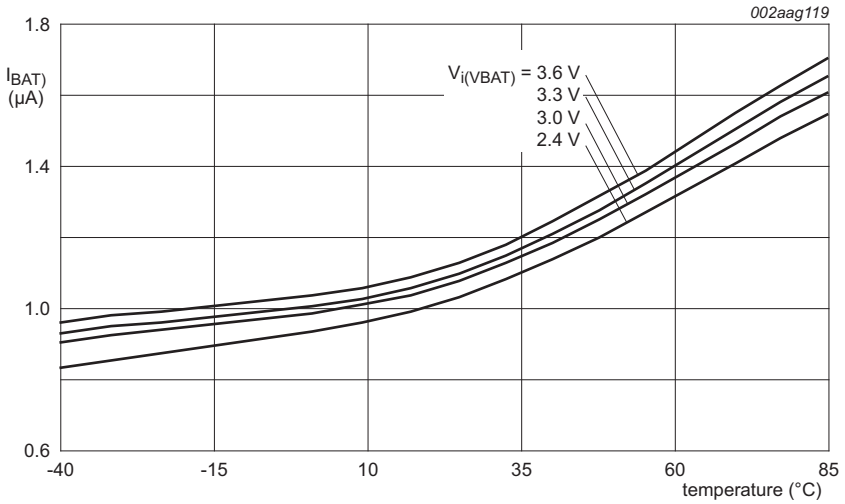
Conditions: BOD disabled.

Fig 8. Deep-sleep mode: typical regulator supply current $I_{DD(Reg)(3V3)}$ versus temperature



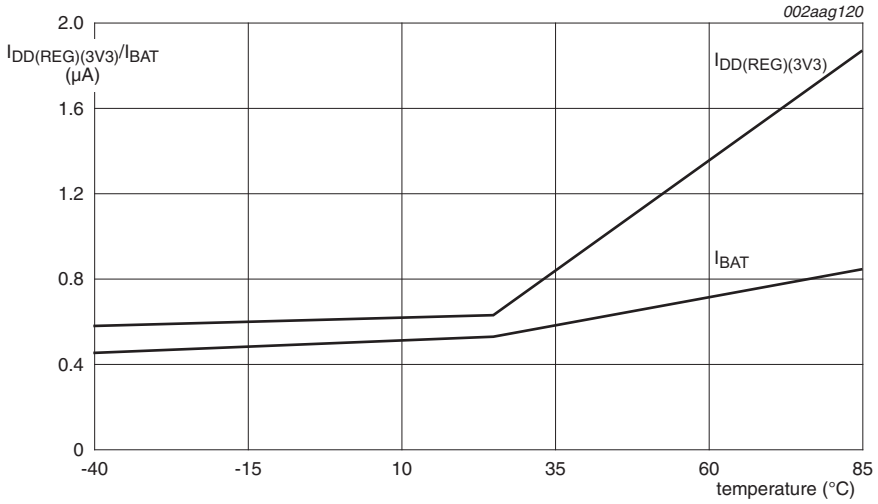
Conditions: BOD disabled.

Fig 9. Power-down mode: Typical regulator supply current $I_{DD(Reg)(3V3)}$ versus temperature



Conditions: $V_{DD(REG)(3V3)}$ floating; RTC running.

Fig 10. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature



Conditions: V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.0 V; RTC running.

Fig 11. Deep power-down mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ and battery supply current I_{BAT} versus temperature

11.2 Peripheral power consumption

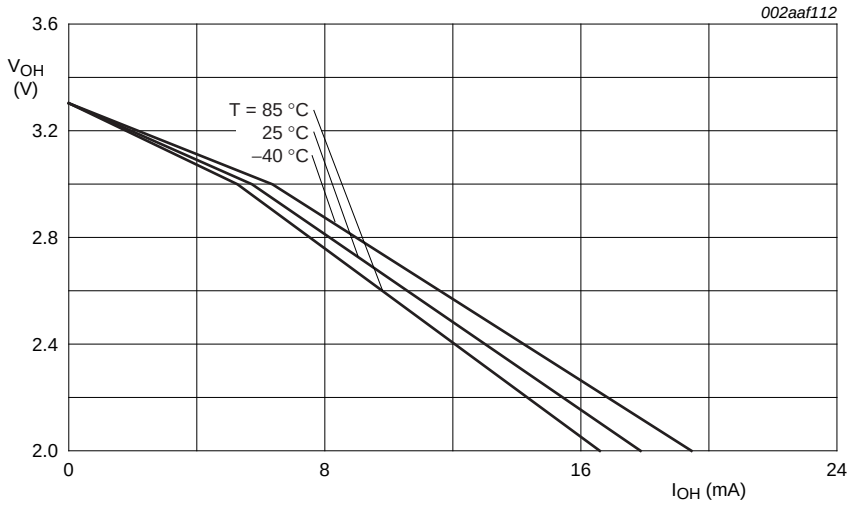
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the PCONP register. All other blocks are disabled and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. The peripheral clock PCLK = CCLK/4.

Table 9. Power consumption for individual analog and digital blocks

Peripheral	Conditions	Typical supply current in mA; CCLK =			Notes
		12 MHz	48 MHz	100 MHz	
Timer		0.03	0.11	0.23	Average current per timer
UART		0.07	0.26	0.53	Average current per UART
PWM		0.05	0.20	0.41	
Motor control PWM		0.05	0.21	0.42	
I2C		0.02	0.08	0.16	Average current per I2C
SPI		0.02	0.06	0.13	
SSP1		0.04	0.16	0.32	
ADC	PCLK = 12 MHz for CCLK = 12 MHz and 48 MHz; PCLK = 12.5 MHz for CCLK = 100 MHz	2.12	2.09	2.07	
CAN	PCLK = CCLK/6	0.13	0.49	1.00	Average current per CAN
CAN0, CAN1, acceptance filter	PCLK = CCLK/6	0.22	0.85	1.73	Both CAN blocks and acceptance filter[1]
DMA	PCLK = CCLK	1.33	5.10	10.36	
QEI		0.05	0.20	0.41	
GPIO		0.33	1.27	2.58	
I2S		0.09	0.34	0.70	
USB and PLL1		0.94	1.32	1.94	
Ethernet	Ethernet block enabled in the PCONP register; Ethernet not connected.	0.49	1.87	3.79	
Ethernet connected	Ethernet initialized, connected to network, and running web server example.	-	-	5.19	

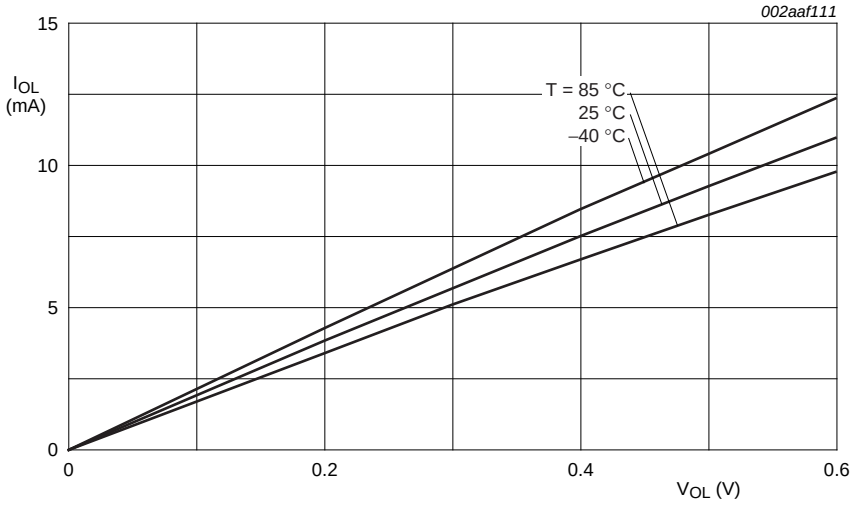
[1] The combined current of several peripherals running at the same time can be less than the sum of each individual peripheral current measured separately.

11.3 Electrical pin characteristics



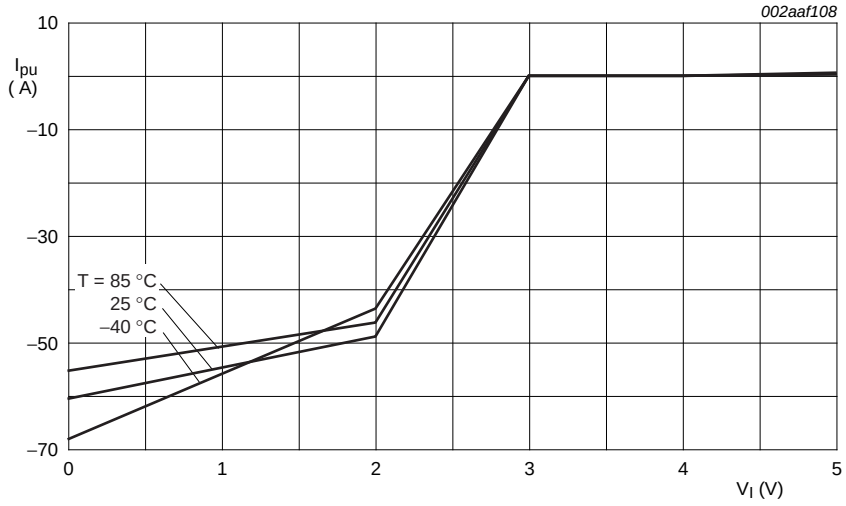
Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 12. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



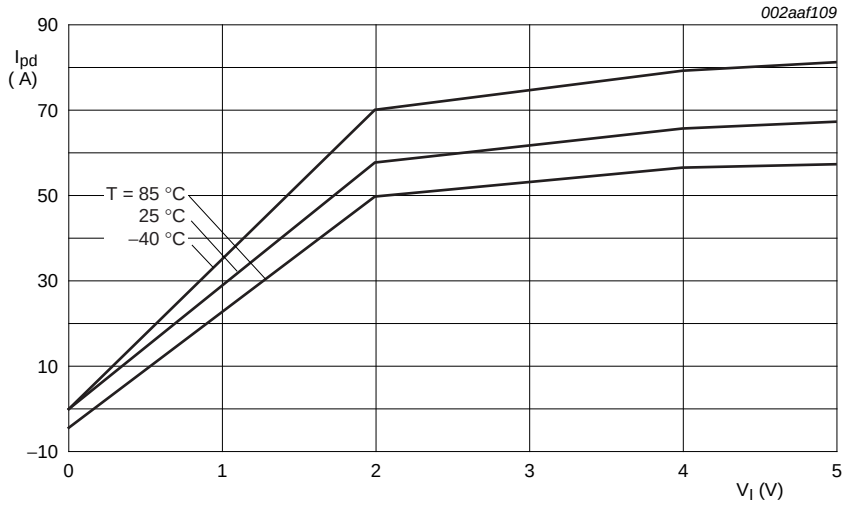
Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 13. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 14. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 15. Typical pull-down current I_{pd} versus input voltage V_I

12. Dynamic characteristics

12.1 Flash memory

Table 10. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

12.2 External clock

Table 11. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency			1	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

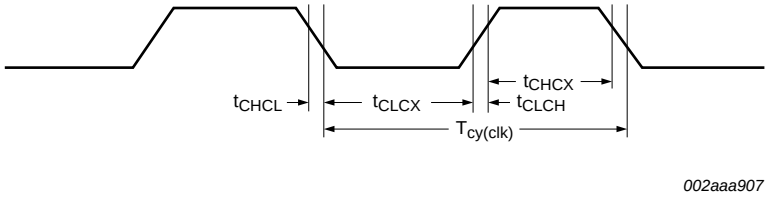


Fig 16. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 Internal oscillators

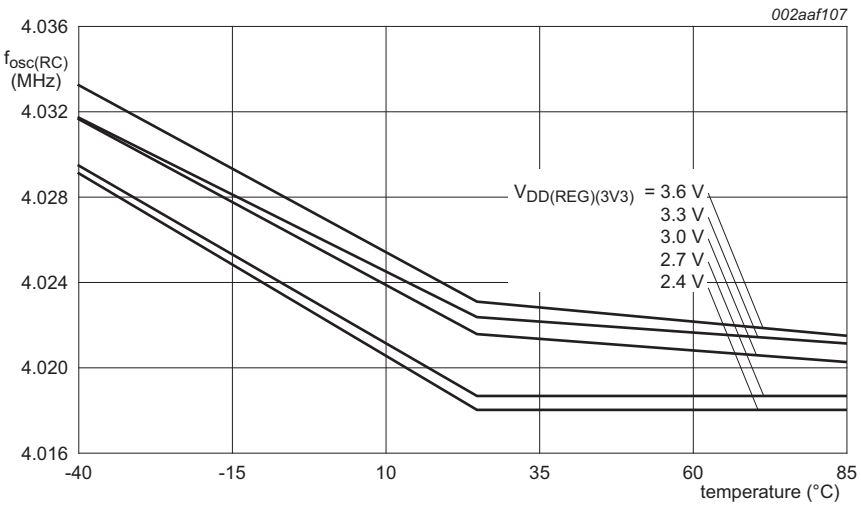
Table 12. Dynamic characteristic: internal oscillators

T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-		3.96	4.02	4.04	MHz
$f_{i(RTC)}$	RTC input frequency	-		-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 4 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 4 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 17. Internal RC oscillator frequency versus temperature

12.4 I/O pins

Table 13. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard I/O pins.

12.5 I²C-bus

Table 14. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][7][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see the I²C-bus specification *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

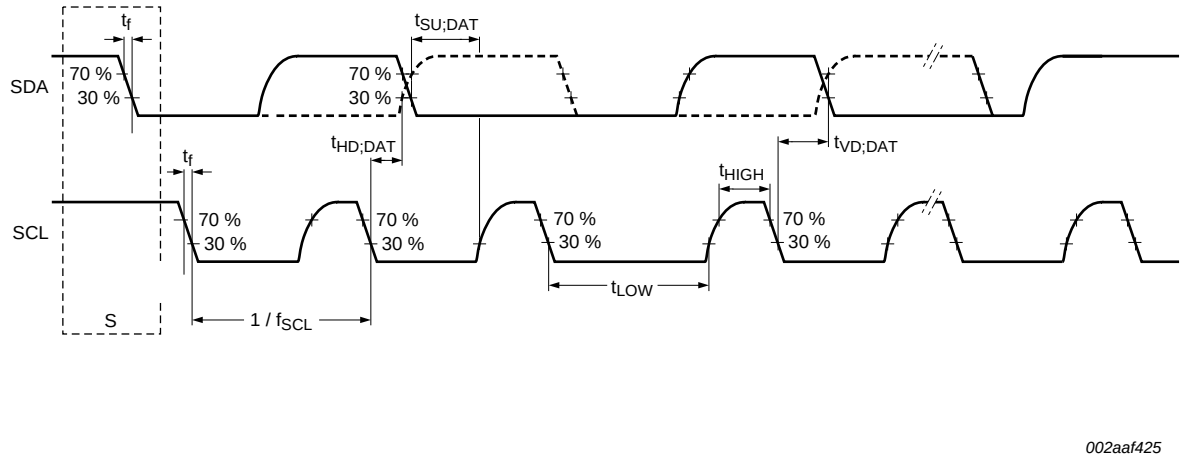


Fig 18. I²C-bus pins clock timing

12.6 I²S-bus interface

Remark: The I²S-bus interface is available on parts LPC1769/68/67/66/65/63. See Table 2.

Table 15. Dynamic characteristics: I²S-bus interface pins

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time		[1]	-	-	35	ns
t_f	fall time		[1]	-	-	35	ns
t_{WH}	pulse width HIGH	on pins I2STX_CLK and I2SRX_CLK	[1]	0.495 × $T_{cy(clk)}$	-	-	-
t_{WL}	pulse width LOW	on pins I2STX_CLK and I2SRX_CLK	[1]	-	-	0.505 × $T_{cy(clk)}$	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2STX_SDA	[1]	-	-	30	ns
		on pin I2STX_WS	[1]	-	-	30	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2SRX_SDA	[1]	3.5	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2SRX_SDA	[1]	4.0	-	-	ns

[1] CCLK = 20 MHz; peripheral clock to the I²S-bus interface PCLK = $^{CCLK}/_{4}$; I²S clock cycle time $T_{cy(clk)}$ = 1600 ns, corresponds to the SCK signal in the *I²S-bus specification*.

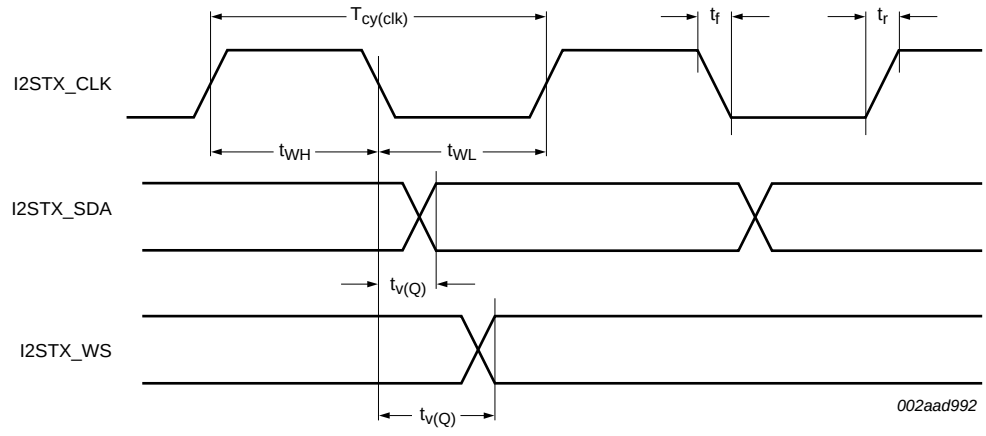


Fig 19. I²S-bus timing (output)

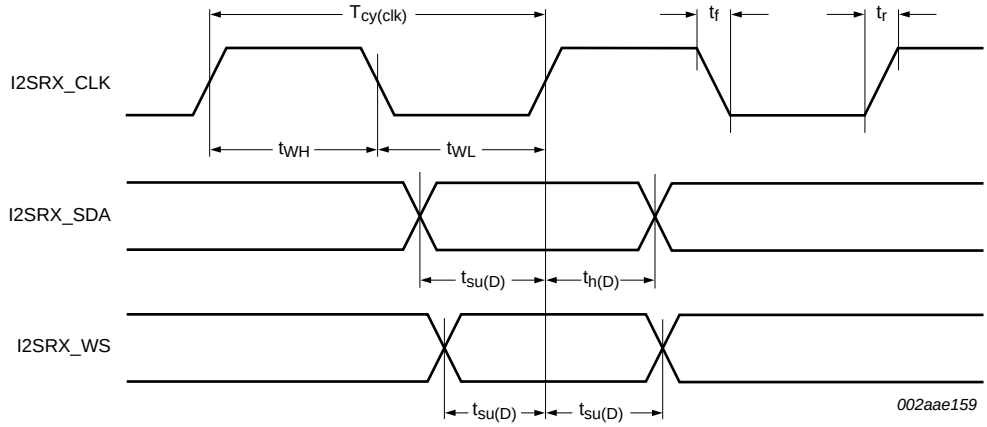


Fig 20. I²S-bus timing (input)

12.7 SSP interface

The maximum SSP speed is 33 Mbit/s in master mode or 8 Mbit/s in slave mode. In slave mode, the maximum SSP clock rate must be 1/12 of the SSP PCLK clock rate.

Table 16. Dynamic characteristics: SSP pins in SPI mode

C_L = 30 pF for all SSP pins; T_{amb} = −40 °C to 85 °C; $V_{DD(3V3)}$ = 3.3 V to 3.6 V; input slew = 1 ns; sampled at 10 % and 90 % of the signal level. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
SSP master					
t_{DS}	data set-up time	in SPI mode	16.1	-	ns
t_{DH}	data hold time	in SPI mode	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	2.5	ns
$t_{h(Q)}$	data output hold time	in SPI mode	0	-	ns
SSP slave					
t_{DS}	data set-up time	in SPI mode	16.1	-	ns
t_{DH}	data hold time	in SPI mode	0	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	$3*T_{cy(PCLK)} + 2.5$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	0	-	ns

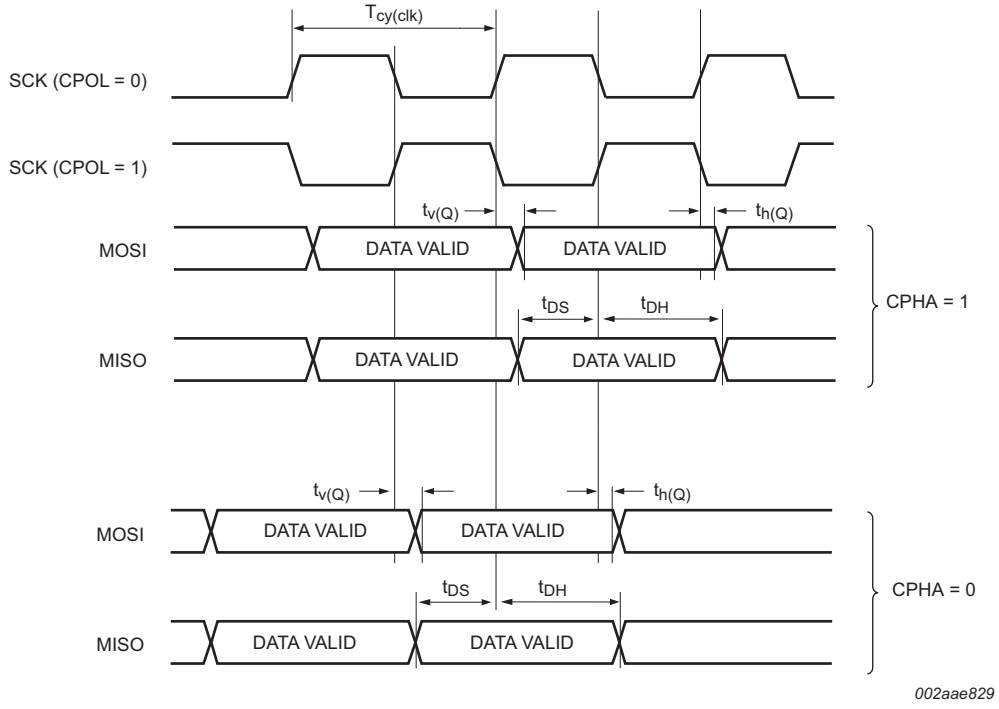


Fig 21. SSP master timing in SPI mode

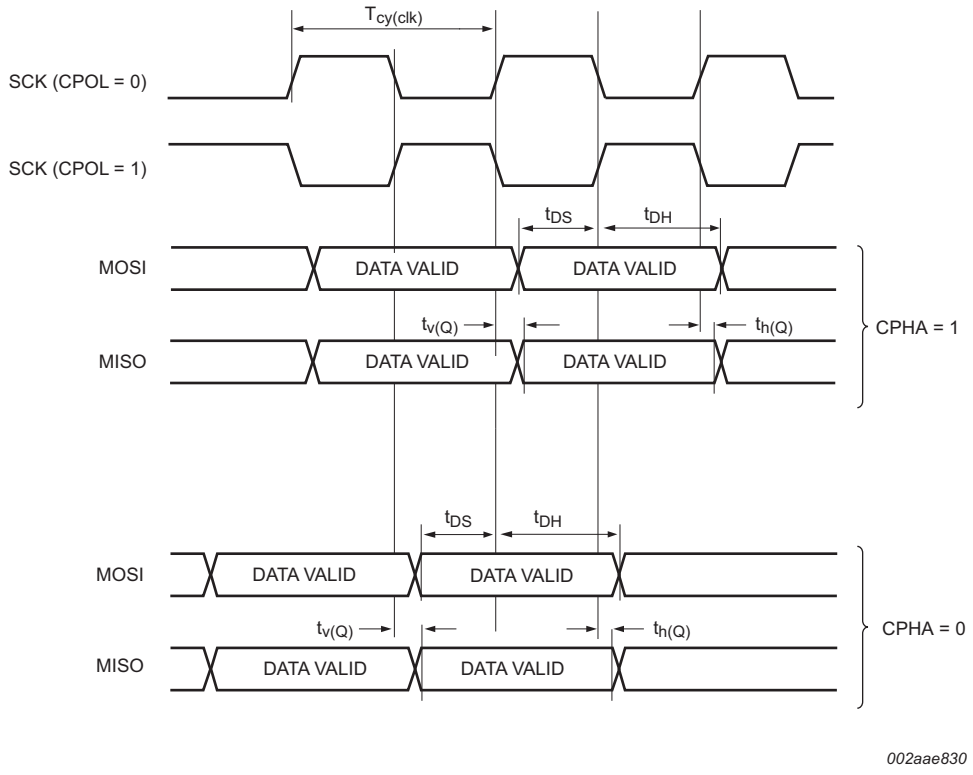


Fig 22. SSP slave timing in SPI mode

12.8 USB interface

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC1769/68/66/65 and as device-only controller on part LPC1764.

Table 17. Dynamic characteristics: USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(3V3)}$; 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 23		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 23		–2	-	+5	ns
t_{JR1}	receiver jitter to next transition			–18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		–9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 23	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 23	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

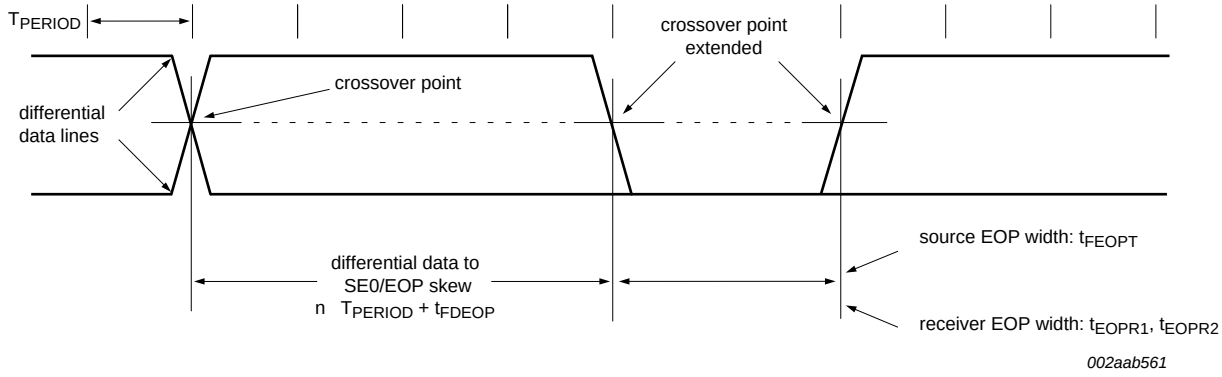


Fig 23. Differential data-to-EOP transition skew and EOP width

12.9 SPI

Table 18. Dynamic characteristics of SPI pins

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time		10	-	-	ns
T_{SPICYC}	SPI cycle time	[1]	79.6	-	-	ns
$t_{SPICLKH}$	SPICLK HIGH time		0.485 × T_{SPICYC}	-	-	ns
$t_{SPICLKL}$	SPICLK LOW time			-	0.515 × T_{SPICYC}	ns
SPI master						
t_{SPIDSU}	SPI data set-up time	[2]	0	-	-	ns
t_{SPIDH}	SPI data hold time	[2]	2 × $T_{cy(PCLK)}$ − 5	-	-	ns
t_{SPIQV}	SPI data output valid time	[2]	2 × $T_{cy(PCLK)}$ + 30	-	-	ns
t_{SPIOH}	SPI output data hold time	[2]	2 × $T_{cy(PCLK)}$ + 5	-	-	ns
SPI slave						
t_{SPIDSU}	SPI data set-up time	[2]	0	-	-	ns
t_{SPIDH}	SPI data hold time	[2]	2 × $T_{cy(PCLK)}$ + 5	-	-	ns
t_{SPIQV}	SPI data output valid time	[2]	2 × $T_{cy(PCLK)}$ + 35	-	-	ns
t_{SPIOH}	SPI output data hold time	[2]	2 × $T_{cy(PCLK)}$ + 15	-	-	ns

[1] $T_{SPICYC} = (T_{cy(PCLK)} \times n) \pm 0.5$ %, n is the SPI clock divider value ($n \geq 8$); PCLK is derived from the processor clock CCLK.

[2] Timing parameters are measured with respect to the 50 % edge of the clock SCK and the 10 % (90 %) edge of the data signal (MOSI or MISO).

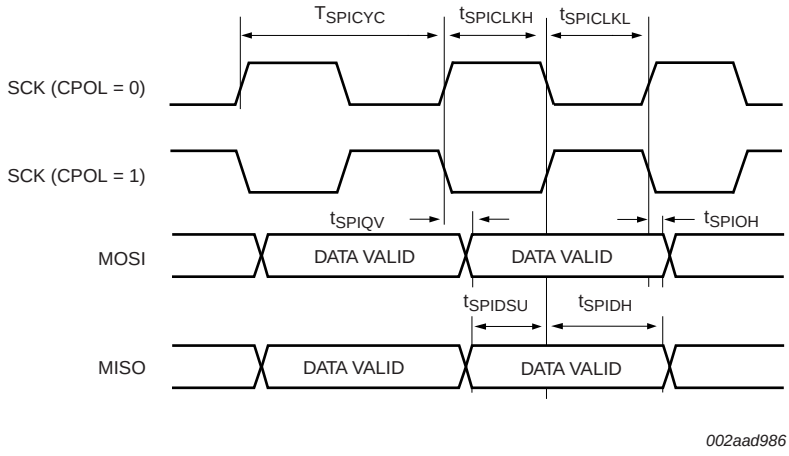


Fig 24. SPI master timing (CPHA = 1)

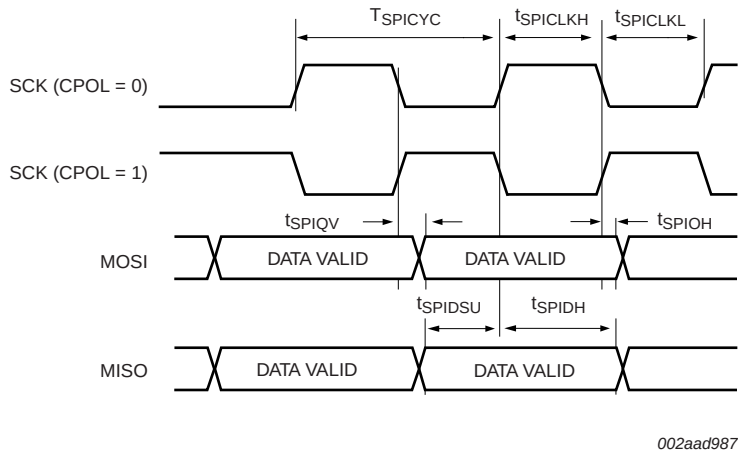


Fig 25. SPI master timing (CPHA = 0)

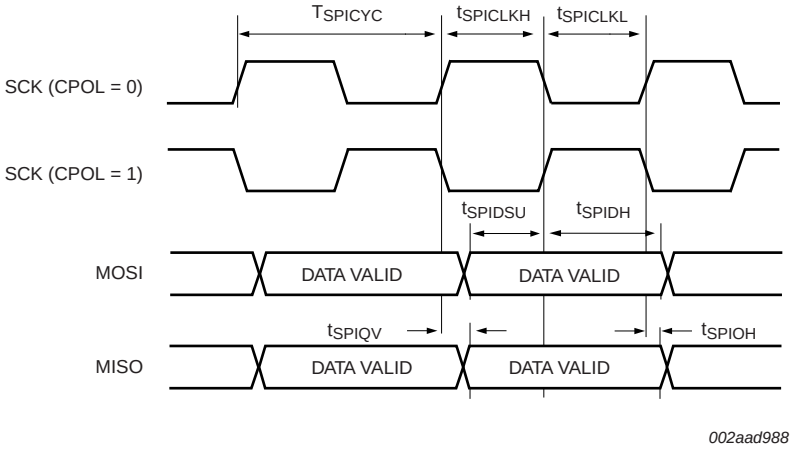


Fig 26. SPI slave timing (CPHA = 1)

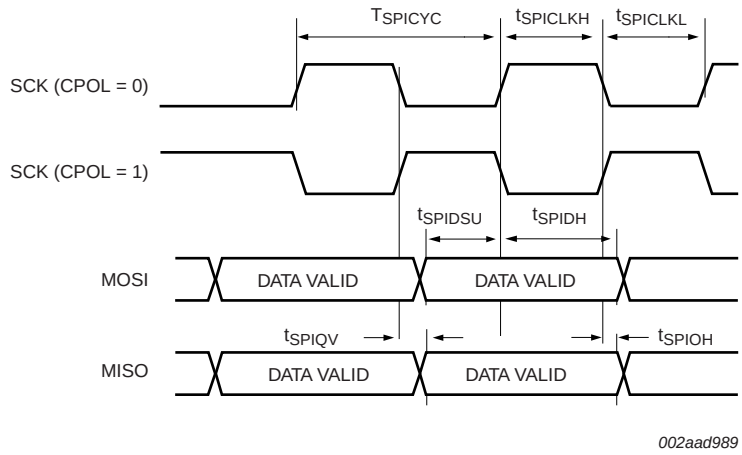


Fig 27. SPI slave timing (CPHA = 0)

13. ADC electrical characteristics

Table 19. ADC characteristics (full resolution)

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 13 MHz; 12-bit resolution.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	15	pF
E_D	differential linearity error		[2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[4]	-	-	±3	LSB
E_O	offset error		[5][6]	-	-	±2	LSB
E_G	gain error		[7]	-	-	0.5	%
E_T	absolute error		[8]	-	-	4	LSB
R_{vsi}	voltage source interface resistance		[9]	-	-	7.5	kΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	13	MHz
$f_{c(ADC)}$	ADC conversion frequency		[10]	-	-	200	kHz

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.

[6] ADCOFFS value (bits 7:4) = 2 in the ADTRM register. See *LPC17xx user manual UM10360*.

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 28.

[9] See Figure 29.

[10] The conversion frequency corresponds to the number of samples per second.

Table 20. ADC characteristics (lower resolution)

T_{amb} = −40 °C to +85 °C unless otherwise specified; 12-bit ADC used as 10-bit resolution ADC.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error		[2][3]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[4]	-	±1.5	-	LSB
E_O	offset error		[5]	-	±2	-	LSB
E_G	gain error		[6]	-	±2	-	LSB
$f_{clk(ADC)}$	ADC clock frequency	$3.0\ V \le V_{DDA} \le 3.6\ V$		-	-	33	MHz
		$2.7\ V \le V_{DDA} < 3.0\ V$		-	-	25	MHz
$f_{c(ADC)}$	ADC conversion frequency	$3\ V \le V_{DDA} \le 3.6\ V$	[7]	-	-	500	kHz
		$2.7\ V \le V_{DDA} < 3.0\ V$	[7]	-	-	400	kHz

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] The ADC is monotonic, there are no missing codes.

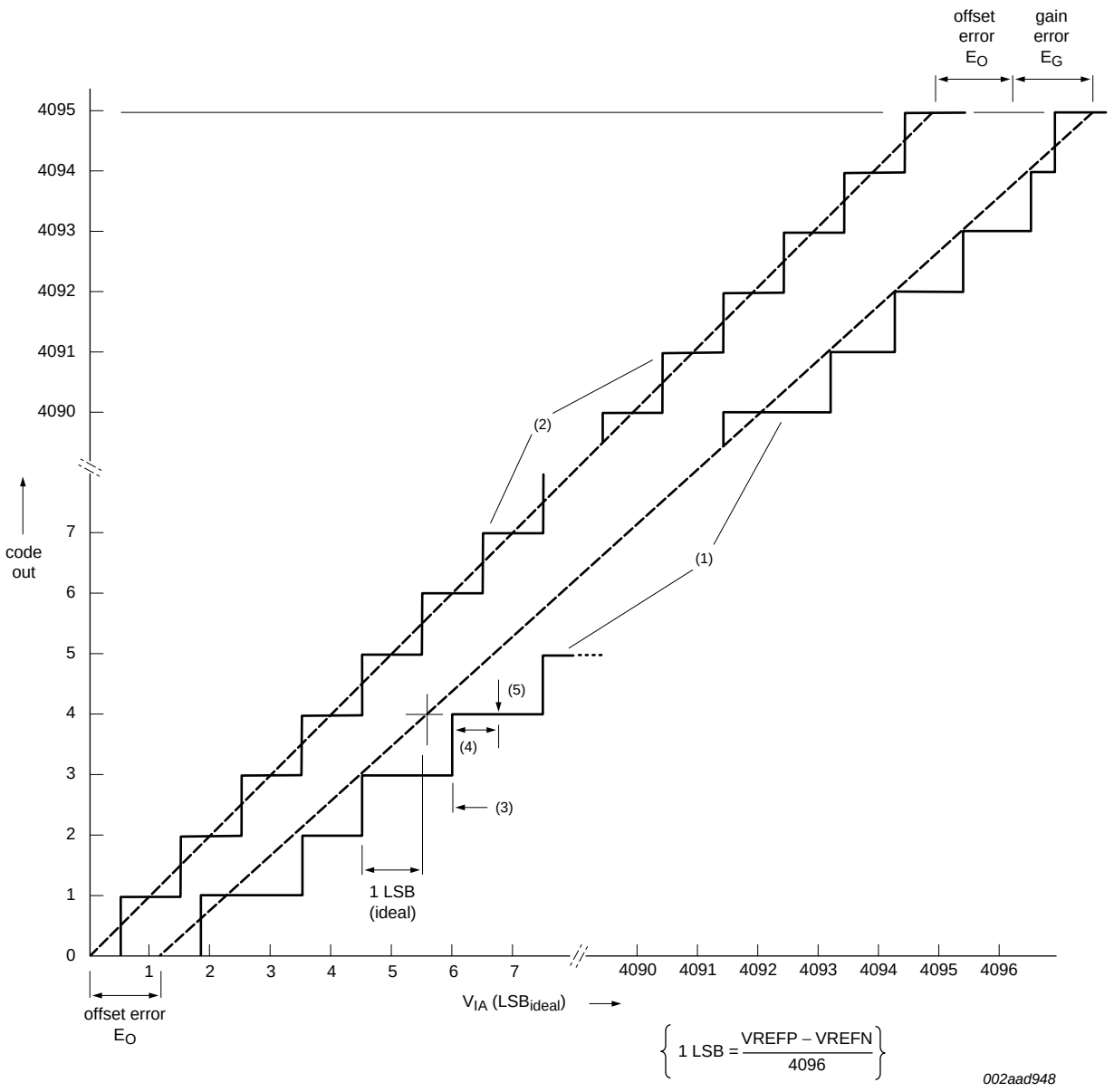
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.

[7] The conversion frequency corresponds to the number of samples per second.



(1) Example of an actual transfer curve.

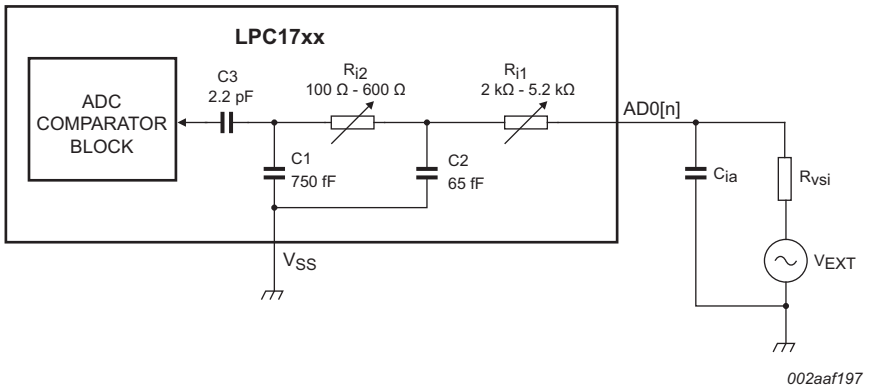
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 28. 12-bit ADC characteristics



The values of resistor components R_{i1} and R_{i2} vary with temperature and input voltage and are process-dependent (see Table 21).

Parasitic resistance and capacitance from the pad are not included in this figure.

Fig 29. ADC interface to pins AD0[n]

Table 21. ADC interface components

Component	Range	Description
R_{i1}	2 kΩ to 5.2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
R_{i2}	100 Ω to 600 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
C1	750 fF	Parasitic capacitance from the ADC block level.
C2	65 fF	Parasitic capacitance from the ADC block level.
C3	2.2 pF	Sampling capacitor.

14. DAC electrical characteristics

Remark: The DAC is available on parts LPC1769/68/67/66/65/63. See Table 2.

Table 22. DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error			-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity			-	±1.5	-	LSB
E_O	offset error			-	0.6	-	%
E_G	gain error			-	0.6	-	%
C_L	load capacitance			-	200	-	pF
R_L	load resistance			1	-	-	kΩ

15. Application information

15.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC1769/68/66/65 and as device-only controller on part LPC1764.

If the LPC1769/68/67/66/65/64/63 V_{DD} is always greater than 0 V while V_{BUS} = 5 V, the V_{BUS} pin can be connected directly to the V_{BUS} pin on the USB connector.

This applies to bus powered devices where the USB cable supplies the system power. For systems where V_{DD} can be 0 V and V_{BUS} is directly applied to the V_{BUS} pin, precautions must be taken to reduce the voltage to below 3.6 V.

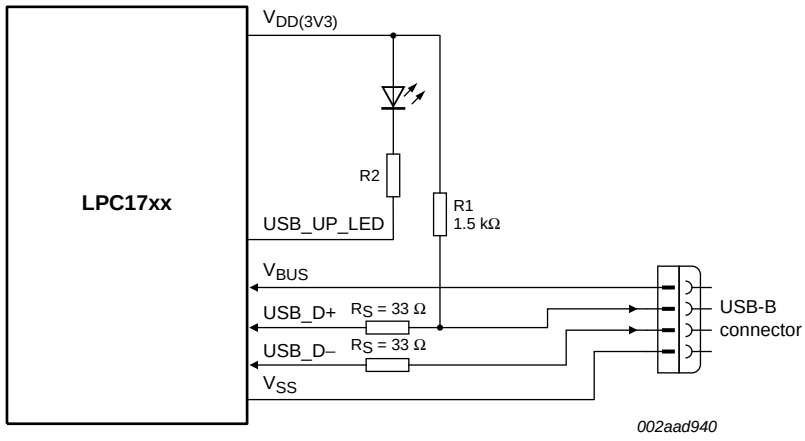


Fig 30. USB interface on a bus-powered device

The maximum allowable voltage on the V_{BUS} pin is 3.6 V. One method is to use a voltage divider to connect the V_{BUS} pin to the V_{BUS} on the USB connector.

The voltage divider ratio should be such that the V_{BUS} pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

Use the following operating conditions:

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V

The voltage divider would need to provide a reduction of 3.6 V/5.25 V or ~0.686 V.

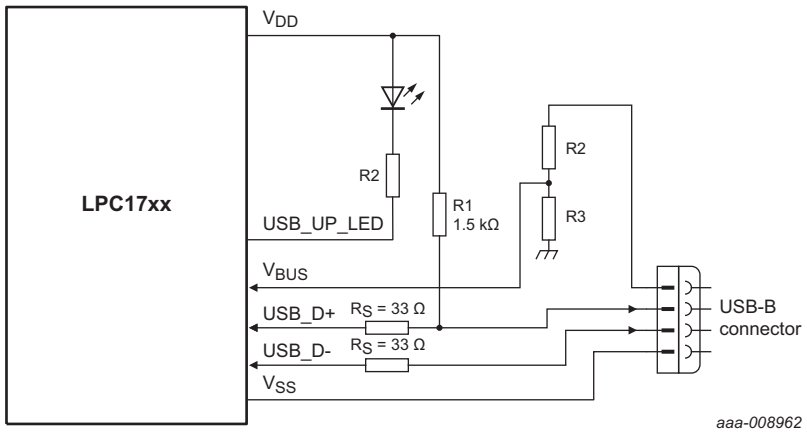


Fig 31. USB interface on a bus-powered device where V_{BUS} = 5 V, V_{DD} not present

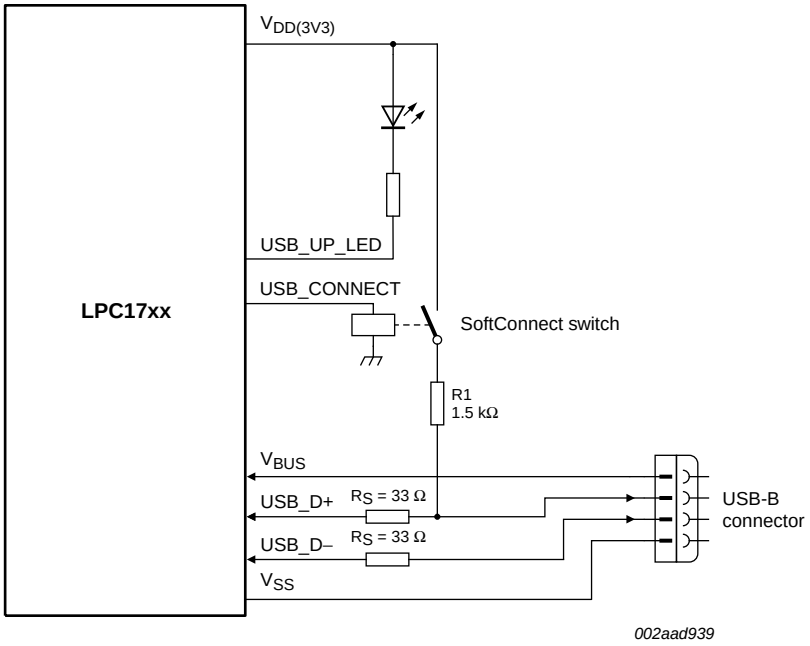


Fig 32. USB interface with soft-connect

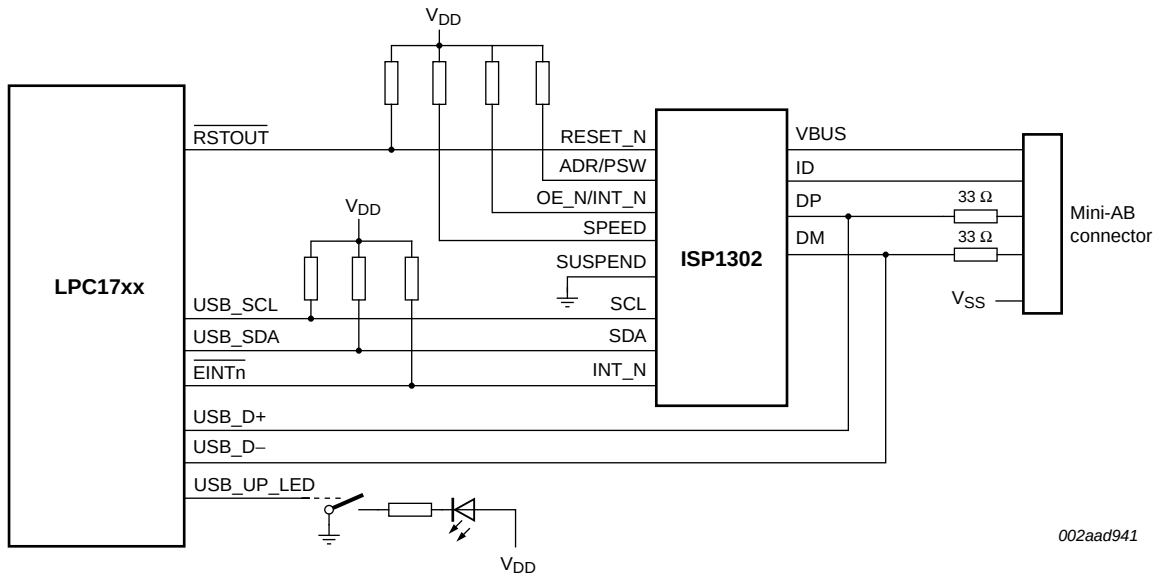


Fig 33. USB OTG port configuration

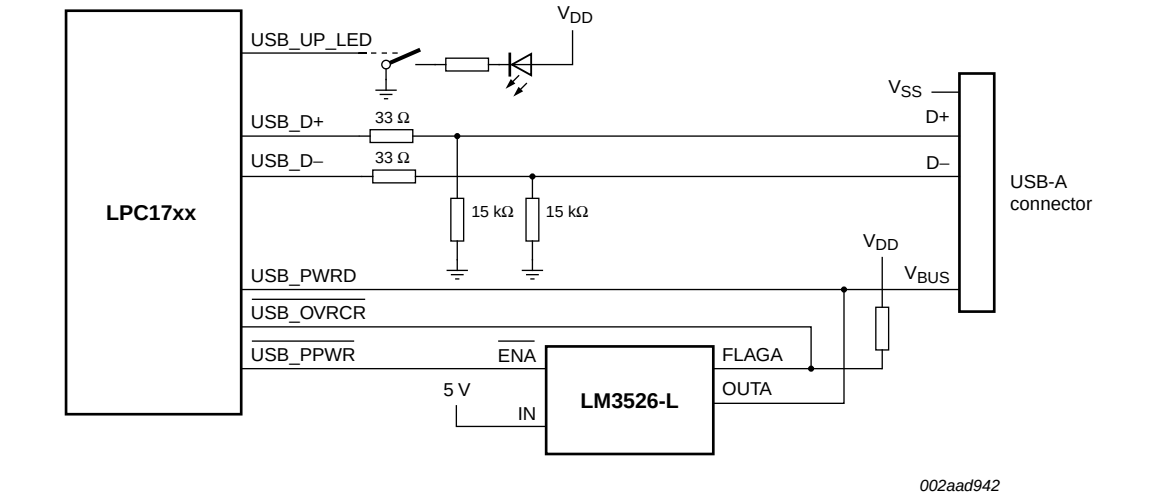


Fig 34. USB host port configuration

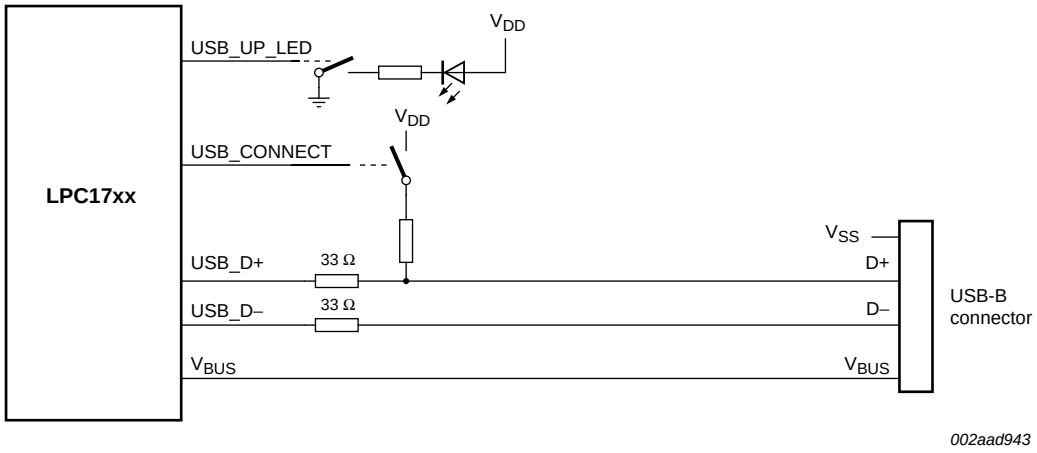


Fig 35. USB device port configuration

15.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

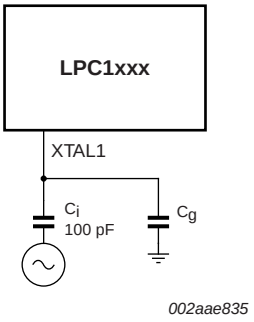


Fig 36. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 36), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 37 and in Table 23 and Table 24. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 37 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

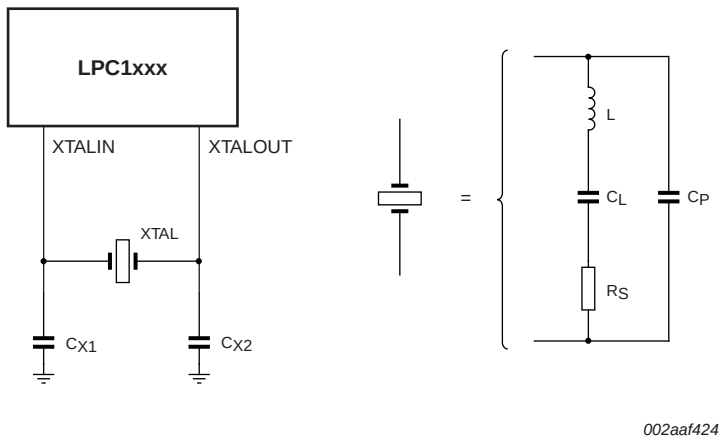


Fig 37. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 23. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 24. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

15.3 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in

order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

15.4 Standard I/O pin configuration

Figure 38 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver: Open-drain mode enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

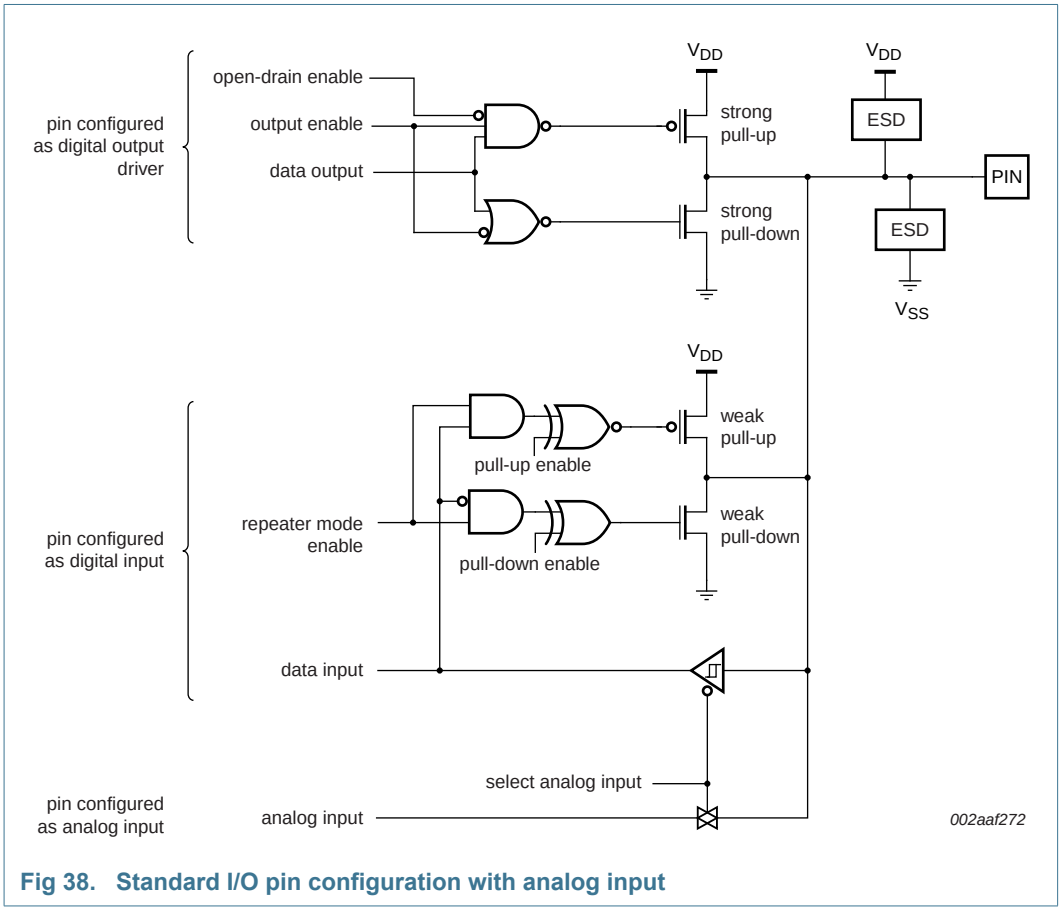


Fig 38. Standard I/O pin configuration with analog input

15.5 Reset pin configuration

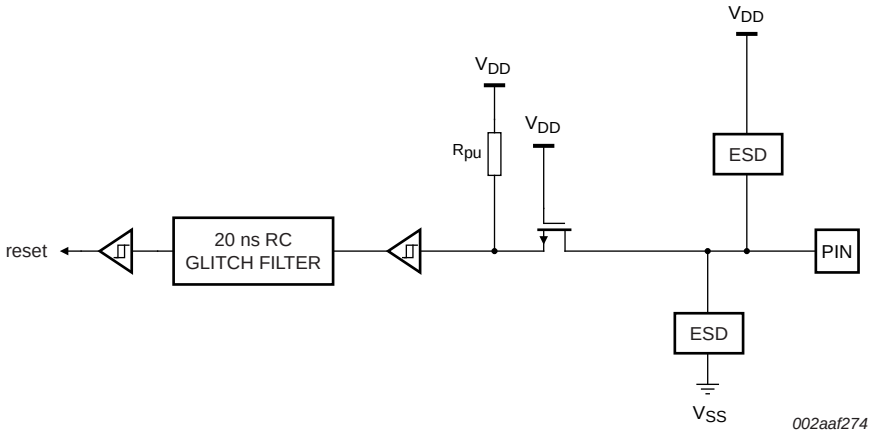


Fig 39. Reset pin configuration

15.6 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC1768.

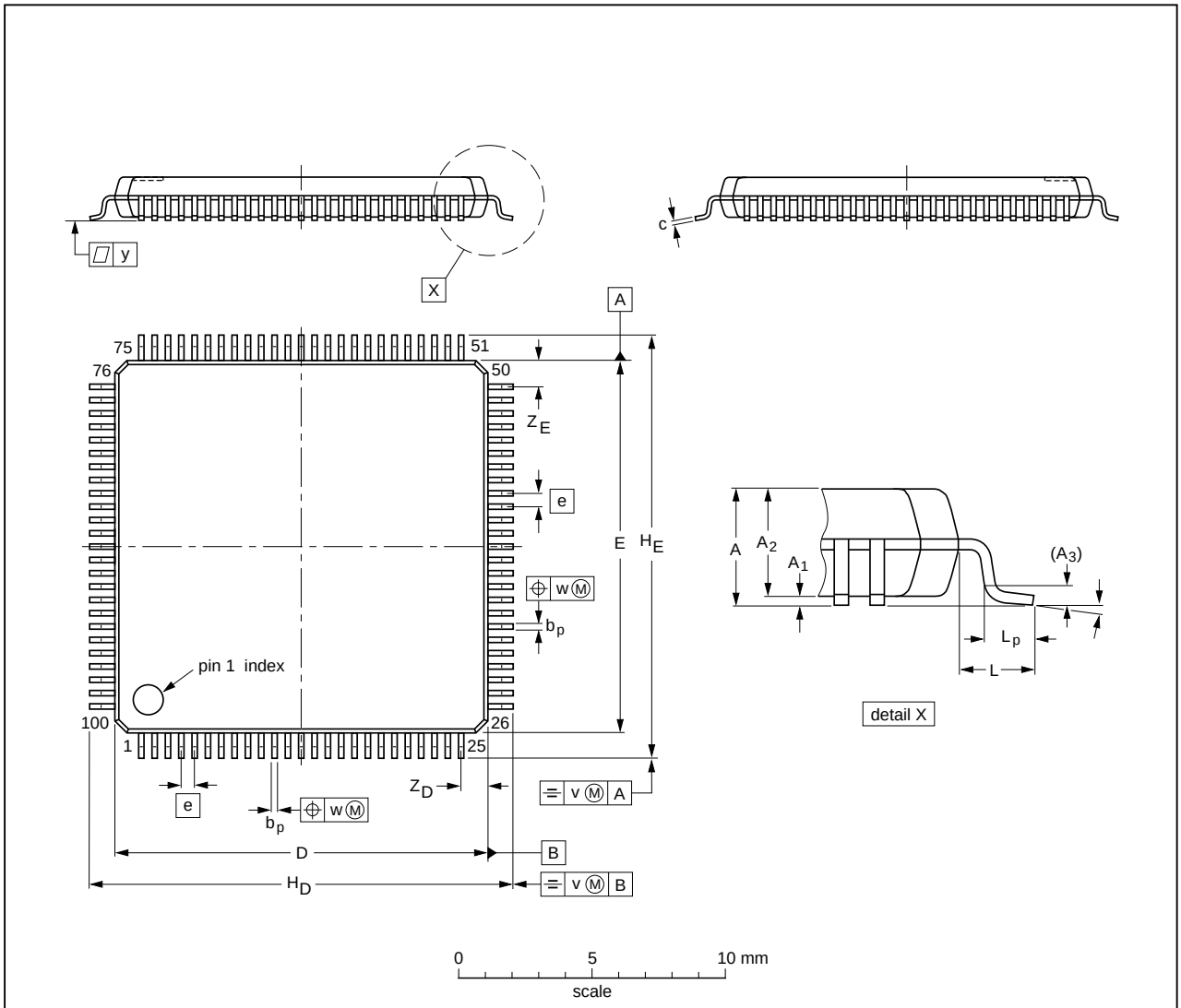
Table 25. ElectroMagnetic Compatibility (EMC) for part LPC1768 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =					Unit
		12 MHz	24 MHz	48 MHz	72 MHz	100 MHz	
Input clock: IRC (4 MHz)							
maximum peak level	150 kHz to 30 MHz	–7	–6	–4	–7	–7	dBµV
	30 MHz to 150 MHz	+1	+5	+11	+16	+9	dBµV
	150 MHz to 1 GHz	–2	+4	+11	+12	+19	dBµV
IEC level[1]	-	O	O	N	M	L	-
Input clock: crystal oscillator (12 MHz)							
maximum peak level	150 kHz to 30 MHz	–5	–4	–4	–7	–8	dBµV
	30 MHz to 150 MHz	–1	+5	+10	+15	+7	dBµV
	150 MHz to 1 GHz	–1	+6	+11	+10	+16	dBµV
IEC level[1]	-	O	O	N	M	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

16. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

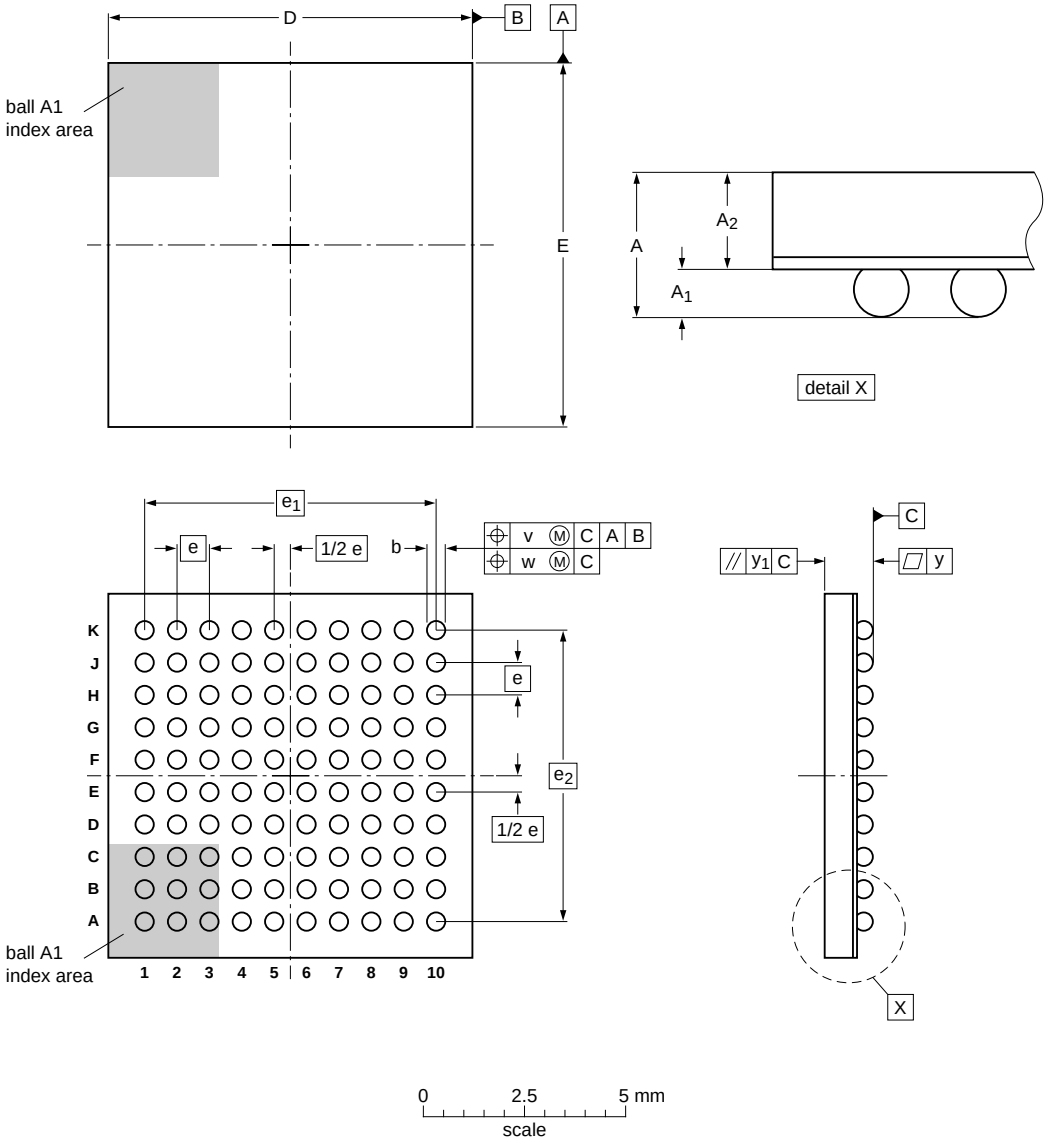
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 40. Package outline SOT407-1 (LQFP100)

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**

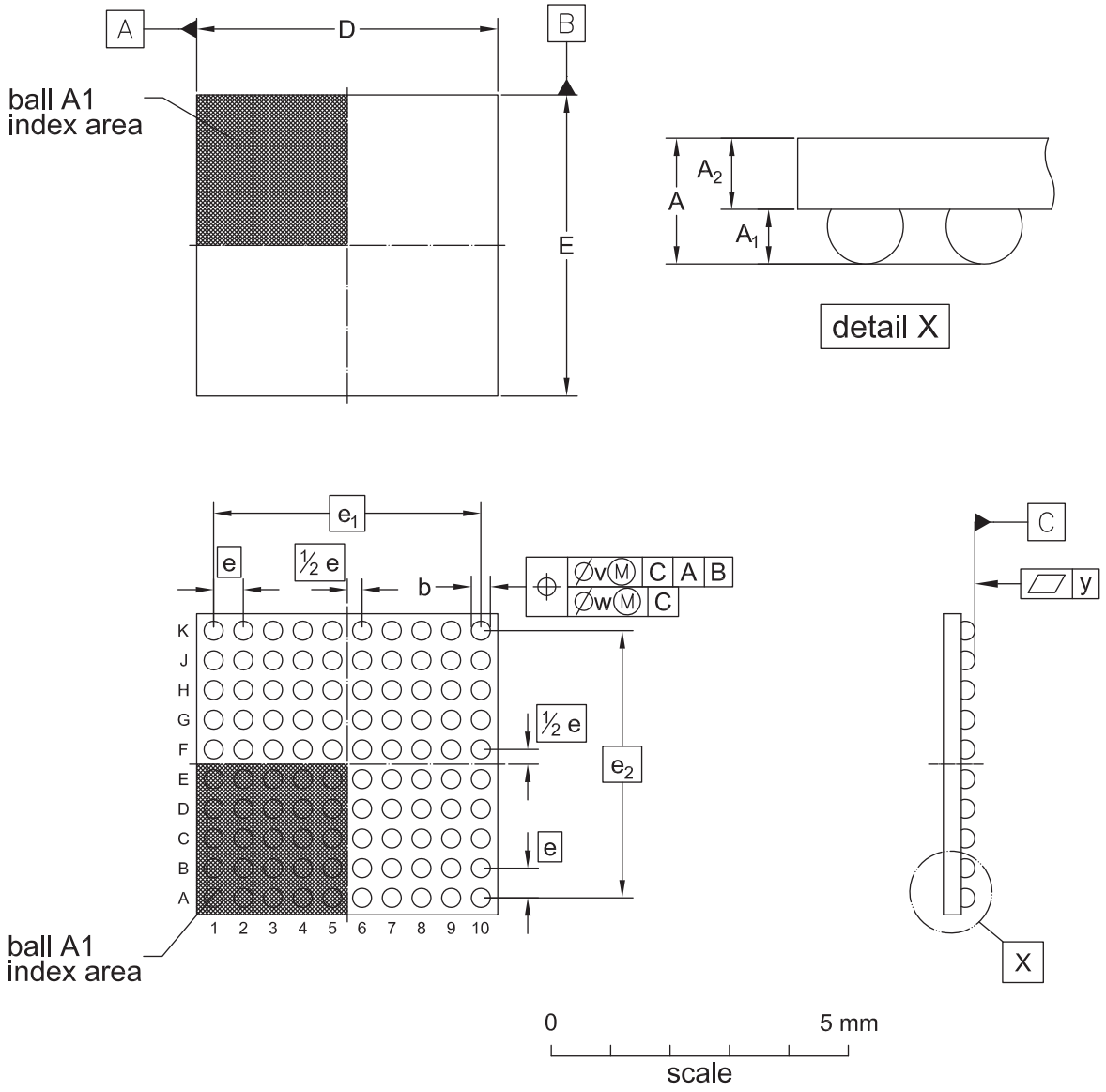


DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 41. Package outline SOT926-1 (TFBGA100)



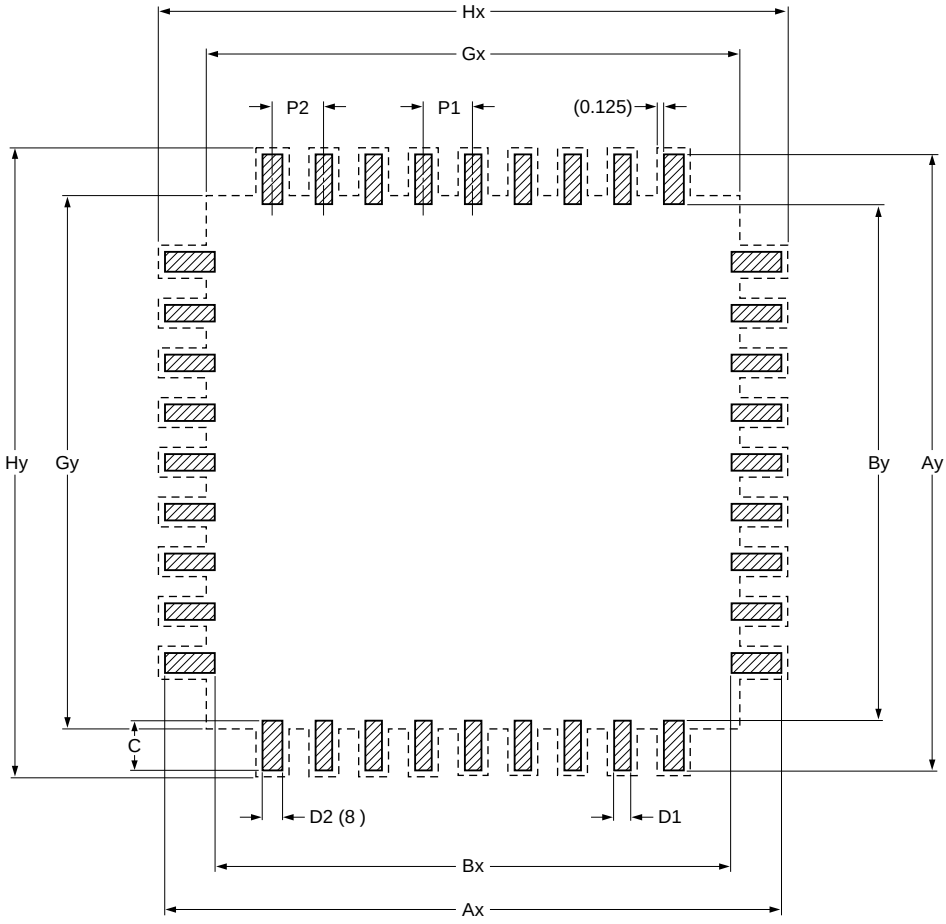
DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX	0.57	0.26	0.325	0.35	5.10	5.10	0.5	4.5	4.5	0.15	0.05	0.03
	NOM	0.53	0.23	0.300	0.32	5.07	5.07						
	MIN	0.49	0.20	0.275	0.29	5.04	5.04						

Fig 42. Package outline SOT1450-2 LPC1768UK (WLCSP100)

17. Soldering

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

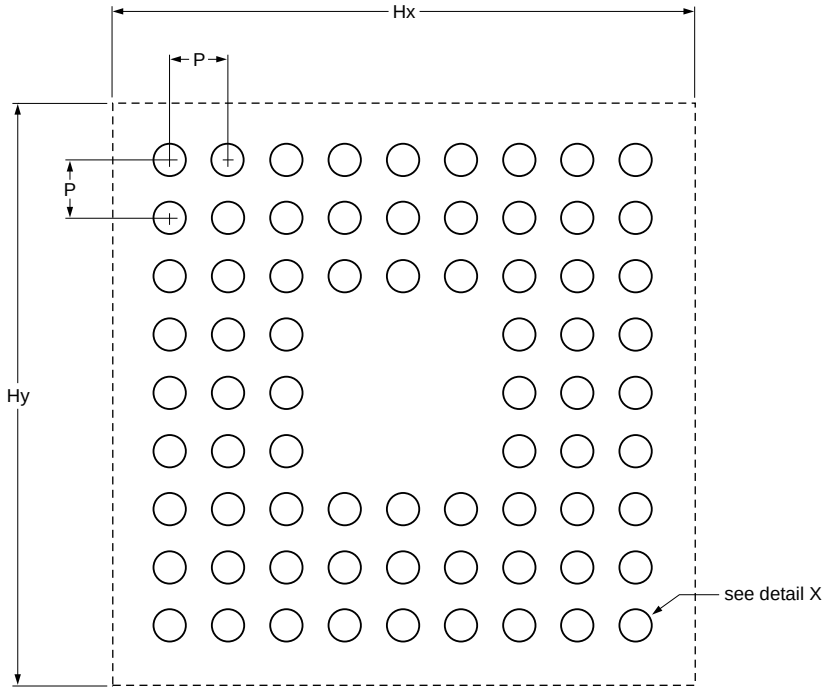
DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

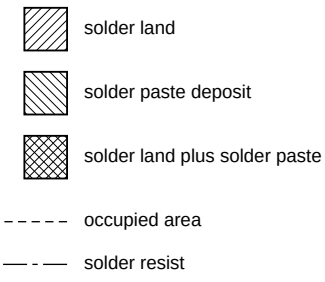
Fig 43. Reflow soldering for the LQFP100 package

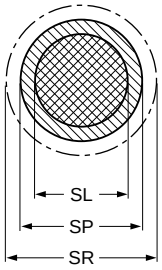
Footprint information for reflow soldering of TFBGA100 package **SOT926-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout





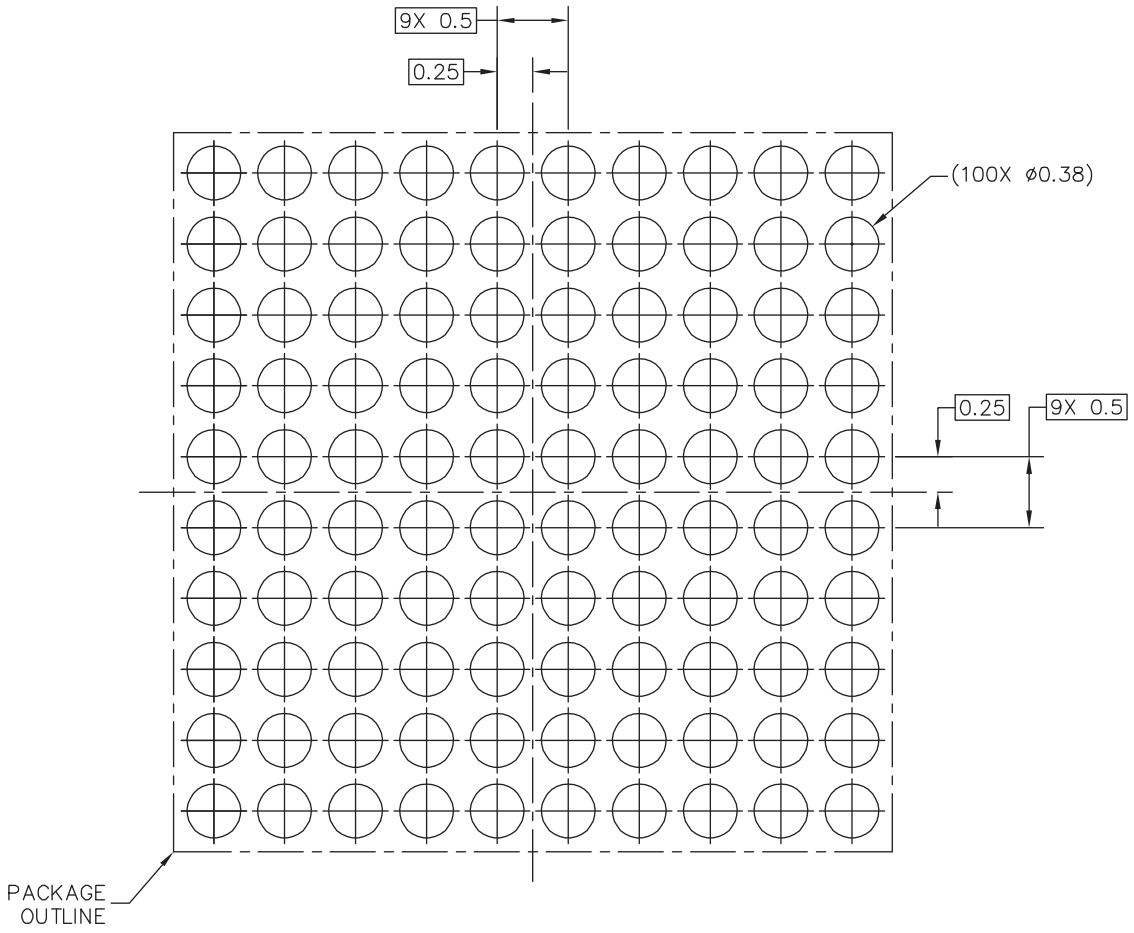
detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.330	0.400	0.480	9.400	9.400

sot926-1_fr

Fig 44. Reflow soldering of the TFBGA100 package



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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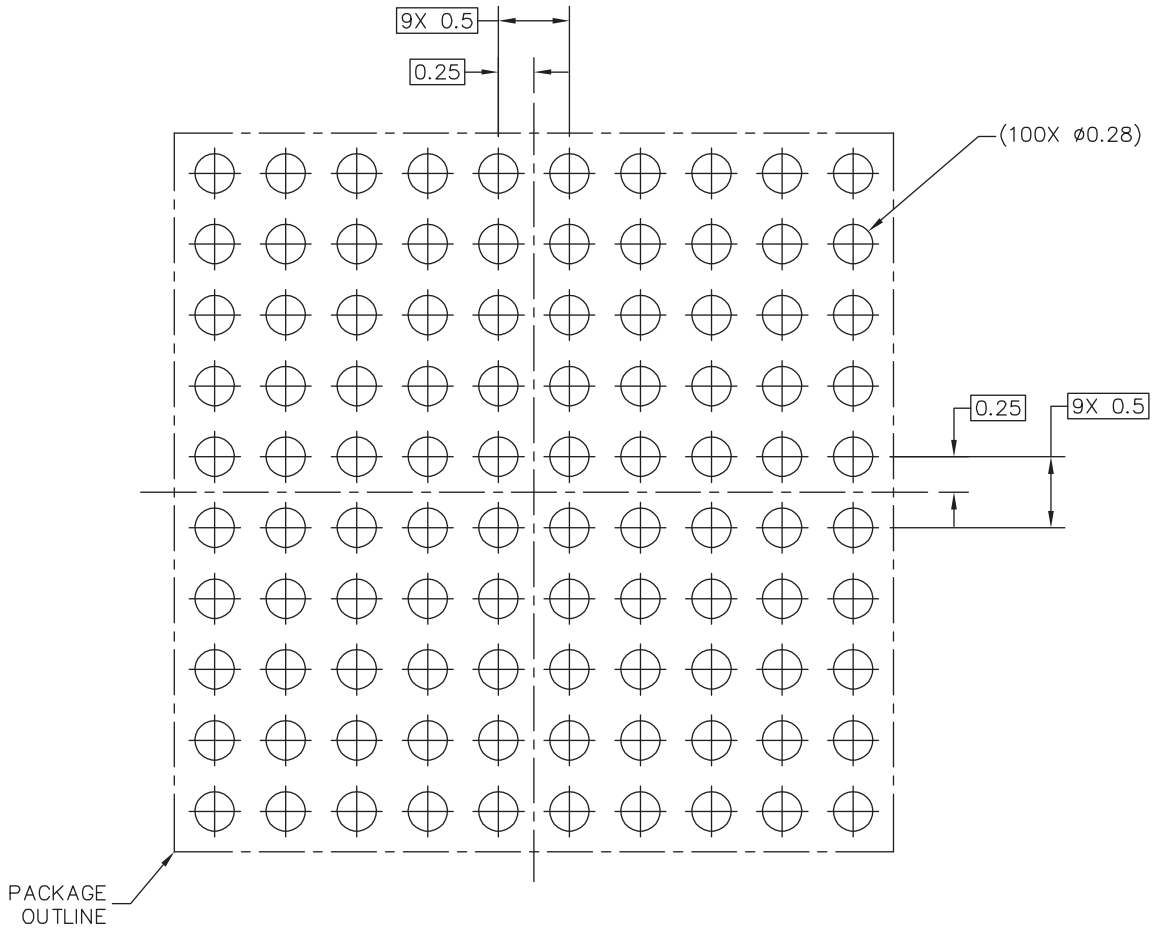
DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450-2	REVISION: 0	

Fig 45. Reflow soldering of the WLCSP100 package (part 1)



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DATE: 06 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1450–2	REVISION: 0	

Fig 46. Reflow soldering of the WLCSP100 package (part 2)

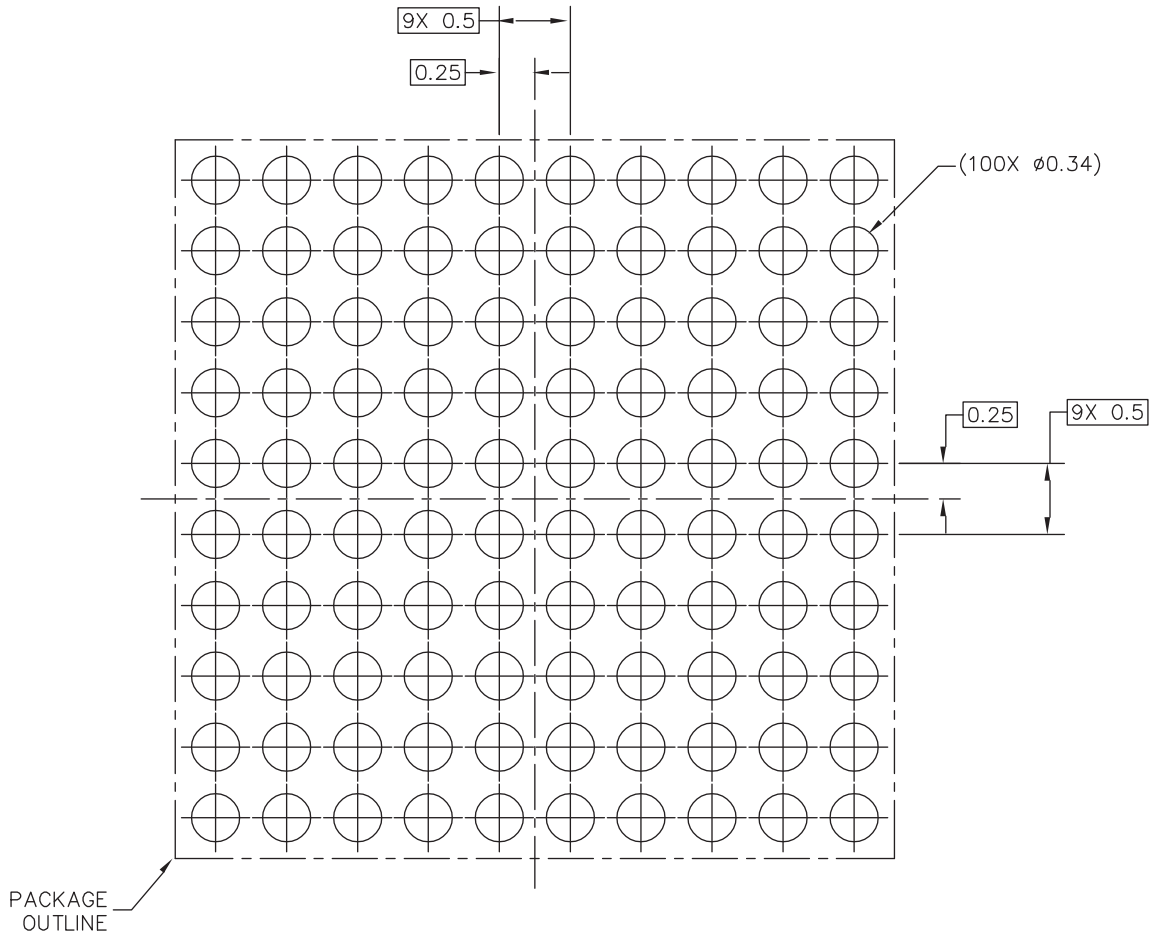

Fig 47. Reflow soldering of the WLCSP100 package (part 3)

18. Abbreviations

Table 26. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RIT	Repetitive Interrupt Timer
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCM	Tightly Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

19. References

[1] LPC176x/5x User manual UM10360:
http://www.nxp.com/documents/user_manual/UM10360.pdf

[2] LPC176x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC176X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

20. Revision history

Table 27. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1769_68_67_66_65_64_63 v.9.10	20200908	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.9
Modifications:	• Added TFBGA100 package to rev C device revision.			
LPC1769_68_67_66_65_64_63 v.9.9	20200317	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.8
Modifications:	• Added device revision C.			
LPC1769_68_67_66_65_64_63 v.9.8	20180504	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.7
Modifications:	• Added Figure 45 “Reflow soldering of the WLCSP100 package (part 1)”, Figure 46 “Reflow soldering of the WLCSP100 package (part 2)”, and Figure 47 “Reflow soldering of the WLCSP100 package (part 3)”.			
LPC1769_68_67_66_65_64_63 v.9.7	20170501	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.6
Modifications:	• Updated Table 2 “Ordering options”: WLCSP100 with body size 100 balls, 5.07 x 5.07 x 0.53mm; was 5.074 x 5.074 x 0.6mm. • Updated Figure 42 “Package outline SOT1450-2 LPC1768UK (WLCSP100)”.			
LPC1769_68_67_66_65_64_63 v.9.6	20150818	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.5
Modifications:	• Changed max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 16 “Dynamic characteristics: SSP pins in SPI mode”. • Updated Section 2 “Features and benefits”: Added Boundary scan Description Language (BSDL) is not available for this device. • Updated Figure 5 “LPC17xx memory map”: APB0 slot 7 (0x4001C000) was "reserved" and changed it to I2C0. • Changed pins for $V_{DD(REG)(3V3)}$ from F4 and F0 to F4 and F10. See Table 5 “Pin description”. • Removed footnote 1: “5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis. This pin is pulled up to a voltage level of 2.3 V to 2.6 V” from TDO/SWO, TCK/SWDCLK, and RTCK, pins. See Table 5 “Pin description”. • Added a column for GPIO pins and device order part number to the ordering options table. See Table 2 “Ordering options”.			
LPC1769_68_67_66_65_64_63 v.9.5	<tbd>	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.4
Modifications:	• SSP timing diagram updated. SSP timing parameters $t_{v(Q)}$, $t_{h(Q)}$, t_{DS}, and t_{DH} added. See Section 12.7 “SSP interface”. • Parameter $T_{j(max)}$ added in Table 6 “Limiting values”. • SSP maximum bit rate in master mode corrected to 33 Mbit/s.			
LPC1769_68_67_66_65_64_63 v.9.4	20140404	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.3
Modifications:	• Added LPC1768UK. • Table 5 “Pin description”: Changed RX_MCLK and TX_MCLK type from INPUT to OUTPUT.			
LPC1769_68_67_66_65_64_63 v.9.3	20140108	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.2
Modifications:	• Table 7 “Thermal resistance (±15 %)”: – Added TFBGA100. – Added ±15 % to table title.			

Table 27. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1769_68_67_66_65_64_63 v.9.2	20131021	Product data sheet	-	LPC1769_68_67_66_65_64 v.9.1
Modifications:	• Table 8 “Static characteristics”: – Added Table note 3 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.” – Added Table note 4 “VDDA for DAC specs are from 2.7 V to 3.6 V.” – V_{DDA}/VREFP spec changed from 2.7 V to 2.5 V. • Table 19 “ADC characteristics (full resolution)”: – Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.” – V_{DDA} changed from 2.7 V to 2.5 V. • Table 20 “ADC characteristics (lower resolution)”: Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”			
LPC1769_68_67_66_65_64_63 v.9.1	20130916	Product data sheet	-	LPC1769_68_67_66_65_64 v.9
Modifications:	• Added Table 7 “Thermal resistance”. • Table 6 “Limiting values”: – Updated min/max values for $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$. – Updated conditions for V_I. – Updated table notes. • Table 8 “Static characteristics”: Added Table note 15 “TCK/SWDCLK pin needs to be externally pulled LOW.” • Updated Section 15.1 “Suggested USB interface solutions”. • Added Section 5 “Marking”. • Changed title of Figure 31 from “USB interface on a self-powered device” to “USB interface with soft-connect”.			
LPC1769_68_67_66_65_64_63 v.9	20120810	Product data sheet	-	LPC1769_68_67_66_65_64 v.8
Modifications:	• Remove table note “The peak current is limited to 25 times the corresponding maximum current.” from Table 5 “Limiting values”. • Change $V_{DD(3V3)}$ to $V_{DD(REG)(3V3)}$ in Section 11.3 “Internal oscillators”. • Glitch filter constant changed to 10 ns in Table note 6 in Table 4. • Description of $\overline{\text{RESET}}$ function updated in Table 4. • Pull-up value added for GPIO pins in Table 4. • Pin configuration diagram for LQFP100 package corrected (Figure 2).			
LPC1769_68_67_66_65_64_63 v.8	20111114	Product data sheet	-	LPC1769_68_67_66_65_64 v.7
Modifications:	• Pin description of USB_UP_LED pin updated in Table 4. • R_{i1} and R_{i2} labels in Figure 27 updated. • Part LPC1765FET100 added. • Table note 10 updated in Table 4. • Table note 1 updated in Table 12. • Pin description of STCLK pin updated in Table 4. • Electromagnetic compatibility data added in Section 14.6. • Section 16 added.			

Table 27. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1769_68_67_66_65_64_63 v.7	20110405	Product data sheet	-	LPC1769_68_67_66_65_64 v.6
Modifications:	• Pin description of pins P0[29] and P0[30] updated in Table note 5 of Table 4. Pins are not 5 V tolerant. • Typical value for Parameter N_{endu} added in Table 9. • Parameter V_{hys} for I^2C bus pins: typical value corrected $V_{hys} = 0.05V_{DD(3V3)}$ in Table 7. • Condition 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V added in Table 16. • Typical values for parameters $I_{DD(REG)(3V3)}$ and I_{BAT} with condition Deep power-down mode corrected in Table 7 and Table note 9, Table note 10, and Table note 11 updated. • For Deep power-down mode, Figure 9 updated and Figure 10 added.			
LPC1769_68_67_66_65_64_63 v.6	20100825	Product data sheet	-	LPC1769_68_67_66_65_64 v.5
Modifications:	• Part LPC1768TFBGA added. • Section 7.30.2; BOD level corrected. • Added Section 10.2.			
LPC1769_68_67_66_65_64_63 v.5	20100716	Product data sheet	-	LPC1769_68_67_66_65_64 v.4
LPC1769_68_67_66_65_64 v.4	20100201	Product data sheet	-	LPC1768_67_66_65_64 v.3
LPC1768_67_66_65_64 v.3	20091119	Product data sheet	-	LPC1768_66_65_64 v.2
LPC1768_66_65_64 v.2	20090211	Objective data sheet	-	LPC1768_66_65_64 v.1
LPC1768_66_65_64 v.1	20090115	Objective data sheet	-	-

21. Legal information

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[2] The term 'short data sheet' is explained in section "Definitions".

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