



**THE DATASHEET OF  
X9400WS24I**



X9400

Low Noise/Low Power/SPI Bus Quad Digitally Controlled Potentiometers (XDCP™)

FN8189  
Rev 4.00  
September 2, 2015

FEATURES

- Four potentiometers per package
- 64 resistor taps
- SPI serial interface for write, read, and transfer operations of the potentiometer
- Wiper resistance, 40Ω typical at 5V.
- Four non-volatile data registers for each potentiometer
- Non-volatile storage of multiple wiper position
- Power-on recall. Loads saved wiper position on power-up.
- Standby current < 1μA max
- System V<sub>CC</sub>: 2.7V to 5.5V operation
- Analog V<sup>+</sup>/V<sup>-</sup>: -5V to +5V
- 10kΩ, 2.5kΩ end to end resistance
- 100 yr. data retention
- Endurance: 100,000 data changes per bit per register
- Low power CMOS
- 24 Ld SOIC and 24 Ld TSSOP
- Pb-free plus anneal available (RoHS compliant)

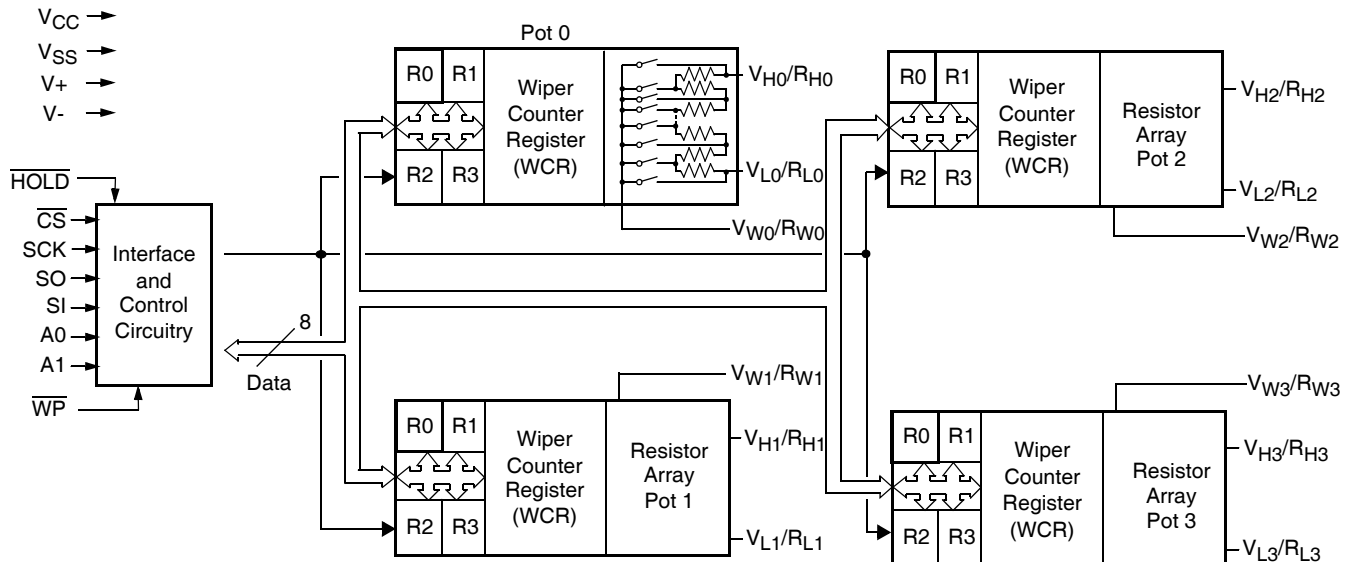
DESCRIPTION

The X9400 integrates four digitally controlled potentiometers (XDCPs) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented using 63 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI serial bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four nonvolatile Data Registers (DR0-3) that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Power-up recalls the contents of DR0 to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

BLOCK DIAGRAM



## Ordering Information

PART NUMBER	PART MARKING	V <sub>CC</sub> LIMITS (V)	POTENTIOMETER ORGANIZATION (k $\Omega$ )	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X9400WS24ZT1 (Note) <b>(No longer available, recommended replacement: X9400WS24IZT1)</b>	X9400WS Z	5 $\pm$ 10%	10	0 to +70	24 Ld SOIC (300 mil) (Pb-free) Tape and Reel	M24.3
X9400WS24IZ* (Note)	X9400WS ZI			-40 to +85	24 Ld SOIC (300 mil) (Pb-free)	M24.3
X9400WV24IZ* (Note)	X9400WV ZI			-40 to +85	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
X9400WV24Z* (Note) <b>(No longer available, recommended replacement: X9400WS24IZT1)</b>	X9400WV Z			0 to +70	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
X9400WS24IZ-2.7* (Note)	X9400WS ZG	2.7 to 5.5		-40 to +85	24 Ld SOIC (300 mil) (Pb-free)	M24.3
X9400WV24IZ-2.7* (Note) <b>(No longer available, recommended replacement: X9400WS24IZT1)</b>	X9400WV ZG			-40 to +85	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
X9400WV24Z-2.7* (Note) <b>(No longer available, recommended replacement: X9400WS24IZT1)</b>	X9400WV ZF			0 to +70	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044

\*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## PIN DESCRIPTIONS

### Host Interface Pins

#### Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

#### Serial Input

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

#### Serial Clock (SCK)

The SCK input is used to clock data into and out of the X9400.

#### Chip Select ( $\overline{CS}$ )

When  $\overline{CS}$  is HIGH, the X9400 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state.  $\overline{CS}$  LOW enables the X9400, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on  $\overline{CS}$  is required prior to the start of any operation.

#### Hold (HOLD)

$\overline{HOLD}$  is used in conjunction with the  $\overline{CS}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{HOLD}$  may be used to pause the serial communication with the controller without resetting

the serial sequence. To pause,  $\overline{HOLD}$  must be brought LOW while SCK is LOW. To resume communication,  $\overline{HOLD}$  is brought HIGH, again while SCK is LOW. If the pause feature is not used,  $\overline{HOLD}$  should be held HIGH at all times.

#### Device Address ( $A_0 - A_1$ )

The address inputs are used to set the least significant 2 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9400. A maximum of 4 devices may occupy the SPI serial bus.

#### Potentiometer Pins

##### $V_H/R_H$ ( $V_{H0}/R_{H0} - V_{H3}/R_{H3}$ ), $V_L/R_L$ ( $V_{L0}/R_{L0} - V_{L3}/R_{L3}$ )

The  $V_H/R_H$  and  $V_L/R_L$  inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

##### $V_W/R_W$ ( $V_{W0}/R_{W0} - V_{W3}/R_{W3}$ )

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

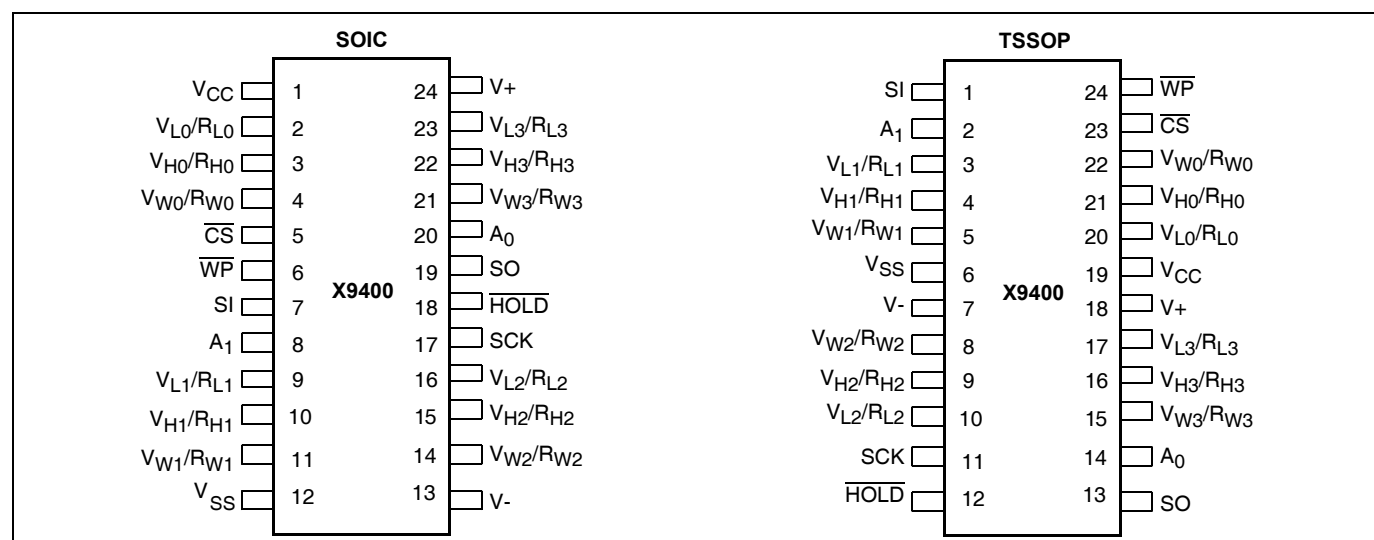
#### Hardware Write Protect Input ( $\overline{WP}$ )

The  $\overline{WP}$  pin when LOW prevents nonvolatile writes to the Data Registers.

#### Analog Supplies ( $V+$ , $V-$ )

The analog Supplies  $V+$ ,  $V-$  are the supply voltages for the XDCP analog section.

## PIN CONFIGURATION



**PIN NAMES**

Symbol	Description
SCK	Serial Clock
SI, SO	Serial Data
A <sub>0</sub> - A <sub>1</sub>	Device Address
V <sub>H0</sub> /R <sub>H0</sub> - V <sub>H3</sub> /R <sub>H3</sub> , V <sub>L0</sub> /R <sub>L0</sub> - V <sub>L3</sub> /R <sub>L3</sub>	Potentiometer Pins (terminal equivalent)
V <sub>W0</sub> /R <sub>W0</sub> - V <sub>W1</sub> /R <sub>W1</sub>	Potentiometer Pins (wiper equivalent)
$\overline{\text{WP}}$	Hardware Write Protection
V <sub>CC</sub>	System Supply Voltage
V <sub>SS</sub>	System Ground
NC	No Connection

**DEVICE DESCRIPTION**

The X9400 is a highly integrated microcircuit incorporating four resistor arrays and their associated registers and counters and the serial interface logic providing direct communication between the host and the XDCP potentiometers.

**Serial Interface**

The X9400 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK.  $\overline{\text{CS}}$  must be LOW and the  $\overline{\text{HOLD}}$  and  $\overline{\text{WP}}$  pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

**Array Description**

The X9400 is comprised of four resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V<sub>H</sub>/R<sub>H</sub> and V<sub>L</sub>/R<sub>L</sub> inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (V<sub>W</sub>/R<sub>W</sub>) output. Within each individual array only one switch may be turned on at a time.

These switches are controlled by a wiper counter register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

**Wiper Counter Register (WCR)**

The X9400 contains four Wiper Counter Registers, one for each XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register or global XFR data register instructions (parallel load); it can be modified one step at a time by the increment/decrement instruction. Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9400 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down.

**Data Registers**

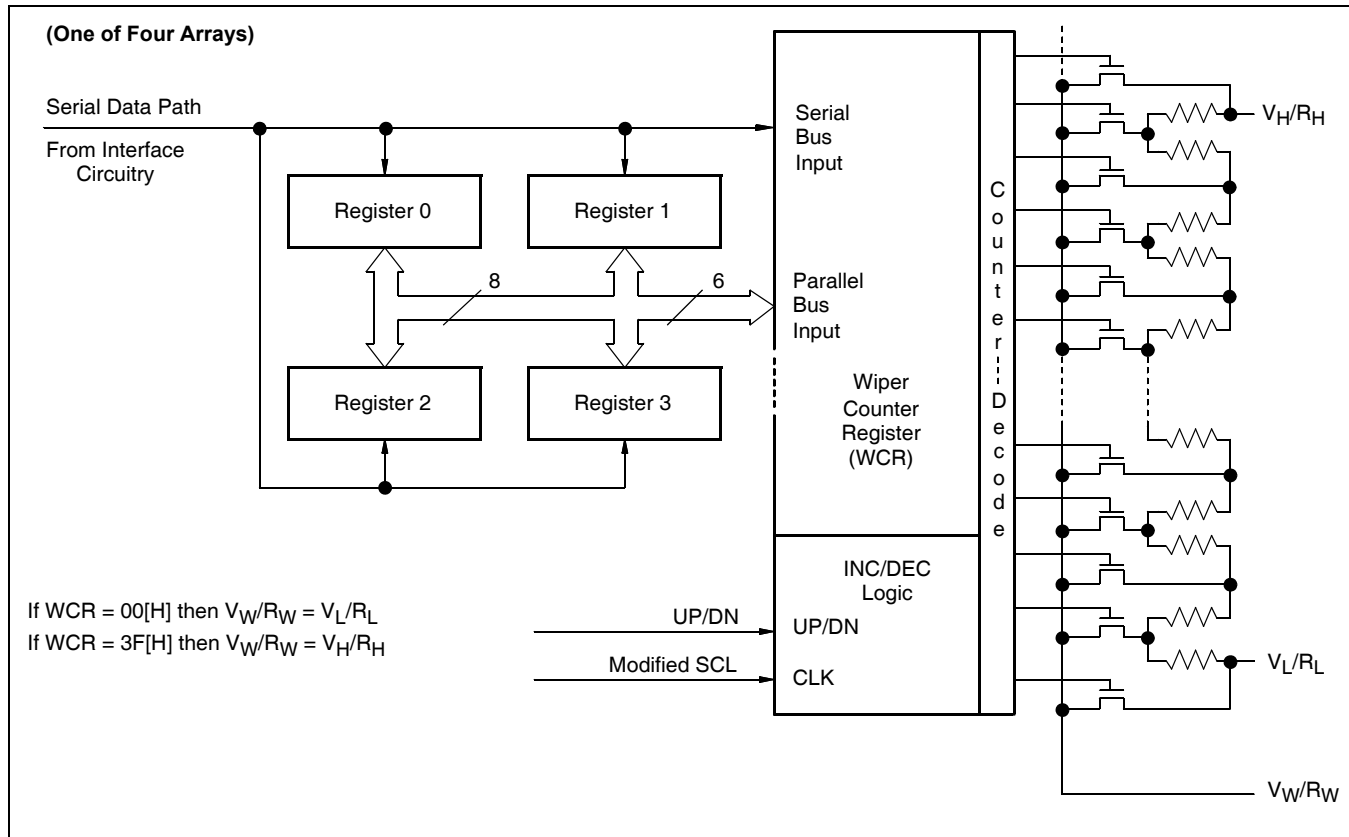
Each potentiometer has four 6-bit nonvolatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the data registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

**Data Register Detail**

(MSB)				(LSB)	
D5	D4	D3	D2	D1	D0
NV	NV	NV	NV	NV	NV

**Figure 1. Detailed Potentiometer Block Diagram**



**Write in Process**

The contents of the Data Registers are saved to nonvolatile memory when the CS pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by a write in process bit (WIP). The WIP bit is read with a read status command.

**INSTRUCTIONS**

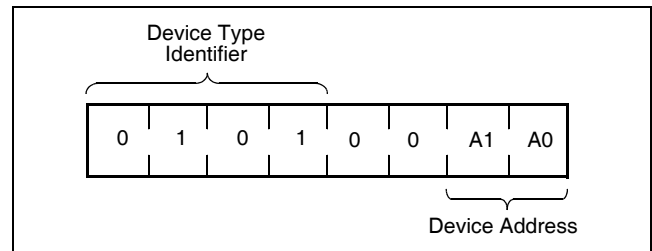
**Identification (ID) Byte**

The first byte sent to the X9400 from the host, following a CS going HIGH to LOW, is called the Identification byte. The most significant four bits of the slave address are a device type identifier, for the X9400 this is fixed as 0101[B] (refer to Figure 2).

The two least significant bits in the ID byte select one of four devices on the bus. The physical device address is defined by the state of the A<sub>0</sub> - A<sub>1</sub> input pins. The X9400 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9400 to successfully continue the command sequence. The A<sub>0</sub> - A<sub>1</sub> inputs can be actively driven by CMOS input signals or tied to V<sub>CC</sub> or V<sub>SS</sub>.

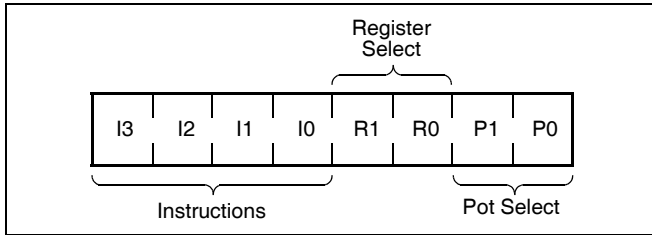
The remaining two bits in the slave byte must be set to 0.

**Figure 2. Identification Byte Format**



**Instruction Byte**

The next byte sent to the X9400 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of the four pots and, when applicable, they point to one of four associated registers. The format is shown below in Figure 3.

**Figure 3. Instruction Byte Format**

The four high order bits of the instruction byte specify the operation. The next two bits ( $R_1$  and  $R_0$ ) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last two bits ( $P_1$  and  $P_0$ ) selects which one of the four potentiometers is to be affected by the instruction.

Four of the ten instructions are two bytes in length and end with the transmission of the instruction byte. These instructions are:

- XFR Data Register to Wiper Counter Register—This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- XFR Wiper Counter Register to Data Register —This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.
- Global XFR Data Register to Wiper Counter Register — This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.
- Global XFR Wiper Counter Register to Data Register — This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

The basic sequence of the two byte instructions is illustrated in Figure 4. These two-byte instructions exchange data between the WCR and one of the data registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by  $t_{WRL}$ . A transfer from the WCR (current wiper position), to a data register is a write to nonvolatile memory and takes a minimum of  $t_{WR}$  to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, where the transfer occurs between all potentiometers and one associated register.

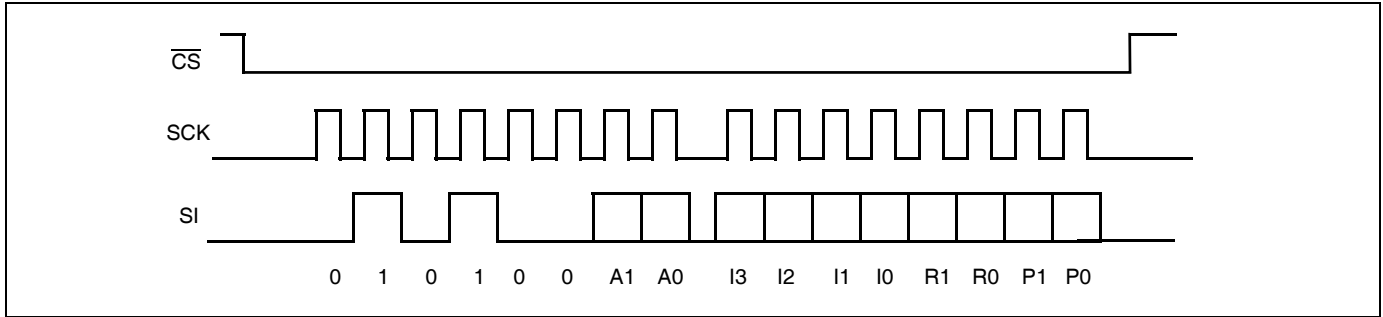
Five instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9400; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

- Read Wiper Counter Register—read the current wiper position of the selected pot,
- Write Wiper Counter Register—change current wiper position of the selected pot,
- Read Data Register—read the contents of the selected data register;
- Write Data Register—write a new value to the selected data register.
- Read Status—This command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

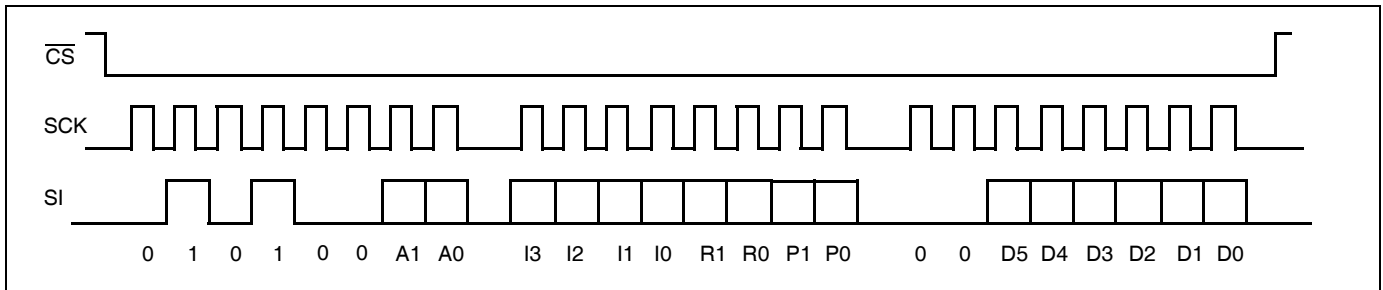
The sequence of these operations is shown in Figure 5 and Figure 6.

The final command is Increment/Decrement. It is different from the other commands, because it's length is indeterminate. Once the command is issued, the master can clock the selected wiper up and/or down in one resistor segment steps; thereby, providing a fine tuning capability to the host. For each SCK clock pulse ( $t_{HIGH}$ ) while SI is HIGH, the selected wiper will move one resistor segment towards the  $V_H/R_H$  terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the  $V_L/R_L$  terminal. A detailed illustration of the sequence and timing for this operation are shown in Figure 7 and Figure 8.

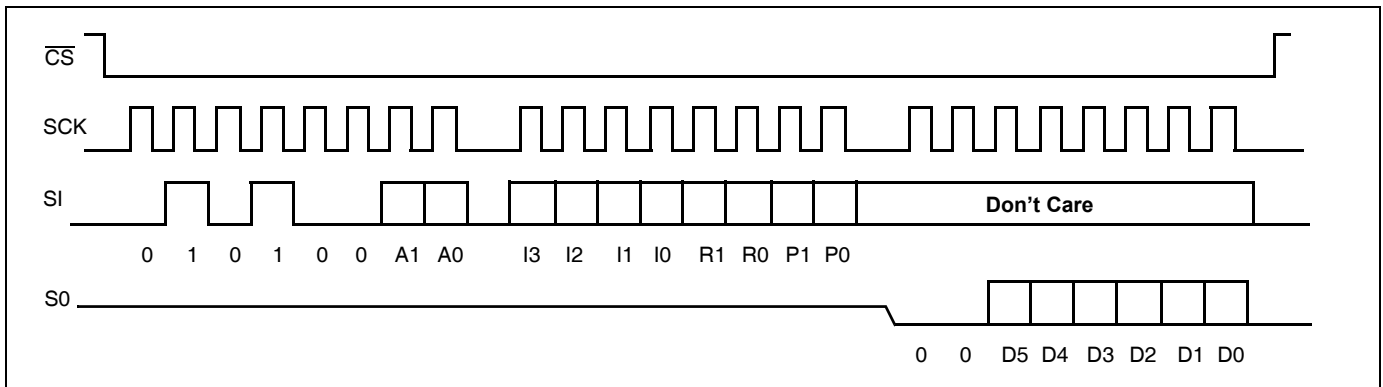
**Figure 4. Two-Byte Instruction Sequence**



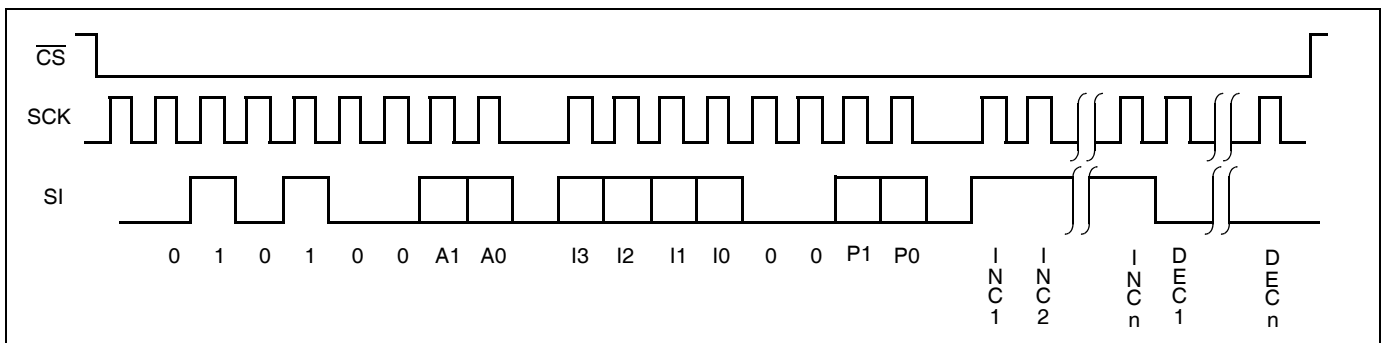
**Figure 5. Three-Byte Instruction Sequence (Write)**



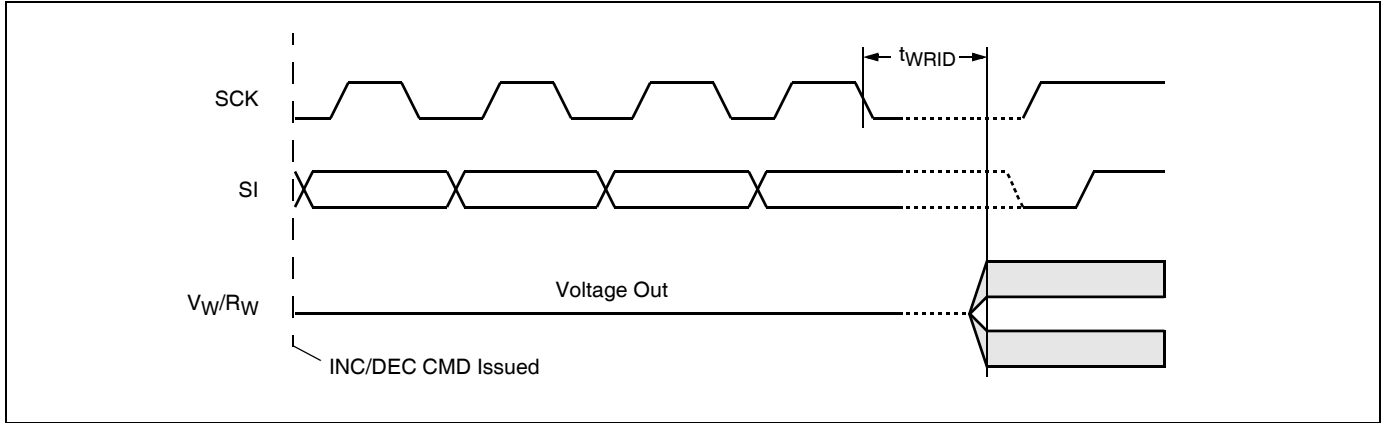
**Figure 6. Three-Byte Instruction Sequence (Read)**



**Figure 7. Increment/Decrement Instruction Sequence**



**Figure 8. Increment/Decrement Timing Limits**



**Table 1. Instruction Set**

Instruction	Instruction Set								Operation
	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	R <sub>1</sub>	R <sub>0</sub>	P <sub>1</sub>	P <sub>0</sub>	
Read Wiper Counter Register	1	0	0	1	0	0	P <sub>1</sub>	P <sub>0</sub>	Read the contents of the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub>
Write Wiper Counter Register	1	0	1	0	0	0	P <sub>1</sub>	P <sub>0</sub>	Write new value to the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub>
Read Data Register	1	0	1	1	R <sub>1</sub>	R <sub>0</sub>	P <sub>1</sub>	P <sub>0</sub>	Read the contents of the Data Register pointed to by P <sub>1</sub> - P <sub>0</sub> and R <sub>1</sub> - R <sub>0</sub>
Write Data Register	1	1	0	0	R <sub>1</sub>	R <sub>0</sub>	P <sub>1</sub>	P <sub>0</sub>	Write new value to the Data Register pointed to by P <sub>1</sub> - P <sub>0</sub> and R <sub>1</sub> - R <sub>0</sub>
XFR Data Register to Wiper Counter Register	1	1	0	1	R <sub>1</sub>	R <sub>0</sub>	P <sub>1</sub>	P <sub>0</sub>	Transfer the contents of the Data Register pointed to by R <sub>1</sub> - R <sub>0</sub> to the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub>
XFR Wiper Counter Register to Data Register	1	1	1	0	R <sub>1</sub>	R <sub>0</sub>	P <sub>1</sub>	P <sub>0</sub>	Transfer the contents of the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub> to the Register pointed to by R <sub>1</sub> - R <sub>0</sub>
Global XFR Data Register to Wiper Counter Register	0	0	0	1	R <sub>1</sub>	R <sub>0</sub>	0	0	Transfer the contents of the Data Registers pointed to by R <sub>1</sub> - R <sub>0</sub> of all four pots to their respective Wiper Counter Register
Global XFR Wiper Counter Register to Data Register	1	0	0	0	R <sub>1</sub>	R <sub>0</sub>	0	0	Transfer the contents of all Wiper Counter Registers to their respective data Registers pointed to by R <sub>1</sub> - R <sub>0</sub> of all four pots
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	P <sub>1</sub>	P <sub>0</sub>	Enable Increment/decrement of the Wiper Counter Register pointed to by P <sub>1</sub> - P <sub>0</sub>
Read Status (WIP bit)	0	1	0	1	0	0	0	1	Read the status of the internal write cycle, by checking the WIP bit.

**Instruction Format**

- Notes:** (1) "A1 ~ A0": stands for the device addresses sent by the master.  
 (2) WPx refers to wiper position data in the Counter Register  
 (3) "I": stands for the increment operation, SI held HIGH during active SCK phase (high).  
 (4) "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

**Read Wiper Counter Register (WCR)**

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				wiper position (sent by X9400 on SO)						$\overline{CS}$ Rising Edge		
	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	P1	P0	0	0	W5	W4	W3	W2		W1	W0
	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	P1	P0	0	0	W5	W4	W3	W2	W1	W0	

**Write Wiper Counter Register (WCR)**

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				Data Byte (sent by Host on SI)						$\overline{CS}$ Rising Edge		
	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	P1	P0	0	0	W5	W4	W3	W2		W1	W0
	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	P1	P0	0	0	W5	W4	W3	W2	W1	W0	

**Read Data Register (DR)**

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR and WCR addresses				Data Byte (sent by X9400 on SO)						$\overline{CS}$ Rising Edge		
	0	1	0	1	0	0	A1	A0	1	0	1	1	R1	R0	P1	P0	0	0	W5	W4	W3	W2		W1	W0
	0	1	0	1	0	0	A1	A0	1	0	1	1	R1	R0	P1	P0	0	0	W5	W4	W3	W2	W1	W0	

**Write Data Register (DR)**

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR and WCR addresses				Data Byte (sent by host on SI)						$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE		
	0	1	0	1	0	0	A1	A0	1	1	0	0	R1	R0	P1	P0	0	0	W5	W4	W3	W2			W1	W0
	0	1	0	1	0	0	A1	A0	1	1	0	0	R1	R0	P1	P0	0	0	W5	W4	W3	W2	W1	W0		

**Transfer Data Register (DR) to Wiper Counter Register (WCR)**

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR and WCR addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	1	0	1	R1	R0	P1	P0	
	0	1	0	1	0	0	A1	A0	1	1	0	1	R1	R0	P1	P0	

**Transfer Wiper Counter Register (WCR) to Data Register (DR)**

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR and WCR addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	1	0	R1	R0	P1	P0		
	0	1	0	1	0	0	A1	A0	1	1	1	0	R1	R0	P1	P0		



**ABSOLUTE MAXIMUM RATINGS**

Temperature under bias .....	-65°C to +135°C
Storage temperature .....	-65°C to +150°C
Voltage on SCK, SCL or any address input with respect to $V_{SS}$ .....	-1V to +7V
Voltage on V+ (referenced to $V_{SS}$ ) .....	10V
Voltage on V- (referenced to $V_{SS}$ ) .....	-10V
(V+) - (V-) .....	12V
Any $V_H$ .....	V+
Any $V_L$ .....	V-
Lead temperature (soldering, 10 seconds) .....	300°C
$I_W$ (10 seconds) .....	±12mA

**COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

Device	Supply Voltage ( $V_{CC}$ ) Limits
X9400	5V ± 10%
X9400-2.7	2.7V to 5.5V

**ANALOG CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
$R_{TOTAL}$	End to end resistance			±20	%	
	Power rating			50	mW	25°C, each pot
$I_W$	Wiper current			±6	mA	
$R_W$	Wiper resistance		150	250	Ω	Wiper Current = ± 1mA, $V_{CC} = 3V$
			40	100	Ω	Wiper Current = ± 1mA, $V_{CC} = 5V$
$V_{v+}$	Voltage on V+ Pin	X9400	+4.5	+5.5	V	
		X9400-2.7	+2.7	+5.5		
$V_{v-}$	Voltage on V- Pin	X9400	-5.5	-4.5	V	
		X9400-2.7	-5.5	-2.7		
$V_{TERM}$	Voltage on any $V_H/R_H$ or $V_L/R_L$ Pin	V-		V+	V	
	Noise		-120		dBV	Ref: 1kHz
	Resolution		1.6		%	
	Absolute linearity <sup>(1)</sup>	-1		+1	MI <sup>(3)</sup>	$R_{W(n)}(actual) - R_{W(n)}(expected)$
	Relative linearity <sup>(2)</sup>	-0.2		+0.2	MI <sup>(3)</sup>	$R_{W(n+1)} - [R_{W(n)} + MI]$
	Temperature coefficient of $R_{TOTAL}$		±300		ppm/°C	
	Ratiometric temp. coefficient			±20	ppm/°C	
$C_H/C_L/C_W$	Potentiometer capacitances		10/10/25		pF	See Spice Macromodel
$I_{AL}$	$R_H, R_L, R_W$ leakage current		0.1	10	μA	$V_{IN} = V_{SS}$ to $V_{CC}$ . Device is in stand-by mode.

- Notes:** (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.  
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.  
(3) MI =  $R_{TOT}/63$  or  $(R_H - R_L)/63$ , single pot

**D.C. OPERATING CHARACTERISTICS** (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> supply current (Active)			400	μA	f <sub>SCK</sub> = 2MHz, SO = Open, Other Inputs = V <sub>SS</sub>
I <sub>CC2</sub>	V <sub>CC</sub> supply current (Nonvolatile Write)			1	mA	f <sub>SCK</sub> = 2MHz, SO = Open, Other Inputs = V <sub>SS</sub>
I <sub>SB</sub>	V <sub>CC</sub> current (standby)			1	μA	SCK = SI = V <sub>SS</sub> , Addr. = V <sub>SS</sub>
I <sub>LI</sub>	Input leakage current			10	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>LO</sub>	Output leakage current			10	μA	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>
V <sub>IH</sub>	Input HIGH voltage	V <sub>CC</sub> × 0.7		V <sub>CC</sub> + 0.5	V	
V <sub>IL</sub>	Input LOW voltage	-0.5		V <sub>CC</sub> × 0.1	V	
V <sub>OL</sub>	Output LOW voltage			0.4	V	I <sub>OL</sub> = 3mA

**ENDURANCE AND DATA RETENTION**

Parameter	Min.	Unit
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	years

**CAPACITANCE**

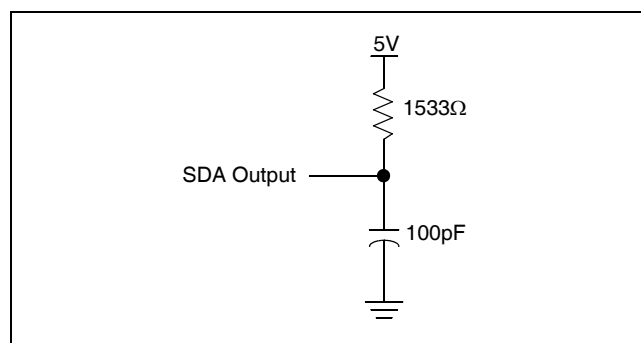
Symbol	Test	Max.	Unit	Test Conditions
C <sub>OUT</sub> <sup>(4)</sup>	Output capacitance (SO)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> <sup>(4)</sup>	Input capacitance (A0, A1, SI, and SCK)	6	pF	V <sub>IN</sub> = 0V

**POWER-UP TIMING**

Symbol	Parameter	Min.	Max.	Unit
t <sub>PUR</sub> <sup>(5)</sup>	Power-up to initiation of read operation		1	ms
t <sub>PUW</sub> <sup>(5)</sup>	Power-up to initiation of write operation		5	ms
t <sub>R V<sub>CC</sub></sub> <sup>(4)</sup>	V <sub>CC</sub> Power-up ramp	0.2	50	V/msec

**POWER-UP REQUIREMENTS** (Power-up sequencing can affect correct recall of the wiper registers)

The preferred power-on sequence is as follows: First V<sub>CC</sub>, then the potentiometer pins, R<sub>H</sub>, R<sub>L</sub>, and R<sub>W</sub>. Voltage should not be applied to the potentiometer pins before V<sub>+</sub> or V<sub>-</sub> is applied. The V<sub>CC</sub> ramp rate specification should be met, and any glitches or slope changes in the V<sub>CC</sub> line should be held to <100mV if possible. If V<sub>CC</sub> powers down, it should be held below 0.1V for more than 1 second before powering up again in order for proper wiper register recall. Also, V<sub>CC</sub> should not reverse polarity by more than 0.5V. Recall of wiper position will not be complete until V<sub>CC</sub>, V<sub>+</sub> and V<sub>-</sub> reach their final value.

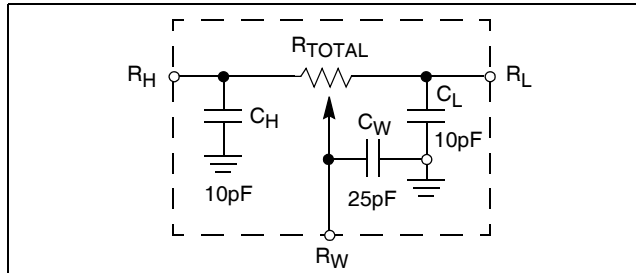
**EQUIVALENT A.C. LOAD CIRCUIT**

## A.C. TEST CONDITIONS

Input pulse levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input rise and fall times	10ns
Input and output timing level	$V_{CC} \times 0.5$

**Notes:** (4) This parameter is periodically sampled and not 100% tested  
 (5)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time the third (last) power supply ( $V_{CC}$ ,  $V+$  or  $V-$ ) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

## SPICE Macro Model



## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

## AC TIMING

Symbol	Parameter	Min.	Max.	Unit
$f_{SCK}$	SSI/SPI clock frequency		2.0	MHz
$t_{CYC}$	SSI/SPI clock cycle time	500		ns
$t_{WH}$	SSI/SPI clock high time	200		ns
$t_{WL}$	SSI/SPI clock low time	200		ns
$t_{LEAD}$	Lead time	250		ns
$t_{LAG}$	Lag time	250		ns
$t_{SU}$	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input setup time	50		ns
$t_H$	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input hold time	50		ns
$t_{RI}$	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input rise time		2	$\mu$ s
$t_{FI}$	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input fall time		2	$\mu$ s
$t_{DIS}$	SO output disable time	0	500	ns
$t_V$	SO output valid time		100	ns
$t_{HO}$	SO output hold time	0		ns
$t_{RO}$	SO output rise time		50	ns
$t_{FO}$	SO output fall time		50	ns
$t_{HOLD}$	$\overline{HOLD}$ time	400		ns
$t_{HSU}$	$\overline{HOLD}$ setup time	100		ns
$t_{HH}$	$\overline{HOLD}$ hold time	100		ns
$t_{HZ}$	$\overline{HOLD}$ low to output in High Z		100	ns
$t_{LZ}$	$\overline{HOLD}$ high to output in Low Z		100	ns
$T_I$	Noise suppression time constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs		20	ns
$t_{CS}$	$\overline{CS}$ deselect time	2		$\mu$ s
$t_{WPASU}$	$\overline{WP}$ , A0 and A1 setup time	0		ns
$t_{WPAH}$	$\overline{WP}$ , A0 and A1 hold time	0		ns

**HIGH-VOLTAGE WRITE CYCLE TIMING**

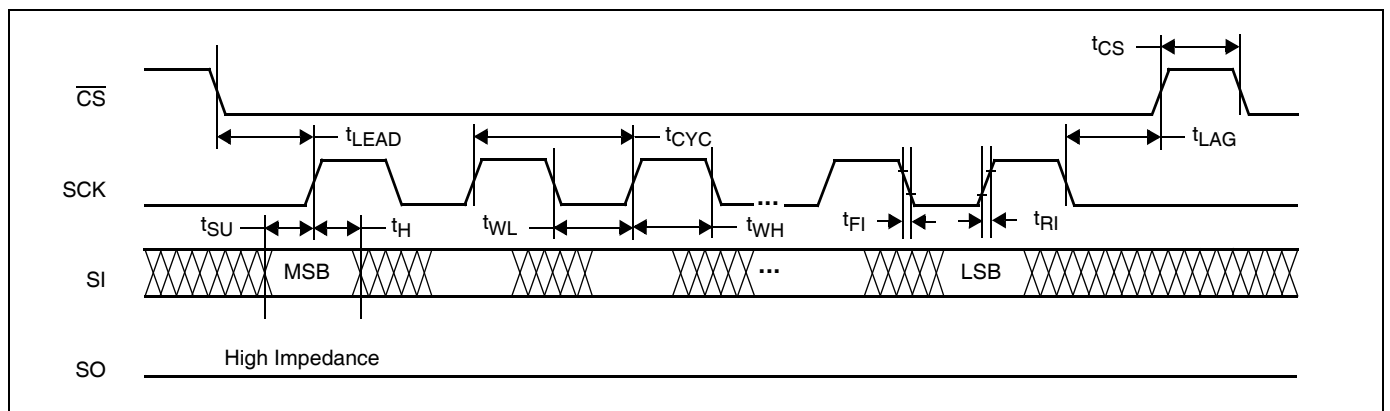
Symbol	Parameter	Typ.	Max.	Unit
$t_{WR}$	High-voltage write cycle time (store instructions)	5	10	ms

**XDCP TIMING**

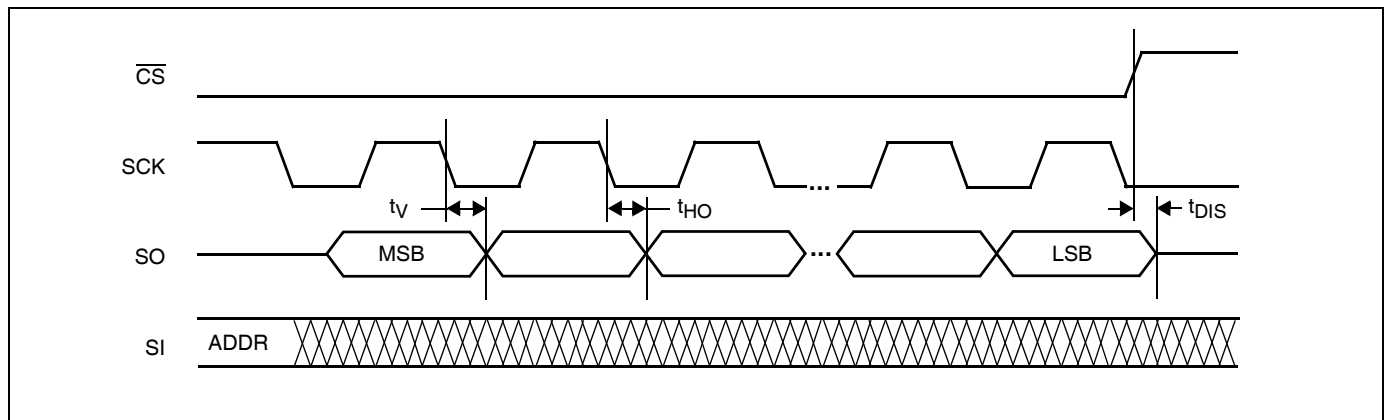
Symbol	Parameter	Min.	Max.	Unit
$t_{WRPO}$	Wiper response time after the third (last) power supply is stable		10	$\mu$ s
$t_{WRL}$	Wiper response time after instruction issued (all load instructions)		10	$\mu$ s
$t_{WRID}$	Wiper response time from an active SCL/SCK edge (increment/decrement instruction)		450	ns

**TIMING DIAGRAMS**

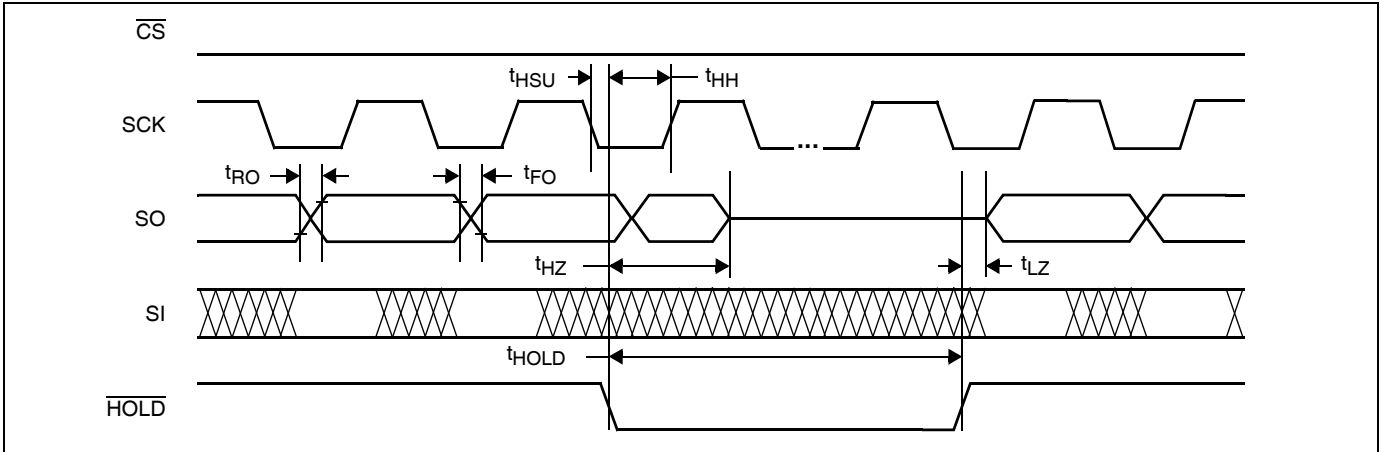
**Input Timing**



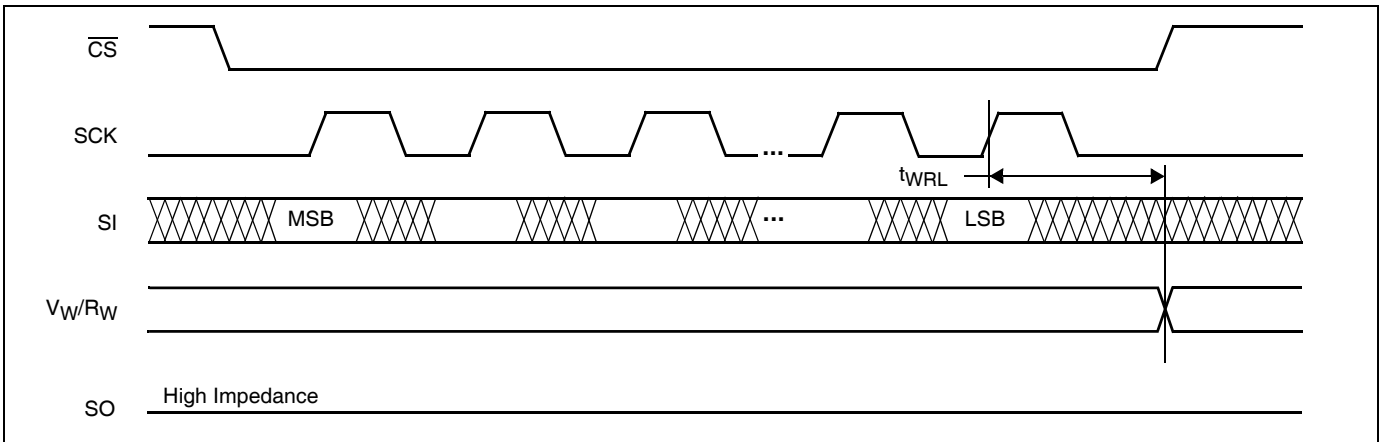
**Output Timing**



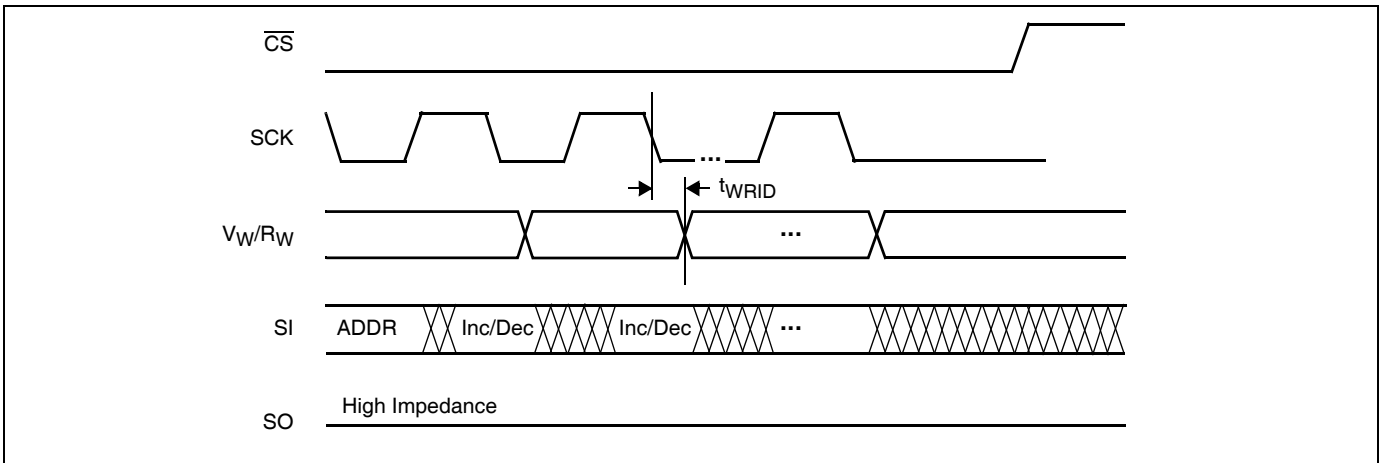
**Hold Timing**



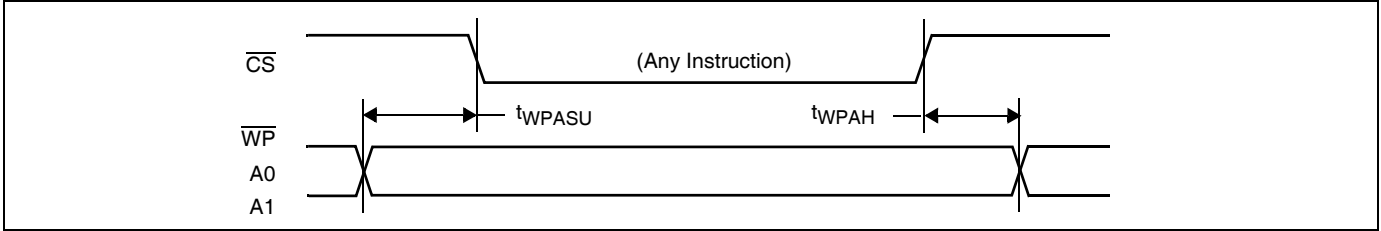
**XDCP Timing (for All Load Instructions)**



**XDCP Timing (for Increment/Decrement Instruction)**

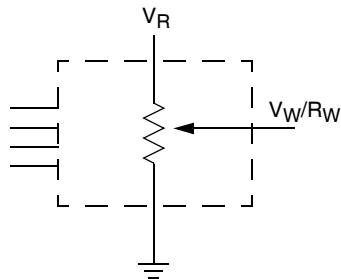


**Write Protect and Device Address Pins Timing**

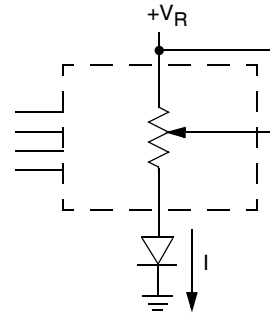


**APPLICATIONS INFORMATION**

**Basic Configurations of Electronic Potentiometers**



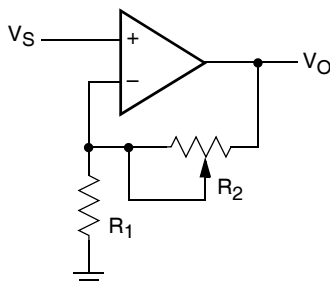
Three terminal Potentiometer;  
Variable voltage divider



Two terminal Variable Resistor;  
Variable current

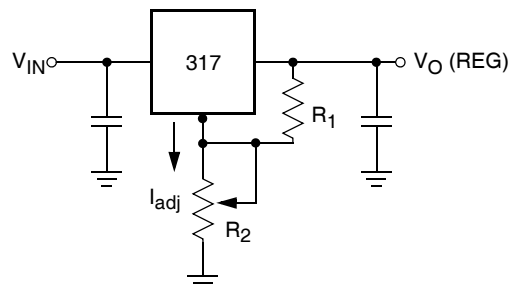
**Application Circuits**

**Noninverting Amplifier**



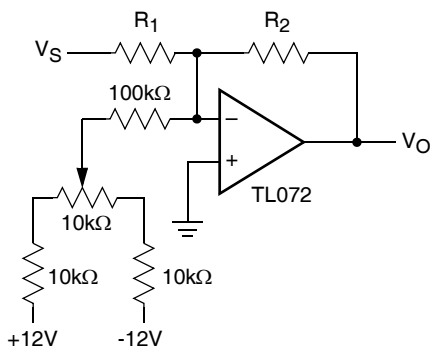
$$V_O = (1 + R_2/R_1) V_S$$

**Voltage Regulator**

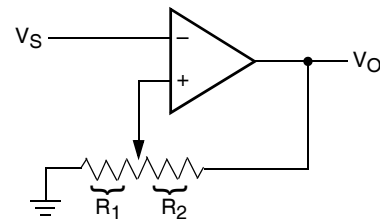


$$V_O (\text{REG}) = 1.25V (1 + R_2/R_1) + I_{\text{adj}} R_2$$

**Offset Voltage Adjustment**



**Comparator with Hysteresis**

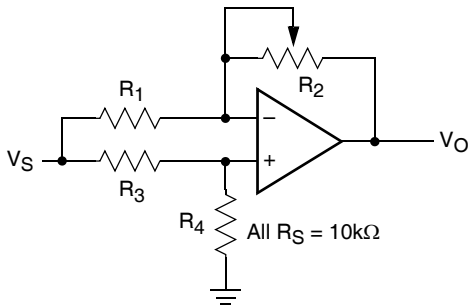


$$V_{UL} = \{R_1/(R_1 + R_2)\} V_O(\text{max})$$

$$V_{LL} = \{R_1/(R_1 + R_2)\} V_O(\text{min})$$

Application Circuits (continued)

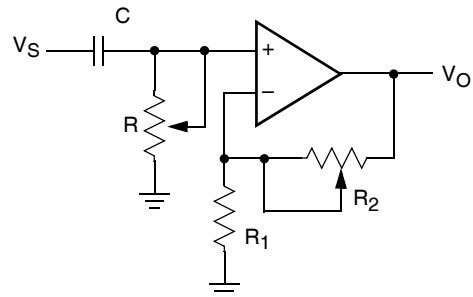
Attenuator



$$V_O = G V_S$$

$$-1/2 \leq G \leq +1/2$$

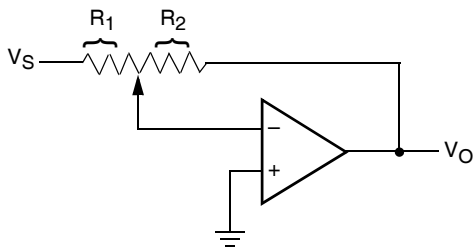
Filter



$$G_O = 1 + R_2/R_1$$

$$f_c = 1/(2\pi RC)$$

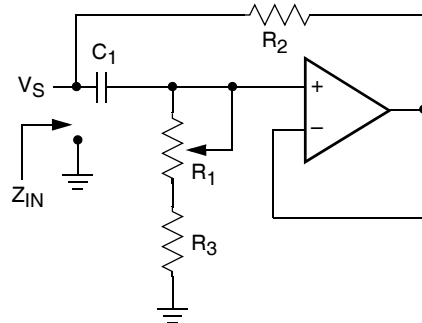
Inverting Amplifier



$$V_O = G V_S$$

$$G = -R_2/R_1$$

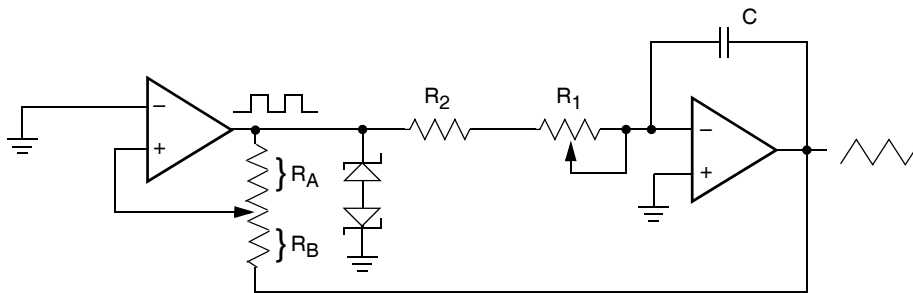
Equivalent L-R Circuit



$$Z_{IN} = R_2 + s R_2 (R_1 + R_3) C_1 = R_2 + s L_{eq}$$

$$(R_1 + R_3) \gg R_2$$

Function Generator



$$\text{frequency} \propto R_1, R_2, C$$

$$\text{amplitude} \propto R_A, R_B$$

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 2, 2015	FN8189.4	Updated Ordering Information Table on page 2. Added Revision History and About Intersil sections. Updated POD M24.3 from rev 1 to rev 2. Changes since rev 1: Updated to new POD standard by removing table listing dimensions and putting dimensions on drawing. Added Land Pattern. Updated POD MDP004 from rev E to rev F. Changes since rev E: Added dimensions (MILLIMETERS) to table column heading.

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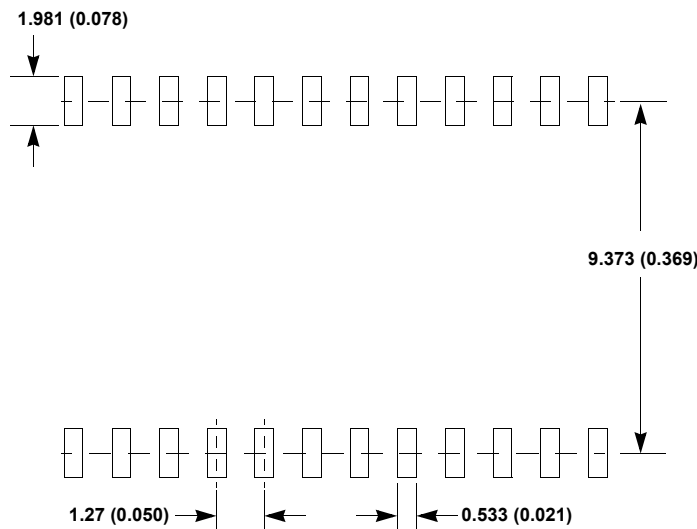
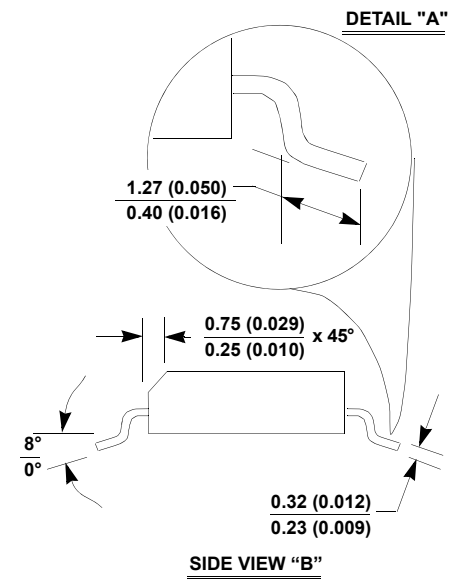
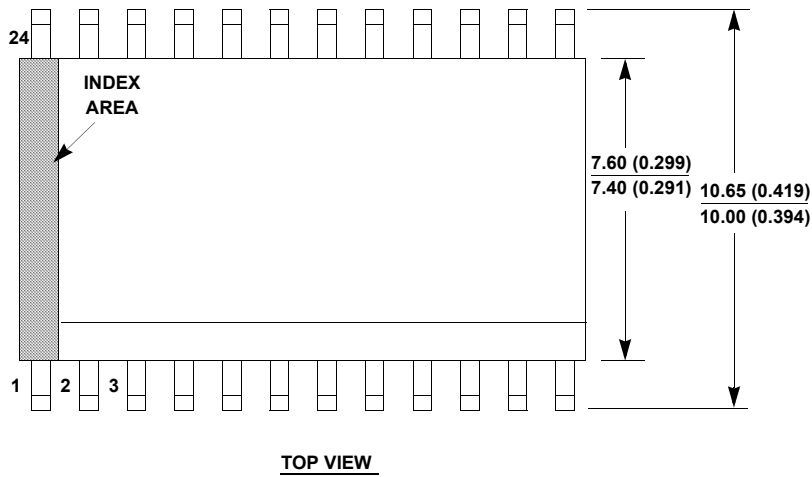
For information regarding Intersil Corporation and its products, see

# Package Outline Drawing

## M24.3

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)

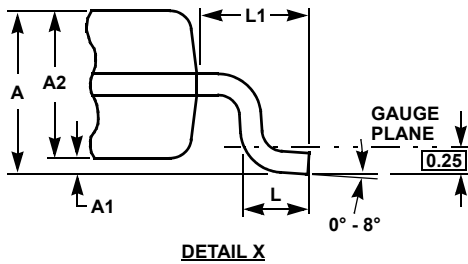
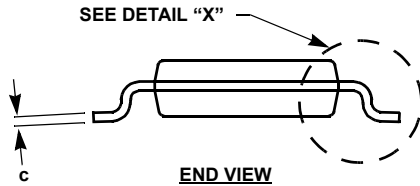
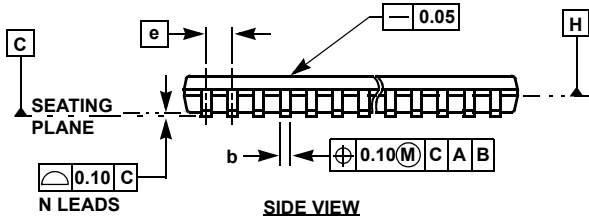
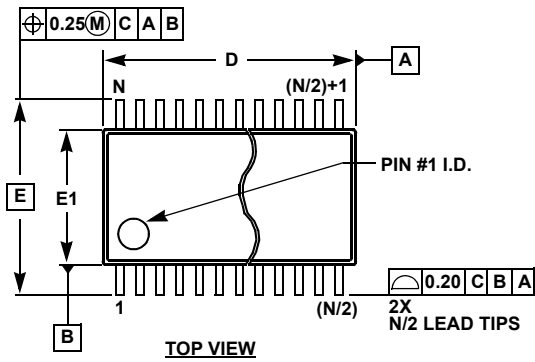
Rev 2, 3/11



**NOTES:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions in ( ) are not necessarily exact.
8. This outline conforms to JEDEC publication MS-013-AD ISSUE C.

**Thin Shrink Small Outline Package Family (TSSOP)**



**MDP0044**

**THIN SHRINK SMALL OUTLINE PACKAGE FAMILY**

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference



Rev. F 2/07

**NOTES:**

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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