THE DATASHEET OF

DS1010-125

DS1010
10-Tap Silicon Delay Line

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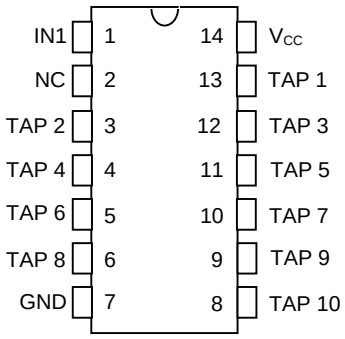
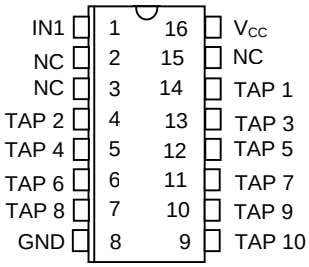
FEATURES

- All-silicon time delay
- 10 taps equally spaced
- Delays are stable and precise
- Leading and trailing edge accuracy
- Delay tolerance ±5% or ±2 ns, whichever is greater
- Economical
- Auto-insertable, low profile
- Standard 14-pin DIP or 16-pin SOIC
- Low-power CMOS
- TTL/CMOS-compatible
- Vapor phase, IR and wave solderable
- Custom delays available
- Fast turn prototypes

PIN ASSIGNMENT



DS1010 14-Pin DIP (300-mil)
See Mech. Drawings Section



DS1010S 16-Pin SOIC
(300-mil)
See Mech. Drawings Section

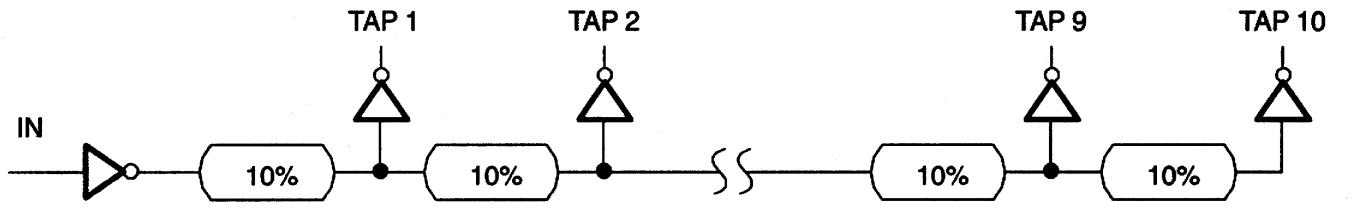
PIN DESCRIPTION

TAP 1 - TAP 10	- TAP Output Number
V_{CC}	- 5 Volts
GND	- Ground
NC	- No Connection
IN	- Input

DESCRIPTION

The DS1010 series delay line has ten equally spaced taps providing delays from 5 ns to 500 ns. The devices are offered in a standard 14-pin DIP which is pin-compatible with hybrid delay lines. Alternatively, a 16-pin SOIC is available for surface mount technology which reduces PC board area. Since the DS1010 is an all-silicon solution, better economy is achieved when compared to older methods using hybrid techniques. The DS1010 series delay lines provide a nominal accuracy of ±5% or ±2 ns, whichever is greater. The DS1010 reproduces the input logic state at the TAP 10 output after a fixed delay as specified by the dash number extension of the part number. The DS1010 is designed to produce both leading and trailing edge with equal precision. Each tap is capable of driving up to 10 74LS type loads. Dallas Semiconductor can customize standard products to meet special needs. For special requests and rapid delivery, call (972) 371-4348.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PHL}, t_{PLH}) Table 1

CATALOG P/N	TOTAL DELAY	DELAY/TAP (ns)
DS1010-50	50	5
DS1010-60	60	6
DS1010-75	75	7.5
DS1010-80	80	8
DS1010-100	100	10
DS1010-125	125	12.5
DS1010-150	150	15
DS1010-175	175	17.5
DS1010-200	200	20
DS1010-250	250	25
DS1010-300	300	30
DS1010-350	350	35
DS1010-400	400	40
DS1010-450	450	45
DS1010-500	500	50

Custom delays available.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 5%)

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
High Level Input Voltage	V_{IH}		2.2		V_{CC} + 0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage Current	I_I	$0.0V \le V_I \le V_{CC}$	-1.0		1.0	µA	
Active Current	I_{CC}	V_{CC}=Max; Period=Min.		40	150	mA	2
High Level Output Current	I_{OH}	V_{CC}=Min. V_{OH}=4			-1.0	mA	
Low Level Output Current	I_{OL}	V_{CC}=Min. V_{OL}=0.5	12			mA	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Pulse Width	t_{WI}	40% of TAP 10 t_{PLH}			ns	8
Input to Tap Delay (leading edge)	t_{PLH}		Table 1		ns	3, 4, 5, 6, 7, 9
Input to Tap Delay (trailing edge)	t_{PHL}		Table 1		ns	3, 4, 5, 6, 7, 9
Power-up Time	t_{PU}			100	ms	
	Period	4 (t_{WI})			ns	8

CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	

NOTES:

1. All voltages are referenced to ground.

2. Measured with outputs open.

3. V_{CC} = 5V @ 25°C. Input-to-tap delays accurate on both rising and falling edges within ±2 ns or ±5% whichever is greater.

4. See “Test Conditions” section.

5. For DS1010 delay lines with a TAP 10 delay of 100 ns or greater, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±2ns or ±3%, whichever is greater.

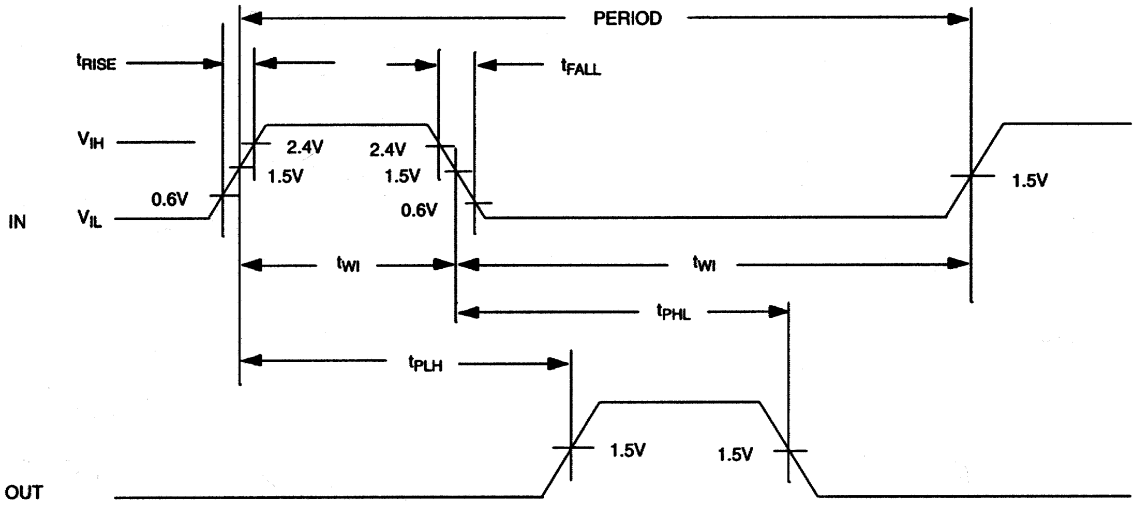
6. For DS1010 delay lines with a TAP 10 delay less than 100 ns, temperature variations from 25°C to 0°C or 70°C may produce an additional input-to-tap delay shift of ±1 ns or ±9%, whichever is greater.

7. All tap delays tend to vary unidirectionally with temperature or voltage changes. For example, if TAP 1 slows down, all other taps will also slow down; TAP 3 can never be faster than TAP 2.

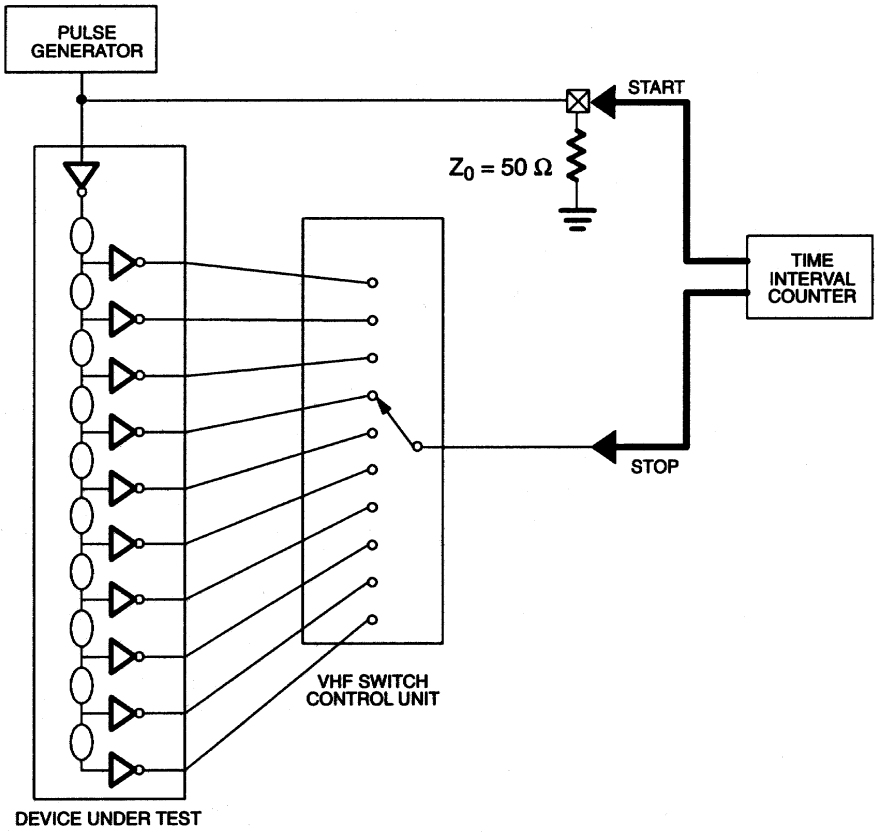
8. Pulse width and period specifications may be exceeded; however, accuracy will be application-sensitive (decoupling, layout, etc.).

9. Certain high-frequency applications not recommended for -50 in 16-pin package. Consult factory.

TIMING DIAGRAM: SILICON DELAY LINE Figure 2



TEST CIRCUIT Figure 3



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_{PLH} (Time Delay Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of any tap output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of any tap output pulse.

TEST SETUP DESCRIPTION

Figure 3 illustrates the hardware configuration used for measuring the timing parameters on the DS1010. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected between the input and each tap. Each tap is selected and connected to the counter by a VHF switch control unit. All measurements are fully automated, with each instrument controlled by a central computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohm max.
Rise and Fall Time:	3.0 ns max.
Pulse Width:	500 ns (1 µs for -500)
Period:	1 µs (2 µs for -500)

OUTPUT:

Each output is loaded with the equivalent of one 74FO4 input gate. Delay is measured at the 1.5V level on the rising and falling edge.

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

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