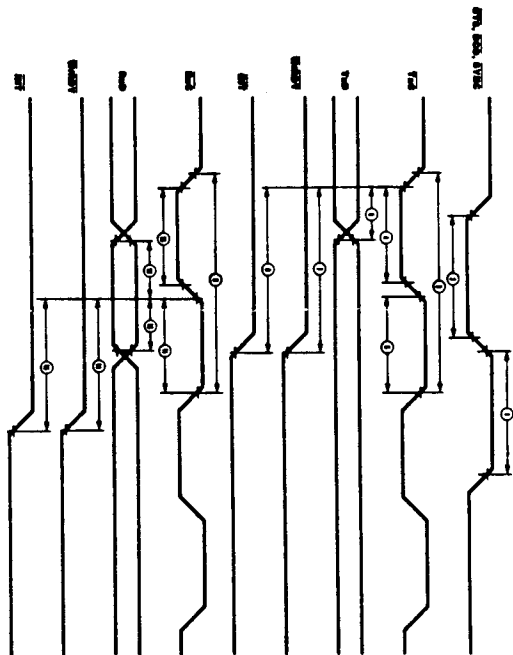




**THE DATASHEET OF
Z0847006PSG**





Zilog

Z08470 Customer
Procurement Spec (CPS)

GENERAL DESCRIPTION

The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel, multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial, converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.

01	1	48	D ₈
02	2	49	D ₇
03	3	50	D ₆
04	4	51	D ₅
05	5	52	D ₄
06	6	53	D ₃
07	7	54	D ₂
08	8	55	D ₁
09	9	56	D ₀
10	10	57	D ₀
11	11	58	D ₀
12	12	59	D ₀
13	13	60	D ₀
14	14	61	D ₀
15	15	62	D ₀
16	16	63	D ₀
17	17	64	D ₀
18	18	65	D ₀
19	19	66	D ₀
20	20	67	D ₀
21	21	68	D ₀
22	22	69	D ₀
23	23	70	D ₀
24	24	71	D ₀
25	25	72	D ₀
26	26	73	D ₀
27	27	74	D ₀
28	28	75	D ₀
29	29	76	D ₀
30	30	77	D ₀
31	31	78	D ₀
32	32	79	D ₀
33	33	80	D ₀
34	34	81	D ₀
35	35	82	D ₀
36	36	83	D ₀
37	37	84	D ₀
38	38	85	D ₀
39	39	86	D ₀
40	40	87	D ₀
41	41	88	D ₀
42	42	89	D ₀
43	43	90	D ₀
44	44	91	D ₀
45	45	92	D ₀
46	46	93	D ₀
47	47	94	D ₀
48	48	95	D ₀
49	49	96	D ₀
50	50	97	D ₀
51	51	98	D ₀
52	52	99	D ₀
53	53	100	D ₀
54	54	101	D ₀
55	55	102	D ₀
56	56	103	D ₀
57	57	104	D ₀
58	58	105	D ₀
59	59	106	D ₀
60	60	107	D ₀
61	61	108	D ₀
62	62	109	D ₀
63	63	110	D ₀
64	64	111	D ₀
65	65	112	D ₀
66	66	113	D ₀
67	67	114	D ₀
68	68	115	D ₀
69	69	116	D ₀
70	70	117	D ₀
71	71	118	D ₀
72	72	119	D ₀
73	73	120	D ₀
74	74	121	D ₀
75	75	122	D ₀
76	76	123	D ₀
77	77	124	D ₀
78	78	125	D ₀
79	79	126	D ₀
80	80	127	D ₀
81	81	128	D ₀
82	82	129	D ₀
83	83	130	D ₀
84	84	131	D ₀
85	85	132	D ₀
86	86	133	D ₀
87	87	134	D ₀
88	88	135	D ₀
89	89	136	D ₀
90	90	137	D ₀
91	91	138	D ₀
92	92	139	D ₀
93	93	140	D ₀
94	94	141	D ₀
95	95	142	D ₀
96	96	143	D ₀
97	97	144	D ₀
98	98	145	D ₀
99	99	146	D ₀
100	100	147	D ₀
101	101	148	D ₀
102	102	149	D ₀
103	103	150	D ₀
104	104	151	D ₀
105	105	152	D ₀
106	106	153	D ₀
107	107	154	D ₀
108	108	155	D ₀
109	109	156	D ₀
110	110	157	D ₀
111	111	158	D ₀
112	112	159	D ₀
113	113	160	D ₀
114	114	161	D ₀
115	115	162	D ₀
116	116	163	D ₀
117	117	164	D ₀
118	118	165	D ₀
119	119	166	D ₀
120	120	167	D ₀
121	121	168	D ₀
122	122	169	D ₀
123	123	170	D ₀
124	124	171	D ₀
125	125	172	D ₀
126	126	173	D ₀
127	127	174	D ₀
128	128	175	D ₀
129	129	176	D ₀
130	130	177	D ₀
131	131	178	D ₀
132	132	179	D ₀
133	133	180	D ₀
134	134	181	D ₀
135	135	182	D ₀
136	136	183	D ₀
137	137	184	D ₀
138	138	185	D ₀
139	139	186	D ₀
140	140	187	D ₀
141	141	188	D ₀
142	142	189	D ₀
143	143	190	D ₀
144	144	191	D ₀
145	145	192	D ₀
146	146	193	D ₀
147	147	194	D ₀
148	148	195	D ₀
149	149	196	D ₀
150	150	197	D ₀
151	151	198	D ₀
152	152	199	D ₀
153	153	200	D ₀
154	154	201	D ₀
155	155	202	D ₀
156	156	203	D ₀
157	157	204	D ₀
158	158	205	D ₀
159	159	206	D ₀
160	160	207	D ₀
161	161	208	D ₀
162	162	209	D ₀
163	163	210	D ₀
164	164	211	D ₀
165	165	212	D ₀
166	166	213	D ₀
167	167	214	D ₀
168	168	215	D ₀
169	169	216	D ₀
170	170	217	D ₀
171	171	218	D ₀
172	172	219	D ₀
173	173	220	D ₀
174	174	221	D ₀
175	175	222	D ₀
176	176	223	D ₀
177	177	224	D ₀
178	178	225	D ₀
179	179	226	D ₀
180	180	227	D ₀
181	181	228	D ₀
182	182	229	D ₀
183	183	230	D ₀
184	184	231	D ₀
185	185	232	D ₀
186	186	233	D ₀
187	187	234	D ₀
188	188	235	D ₀
189	189	236	D ₀
190	190	237	D ₀
191	191	238	D ₀
192	192	239	D ₀
193	193	240	D ₀
194	194	241	D ₀
195	195	242	D ₀
196	196	243	D ₀
197	197	244	D ₀
198	198	245	D ₀
199	199	246	D ₀
200	200	247	D ₀
201	201	248	D ₀
202	202	249	D ₀
203	203	250	D ₀
204	204	251	D ₀
205	205	252	D ₀
206	206	253	D ₀
207	207	254	D ₀
208	208	255	D ₀
209	209	256	D ₀
210	210	257	D ₀
211	211	258	D ₀
212	212	259	D ₀
213	213	260	D ₀
214	214	261	D ₀
215	215	262	D ₀
216	216	263	D ₀
217	217	264	D ₀
218	218	265	D ₀
219	219	266	D ₀
220	220	267	D ₀
221	221	268	D ₀
222	222	269	D ₀
223	223	270	D ₀
224	224	271	D ₀
225	225	272	D ₀
226	226	273	D ₀
227	227	274	D ₀
228	228	275	D ₀
229	229	276	D ₀
230	230	277	D ₀
231	231	278	D ₀
232	232	279	D ₀
233	233	280	D ₀
234	234	281	D ₀
235	235	282	D ₀
236	236	283	D ₀
237	237	284	D ₀
238	238	285	D ₀
239	239	286	D ₀
240	240	287	D ₀
241	241	288	D ₀
242	242	289	D ₀
243	243	290	D ₀
244	244	291	D ₀
245	245	292	D ₀
246	246	293	D ₀
247	247	294	D ₀
248	248	295	D ₀
249	249	296	D ₀
250	250	297	D ₀
251	251	298	D ₀
252	252	299	D ₀
253	253	300	D ₀
254	254	301	D ₀
255	255	302	D ₀
256	256	303	D ₀
257	257	304	D ₀
258	258	305	D ₀
259	259	306	D ₀
260	260	307	D ₀
261	261	308	D ₀
262	262	309	D ₀
263	263	310	D ₀
264	264	311	D ₀
265	265	312	D ₀

DC CHARACTERISTICS

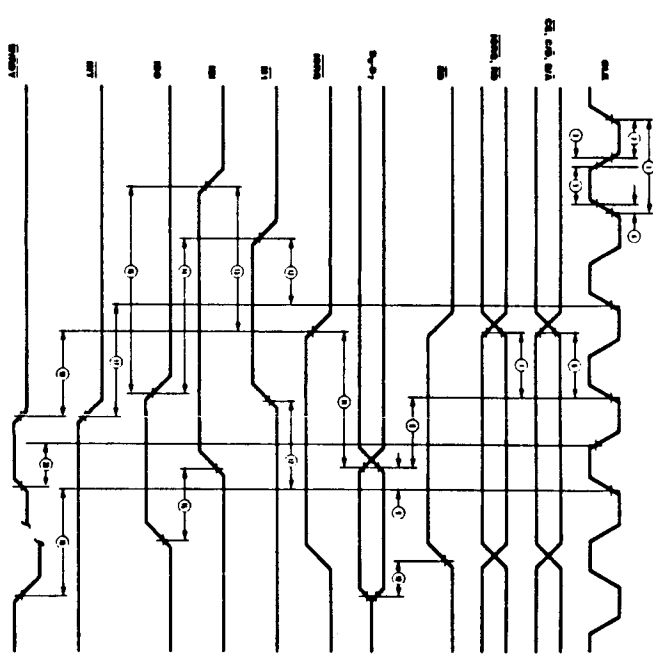
Symbol	Parameter	Min	Max	Units	Test Conditions
V _{CC}	Clock Input Low Voltage	-0.2*	+0.45*	V	V _{CC} = 2.0 mA 0.4 < V _{IN} < 2.0 V 0.4 < V _{OUT} < 2.0 V P _{AV} < 100 mW
V _{CC}	Clock Input High Voltage	V _{CC} - 0.8*	+0.85*	V	
V _{IN}	Input Low Voltage	-0.2*	+0.18*	V	
V _{IN}	Input High Voltage	+2.0*	+0.85*	V	
V _{OH}	Output Low Voltage	+0.4*	+0.4*	V	
V _{OH}	Output High Voltage	+2.4*	V	V	
I _{OL}	Input/3-Steer Output Leakage Current	-10*	+10*	µA	
I _{OH}	Input/3-Steer Output Leakage Current	-40*	+10*	µA	
I _{CC}	Power Supply Current		100*	mA	
V _{CE}	Power Supply Current		100*	mA	

* Tested
 † Guaranteed by Design
 ‡ Guaranteed by Characterization

AC CHARACTERISTICS*

Number	Symbol	Parameter	280-4 DART		280-6 DART	
			Min	Max	Min	Max
1	T _{DC}	Clock Cycle Time	250*	4000*	185*	4000*
2	T _{WH}	Clock Width (High)	105*	2000*	70*	2000*
3	T _{WC}	Clock Fall Time		30*		15*
4	T _{WC}	Clock Rise Time		30*		15*
5	T _{WC}	Clock Width (Low)	105*	2000*	70*	2000*
6	T _{ANDQ}	CE, C _{EN} Setup to Clock Setup Time	145*		80*	
7	T _{ANDQ}	RE ₁ , RD ₁ Setup to Clock Setup Time	115*		80*	
8	T _{ANDQ}	Clock 1 to Data Out Delay		220*		150*
9	T _{ANDQ}	Data In to Clock 1 Setup (Write or Hit Cycle)	50*		30*	
10	T _{ANDQ}	RD ₁ to Data Out Read Delay		110*		80*
11	T _{ANDQ}	RE ₁ to Data Out Delay (TRACK Cycle)		180*		100*
12	T _{ANDQ}	RE ₁ to Clock 1 Setup Time	80*		75*	
13	T _{ANDQ}	RE ₁ to RE ₂ Setup Time (TRACK Cycle)	140*		120*	
14	T _{ANDQ}	RE ₁ to RE ₁ Delay (format before hit)	180*		180*	
15	T _{ANDQ}	RE ₁ to RE ₁ Delay (after ED decode)	100*		70*	
16	T _{ANDQ}	RE ₁ to RE ₁ Delay	100*		70*	
17	T _{ANDQ}	Clock 1 to RT ₁ Delay	200*		150*	
18	T _{ANDQ}	RE ₁ or CE ₁ to W/RDY ₁ Delay (Ready Mode)	210*		175*	
19	T _{ANDQ}	Clock 1 to W/RDY ₁ Delay (Ready Mode)	120*		100*	
20	T _{ANDQ}	Clock 1 to W/RDY ₁ Read Delay (Hit Mode)	130*		110*	

* Units in microseconds (µs)
 † Tested
 ‡ Guaranteed by Design
 ‣ Guaranteed by Characterization



AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	280-4 DART		280-6 DART	
			Min	Max	Min	Max
1	T _{WH}	Pulse Width (High)	200*	200*		
2	T _{WH}	Pulse Width (Low)	200*	200*		
3	T _{WC}	CE Cycle Time	400*	300*	300*	300*
4	T _{WC}	CE Width (Low)	180*	100*	100*	100*
5	T _{WC}	CE Width (High)	180*	100*	100*	100*
6	T _{ANDQ}	CE ₁ to RD Delay	300*		220*	
7	T _{ANDQ}	CE ₁ to W/RDY ₁ Delay (Ready Mode)	5*	9*	5*	9*
8	T _{ANDQ}	CE ₁ to RT ₁ Delay	5*	9*	5*	9*
9	T _{ANDQ}	RE ₁ Cycle Time	400*	300*	300*	300*
10	T _{ANDQ}	RE ₁ Width (Low)	180*	100*	100*	100*
11	T _{ANDQ}	RE ₁ Width (High)	180*	100*	100*	100*
12	T _{ANDQ}	RD ₁ to RE ₂ Setup Time (Hit Mode)	0*	0*	0*	0*
13	T _{ANDQ}	RD ₁ Hold Time (Hit Mode)	140*	100*		
14	T _{ANDQ}	RE ₁ to W/RDY ₁ Delay (Ready Mode)	10*	13*	10*	13*
15	T _{ANDQ}	RE ₁ to RT ₁ Delay	10*	13*	10*	13*

* In all modes, the System Clock rate must be at least five times the maximum data rate. RESET must be active a minimum of one complete clock cycle.
 † Units equal to System Clock Period.
 ‡ Units in microseconds (µs)
 ‣ Tested
 ․ Guaranteed by Design
 ‥ Guaranteed by Characterization

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View Z0847006PSG on WIN SOURCE](#)

 [Zilog Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management