THE DATASHEET OF

UCC5390SCDEVM-010

UCC5390SCD With Isolated Bias Supply

This manual describes the UCC5390SCD evaluation module (EVM). The UCC539SCD EVM is designed to be embedded into a power system by attaching directly to the power FET or IGBT in both TO-220 or TO-247 packages. This approach helps power system designers verify the performance of the UCC53x0x drivers and the SN6505B-based bias supply during the early stage of the design in actual system operating conditions.

WARNING

Although these devices provide galvanic isolation of up to 3000 V, the EVM cannot be used for isolation voltage testing.

Voltage exceeding the EVM ratings (V_{CC1} > 15 V, V_{CC2} – V_{EE2} > 33 V, and IGBT collector-emitter voltage V_{CE} > 50 V) can damage the EVM, and result in personal injury.

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Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The UCC5390SCDEVM-010 device is a complete, single-channel, isolated gate driver board with a reconfigurable bias supply, which provides a wide range of drive voltages. This EVM from TI is based on a 17-A, split output, basic insulation UCC5390SCD driver in a SOIC-8 package. The EVM also includes a SN6505B-based bias supply that can be configured for single or split-rail drive voltage from 11 V to 33 V, covering a wide range of Si and SiC FETs and IGBTs. Compact form factor, 1.5” × 0.83” × 0.3”, and embedded footprints for TO-220 and TO-247 power device packages, allow for easy, direct connection to FETs or IGBTs in the power system, for comprehensive performance evaluation

2 General Overview

The UCC5390SCDEVM-010 device uses a 17-A, split output driver, UCC5390SCD, and an SN6505B-based bias supply. The EVM can be configured with or without split rail, for optimal drive voltages depending on the specific application. By default, the bias supply is configured as a split-rail supply providing 18-V turn ON and –4-V turn OFF, which is optimal for many SiC FETs. Figure 1 shows the block diagram of the EVM.

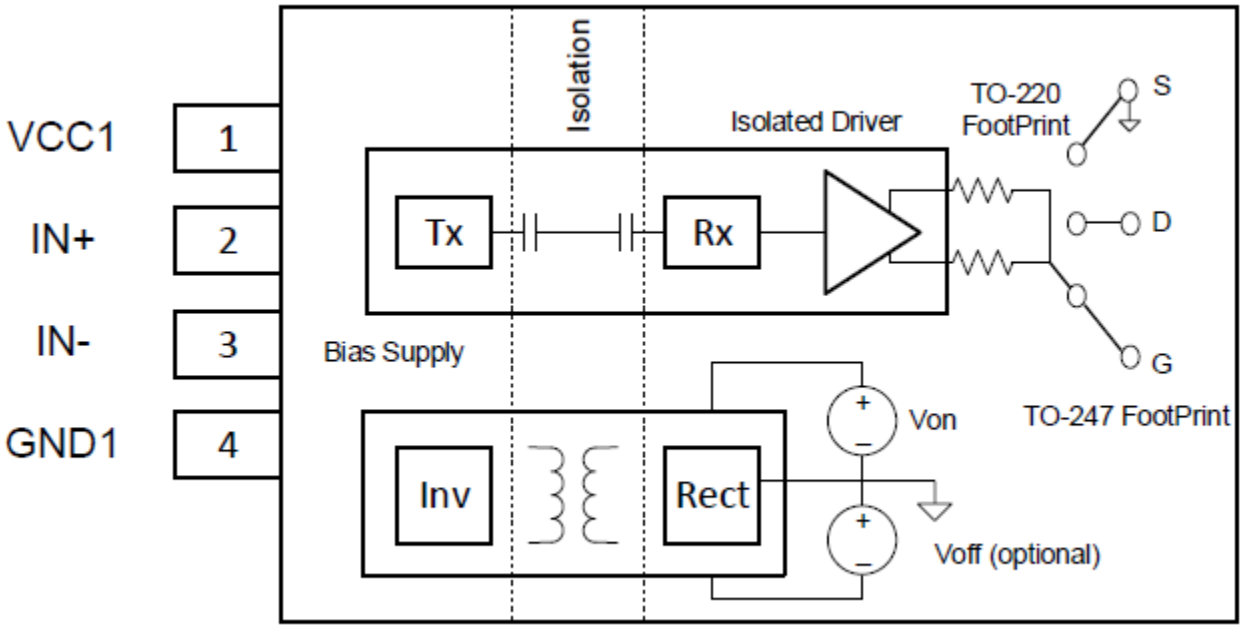

Figure 1. UCC5390SCDEVM-010 Functional Block Diagram

Figure 2 shows the board image of the EVM.

Figure 2. UCC5390SCDEVM-010 Board Image

The EVM includes an isolated driver, UCC5390SCD, and bias supply, SN6505B. The UCC5390SCD device is part of the UCC53xx family of drivers, in an 8-pin SOIC package including variants with different pinout configurations and drive strengths. For this design, the UCC5390SCD device, with split output, 17-A, and typical current capability, has been selected for its ability to optimally drive FETs and IGBTs in mid- and high-power applications. The SN6505B device is a push-pull transformer driver, operating at 420 kHz to provide a compact bias solution for isolated drivers, digital isolators, sense circuits, and various communication buses. See the UCC53x0 3-kVRMS Single-Channel Isolated Gate Drivers data sheet and SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet for more information about the UCC5390 isolated driver and SN6505B transformer driver.

The primary side of the EVM is supplied by a 3-V to 5.5-V external voltage source. This voltage is converted and isolated through a high-frequency transformer to provide bias voltage from 11-V up to 33-V range to the secondary isolated side of the driver. Bias supply is an unregulated DC-DC transformer, so the variation of primary voltage directly impacts the secondary side voltage. Therefore, TI recommends an external voltage source regulated within 5% to 10% for this design. The driver has two inputs: inverted and non-inverted. One input can be used for the PWM signal and the other as Enable. The driver has split outputs that, through gate resistors, are connected to output holes to allow direct soldering to the power device in TO-220 or TO-247 packages. The secondary side of the bias supply includes a rectifier circuit that can be configured as center-tapped or bridge, therefore expanding the range of available bias voltage. The secondary side also includes a circuit to generate a split rail with negative turn OFF bias for applications and power devices where dv/dt-induced, spurious turn ON may be a potential issue.

2.1 Features

- Compact, isolated gate driver board for direct connection to power FETs and IGBTs in high-voltage, mid-, and high-power converters and inverters
- Split output, 17-A, typical sink and source drive current for optimal turn ON and turn OFF settings
- Single or split rail bias supply configuration in 11-V to 33-V range
- Robust, noise-immune solution with CMTI > 100 V per ns
- Supports 3-kVrms basic isolation
- Provides up to 0.8-W drive power using 80% efficient bias supply

2.2 I/O Description

Table 1 lists the connection descriptions.

Table 1. Connection Descriptions

Pin	Description
VCC1	VCC positive input. Powers driver and bias ICs, uses 3-V to 5.5-V range
GND1	Ground and reference plane, VCC, IN+, and IN– negative input
IN+	Non-inverting input of driver IC
IN–	Inverting input of driver IC
S	Source connection to external FET in TO-220 or TO-247 package
G	Gate connection to external FET in TO-220 or TO-247 package
D	Drain connection to external FET in TO-220 or TO-247 package

3 Electrical Specifications

Table 2 shows the electrical parameters of the UCC5390SCDEVM-010.

Table 2. UCC5390SCDEVM-010 Electrical Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Primary input supply voltage (Vcc1)		3		5.5	V
Input signal rising threshold				0.7 × Vcc1	
Input signal falling threshold		0.3 × Vcc1			
OUTPUT CONDITIONS					
Gate drive voltage	Depends on Vcc1	11		33	V
Source current		10	17		A
Propagation delay		10	17		ns
Drive power	At 25°C			0.8	W
SYSTEM CHARACTERISTICS					
CMTI		100			V/ns
Basic isolation		3			kVrms
Capacitance through isolation				5	pF
Operating ambient		–40	25	85	
Board size	Length × width × height	1.5 × 0.83 × 0.3	1.5 × 0.83 × 0.3	1.5 × 0.83 × 0.3	inch
Drive area size	Length × width × height	0.95 × 0.83 × 0.3	0.95 × 0.83 × 0.3	0.95 × 0.83 × 0.3	inch

4 Detailed Description

The following sections provide a detailed description of the EVM.

4.1 Schematics

By default, the EVM is configured for drive pulse outputs, 18 V to turn ON, and –4 V to turn OFF, when a 3.3-V supply voltage is applied to the input. Different settings are possible, described as follows. The configuration procedure is described based on the schematic shown in Figure 3.

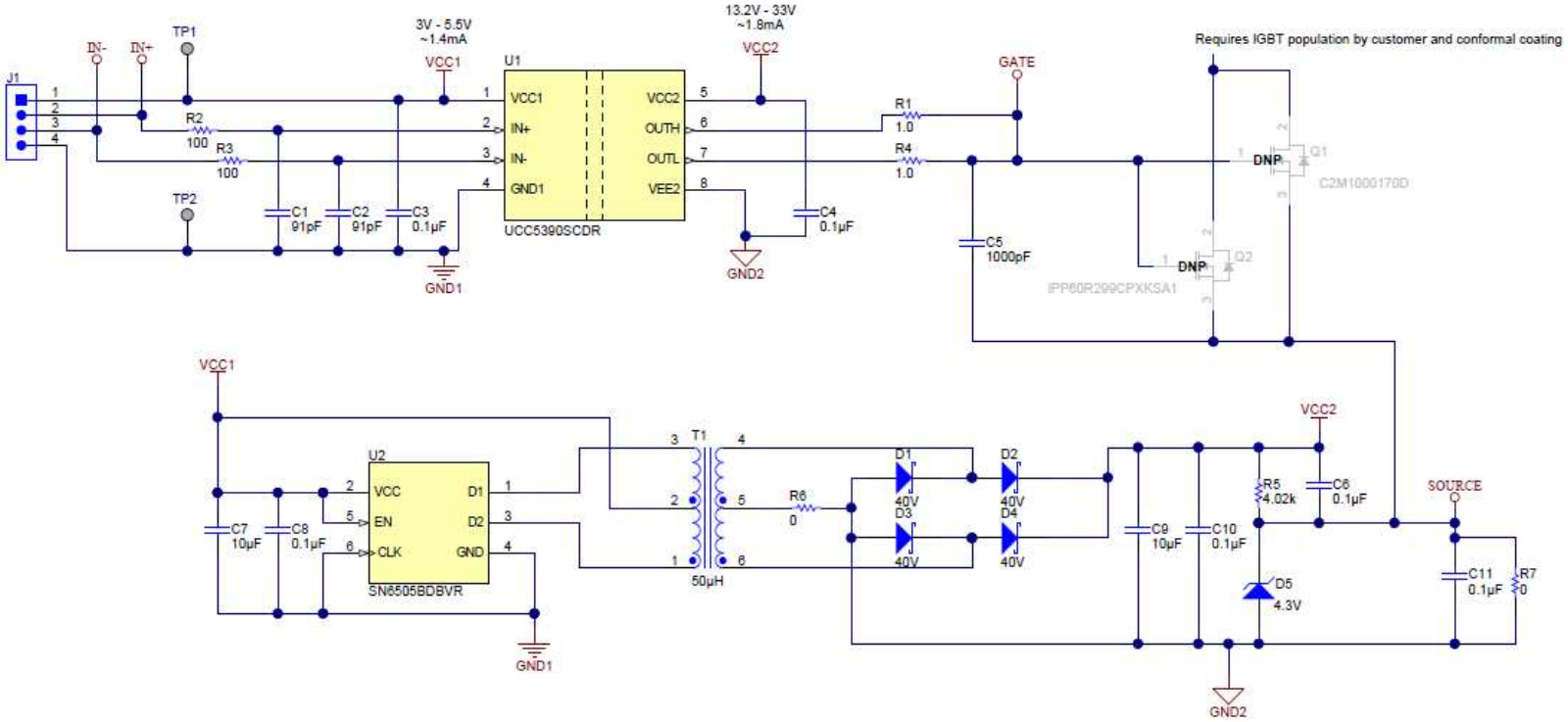

Figure 3. UCC5390SCDEVM-010 Electrical Schematic

4.2 Driver Circuit Description

The supply voltage and input signals for driver U1 and bias supply U2 are applied through header J1. Capacitors C3, C7, and C8 are located as close as possible to the VCC1 and GND1 terminals of U1 and U2, to minimize EMI while operating as part of high dv/dt and di/dt power system. Resistors R2 and R3 and capacitors C1 and C2 provide additional filtering to protect input signals. These filters are optional and may not be used in the systems where noise is limited. The secondary side noise decoupling is provided by capacitors C2, C6, C9, C10, and C11. Split outputs of the driver U1 through gate resistors R1 and R4 are connected to FETs Q1 and Q2. These FETs are not populated on the board and their through hole footprints are used to solder the board for evaluation on a system level, as it is shown in Figure 5. On this board, the gate resistors have been selected at 1 Ω. However, as was described in Section 4.1, gate resistor values determine switching rise and fall time with the power losses inside the driver IC, therefore their values can be changed for specific requirements. Capacitor C5 can be used to estimate drive current capability by measuring rise and fall time using the board separately. It is not populated on boards intended to be used in a power system.

4.3 FET Recommendation

This board can be used with both IGBT and MOSFET-based power systems. FET selection does not impact the board maximum power. The UCC5390S device limits the power dissipated by the board.

4.4 Bias Supply Circuit and Setting Description

By default, the bias supply outputs are set for 18 V turn ON voltage and –4V turn OFF voltage. The output split rail is provided by Zener diode D5, resistor R5, and capacitors C6 and C11, with jumpers R7 and R6 removed. If a different turn OFF voltage is needed, a proper voltage-rated Zener diode and resistor can be selected. If a split rail is not needed, then jumper R7 must be placed on the board and resistor R5 can be removed. This will reduce overall power consumption initially dissipated inside resistor R5 and Zener diode D5. Another bias supply option is possible by configuring the rectifier circuit as center-tapped or bridge. Bridge configuration is provided by removing jumper R6. In this case, for the same input voltage VCC, the output bias voltage is doubled versus the center-tapped rectifier. For the center-tapped rectifier, the diodes D1 and D3 must be removed, and jumper R6 placed onboard. Table 3 lists possible combinations of bias voltages, depending on nominal input voltage and rectifier configurations. These voltages obviously depend on the transformer turn ratio. For this board, a transformer, 750342879, from Würth-Midcom with a turn ratio 1:3.5 has been selected.

Table 3. Bias Voltage Configurations

Configuration	Modification	Input (V)	Output (V)
Center-tapped, single output	Remove D1, D3, R5; place R7 and R6	3.6	11
		5	17
Bridge, single output	Remove R5 and R6; place D1, D3, R7	3.3	22
		5	34
Center-tapped, split output	Remove D1, D3, R7; place R5 and R6	3.6	+7/–4
		5	+13/-4
Bridge, split output	Remove R7 and R6; place D1, D3, R5	3.3	+18/-4
		5	+30/–4

5 Test Summary

5.1 Definitions

This test procedure details how to configure the test setup and capture key waveforms of the UCC5390SCDEVM-010 boards when they operate in power system as part of a high voltage buck converter.

5.2 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the UCC53x0 EVM. Observe all safety precautions.

CAUTION:

Caution! Warning: Hot surface contact may cause burns. Do not touch.

HOT SURFACE:

Precautions when operating.

HIGH VOLTAGE:

Danger: High voltage! The UCC53x0 device has an isolation boundary, but does not have safety rated reinforced isolation. If you apply high voltage to this board, all terminals should be considered high voltage. Electric shock is possible when connecting the board to live wire.

The board should be handled with care by a professional. For safety, TI highly recommends use of isolated test equipment with overvoltage and overcurrent protection.

CAUTION

- ❑ Do not leave the EVM unattended while powered.
- ❑ All high voltage, high temperature, and hazard safety rules, applied to the power system where these EVMs are embedded for bench evaluation, must be strictly followed.

5.3 Equipment

5.3.1 Power Supplies

TI recommends the following or similar DC power supplies for tests:

- At least up to 6-V and 1-A power supply for powering the EVM, for example: BK Precision, series 1715
- At least up to 1000-V and 1-A power supply for powering the power stage at the system level evaluation, for example: Glassman FL1500 1.0

5.3.2 Function Generator

One 2-channel function generator over 20 MHz, for example: Tektronix AFG3102

5.3.3 BNC Feed-Thru Terminator

Two 50-Ω BNC male to female feed-thru terminators DC to 1 GHz, for example: Tektronix 011-0049-02

5.3.4 Oscilloscope

Oscilloscope 500-MHz or higher with four channels, for example: Tektronix DPO7104

5.3.5 Oscilloscope Probes

- At least 500-MHz bandwidth passive voltage probe, for example: Tektronix P6139A
- Two, at least 200-MHz bandwidth, 1000-V common mode differential voltage probes, for example: Tektronix THDP020
- At least 50-MHz bandwidth current sense probe, for example: Tektronix TCP202

5.3.6 Digital Multi-Meters

Two digital multi-meters for evaluation of the EVM alone, and four digital multi-meters for evaluation on the system level with a buck converter: for example Fluke 187

5.3.7 Electronic Load

Electronic load for system-level evaluation up to 500-V and 800-W, for example Kikusui PLZ603WH

5.3.8 Function Generator Settings

lists the 2-channel function generator settings.

Table 4. Two-Channel Function Generator Settings

Output	Mode	Frequency	Width	Delay	High	Low	Output Impedance	Termination
Channel A	Pulse	100 KHz	4.5 µs	0 ns	3 V	0 V	50 Ω	Feed-thru 50 Ω
Channel B				5 µs				

5.3.9 Initial Oscilloscope Settings

Table 5 lists the initial oscilloscope settings. Because various bandwidth probes are used, it is recommended to de-skew all channels to minimize delay differences.

Table 5. Initial Oscilloscope Settings

Output	Bandwidth	Probe	Coupling	Vertical Scale	Horizontal Scale	Measured Waveforms
Channel 1	≥ 50 MHz	TCP202	DC	2 A/div	2 µs/div	Inductor current
Channel 2	≥ 200 MHz	THDP020	DC	10 V/div	2 µs/div	Vgs, upper FET
Channel 3	≥ 200 MHz	THDP020	DC	200 V/div	2 µs/div	Vds, lower FET
Channel 4	≥ 500 MHz	P6139A	DC	10 V/div	2 µs/div	Vgs, lower FET

5.3.10 Bench Setup

This EVM is designed to ensure easy and close connection to the power stage FET or IGBT in the TO-220 or TO-247 package. Figure 4 shows an example of how the drive board can be attached and soldered directly to the power FET terminals.

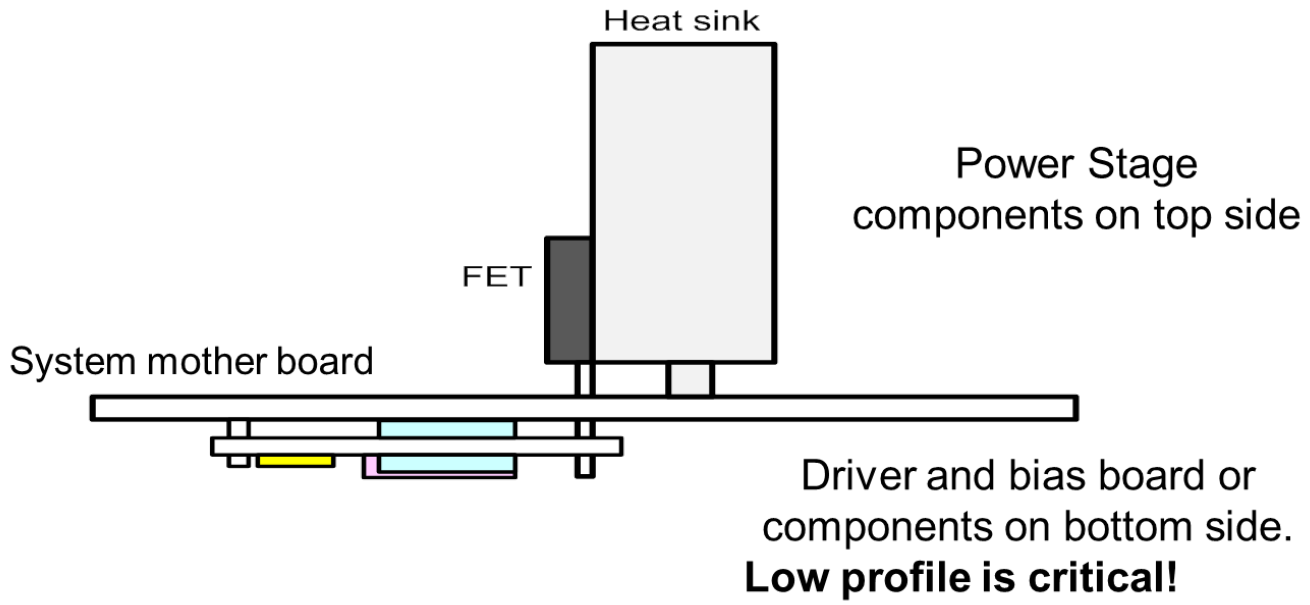

Figure 4. Soldering UCC5390SCDEVM-010 Board for System Level Evaluation

Figure 5 shows an example of the EVM evaluation as part of a system arranged as a buck converter.

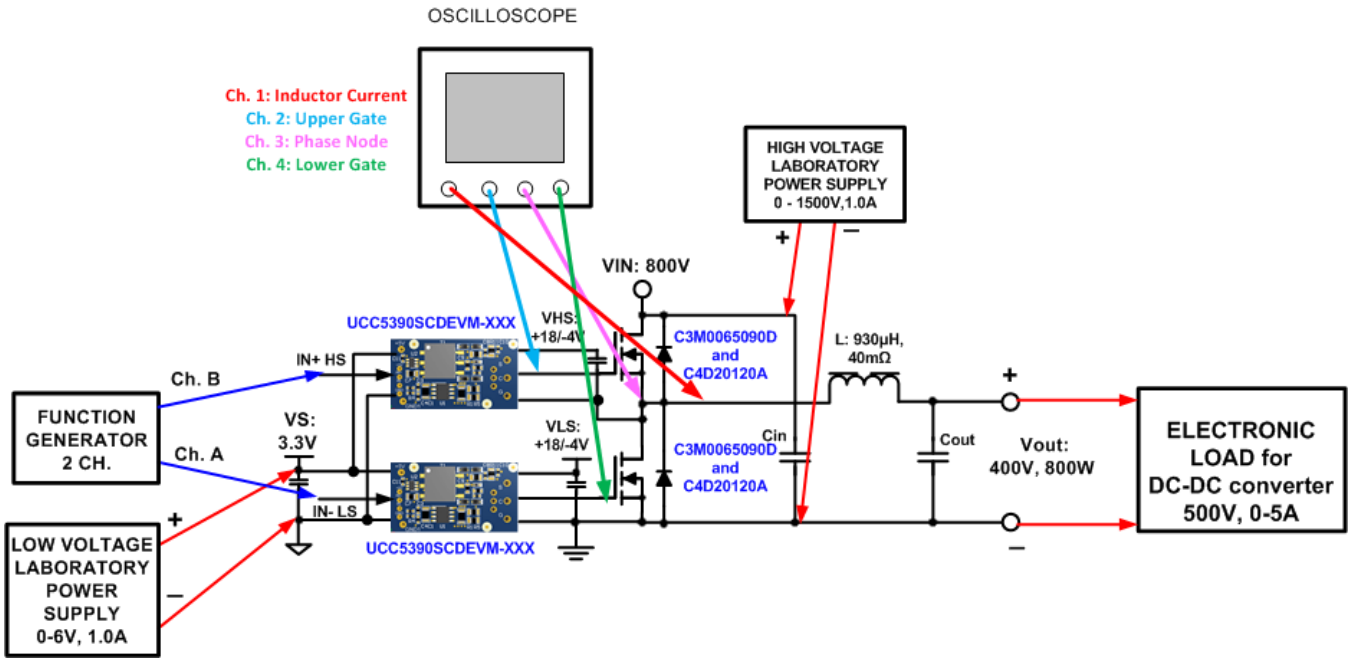

Figure 5. Test Setup for UCC5390SCDEVM-010 System Level Evaluation

One example is a buck converter using SiC FETs, C3M0065090D, and SiC diodes, C4D20120, selected in this case for evaluation of the EVM boards. Users can use different power devices and different topologies that fit their projects and applications. The following is the test procedure recommended for this test setup.

6 Power Up, Capturing Waveforms, and Power Down

1. Before beginning the power up test procedure, verify the connections in Figure 5 and the function generator and oscilloscope settings.
2. Connect the function generator outputs to the EVM inputs using the BNC feed-thru terminators. Follow all company-related safety rules applied to the voltage levels used during evaluation.
3. Enable the low-voltage power supply and gradually increase the voltage up to 3.3 V.
4. Do not enable the high voltage power supply for now.
5. Enable the function generator outputs channel A and channel B.
6. Verify that gate voltages of the lower and upper FETs are similar to that shown in Figure 6.

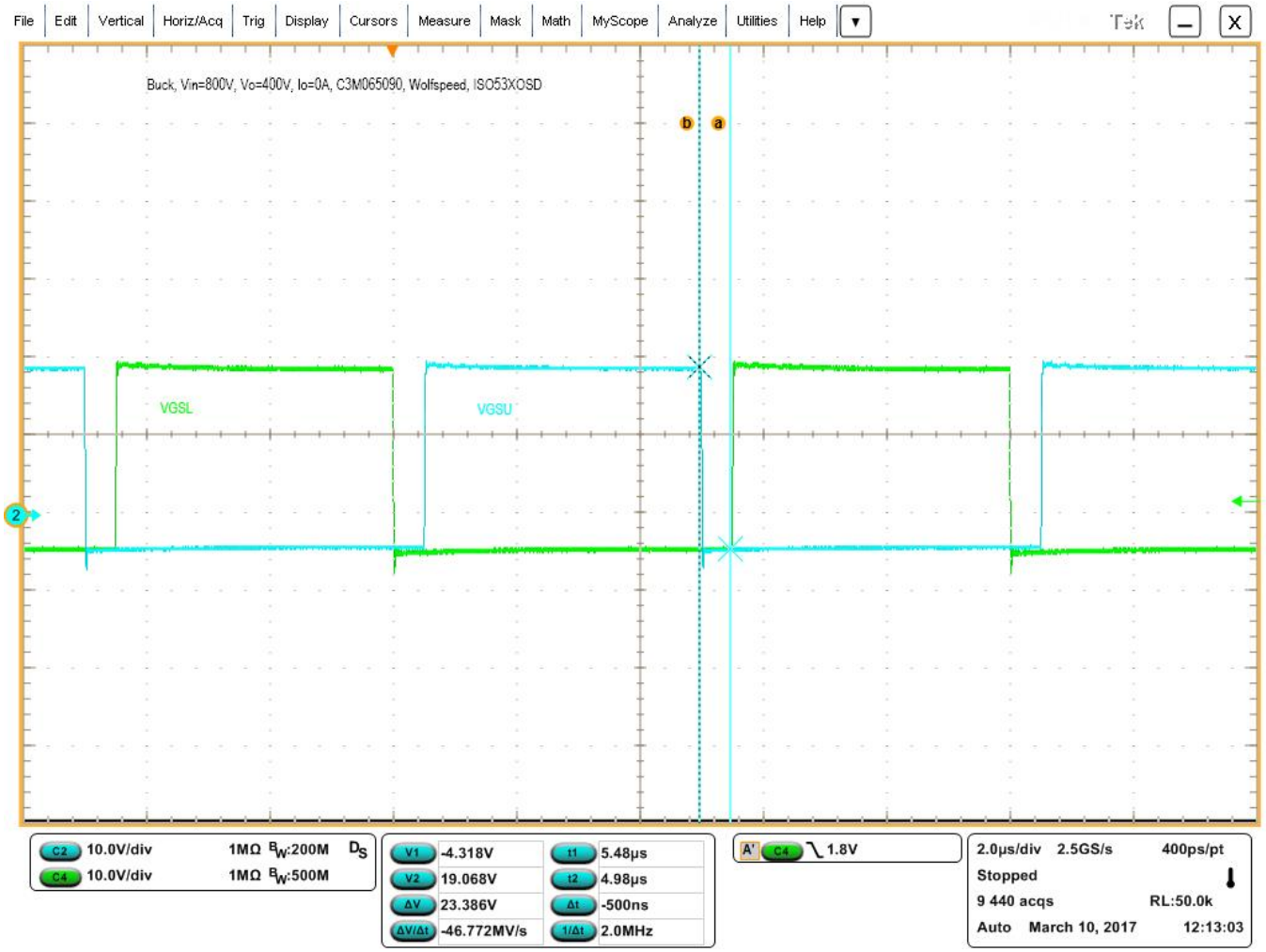

Figure 6. Gate-Source Driver Voltage

1. Expand the horizontal scale of oscilloscope from 2 µs/div to 10 ns/div, and verify rise and fall time of the driver board indicating high output current capability of UCC5390SCD driver ICs (Figure 7 and Figure 8).
2. Return to the initial horizontal scale 2 µs/div.
3. Set the electronic load to 0-A current.
4. Enable the high voltage power supply and gradually increase in voltage from 0 V to 800 V. The waveforms should look similar to Figure 9.
5. Explore the rising and falling edges of the phase node (Vds of lower FET) by changing horizontal scale to 100 ns/div. as it is shown in Figure 10 and Figure 11. Verify that at 0-A load both edges are under soft switching with minimum ringing.
6. Return to the initial horizontal scale 2 µs/div.
7. Gradually increase the load current up to 1.0 A. The waveforms should look similar to Figure 9. Explore the rising and falling edges of the phase node (Vds of lower FET) by changing horizontal scale to 10 ns/div for rising edge and 100 ns/div. for falling edge as it is shown in Figure 13 and Figure 14.
8. Verify that at load 1.0 A, the rising edge is under hard switching with increased ringing versus the falling edge that is under soft switching.
9. Return to the initial horizontal scale 2 µs/div.
10. Gradually reduce the voltage of the high voltage supply down to 0 V.
11. Disable channel A and channel B of function generator.

12. Reduce the voltage of the low voltage supply down to 0 A.

Power down is complete.

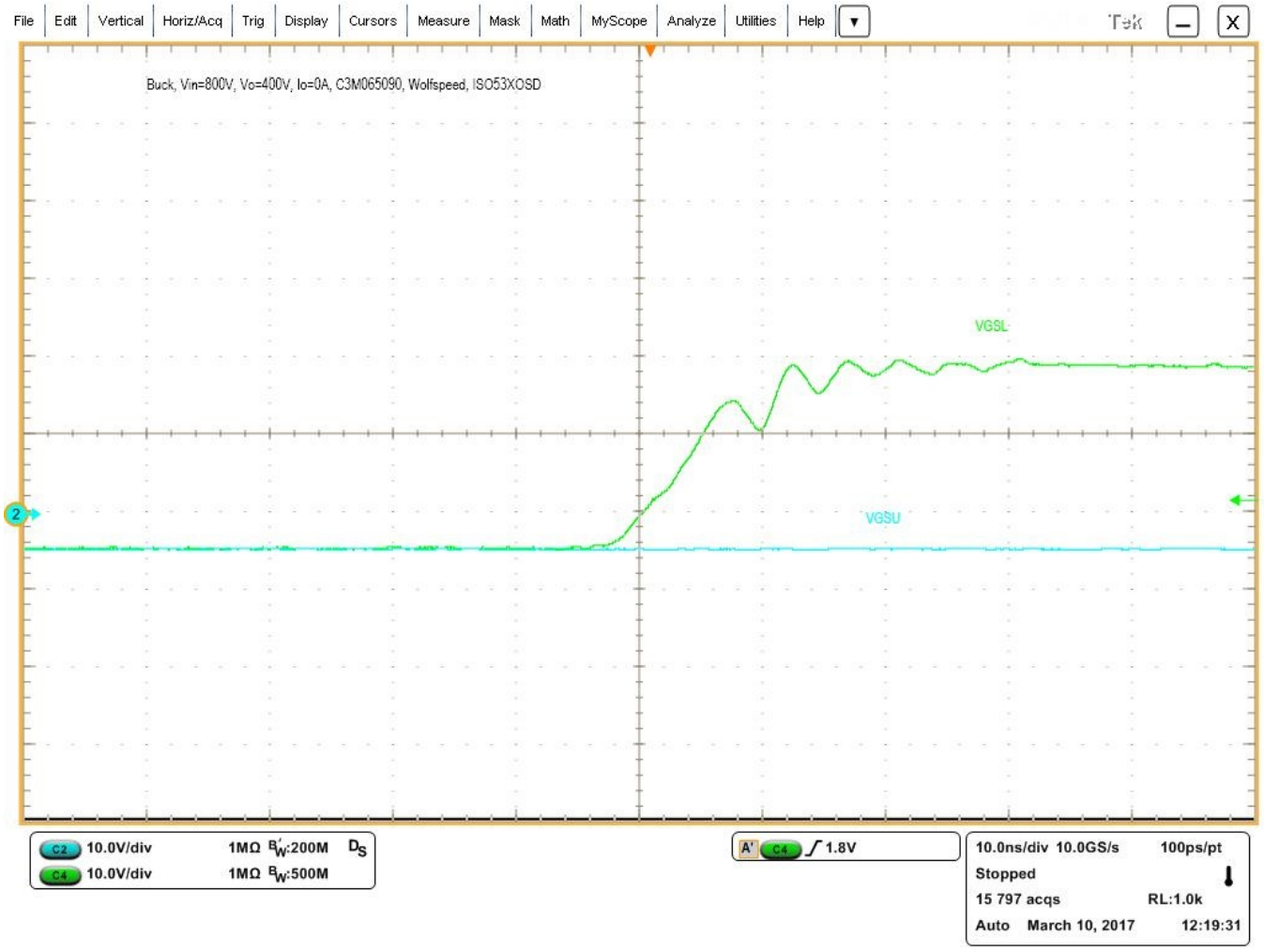

Figure 7. Expanded Gate-Source Drive Voltage Rise Time

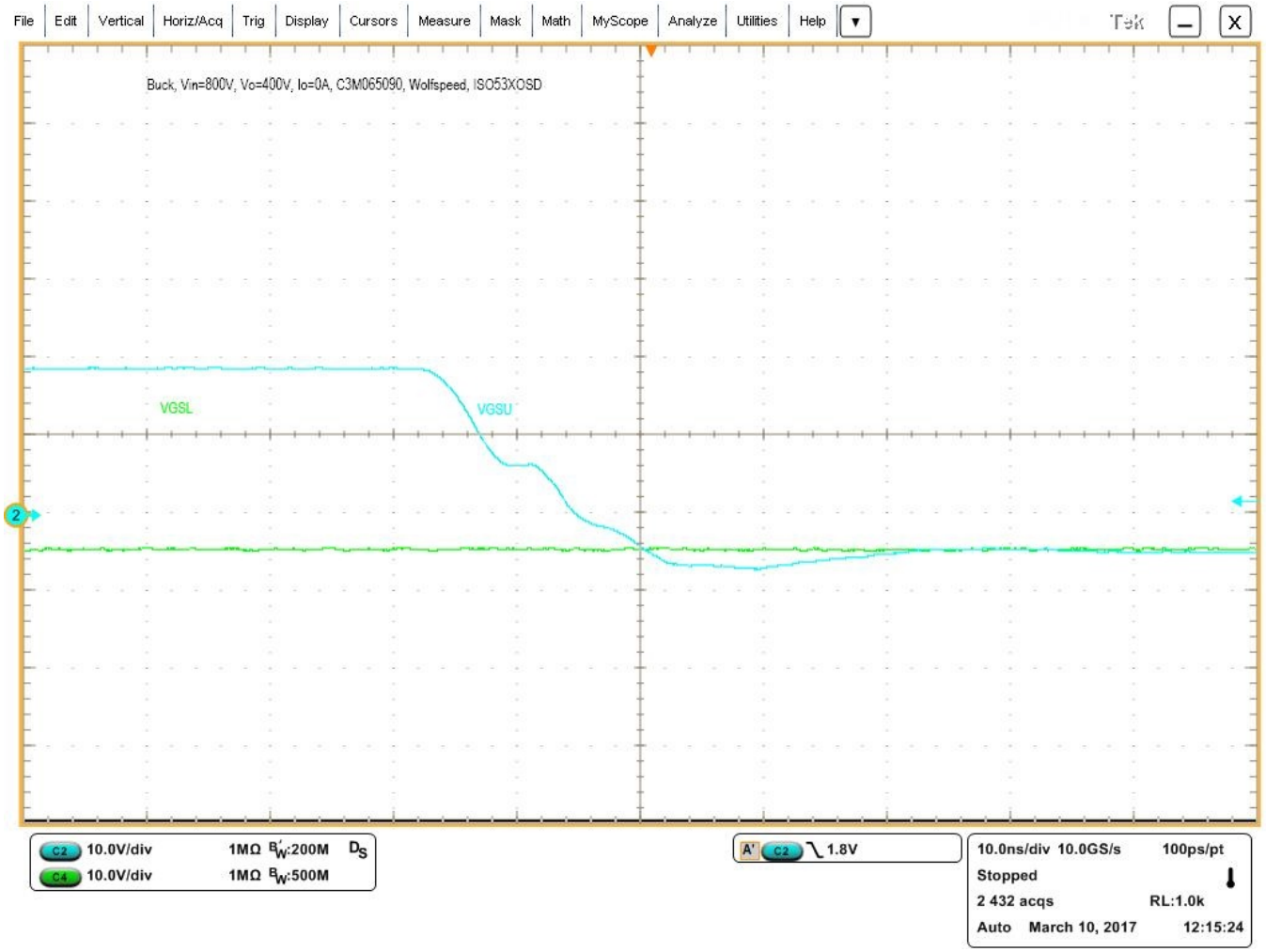

Figure 8. Expanded Gate-Source Drive Voltage Fall Time

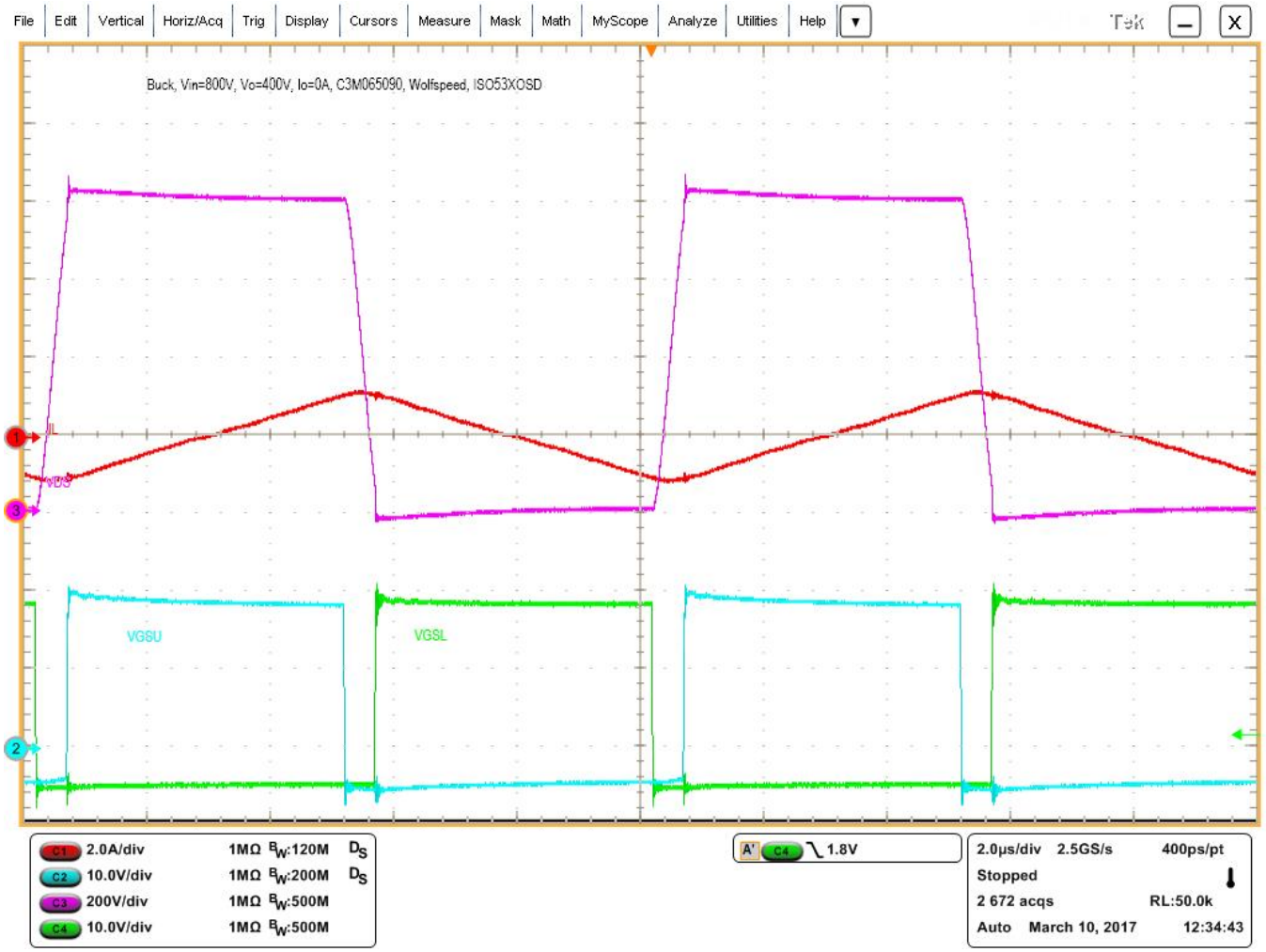

Figure 9. Inductor Current (Red), Drain-Source (Pink) and Gate-Source Drive Voltages (Blue and Green) at 800-V Input, 0-A Output

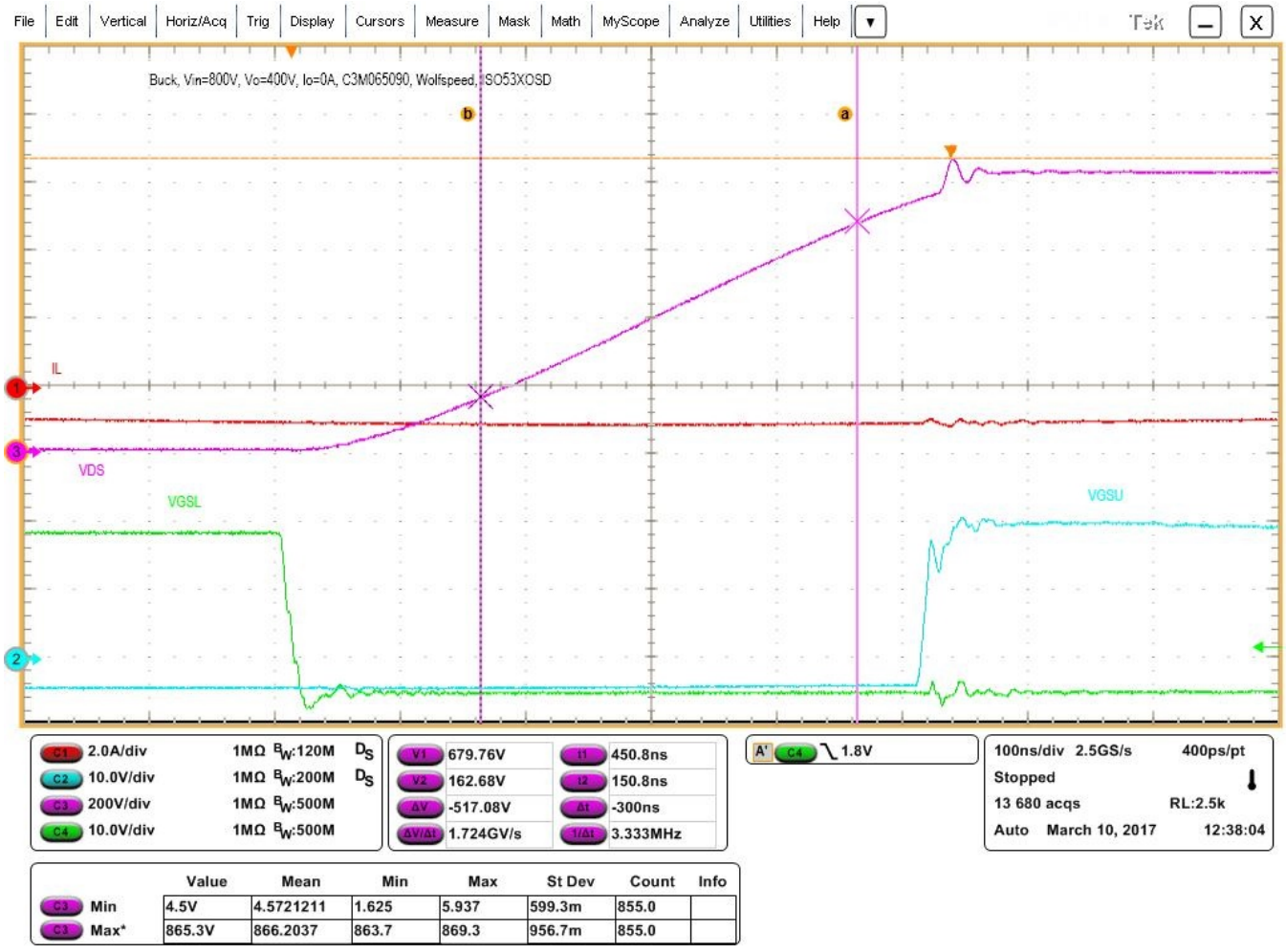

Figure 10. Expanded Soft Switching Waveforms During Vds Rise

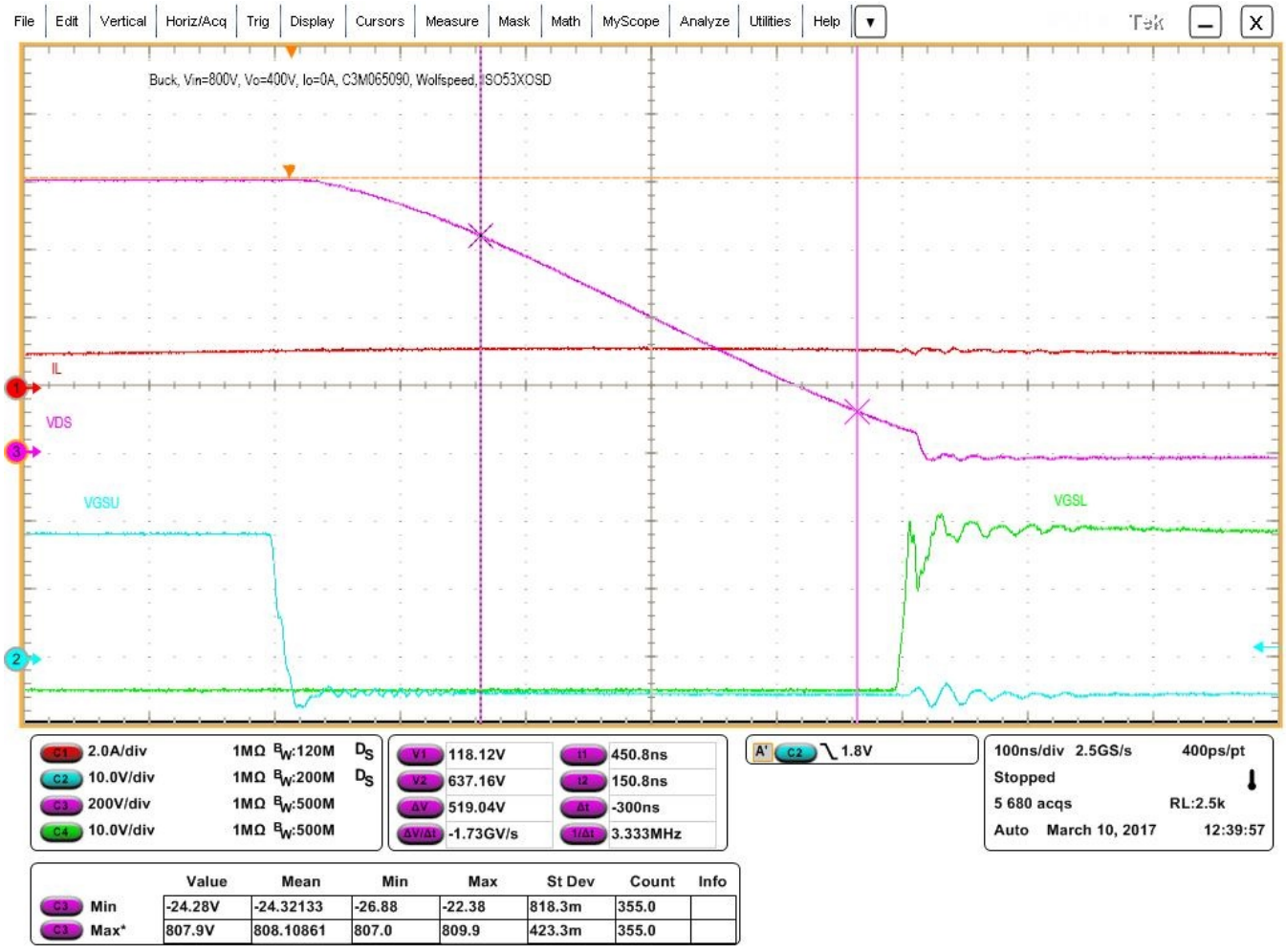

Figure 11. Expanded Soft Switching Waveforms During Vds Fall

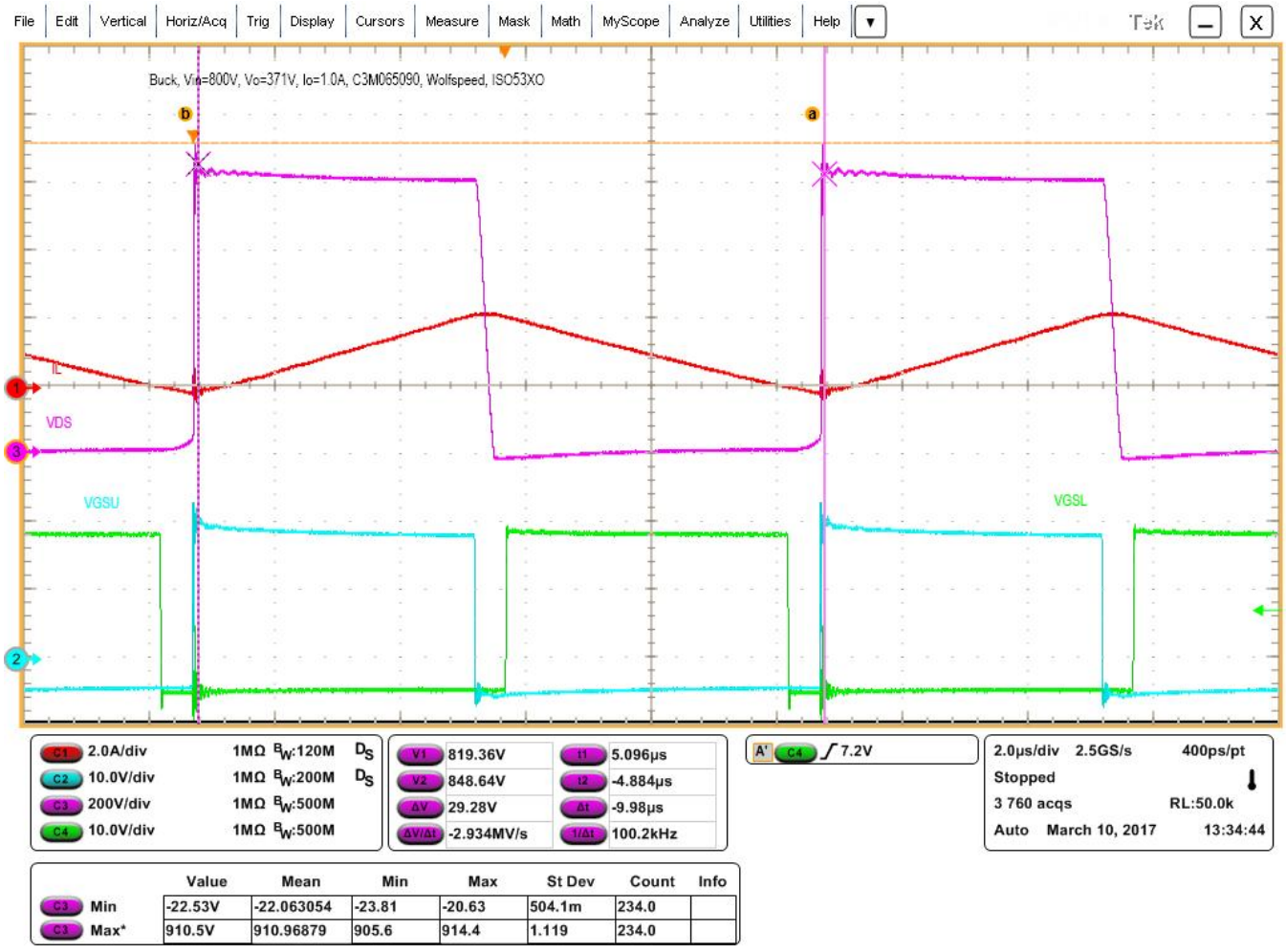

Figure 12. Inductor Current (Red), Drain-Source (Pink) and Gate-Source Drive Voltages (Blue and Green) at 800-V Input, 1.0-A Output

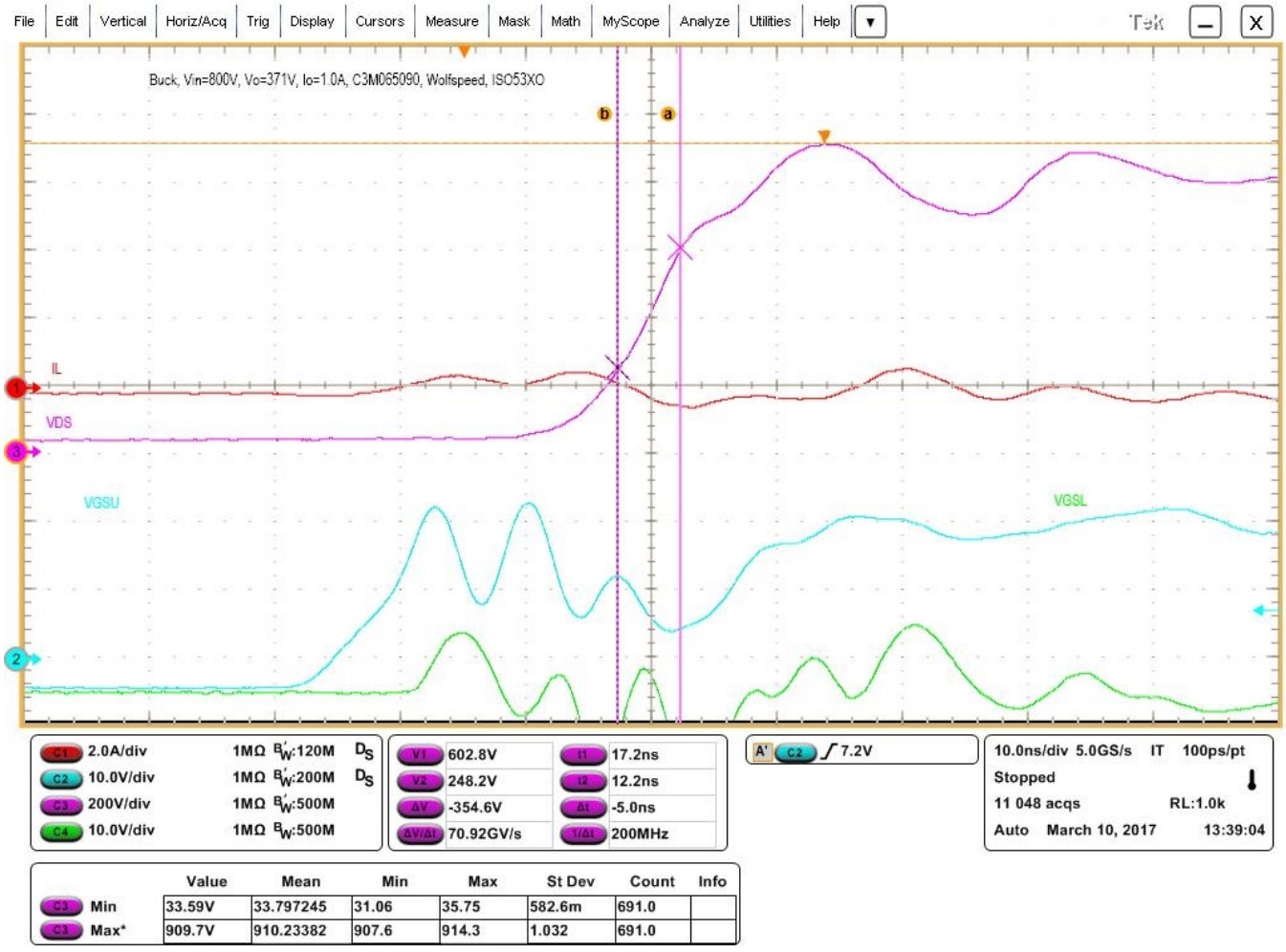

Figure 13. Expanded Hard, 71 V per ns Switching Waveforms During Vds Rise

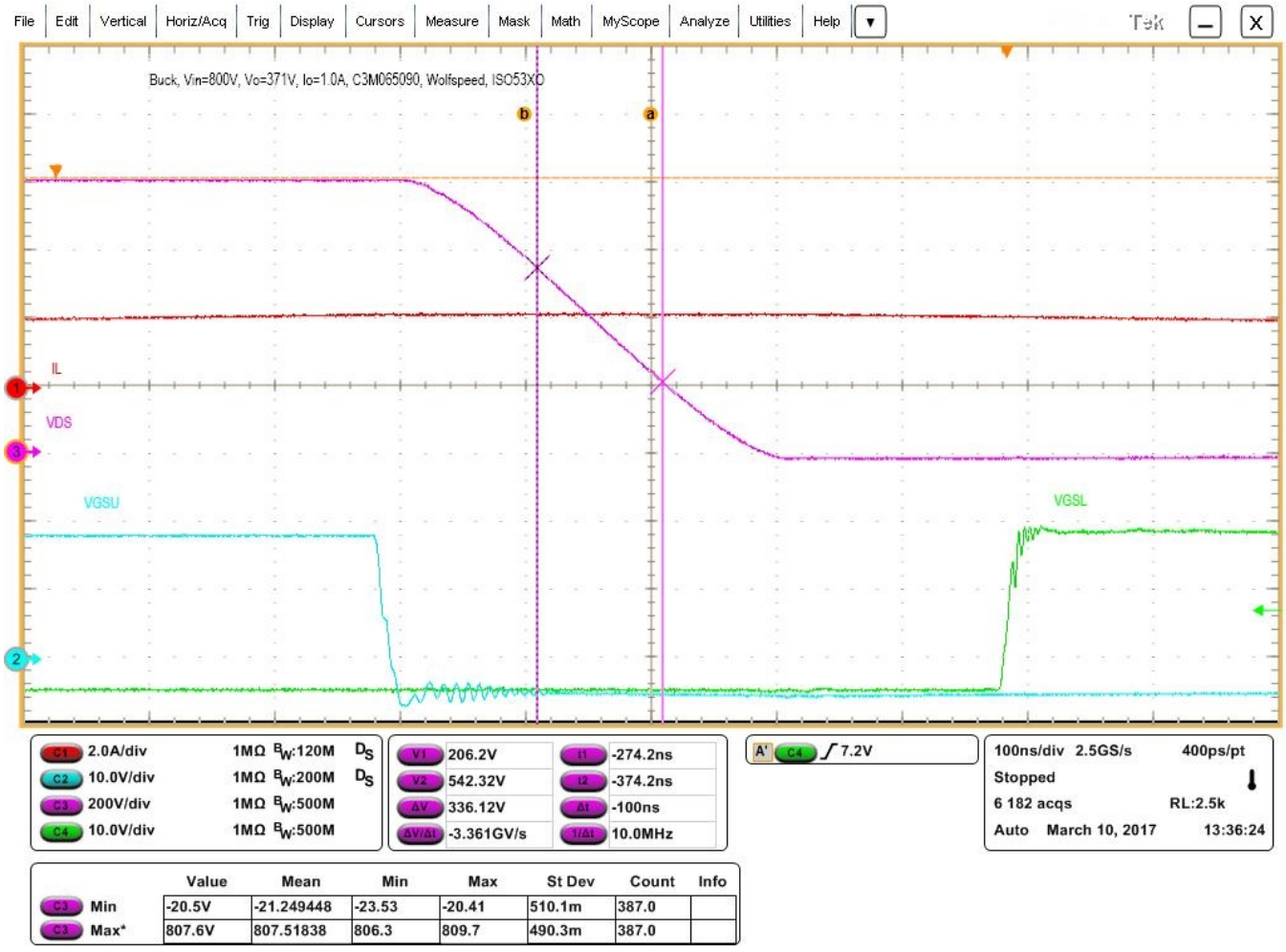

Figure 14. Expanded Soft, 3.4 V per ns Switching Waveforms During Vds Fall

7 Bias Supply Performance

This section shows the bias supply efficiency, voltage regulation, and switching waveforms at different configurations. These measurements have been fulfilled only with the bias supply components populated onboard to avoid the impact of the driver circuit.

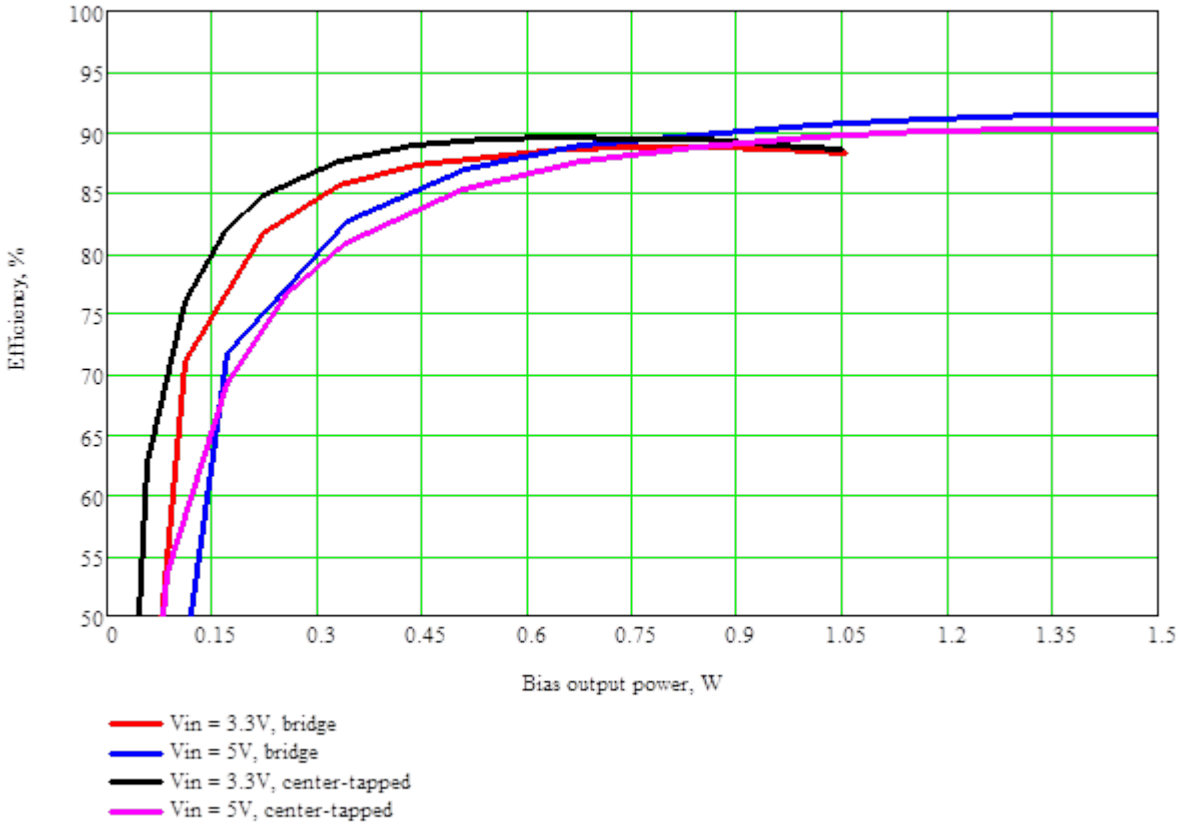

Figure 15. Bias Supply Efficiency at Different Configurations

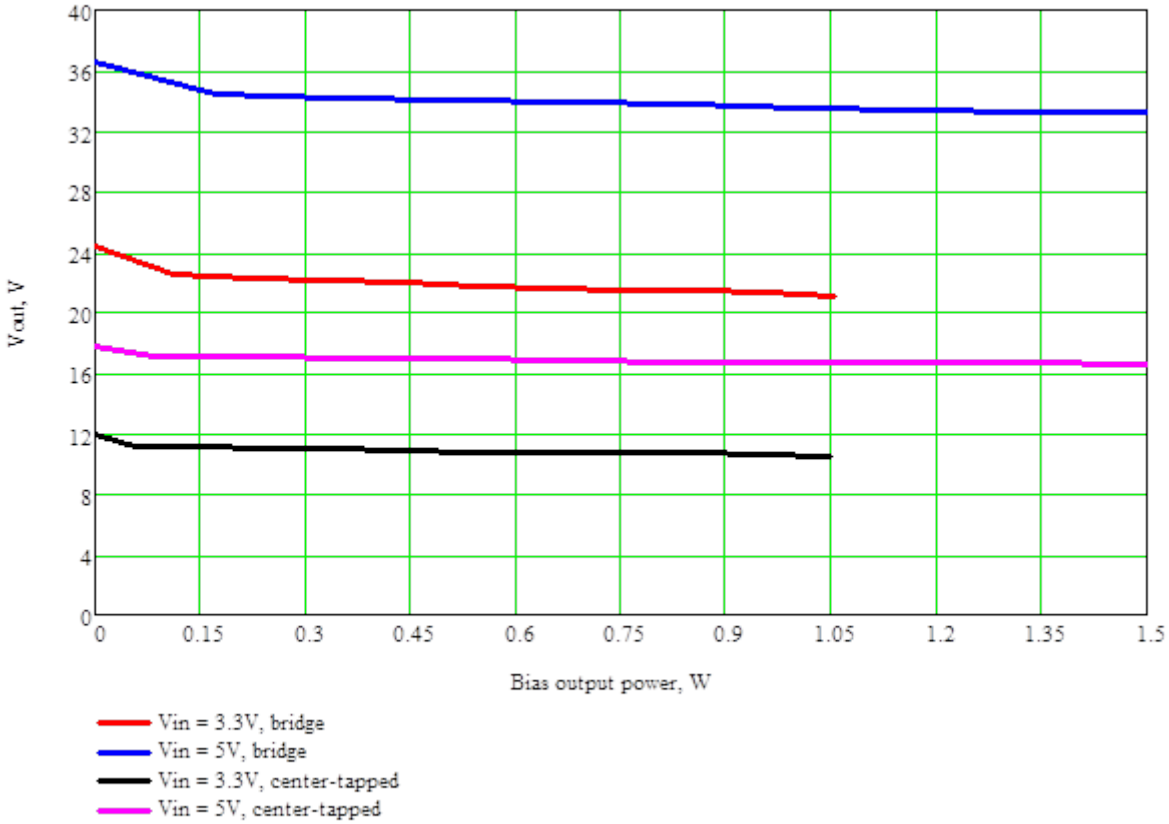

Figure 16. Bias Supply Regulation at Different Configurations

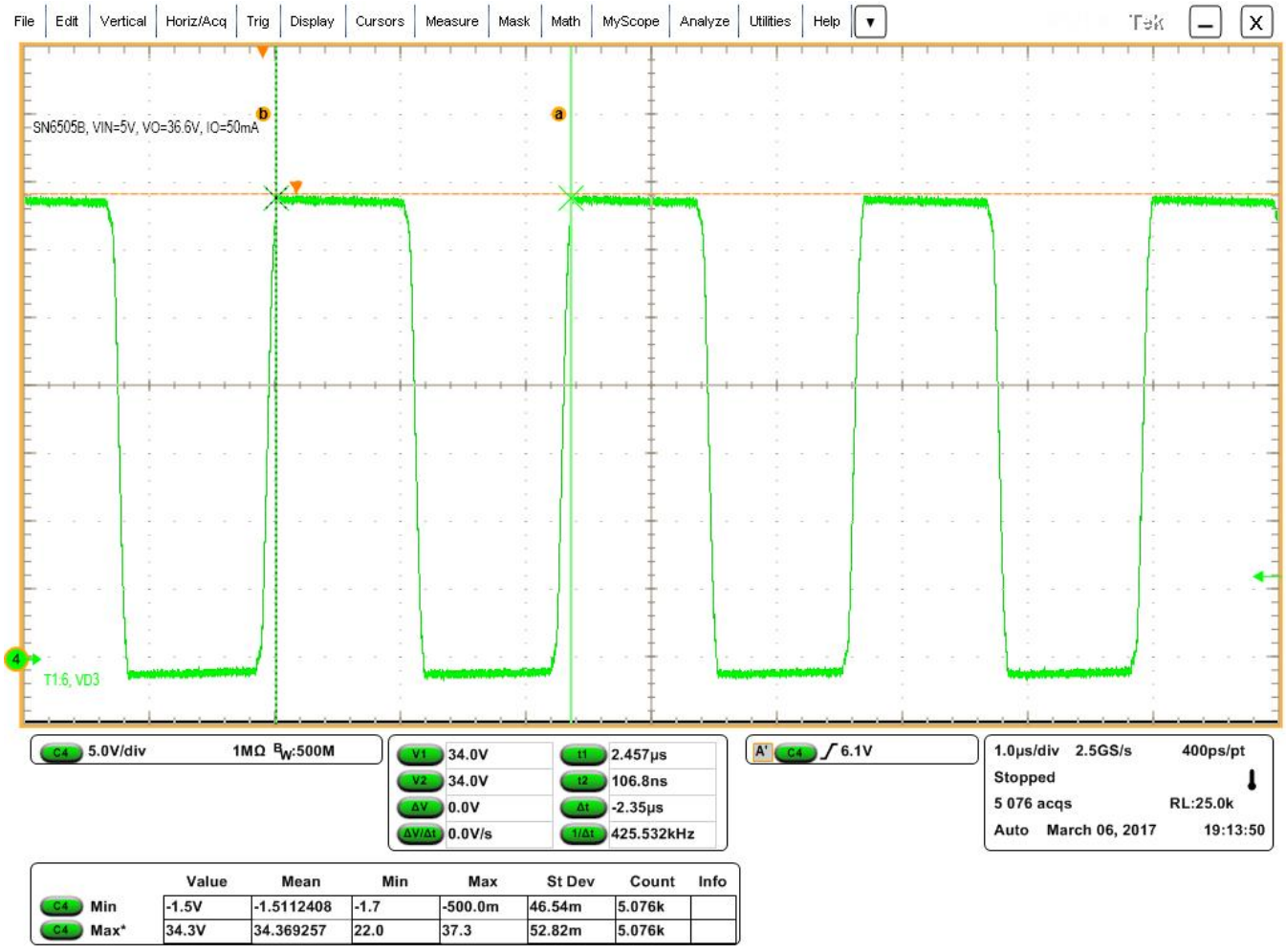

Figure 17. Bias Supply Secondary Side Switching Waveforms

8 Bill of Materials

Table 6. Bill of Materials

Designator	QTY	Value	Package Reference	Part Number	Manufacturer	Description	Alternate Part Number	Alternate Manufacturer
C3, C4	2	0.1 µF	1206	12061C304JAT2A	AVX	Capacitor, ceramic, 0.1 µF, 100 V, ±5%, X7R, 1206	885012208118	Wurth Electronic
C1, C2	2	91 pF	0402	GRM1555C3H910JA01D	MuRata	Capacitor, ceramic, 91 pF, 50 V, ±5%, C0G/NP0, 0402		
C7	1	10 µF	0805	GRM21BZ71E106KE15L	MuRata	Capacitor, ceramic, 10 µF, 25 V, ±10%, X7R, 0805		
C6, C10	2	0.1 µF	0402	C1005X7R1H104K050BB	TDK	Capacitor, ceramic, 0.1 µF, 50 V, ±10%, X7R, 0402		
C9	1	10 µF	0805	GRM21BR6YA106KE43L	MuRata	Capacitor, ceramic, 10 µF, 35 V, ±10%, X5R, 0805		
C11, C8	2	0.1 µF	0402	GRM155R61A104KA01D	MuRata	Capacitor, ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402	885012105010	Wurth Electronic
C5	1	100 pF	0603	0603ZC102KAT2A	AVX	Capacitor, ceramic, 1 PF, 10 V, ±10%, X7R, 0603	885012206008	Wurth Electronic
D5	1	4.3 V	SOD-523	BZT52C4V3T-7	Diodes, Inc	Diode, Zenner, 4.3 V, 300 mW, SOD-523		
D1, D2, D3, D4	4	40 V	SOD-523	B0540WS-7	Diodes, Inc	Diode, Schottky, 40 V, 0.5 A, SOD-323		
J1	1			TSW-104-08-G-S-RA	Samtec	Header, 100 mill, 4 × 1, Gold, R/A, TH	61300411021	Wurth Electronic
Q1	N/P		Footprint only	C2M1000170D	Cree	MOSFET, N-CH, 1700 V 5 A, TO-247		
Q2	N/P		Footprint only	IPP60R299CPXKSA1	Infineon technologies	MOSFET, N-CH, 600 V 11 A, TO-220AB		
R1, R4	2	1	0805	CRCW08051R00JNEA	Vishay-Dale	RES, 1.0, 5%, 0.125 W, 0805		
R2,R3	2	100	0402	CRCW0402100RFKED	Vishay-Dale	RES, 100, 1%, 0.063 W, 0402		
R5	1	4.02 k	0805	CRCW08054K02FKEA	Vishay-Dale	RES, 4.02 k, 1%, 0.125 W, 0805		
R7, R6	2	0	0603	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603		
T1	1			750342879	Würth Elektronik	Transformer, 50 uH, SMT	GT17005	ICE Components
U1	1		Texas Instruments	UCC5390SCD	Texas Instruments	0.5, 2, 4, 6 A, 10-A Isolated IGBT Gate Drivers with High CMTI, D0008B (SOIC-8)		
U2	1		Texas Instruments	SN6505BDBVR	Texas Instruments	Low-noise, 1 A, 420-KHz Transformer Driver, DBV0006A (SOT-6)		

9 Layout Diagrams

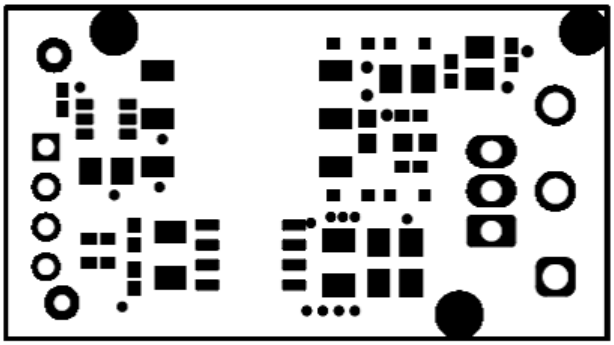

Figure 18. Top Solder Mask

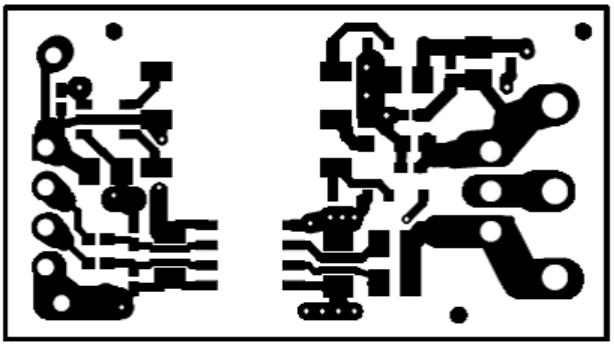

Figure 19. Top Layer

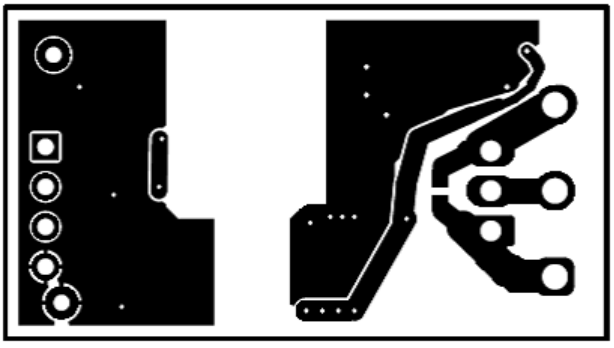

Figure 20. Bottom Layer

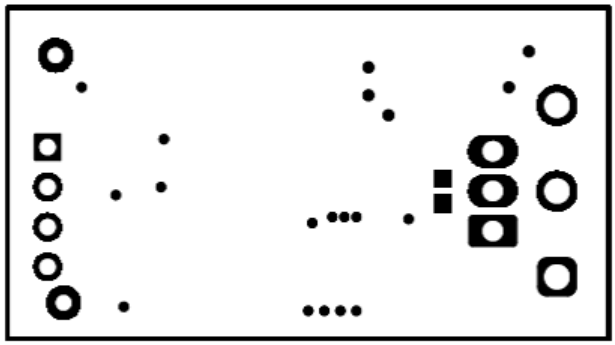

Figure 21. Bottom Solder Mask

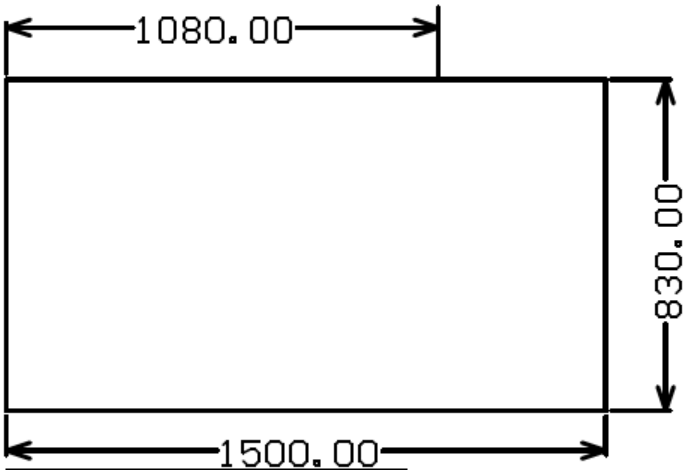

Figure 22. Mechanical Dimensions

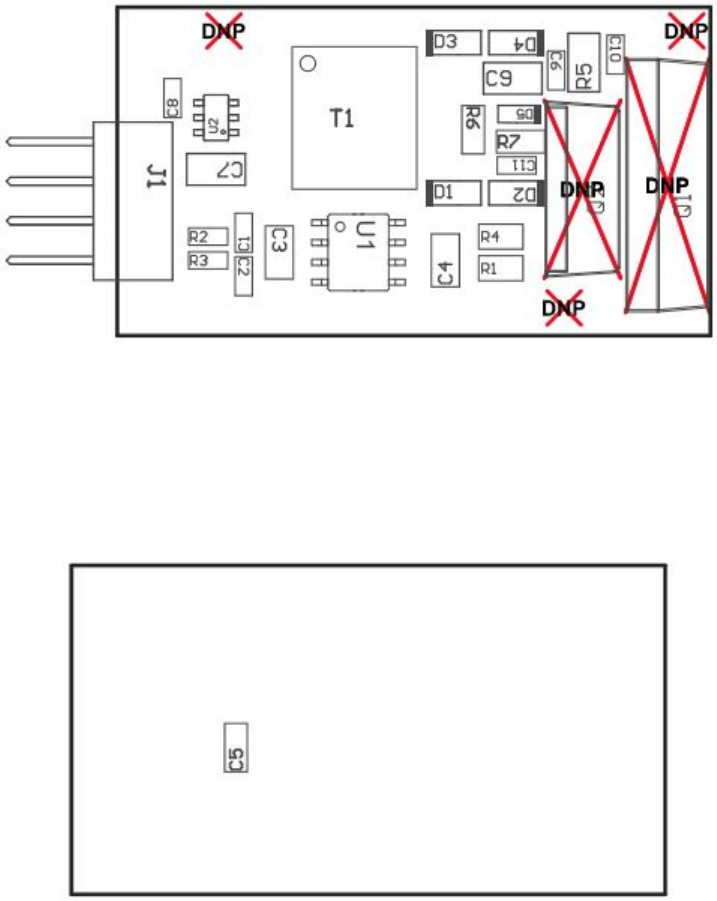

Figure 23. Assembly Drawings

10 References

- Texas Instruments, UCC5390 Product Folder
- Texas Instruments, SN6505B Product Folder

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2017) to A Revision	Page
• Changed Expanded Hard, 71 V per ns Switching Waveforms During 3.4 V per ns Vds Fall image to Expanded Soft, 3.4 V per ns Switching Waveforms During Vds Fall image	20
• Added alternate part number and alternate manufacturer columns to BOM	24

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3 *Regulatory Notices:*

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

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4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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