



**THE DATASHEET OF
NCV2393DR2G**



NCV2393, TS393

Micropower Dual CMOS Voltage Comparator

The NCV2393 and TS393 are micropower CMOS dual voltage comparators. They feature extremely low consumption of 6 μA typical per comparator and operate over a wide temperature range of $T_A = -40$ to 125°C . The NCV2393 and TS393 are available in an SOIC-8 package.

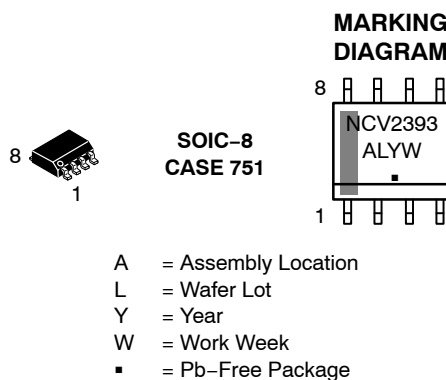
Features

- Extremely Low Supply Current: 6 μA Typical Per Channel
- Wide Supply Range: 2.7 to 16 V
- Extremely Low Input Bias Current: 1 pA Typical
- Extremely Low Input Offset Current: 1 pA Typical
- Input Common Mode Range Includes V_{SS}
- High Input Impedance: $10^{12} \Omega$
- Pin-to-Pin Compatibility with Dual Bipolar LM393
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

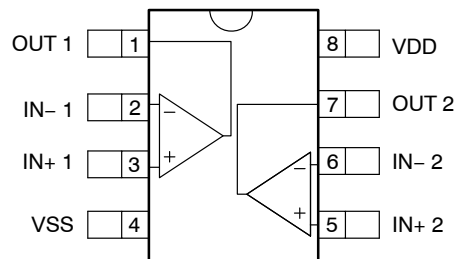


ON Semiconductor®

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PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|---------------------|--------------------|
| NCV2393DR2G | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| TS393DR2G | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PIN DESCRIPTION

| Pin | Name | Type | Description |
|-----|-------|--------|--|
| 1 | OUT 1 | Output | Output of comparator 1. The open-drain output requires an external pull-up resistor. |
| 2 | IN- 1 | Input | Inverting input of comparator 1 |
| 3 | IN+ 1 | Input | Non-inverting input of comparator 1 |
| 4 | VSS | Power | Negative supply |
| 5 | IN+ 2 | Input | Non-inverting input of comparator 2 |
| 6 | IN- 2 | Input | Inverting input of comparator 2 |
| 7 | OUT 2 | Output | Output of comparator 2. The open-drain output requires an external pull-up resistor. |
| 8 | VDD | Power | Positive supply |

ABSOLUTE MAXIMUM RATINGS (Note 1)

Over operating free-air temperature, unless otherwise stated

| Parameter | Limit | Unit |
|---|-------|------|
| Supply Voltage, V_S ($V_{DD}-V_{SS}$) | 18 | V |

INPUT AND OUTPUT PINS

| | | |
|---|----------|----|
| Input Voltage (Note 2) | 18 | V |
| Input Differential Voltage, V_{ID} (Note 3) | ± 18 | V |
| Input Current (through ESD protection diodes) | 50 | mA |
| Output Voltage | 18 | V |
| Output Current | 20 | mA |

TEMPERATURE

| | | |
|----------------------|-------------|----|
| Storage Temperature | -65 to +150 | °C |
| Junction Temperature | 150 | °C |

ESD RATINGS

| | | |
|------------------|------|---|
| Human Body Model | 1500 | V |
| Machine Model | 50 | V |

LATCH-UP RATINGS

| | | |
|------------------|-----|----|
| Latch-up Current | 100 | mA |
|------------------|-----|----|

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Stresses beyond the absolute maximum ratings can lead to reduced reliability and damage.
- Excursions of input voltages may exceed the power supply level. As long as the common mode voltage [$V_{CM} = (V_{IN+} + V_{IN-})/2$] remains within the specified range, the comparator will provide a stable output state. However, the maximum current through the ESD diodes of the input stage must strictly be observed.
- Input differential voltage is the non-inverting input terminal with respect to the inverting input terminal. To prevent damage to the gates, each comparator includes back-to-back zener diodes between input terminals. When differential voltage exceeds 6.2 V, the diodes turn on. Input resistors of 1 k Ω have been integrated to limit the current in this event.
- This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per AEC-Q100-002 (JEDEC standard: JESD22-A114)
ESD Machine Model tested per AEC-Q100-003 (JEDEC standard: JESD22-A115)
Latch-up Current tested per JEDEC standard: JESD78.

THERMAL INFORMATION (Note 5)

| Thermal Metric | Symbol | Value | Unit |
|------------------------------|---------------|-------|------|
| Junction-to-Ambient (Note 6) | θ_{JA} | 190 | °C/W |
| Junction-to-Case Top | Ψ_{JT} | 107 | °C/W |

- Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
- Multilayer board, 1 oz. copper, 400 mm² copper area, both junctions heated equally

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OPERATING CONDITIONS

| Parameter | Symbol | Limit | Unit |
|--------------------------------------|--------|-------------|------|
| Supply Voltage ($V_{DD} - V_{SS}$) | V_S | +2.7 to +16 | V |
| Operating Free Air Temperature Range | T_A | -40 to +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_S = +3\text{ V}$

(**Boldface** limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, guaranteed by characterization and/or design.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------|--------|------------|-----|-----|-----|------|
|-----------|--------|------------|-----|-----|-----|------|

INPUT CHARACTERISTICS

| | | | | | | |
|-------------------------------|----------|---|----------------------------|-----|--------------------------------|----|
| Offset Voltage | V_{OS} | $V_{CM} = \text{mid-supply}$ | | 1.4 | 13 | mV |
| | | | | | 14 | mV |
| Input Bias Current (Note 7) | I_{IB} | $V_{CM} = \text{mid-supply}$ | | 1 | | pA |
| | | | | | 600 | pA |
| Input Offset Current (Note 7) | I_{OS} | $V_{CM} = \text{mid-supply}$ | | 1 | | pA |
| | | | | | 300 | pA |
| Input Common Mode Range | V_{CM} | | V_{SS} | | $V_{DD} - 1.5$ | V |
| | | | V_{SS} | | $V_{DD} - 2$ | V |
| Common Mode Rejection Ratio | CMRR | $V_{CM} = V_{SS}$ to $V_{CM} = V_{DD} - 1.5\text{ V}$ | | 70 | | dB |

OUTPUT CHARACTERISTICS

| | | | | | | |
|---------------------|----------|--|--|----------------|----------------------------------|----|
| Output Voltage Low | V_{OL} | $V_{ID} = -1\text{ V}$, $I_{OL} = +6\text{ mA}$ | | $V_{SS} + 300$ | $V_{SS} + 450$ | mV |
| | | | | | $V_{SS} + 700$ | mV |
| Output Current High | I_{OH} | $V_{ID} = +1\text{ V}$, $V_{OH} = +3\text{ V}$ | | 2 | 40 | nA |
| | | | | | 1000 | nA |

DYNAMIC PERFORMANCE

| | | | | | | |
|-------------------------------|-----------|---|----------------|-----|--|---------------|
| Propagation Delay Low to High | t_{PLH} | $V_{CM} = \text{mid-supply}$, $f = 10\text{ kHz}$, $R_{PU} = 5.1\text{ k}\Omega$, $C_L = 50\text{ pF}$ | 5 mV overdrive | 2.1 | | μs |
| | | | TTL input | 0.6 | | μs |
| Propagation Delay High to Low | t_{PHL} | $V_{CM} = \text{mid-supply}$, $f = 10\text{ kHz}$, $R_{PU} = 5.1\text{ k}\Omega$, $C_L = 50\text{ pF}$ | 5 mV overdrive | 3.9 | | μs |
| | | | TTL input | 0.2 | | μs |

POWER SUPPLY

| | | | | | | |
|------------------------------|----------|--------------------------------------|--|----|-----------|---------------|
| Power Supply Rejection Ratio | PSRR | $V_S = +3\text{ V}$ to $+5\text{ V}$ | | 70 | | dB |
| Quiescent Current | I_{DD} | Per channel, no load, output = LOW | | 6 | 15 | μA |
| | | | | | 20 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by characterization and/or design.

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ELECTRICAL CHARACTERISTICS: $V_S = +5\text{ V}$, unless otherwise noted

(**Boldface** limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, guaranteed by characterization and/or design.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------|--------|------------|-----|-----|-----|------|
|-----------|--------|------------|-----|-----|-----|------|

INPUT CHARACTERISTICS

| | | | | | | |
|----------------------------------|----------|--|----------|-----|----------------|----|
| Offset Voltage | V_{OS} | $V_{CM} = \text{mid-supply V}, V_S = 5\text{ V to } 10\text{ V}$ | | 1.4 | 13 | mV |
| | | | | | 14 | mV |
| Input Bias Current (Note 8) | I_{IB} | $V_{CM} = \text{mid-supply}$ | | 1 | | pA |
| | | | | | 600 | pA |
| Input Offset Current (Note 8) | I_{OS} | $V_{CM} = \text{mid-supply}$ | | 1 | | pA |
| | | | | | 300 | pA |
| Input Common Mode Range | V_{CM} | | V_{SS} | | $V_{DD} - 1.5$ | V |
| | | | V_{SS} | | $V_{DD} - 2$ | V |
| Common Mode Rejection Ratio | CMRR | $V_{CM} = V_{SS}$ to $V_{CM} = V_{DD} - 1.5\text{ V}$ | | 71 | | dB |

OUTPUT CHARACTERISTICS

| | | | | | | |
|---------------------|----------|---|--|----------------|----------------------------------|----|
| Output Voltage Low | V_{OL} | $V_{ID} = -1\text{ V}, I_{OL} = +6\text{ mA}$ | | $V_{SS} + 260$ | $V_{SS} + 350$ | mV |
| | | | | | $V_{SS} + 550$ | mV |
| Output Current High | I_{OH} | $V_{ID} = +1\text{ V}, V_{OH} = +5\text{ V}$ | | 2 | 40 | nA |
| | | | | | 1000 | nA |

DYNAMIC PERFORMANCE

| | | | | | | |
|----------------------------------|------------|--|-----------------|-----|--|---------------|
| Fall Time | t_{FALL} | 50 mV overdrive, $f = 10\text{ kHz}, R_{PU} = 5.1\text{ k}\Omega,$ $C_L = 50\text{ pF}$ | | 25 | | ns |
| Propagation Delay Low to High | t_{PLH} | $V_{CM} = \text{mid-supply},$ $f = 10\text{ kHz}, R_{PU} = 5.1\text{ k}\Omega,$ $C_L = 50\text{ pF}$ | 5 mV overdrive | 2.1 | | μs |
| | | | 10 mV overdrive | 1.2 | | μs |
| | | | 20 mV overdrive | 0.8 | | μs |
| | | | 40 mV overdrive | 0.5 | | μs |
| | | | TTL input | 0.6 | | μs |
| Propagation Delay High to Low | t_{PHL} | $V_{CM} = \text{mid-supply},$ $f = 10\text{ kHz}, R_{PU} = 5.1\text{ k}\Omega,$ $C_L = 50\text{ pF}$ | 5 mV overdrive | 5.8 | | μs |
| | | | 10 mV overdrive | 3.2 | | μs |
| | | | 20 mV overdrive | 1.7 | | μs |
| | | | 40 mV overdrive | 1.0 | | μs |
| | | | TTL input | 0.3 | | μs |

POWER SUPPLY

| | | | | | | |
|---------------------------------|----------|--------------------------------------|--|----|-----------|---------------|
| Power Supply Rejection Ratio | PSRR | $V_S = +5\text{ V to } +10\text{ V}$ | | 80 | | dB |
| Quiescent Current | I_{DD} | Per channel, no load, output = LOW | | 6 | 15 | μA |
| | | | | | 20 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by characterization and/or design

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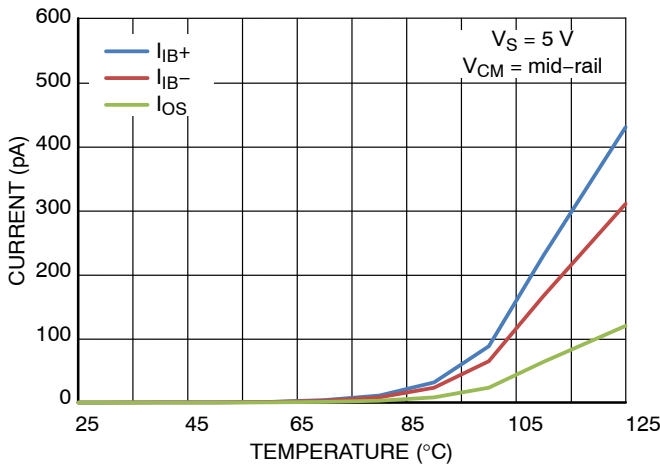


Figure 1. I_{IB} and I_{OS} vs. Temperature

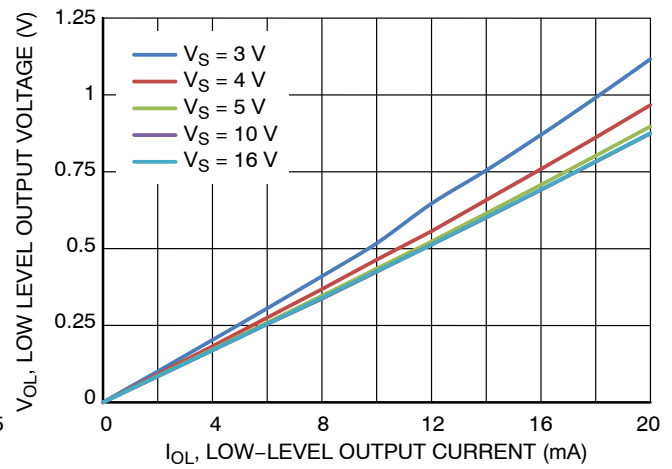


Figure 2. V_{OL} vs. I_{OL}

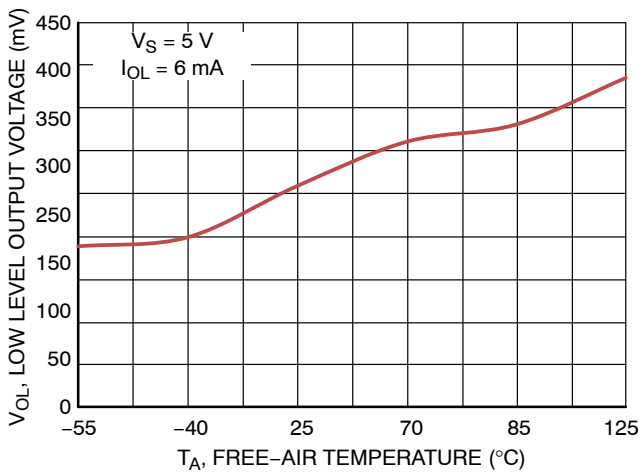


Figure 3. V_{OL} vs. Temperature

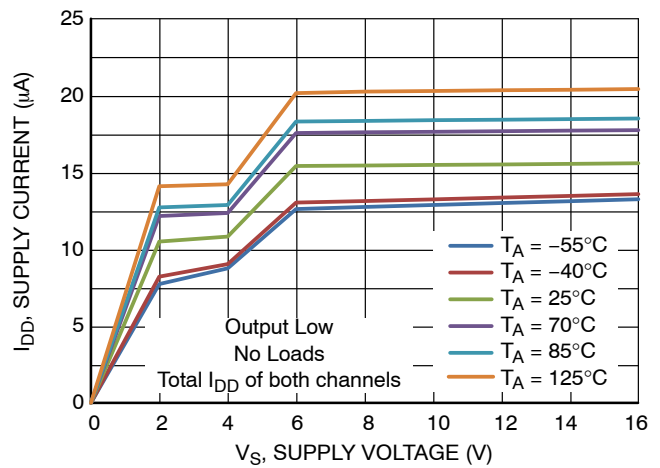


Figure 4. I_{DD} vs. V_S

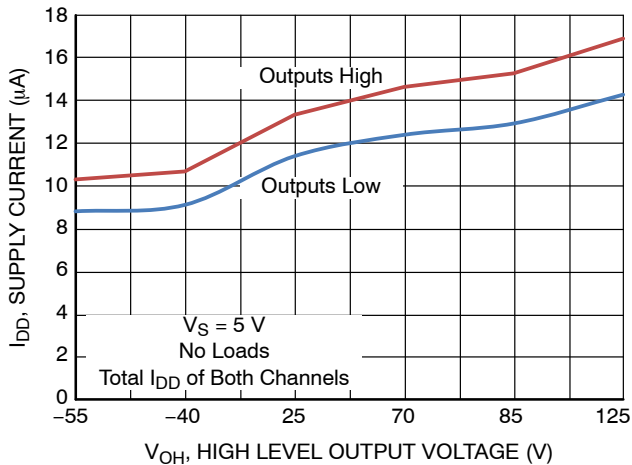


Figure 5. I_{DD} vs. Temperature

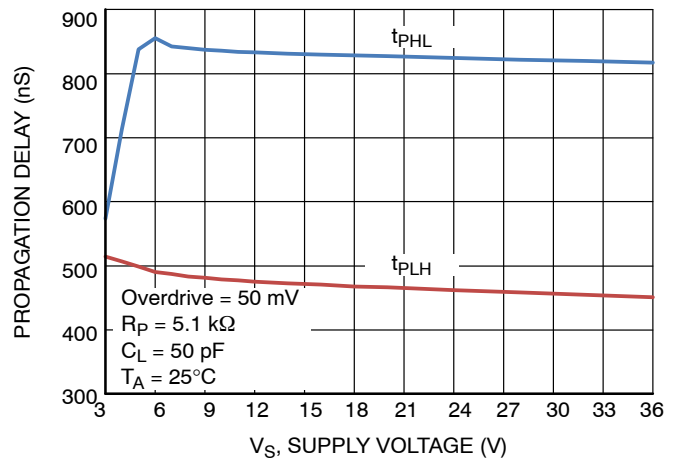


Figure 6. Propagation Delay vs. V_S

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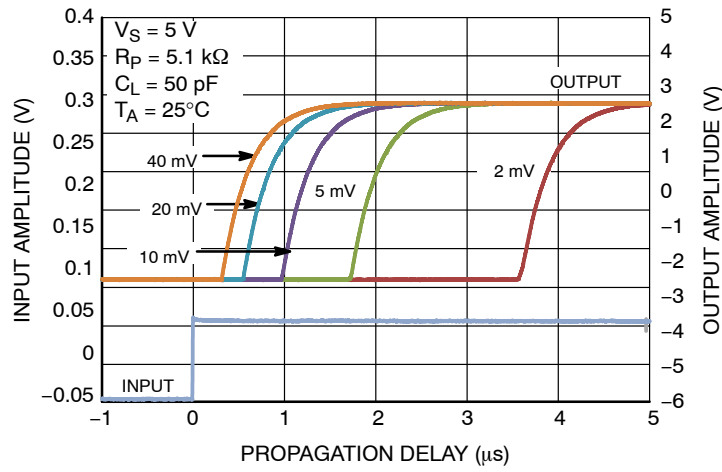


Figure 7. t_{pLH} vs. Overdrive

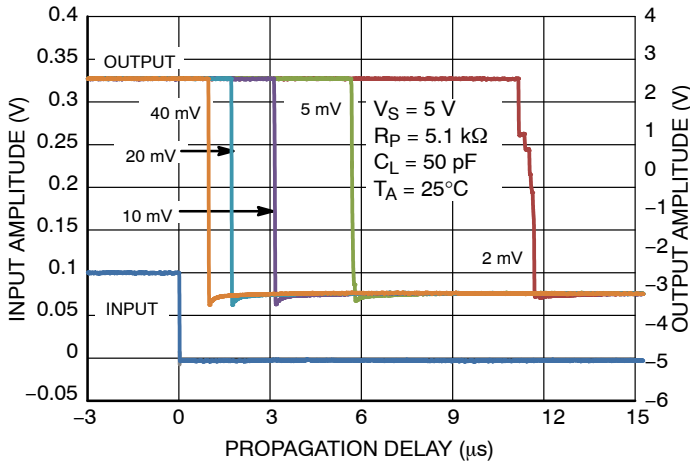


Figure 8. t_{pHL} vs. Overdrive

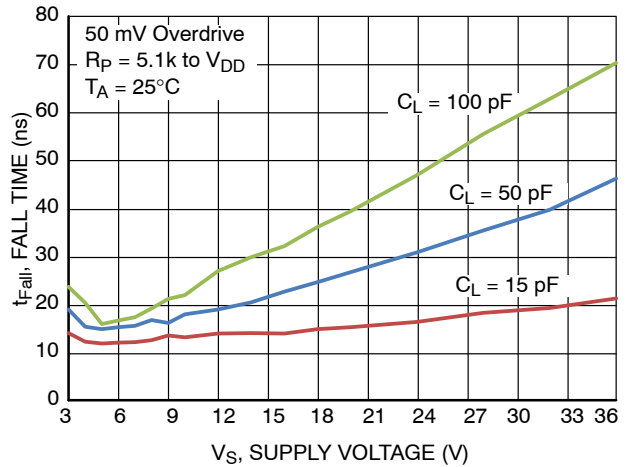


Figure 9. Fall Time vs. V_S

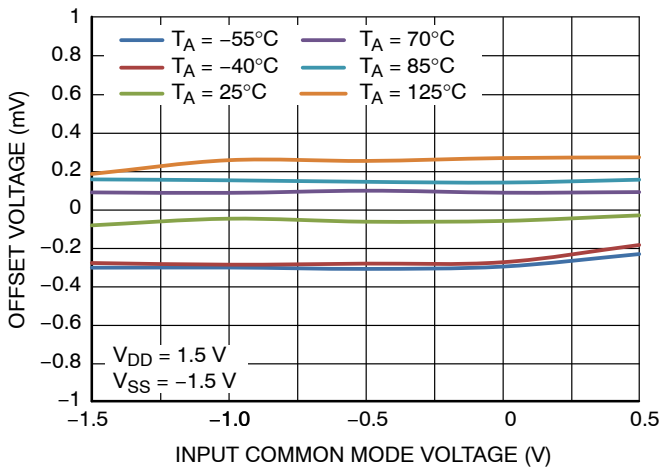


Figure 10. V_{OS} vs. V_{CM} ($V_S = 3 V$)

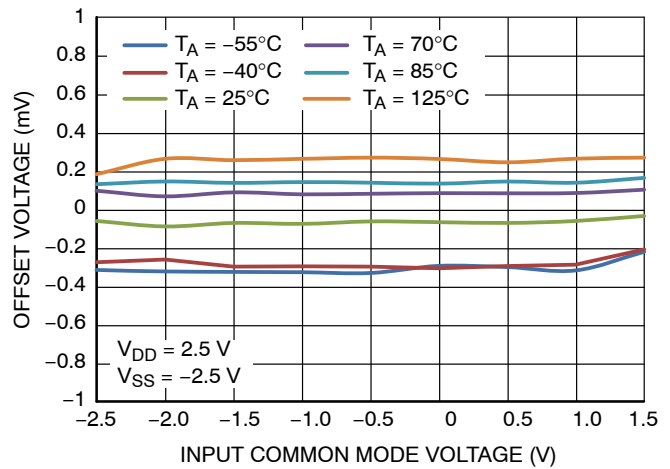
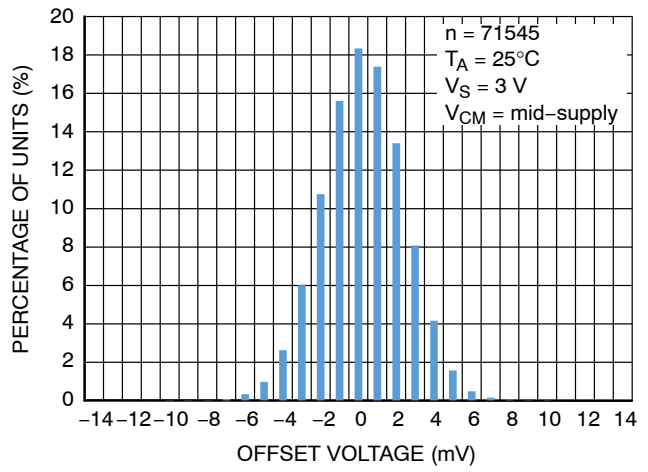
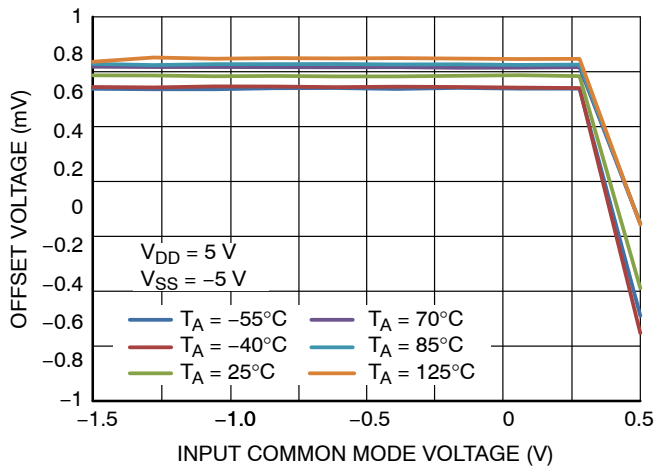


Figure 11. V_{OS} vs. V_{CM} ($V_S = 5 V$)

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

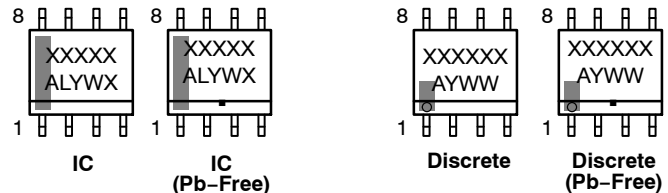
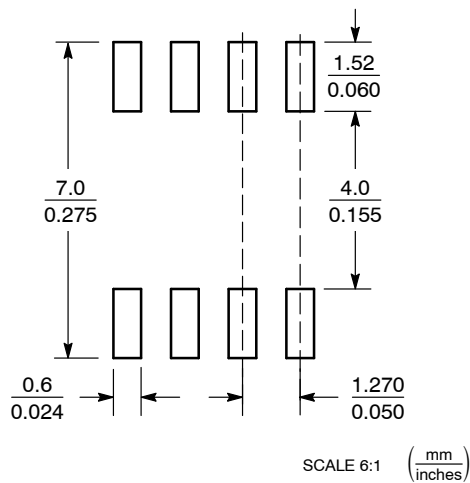


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

GENERIC MARKING DIAGRAM*

SOLDERING FOOTPRINT*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

| | | |
|------------------|-------------|--|
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| DESCRIPTION: | SOIC-8 NB | PAGE 1 OF 2 |

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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| DESCRIPTION: | SOIC-8 NB | PAGE 2 OF 2 |

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