



**THE DATASHEET OF
ESD201B203LRHE6327XTSA1**



TVS Diode

Transient Voltage Suppressor Diodes

ESD201-B2-03LRH

Bi-directional Dual Diode for ESD/Transient Protection

ESD201-B2-03LRH

Data Sheet

Revision 1.1, 2012-09-26
Final

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Revision History: Rev. 1.0, 2012-09-19

Page or Item	Subjects (major changes since previous revision)
Revision 1.1, 2012-09-26	
3	Small changes in the Features

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Last Trademarks Update 2010-10-26

1 Bi-directional Dual Diode for ESD / Transient Protection

1.1 Features

- ESD / Transient protection of signal lines according to:
 - IEC61000-4-2 (ESD): ± 20 kV (air/contact discharge)
 - IEC61000-4-4 (EFT): 40 A (5/50 ns)
 - IEC61000-4-5 (surge): 2.5 A (8/20 μ s)
- Dual diode with small form factor of 0402 package size
- Bi-directional, symmetrical working voltage: $V_{RWM} = \pm 5.5$ V max.
- Low capacitance: $C_L = 5$ pF typ
- Very low clamping voltage, low dynamic resistance down to: $R_{DYN} = 0.22$ typ
- Pb-free (RoHS compliant) and halogen free package



1.2 Application Examples

- ESD protection to keypad, touchpad, buttons, audio lines, ect.

1.3 Product Description

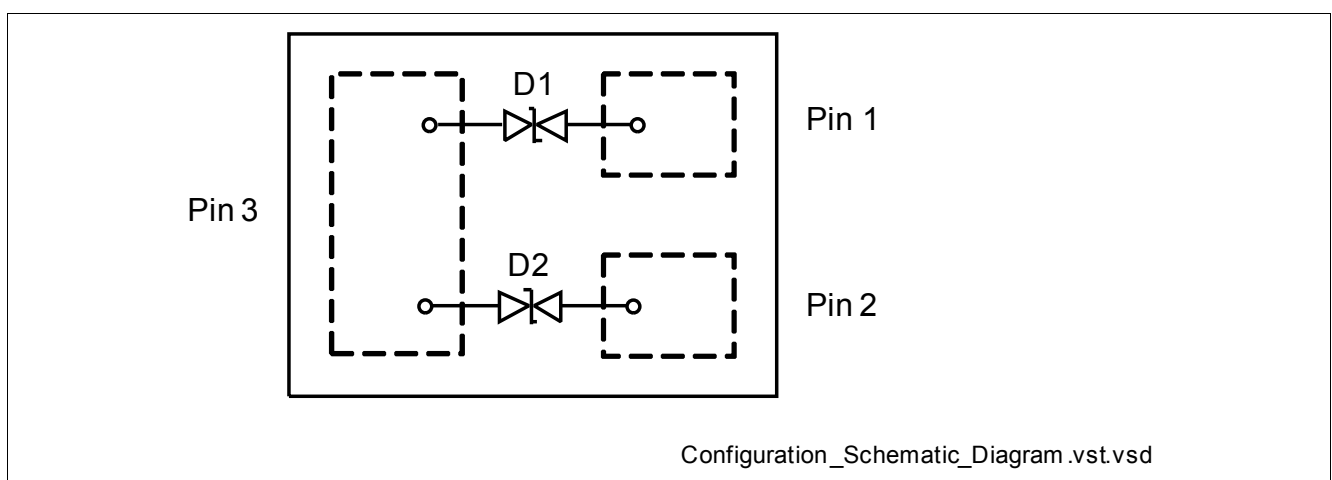


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
ESD201-B2-03LRH	TSLP-3-9	2 line, bi-directional	44

2 Characteristics

2.1 Maximum Ratings

Table 2-1 Maximum Ratings at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD air/contact discharge ¹⁾	V_{ESD}	-	-	20	kV
Operating temperature range	T_{OP}	-55	-	125	$^\circ\text{C}$
Storage temperature	T_{stg}	-65	-	150	$^\circ\text{C}$

1) V_{ESD} according to IEC61000-4-2 ($R = 330\ \Omega$, $C = 150\ \text{pF}$ discharge network)

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.2 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

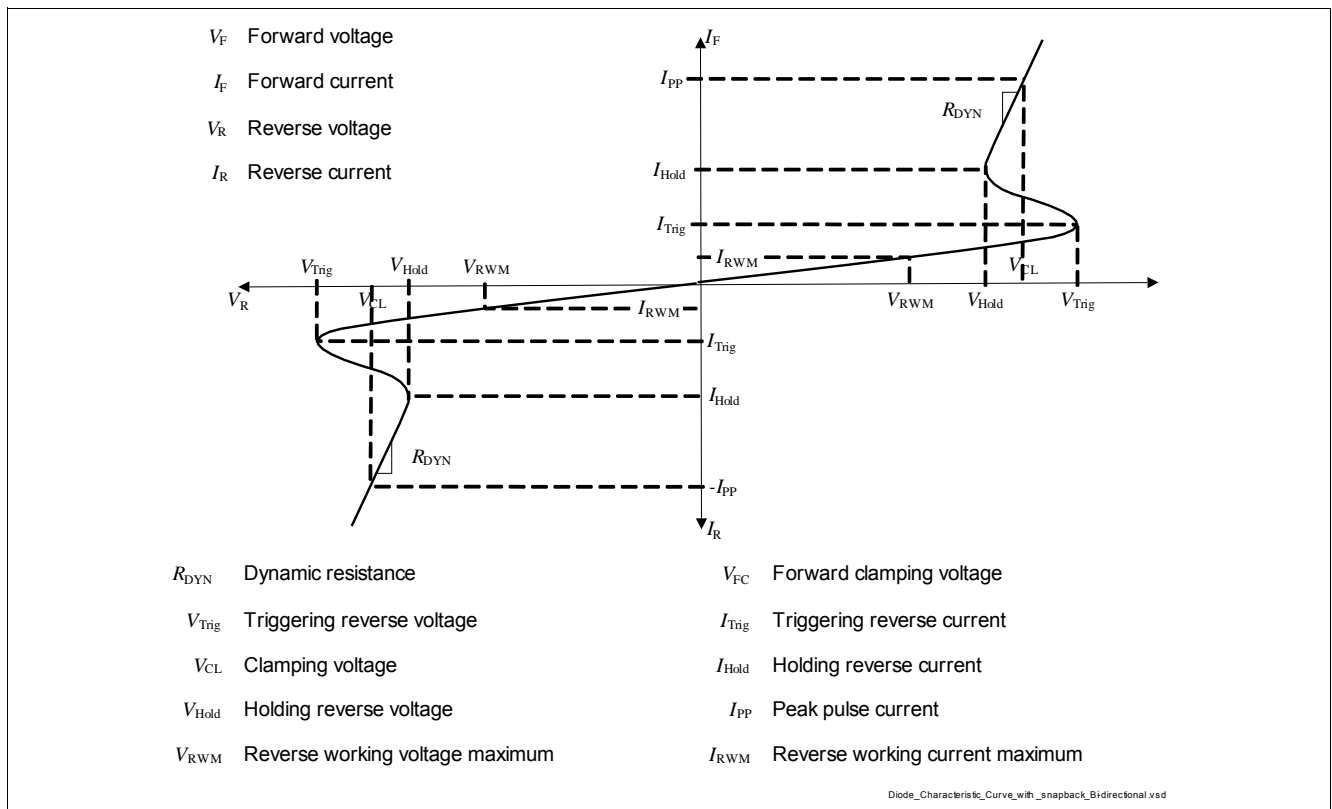


Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-5.5	–	5.5	V	
Reverse current	I_R	–	–	100	nA	$V_R = 5.5\text{ V}$

Table 2-3 AC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance to GND	C_L	–	5	7	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$

Table 2-4 ESD Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ¹⁾ Pin1 or Pin2 to Pin3 (GND) Pin3 (GND) to Pin1 or Pin2	V_{CL}	–	12.1 10.2	–	V	$t_p = 100\text{ ns}$ $I_{PP} = 16\text{ A}$ $I_{PP} = 16\text{ A}$
Dynamic resistance ¹⁾ Pin1 or Pin2 to Pin3 (GND) Pin3 (GND) to Pin1 or Pin2	R_{DYN}	–	0.37 0.22	–	Ω	$t_p = 100\text{ ns}$

1) Please refer to Application Note AN210[1]. TSLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$

3 Typical Characteristics

The curves are all specified at $T_A = 25\text{ }^\circ\text{C}$

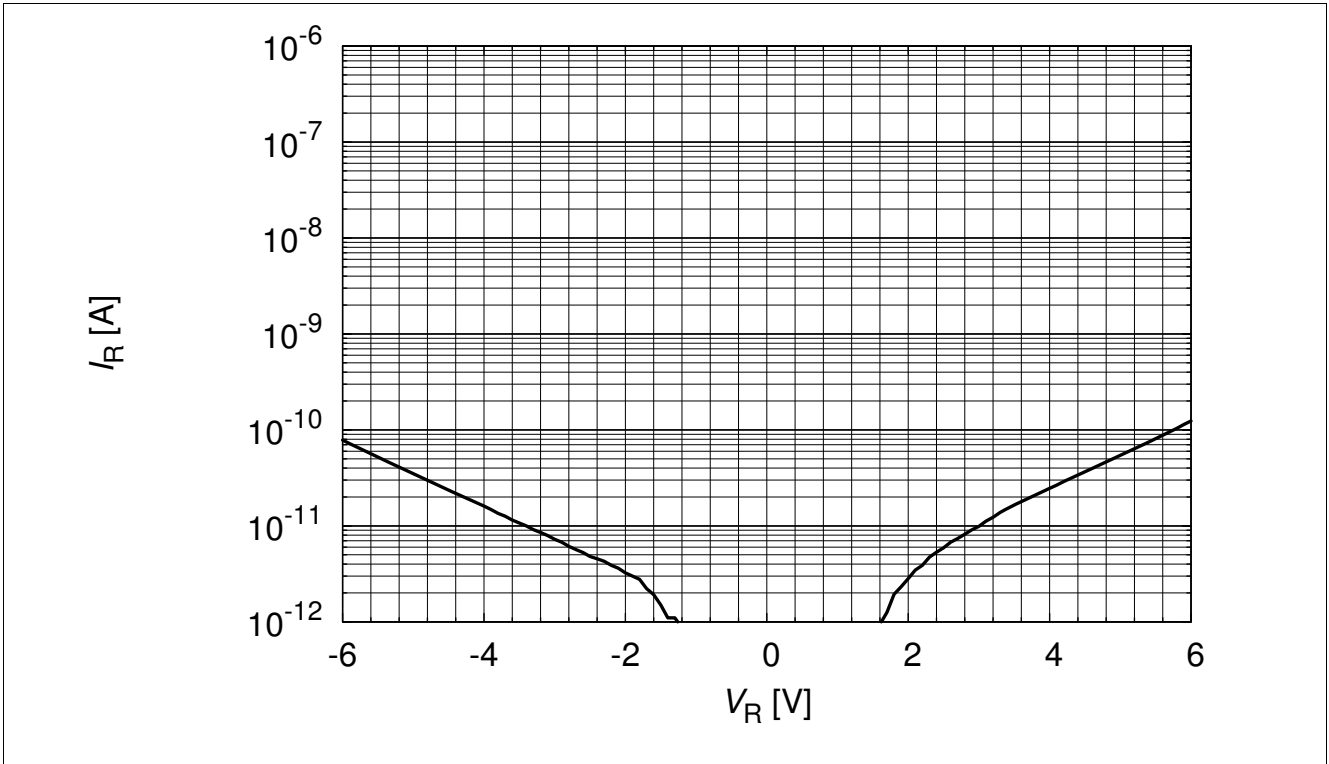


Figure 3-1 Reverse current: $I_R = f(V_R)$

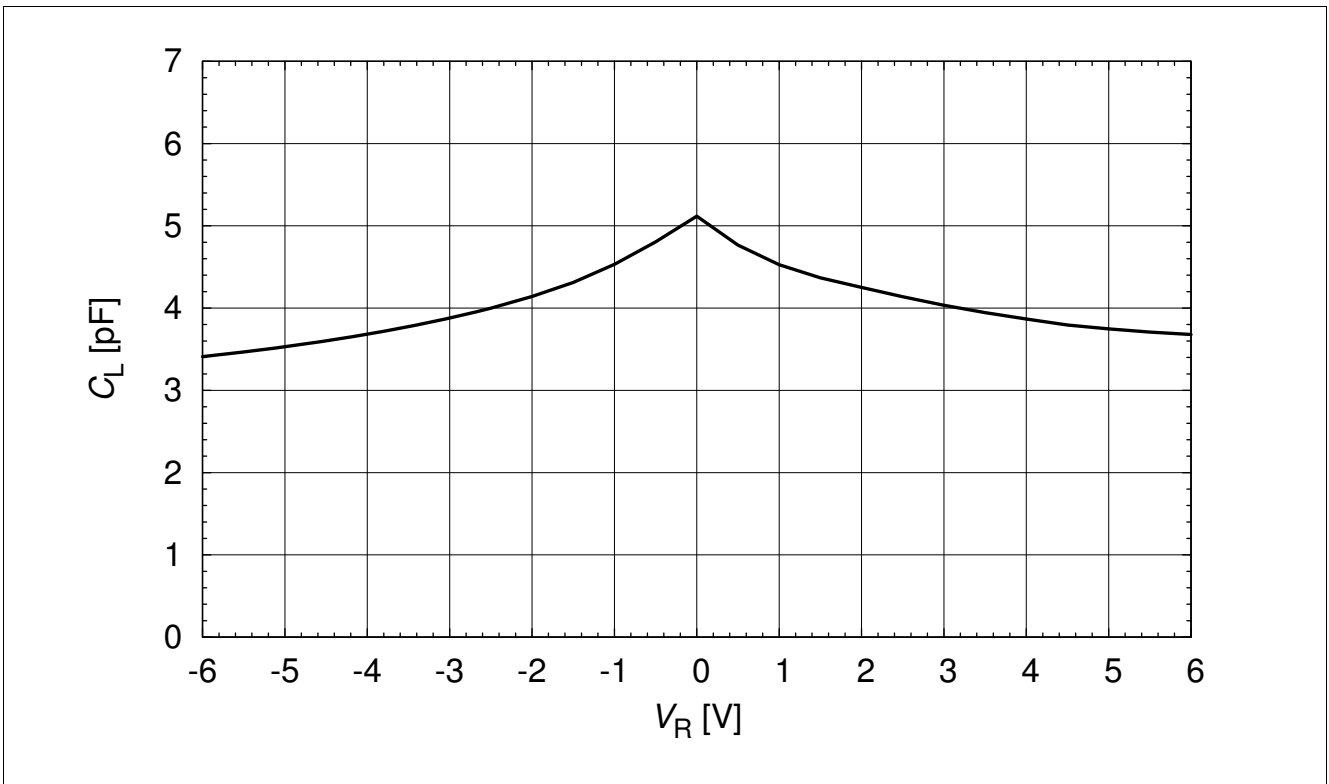


Figure 3-2 Line capacitance $C_L = f(V_R), f = 1\text{ MHz}$

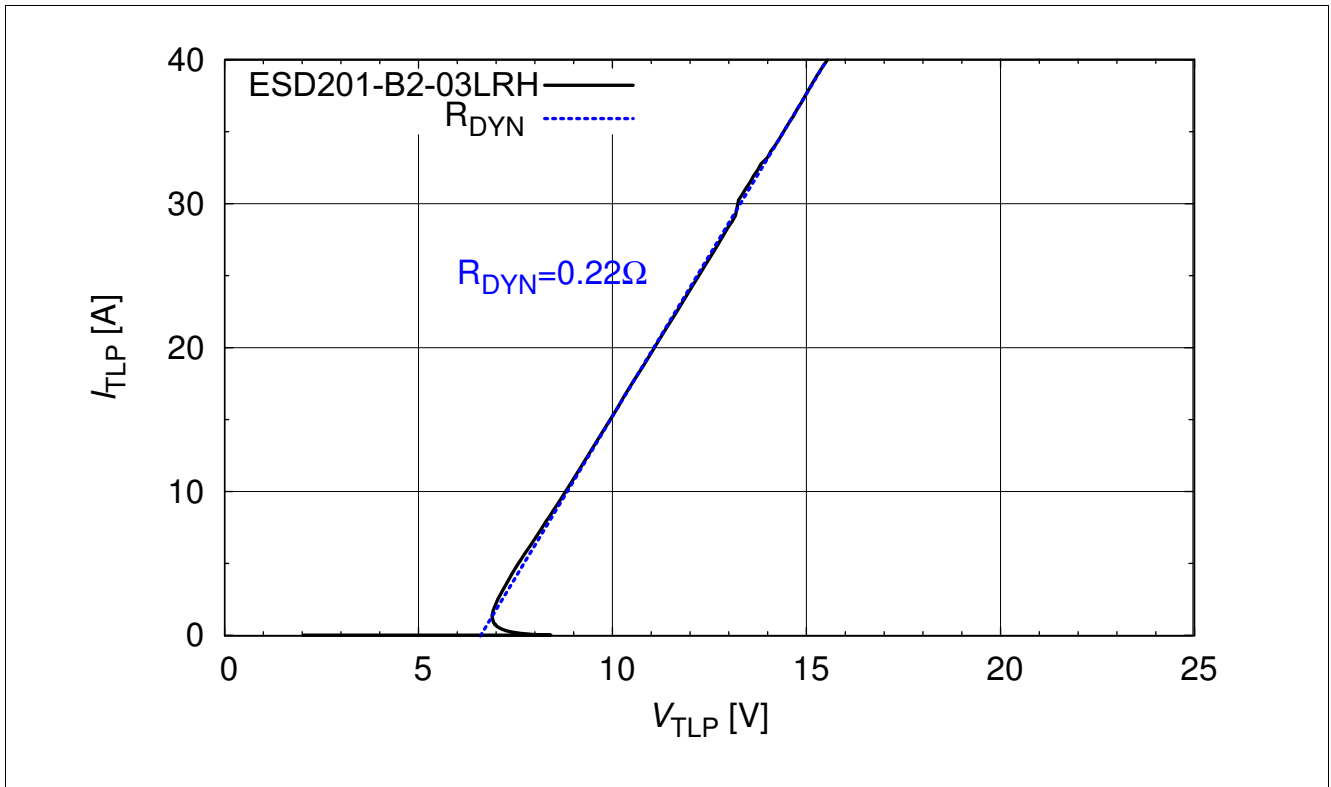


Figure 3-3 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ GND to Line

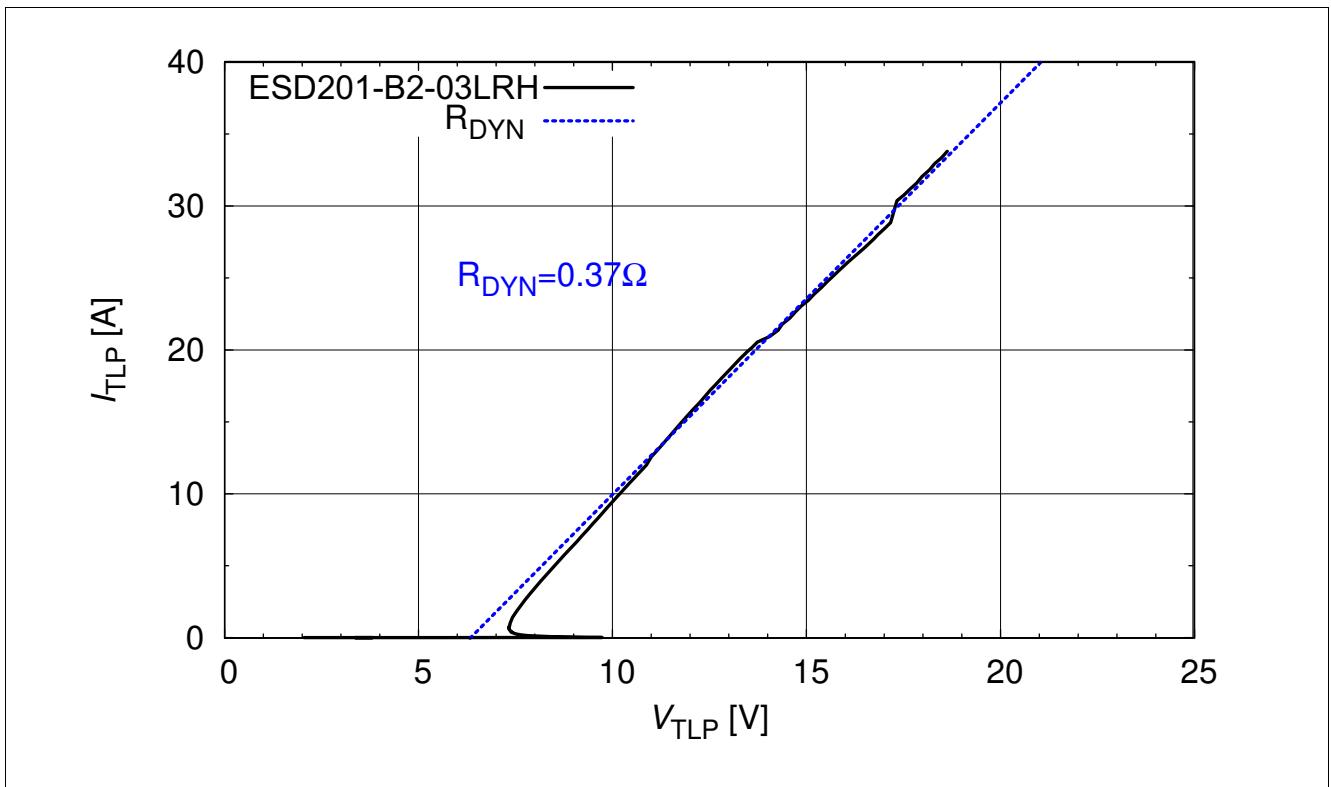


Figure 3-4 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ Line to GND

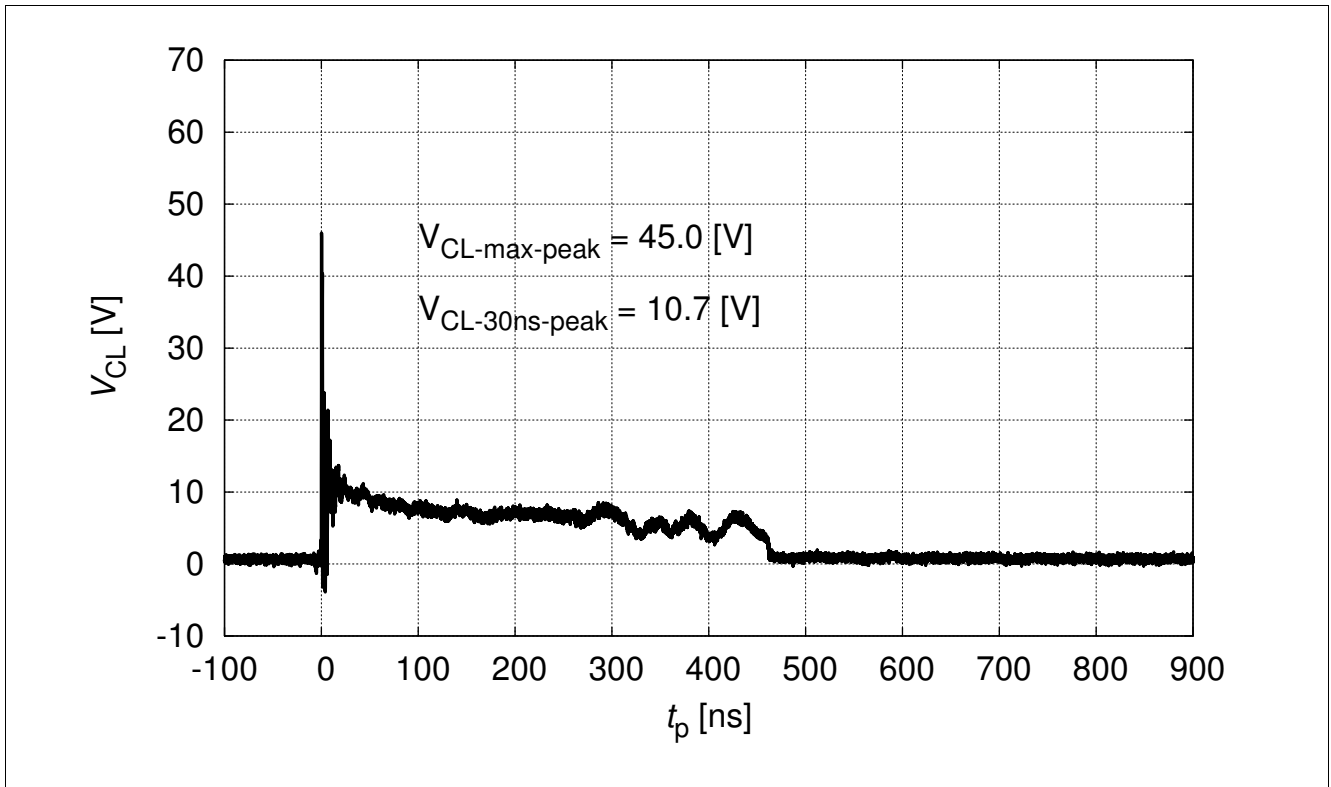


Figure 3-5 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse

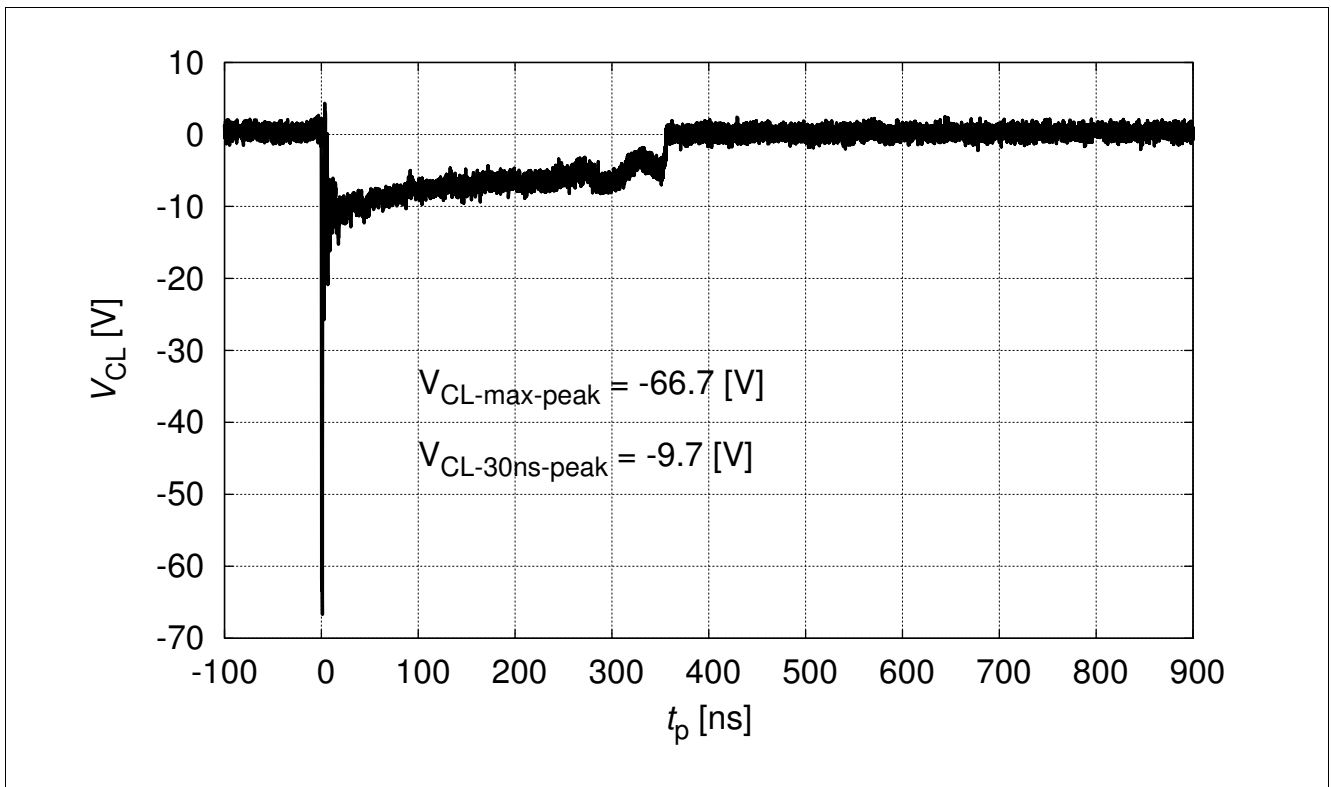


Figure 3-6 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse

4 Package Information

4.1 TSLP-3-9

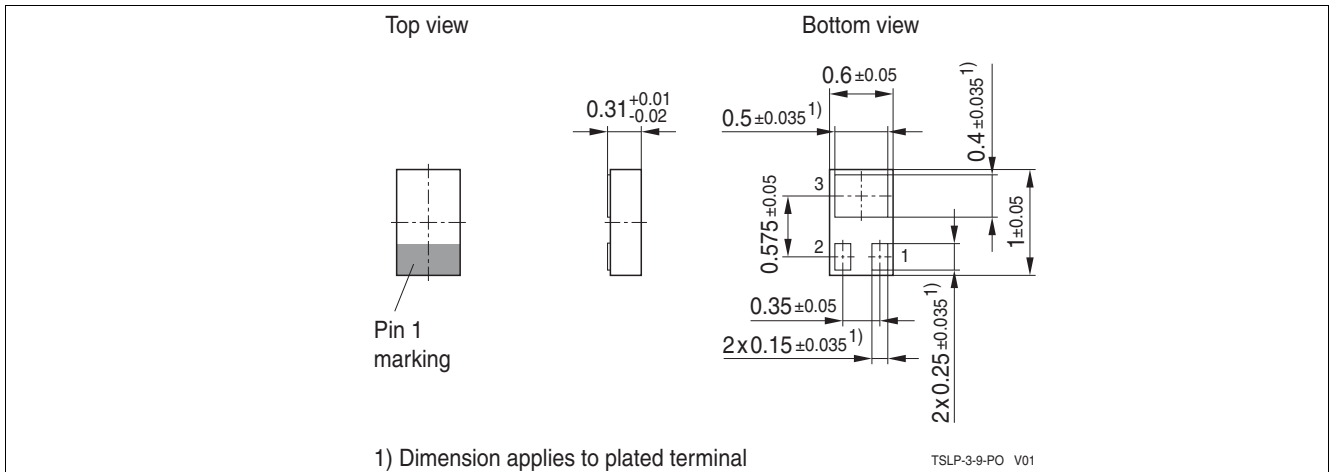


Figure 4-1 TSLP-3-9 Package outline

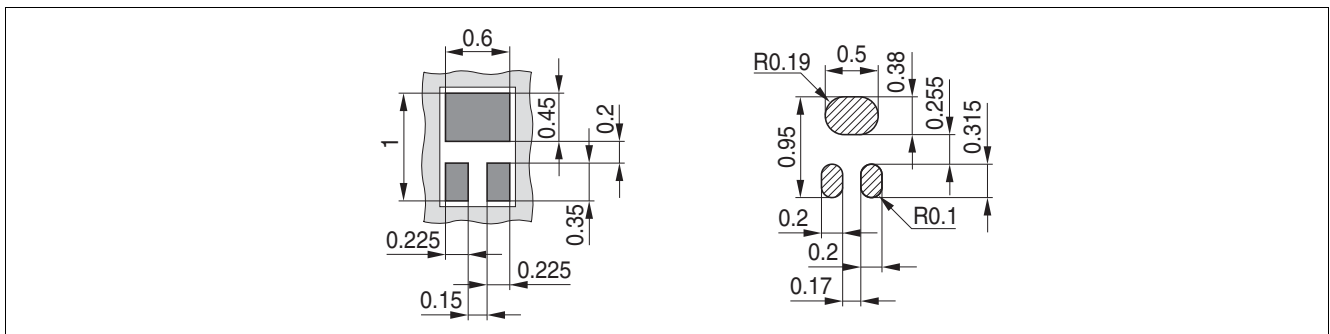


Figure 4-2 TSLP-3-9 Footprint

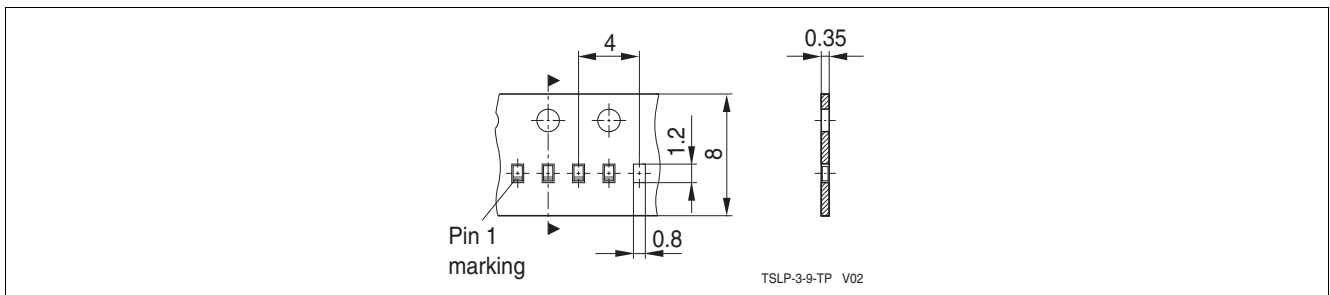


Figure 4-3 TSLP-3-9 Packing

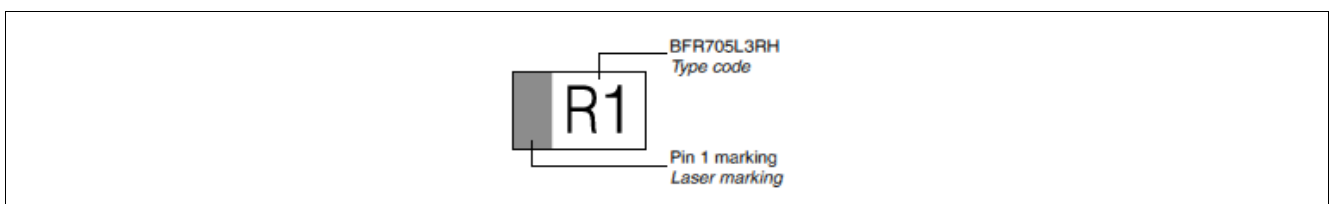


Figure 4-4 TSLP-3-9 Marking (example)

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

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