Structure Silicon Monolithic Integrated Circuit

Product Name Sound Generator for Cellular Phone

Product No. BU8793KN

Features 16 harmonies generator available at the same time
128 sounds + drum set 47 sounds generation

◯Absolute Maximum Ratings(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating	Unit	Remarks
Power supply voltage	VDD	-0.3 - +4.5	V	
Voltage applied to pin	VIN	DVSS-0.3 - DVDD+0.3	V	
Input current	IIN	-1 - +1	mA	
Allowable dissipation	Pd	370*1	mW	The guaranteed value for the single unit IC
Storage temperature range	Tstg	-50 - 125	℃	
Operating temperature range	Topr	-40 - 85	℃	

(∗1) When Ta is above 25°C, reduce 3.7mW per 1°C.

◯Recommended operating conditions(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	VDD	2.7	3.0	3.6	V	
Ambient temperature	Ta	-40	25	85	℃	
MCLK input frequency	FMCLK	12.5	-	18	MHz	Scale precision is within 0.2%
SCLK input frequency	FSCLK	-	-	MCLK	MHz	
MCLK duty	DMCLK	40	50	60	%	
SCLK duty	DSCLK	40	50	60	%	
ANOUT pin load resistance	ZAN	12	-	-	kΩ	The AC load resistance value. Apply to ANOUT-R,ANOUT-L and ANOUT-Mono pins.

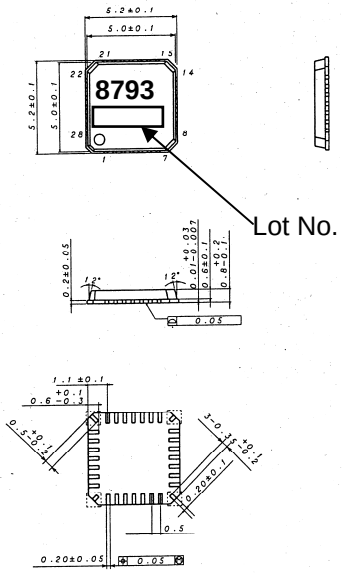
This chip is not designed to protect itself against radioactive rays.

○Electrical Characteristics

(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Digital DC characteristics						
High-level input voltage	VIH	0.7 DVDD	-	-	V	
Low-level input voltage	VIL	-	-	0.25 DVDD	V	
High-level input current	IIH			10	μA	VIH=DVDD
Low-level input current	IIL	-10	-	-	μA	VIL=DVSS
High-level output voltage	VOH	DVDD -0.3	-	-	V	IOH=-0.8mA
Low-level output voltage	VOL	-	-	DVSS +0.3	V	IOL=0.8mA
Analog DC characteristics						
VREF pin voltage	VAGND	0.475 AVDD	0.5 AVDD	0.525 AVDD	V	IOUT=0A (no load)
ANOUT pin voltage	VOUT	0.47 AVDD	0.5 AVDD	0.53 AVDD	V	IOUT=0A (no load) when not playing
General characteristics						
VREF pin rise time	TRVR	-	70	100	mS	When Capa=1μF between VREF and AVss NRST=L ->H
Analog (ANOUT pin) characteristics						
ANOUT amplitude	VMAX	-	0.667 AVDD	-	Vp-p	Theoretical value of dynamic range
Current consumption Vdd=3V, Internal operation frequency=13MHz						
Analog Idd	IDD1	-	1.3	3	mA	Playing
Digital Idd	IDD2	-	16.5	22	mA	Playing
Analog Idd	IDD3	-	0	1	μA	Standby mode
Digital Idd	IDD4	-	0	5	μA	Standby mode

○ External measure and View



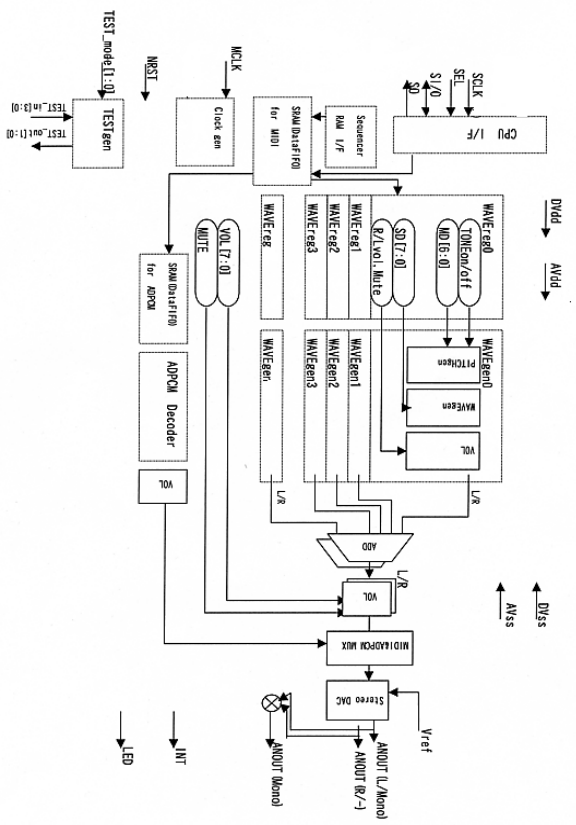
VQFN28 (Unit:mm)

○ Pin layout diagram

Pin NO.	Pin name
15.6	Test-out[1:0]
20	INT
17	LED
14	DVdd
16	DVss
22.21. 8.7	Test-in[3:]
28	ANOUT-R
1	VREF
2	VANOUT-L (L/Mono)
3	Avss
27	Avdd
5	ANOUT-Mono (Mono)
26.24	Test-Mode[1:0]
23	MCLK
9	SO
10	SI/O
12	SCLK
13	SEL
19	NRST

* Use the chip with the same voltage of DVDD(digital power supply) and AVDD (analog power supply).

○Block diagram



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Others

In case of use this LSI, please peruse some other detail documents, we called ,Technical note, Functinal description, Application note.

Notes

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