THE DATASHEET OF

BU8732AKV-E2

CODEC IC for digital mobile phone

BU8732AKV

BU8732AKV is a PCM codec IC for digital cellular phones. This includes plenty of analog input / output functions such as a 14bit precision linear. μ / A-LAW codec, a microphone amplifier with two systems, amplifiers for speaker and earphone and a switch transistor for driving a ringer. This IC is the most suitable for both PDC system and CDMA system cellular phones.

●Application

Digital cellular phones with CDMA system, Digital cellular phones with PDC system.

●Features

1) +3V single power supply. (V_{DD}=2.7 to 3.3V)
2) 14bit precision linear・μ / A-LAW codec.
3) Transmission filter of the codec block is in conformity to the ITU-T recommendation G. 714.
4) Built-in PLL circuit for system clock generation.
5) Built-in DSP I/F which is in conformity with PDC and N-CDMA.
6) Arbitrary setting of the clock frequency of PCM data transmission is allowed :
   μ / A-LAW 64kHz to 2048kHz
   Linear 128kHz to 2048kHz
7) Plenty of input / output analog functions :
   - Two systems of built-in microphone amplifier (differential input type, single input type)
   - Built-in speaker amplifier for receiver (32Ω BTL type)
   - Built-in speaker amplifier for earphone (32Ω single type)
   - Built-in speaker amplifier for REXT of call receiving system (600Ω)
   - Built-in electronic volumes for gain adjustment. (Call-receiving system, call sending system, TONE system)
   - Built-in input / output circuit for data signal which allows external connection.
   - Pop noise of REXT earphone and receiver outputs at the time of switching on and off the power supply is reduced by means of soft mute.
8) A built-in function to generate DTMF signals and musical scale tones is provided in the tone signal generating block.
9) Built-in switch transistor for driving a ringer.
10) VQFP 48 pin package.

●**Absolute maximum rating** (Ta=25°C unless specified particularly)

Parameter	Symbol	Limits	Unit
Digital power supply voltage	DV_{DD}	–0.3 to +4.5	V
Analog power supply voltage	RXV_{DD}	–0.3 to +4.5	V
	TXV_{DD}	–0.3 to +4.5	V
Digital pin apply voltage	V_{TD}	DV_{SS}–0.3 to DV_{DD}+0.3	V
Analog pin apply voltage	V_{TA}	RXV_{SS}–0.3 to RXV_{DD}+0.3	V
		TXV_{SS}–0.3 to TXV_{DD}+0.3	V
Input current	I_{IN}	–10 to +10	mA
Power dissipation	Pd	400 ∗1	mW
Storage temperature range	Tstg	–50 to +125	°C
Operation temperature range	Ta	–30 to +85	°C

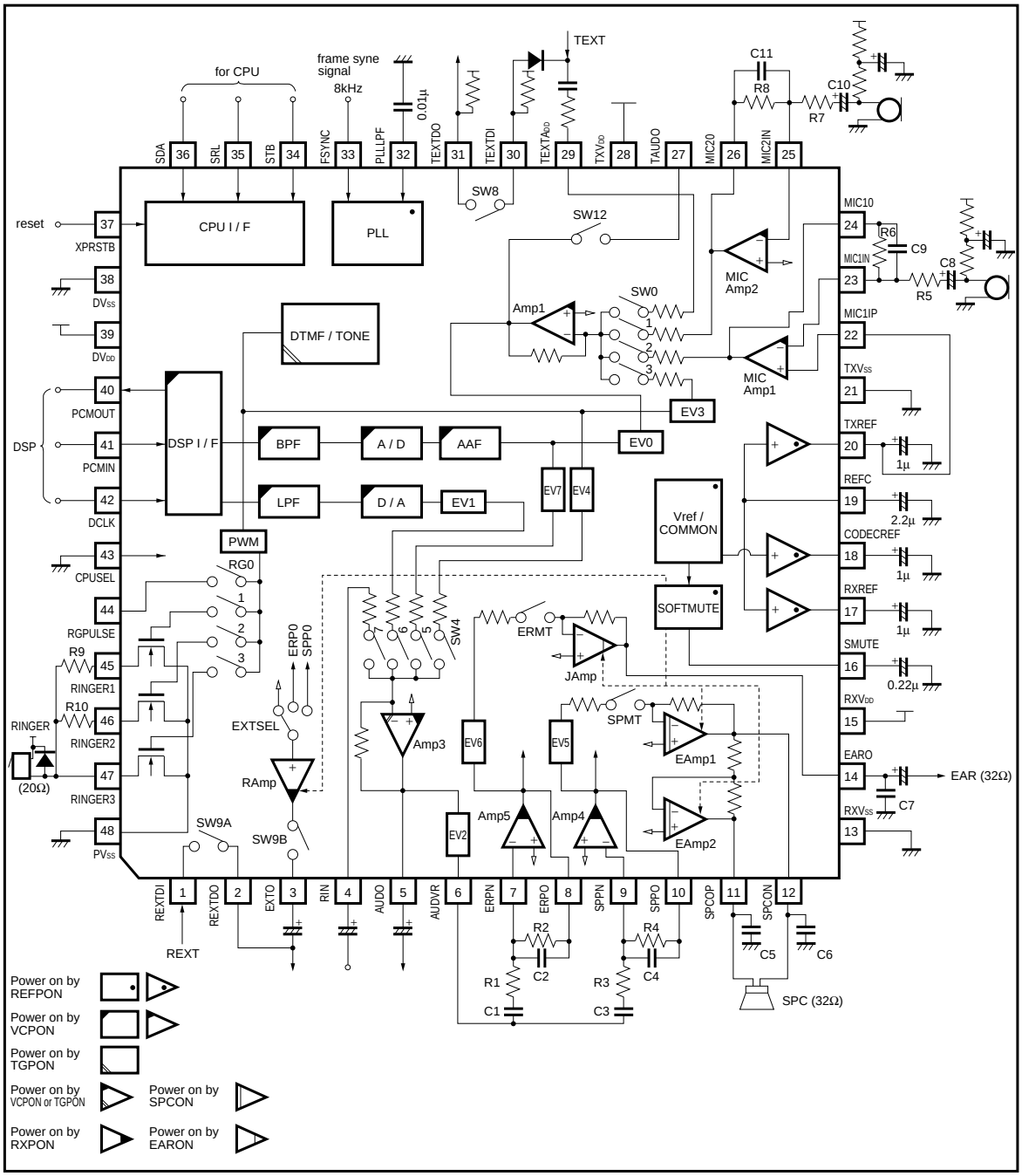
∗1 Drops by 4.0mW per 1°C when used at more than Ta=25°C.

●**Recommendable operation condition** (Ta=25°C unless specified particularly)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital power supply voltege	DV_{DD}	2.7	–	3.3	V
Analog power supply voltege	RXV_{DD}	2.7	–	3.3	V
	TXV_{DD}	2.7	–	3.3	V

◎Radiation resistance is not included design.

●**Block diagram**



●Pin descriptions

Pin No.	Pin name	I / O	Terminal function	Minimum load resistance[Ω]	Maximum load capacitance[F]
1	REXTDI	I / O	Input of the data signal of receive	–	–
2	REXTDO	I / O	Output of the data signal of receive	–	–
3	EXTO	O	Amplifier output for the gain adjustment of receive signal	600	–
4	RIN	I	Direct input of the voice of receive	–	–
5	AUDO	O	Direct output of receive signal	50k	50p
6	AUDVR	O	External output of receive signal	50k	50p
7	ERPN	I	Inverted amplifier input for the earphone gain adjustment	–	–
8	ERPO	O	Amplifier output for the earphone gain adjustment	50k	50p
9	SPPN	I	Inverted amplifier input for the speaker gain adjustment	–	–
10	SPPO	O	Amplifier output for the speaker gain adjustment	50k	50p
11	SPCOP	O	Non-ineverted speaker amplifier output for the receiver	30(BTL)	–
12	SPCON	O	Inverted speaker amplifier output for the receiver	30(BTL)	–
13	RXV_{SS}	–	Analog grounding for the receive	–	–
14	EARO	O	Speaker amplifier output for the earphone	30	–
15	RXV_{DD}	–	Analog power source for the receive	–	–
16	SMUTE	I	Time constant terminal for the soft mute setting	–	0.22μ*1
17	RXREF	O	Analog reference voltage output for the receive	–	1μ*1
18	CODCREF	O	Analog reference voltage output for codec	–	1μ*1
19	REFC	O	Analog reference voltage output	–	2.2μ*1
20	TXREF	O	Analog reference voltage output for the transmit	–	1μ*1
21	TXV_{SS}	–	Analog grounding for the transmit	–	–
22	MIC1IP	I	Non-inverted input of the microphone amplifier 1	–	–
23	MIC1IN	I	Inverted input of the microphone amplifier 1	–	–
24	MIC1O	O	Output of microphone amplifier 1	50k	50p
25	MIC2IN	I	Inverted input of the microphone amplifier 2	–	–
26	MIC2O	O	Output of microphone amplifier 2 output	50k	50p
27	TAUDO	O	External output of transmit signal	50k	50p
28	TXV_{DD}	–	Analog power source for the transmit	–	–
29	TEXTADD	I	Additive input of the transmit signal	–	–
30	TEXTDI	I / O	Input of the data signal of transmit	–	–
31	TEXTDO	I / O	Output of the data signal of transmit	–	–
32	PLLLPF	I / O	Filter connection input/output for PLL	–	0.01μ*1
33	FSYNC	I	PLL reference clock input	–	–
34	STB	I	Strobe input for CPU I/F	–	–
35	SCL	I / O	Shift clock input for CPU I/F	–	–
36	SDA	I / O	Address data input for CPU I/F	–	–
37	XPRSTB	I	System reset input (L: reset)	–	–
38	DV_{SS}	–	Grounding for digital	–	–
39	DV_{DD}	–	Power supply for digital	–	–
40	PCMOUT	O	Output of PCM signal	–	–
41	PCMIN	I	Input of PCM signal	–	–
42	DCLK	I	Shift clock input for PCM signal	–	–

*1 Standard value

Pin No.	Pin name	I / O	Terminal function	Minimum load resistance[Ω]	Maximum load capacitance[F]
43	CPUSEL	I	Fixed to GND, Fixed "L"	–	–
44	RGPULSE	O	Pulse output for the ringer	–	–
45	RINGER1	O	Open drain output of the ringer driving transistor	100(at 3V)	–
46	RINGER2	O	Open drain output of the ringer driving transistor	60(at 3V)	–
47	RINGER3	O	Open drain output of the ringer driving transistor	20(at 3V)	–
48	PV_{SS}	–	Grounding for ringer	–	–

∗1 Standard value

●Electrical characteristics

(Ta=25°C, DV_{DD}=RXV_{DD}=TXV_{DD}=3.0V, FSYNC=8kHz, gain 0dB unless specified particularly)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current consumption(Note 1)	I_{DD1}	–	8.0	11.5	mA	Full operation (Note2)
	I_{DD2}	–	7.0	10.2		Reference / Voice / SPC ON (Note2)
	I_{DD3}	–	6.0	8.6		Reference / Voice / EAR ON (Note2)
	I_{DD4}	–	5.4	7.8		Reference / Voice / RAMP ON (Note2)
	I_{DD5}	–	5.1	7.3		Reference / Voice ON (Note2)
	I_{DD6}	–	3.7	5.3		Reference / Tone ON (Note2)
	I_{DD7}	–	3.3	4.8		Reference ON (Note2)
	I_{DD8}	–	0.1	20	µA	All power down, FSYNC, Fixed DCLK terminal
Digital "H" level input voltage	V_{IH}	$0.8DV_{DD}$	–	–	V	
Digital "L" level input voltage	V_{IL}	–	–	$0.2DV_{DD}$	V	
Digital "H" level input current	I_{IH}	–	–	10	µA	V_{IH}=DV_{DD}
Digital "L" level input current	I_{IL}	–10	–	–	µA	V_{IL}=0V
Digital "H" level output voltage	V_{OH}	DV_{DD}-0.5	–	–	V	I_{OH}= –1mA
Digital "L" level output voltage	V_{OL}	–	–	0.5	V	I_{OL}=1mA

∗1) Power supply voltage (DV_{DD}, RXV_{DD}, TXV_{DD}) is 3V. Digital and analog output terminals are free from load.
All the digital terminals except FSYNC. CLK terminal are connected to either DV_{DD} or DV_{SS}.
Analog terminals are connected with an appropriate resistance to TXREF or RXREF.
The soft mute is in the canceled status. (SMUTE="0")

∗2) FSYNC=8kHz, DCLK=256kHz

●Electrical characteristics

(Ta=25°C, DV_{DD}=RXV_{DD}=TXV_{DD}=3.0V, FSYNC=8kHz, DCLK=256kHz, gain 0dB, input signal frequency=1 kHz, 30 kHz LFP, specified particularly)

< CODEC block >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Transmit signal-to-distortion ratio TEXTADD→PCMOUT	S_{DT}	35	–	–	dB	1020Hz input (LINEAR) ∗3)	0 to –40dBm0
		29	–	–			–40dBm0
		24	–	–			–45dBm0
Receive signal-to-distortion ratio PCMIN→AUDO	S_{DR}	35	–	–	dB	1020Hz input (LINEAR) ∗3)	0 to –40dBm0
		29	–	–			–40dBm0
		24	–	–			–45dBm0
Transmit Gain error TEXTA_{DD}→PCMOUT	G_{TX}	–0.3	–	0.3	dB	1020Hz, (LINEAR) ∗3) Reference level= –10dBm0	+3 to –40dBm0
		–0.6	–	0.6			–40 to –50dBm0
		–1.6	–	1.6			–50 to –55dBm0
Receive Gain error PCMIN→AUDO	G_{RX}	–0.3	–	0.3	dB	1020Hz, (LINEAR) ∗3) Reference level= –10dBm0	+3 to –40dBm0
		–0.6	–	0.6			–40 to –50dBm0
		–1.6	–	1.6			–50 to –55dBm0
Transmit reference signal level	V_{ITX}	0.257	0.346	0.436	Vrms	1020Hz, 0dBm0 EV0=0dB, (LINEAR) ∗3)	TEXTA_{DD}→ PCMOUT
Receive reference signal level	V_{ORX}	0.291	0.346	0.411	Vrms	1020Hz, 0dBm0 EV1=0dB, (LINEAR) ∗3)	PCMIN→AUDO
Transmit Gain relative to input signal gain at 1.02KHz TEXTA_{DD}→PCMOUT	G_{RTX}	24	–	–	dB	1020Hz, 0dBm0 Input reference EV0=0dB, (LINEAR)	0.06kHz
		0	–	2.5			0.2kHz
		–0.3	–	0.3			0.3 to 3.0kHz
		–0.3	–	0.9			3.4kHz
		0	–	–			3.6kHz
		6.5	–	–			3.78kHz
Receive Gain relative to input signal gain at 1.02KHz PCMIN→AUDO	G_{RRX}	–0.3	–	0.3	dB	1020Hz, 0dBm0 Input reference EV1=0dB, (LINEAR)	0.3 to 3.0kHz
		–0.3	–	0.9			3.4kHz
		0	–	–			3.6kHz
		6.5	–	–			3.78kHz
Transmit noise level TEXTADD→PCMOUT	V_{NTX}	–	–	–65	dBV	EV0=0dB, (LINEAR) ∗3)	
Receive noise level PCMIN→AUDO	V_{NRX}	–	–	–70	dBV	PCMIN= "L" fixed, EV1=0dB, (LINEAR) ∗3)	
Noise level of speaker amplifier for receiver	V_{NSPC}	–	–90	–	dBV	SPCOP-SPCON, R_L=32Ω Connect SPPN-SPPO ∗3)	
Noise level of speaker amplifier for earphone	V_{NEAR}	–	–93	–	dBV	EARO, R_L=32Ω Connect ERPN-ERPO ∗3)	

∗3) Using C-MESSAGE filter

< Analog element (1) >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Max. Closed loop gain	G_{CMIC1}	40	–	–	dB	MICAMP1, THD<5%
	G_{CMIC2}	40	–	–		MICAMP2, THD<5%
	G_{CAMP4}	40	–	–		AMP4, THD<5%
	G_{CAMP5}	40	–	–		AMP5, THD<5%
Min. Load impedance	R_{LTX}	50k	–	–	Ω	MIC10, MIC20, TAUDOGND
	R_{LRX}	50k	–	–		AUDO, AUDVR, ERPO, SPPO⇔GND
	R_{LEXT}	600	–	–		EXTO⇔GND
	R_{LSPC}	30	–	–		SPCOP-SPCON
	R_{LEAR}	30	–	–		EARO-GND
Max. Load capacitance	C_{LTX}	–	–	50p	F	MIC10, MIC20, TAUDO⇔GND
	C_{LRX}	–	–	50p		AUDO, ERPO, SPPO⇔GND
Max. Output level	V_{OTX}	0.707	–	–	Vrms	MIC10, MIC20, TAUDO R_L=50kΩ, C_L=50pF, THD<5%
	V_{ORX}	0.707	–	–		AUDO, AUDVR, ERPO, SPPO R_L=50kΩ, C_L=50pF, THD<5%
	V_{OSPC}	0.791	1.130	–		SPCOP-SPCON R_L=32Ω, THD<5%
	V_{OEAR}	0.485	0.693	–		EARO R_L=32Ω, THD<5%
	V_{OEXT}	0.393	0.562	–		EXTO R_L=600Ω, THD<5%
Absolute gain error of AMP1	G_{VAMP11}	–1.5	–	1.5	dB	$TEXTA_{DD}$→TAUDO SW0=SW12=ON, SW1=SW2=SW3=OFF
	G_{VAMP12}	–1.5	–	1.5		MIC20→TAUDO SW1=SW12=ON, SW0=SW2=SW3=OFF
	G_{VAMP13}	–1.5	–	1.5		MIC10→TAUDO SW2=SW12=ON, SW0=SW1=SW3=OFF
Absolute gain error of AMP3	G_{VAMP31}	–1.5	–	1.5	dB	RIN→AUDO SW7=ON, SW4=SW5=SW6=OFF

< Analog element (2) >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Max. Volume level	G_{EV0H}	10.8	12	13.2	dB	EV0=12dB, TEXTADD→PCMOUT
	G_{EV1H}	1.8	3	4.2		EV1=3dB, PCMIN→AUDO
	G_{EV2H}	–1.2	0	1.2		EV2=0dB, RIN→AUDVR
	G_{EV3H}	4.8	6	7.2		EV3=6dB, DTMF / TONE→TAUDO
	G_{EV4H}	4.8	6	7.2		EV4=6dB, DTMF / TONE→AUDO
	G_{EV5H}	–1.2	0	1.2		EV5=0dB, SPPO→SPCON
	G_{EV6H}	–1.2	0	1.2		EV6=0dB, ERPO→EARO
	G_{EV7H}	–6.2	–5	–3.2		EV7= –5dB, TEXTADD→AUDO, EV0=0dB
Min. volume level	G_{EV0L}	–20.2	–19	–17.8	dB	EV0= –19dB, TEXTADD→PCMOUT
	G_{EV1L}	–5.2	–4	–2.8		EV1= –4dB, PCMIN→AUDO
	G_{EV2L}	–32.2	–31	–29.8		EV2= –31dB, RIN→AUDVR
	G_{EV3L}	–27	–25	–23		EV3= –25dB, DTMF / TONE→TAUDO
	G_{EV4L}	–27	–25	–23		EV4= –25dB, DTMF / TONE→AUDO
	G_{EV5L}	–16.2	–15	–13.8		EV5= –15dB, SPPO→SPCON
	G_{EV6L}	–16.2	–15	–13.8		EV6= –15dB, ERPO→EARO
	G_{EV7L}	–21.2	–20	–18.8		EV7= –20dB, TEXTADD→AUDO, EV0=0dB
Output muting level	G_{VSW0}	–	–	–60	dBV	SW0=SW1=SW2=SW3=OFF, SW12=ON 0dBm0 input, TEXTADD→TAUDO
	G_{VSW1}	–	–	–60		SW0=SW1=SW2=SW3=OFF, SW12=ON 0dBm0 input, MIC20→TAUDO
	G_{VSW2}	–	–	–60		SW0=SW1=SW2=SW3=OFF, SW12=ON 0dBm0 input, MIC10→TAUDO
	G_{VSW3}	–	–	–60		SW0=SW1=SW2=SW3=OFF, SW12=ON HTONE 1KHz, EV3=0dB DTMF / TONE→TAUDO
	G_{VSW4}	–	–	–60		SW4=SW5=SW6=SW7=OFF HTONE 1KHz, EV4=0dB DTMF / TONE→AUDO
	G_{VSW5}	–	–	–60		SW4=SW5=SW6=SW7=OFF 0dBm0 input, EV0=EV7=0dB TEXTADD→AUDO
	G_{VSW6}	–	–	–60		SW4=SW5=SW6=SW7=OFF 0dBm0 input, EV1=0dB, PCMIN→AUDO
	G_{VSW7}	–	–	–60		SW4=SW5=SW6=SW7=OFF 0dBm0 input, RIN→AUDO
	G_{VSW12}	–	–	–60		SW1=SW2=SW3=OFF, SW0=SW12=ON 0dBm0 input, TEXTADD→TAUDO

< Tone block >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Tone output level	V_{TNH}	–16	–14	–12	dBV	HTONE 2kHz, DTMF / TONE→AUDO EV4=0dB
		–16	–14	–12		HTONE 2kHz, DTMF / TONE→TAUDO EV3=0dB
	V_{TNL}	–16	–14	–12		LTONE 384Hz, DTMF / TONE→AUDO EV4=0dB
Tone distortion	S_{DTN}	–	–	–25	dB	HTONE 1kHz, DTMF / TONE→AUDO EV4=0dB

< Reference block >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output reference signal Voltage	V_{OTX}	–	1.5	–	V	TXREF, All power on
	V_{ORX}	–	1.5	–		RXREF, All power on
	V_{OCODEC}	–	1.4	–		CODECREF, All power on
input/output current	I_{OTX}	–10	–	10	µA	TXREF, All power on, $V_{OTX} \pm 50mV$
	I_{ORX}	–10	–	10		RXREF, All power on, $V_{ORX} \pm 50mV$
	I_{OCODEC}	–10	–	10		CODECREF, All power on, $V_{OCODEC} \pm 50mV$

< Ringer driver block >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Max. output drive current	I_{ORG1}	30	–	–	mA	RINGER1=ON, Vsat<0.3
	I_{ORG2}	50	–	–		RINGER2=ON, Vsat<0.4
	I_{ORG3}	150	–	–		RINGER3=ON, Vsat<0.7
Leakage current	I_{L1}	–	–	5	µA	RINGER1=OFF, V_O=3V
	I_{L2}	–	–	5		RINGER2=OFF, V_O=3V
	I_{L3}	–	–	5		RINGER3=OFF, V_O=3V

●Digital AC characteristics

(Ta=25°C, DV_{DD}=RXV_D =TXV_{DD}=3.0V, FSYNC=8kHz, DCLK=256 kHz, unless specified particularly Gain= 0db)

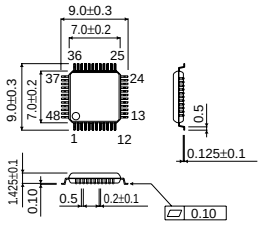
< Serial interface timing >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Data clock frequency (DCLK)	f_{CLK}	64	–	2048	kHz	μ / A-LAW
		128	–	2048		Linear
Frame Sync Frequency (FSYNC)	f_{SYNC}	7.996	8.000	8.004	kHz	FSYNC frequency
Input transition time 0 → 1	T_{IR}	–	–	20	ns	Signal rise time
Input transition time 1 → 0	T_{IF}	–	–	20	ns	Signal fall time
PCMIN Set up time	T_{RS}	100	–	–	ns	DCLK↓ –PCMIN
PCMIN Hold time	T_{RH}	100	–	–	ns	DCLK↓ –PCMIN
Other timings	T_{SR}	100	–	–	ns	DCLK↓ –FSYNC↑
	T_{SS}	100	–	–		DCLK↓ –PCMOUT
	T_{SH}	100	–	–		DCLK↓ –PCMOUT

< Write timing for the internal registers >

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCL frequency	f_{SCL}	–	–	3	MHz	SCL clock frequency
SDA input set up time	$t_{SU:DATA}$	100	–	–	ns	SDA↓ –SCL↓
SDA input hold time	$t_{HD:DATA}$	100	–	–	ns	SDA↓ –SCL↑
Input hold time	t_{sud}	333	–	–	ns	SCL↑ –STB↑
Input setup time	t_{htd}	1000	–	–	ns	SCL↑ –STB↓
STB input hold time	t_{pwd}	667	–	–	ns	STB↑ –STB↓

●External dimensions (Unit : mm)



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