



**THE DATASHEET OF
PI6C5922504ZHIEX**



PI6C5922504

2.5 GHz 1:4 LVDS Fanout Buffer with Internal Termination

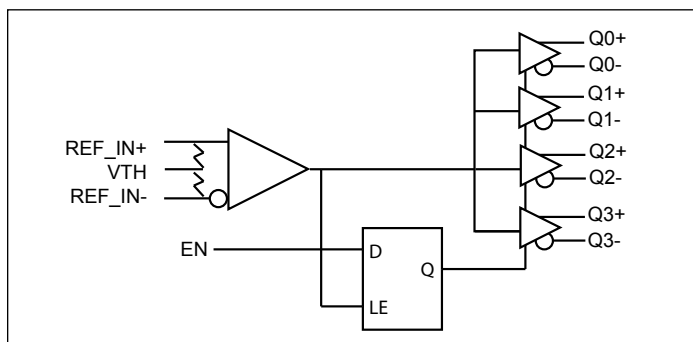
Features

- $F_{MAX} < 2.5\text{GHz}$
- 4 pairs of differential LVDS outputs
- Low additive jitter, $< 0.05\text{ps}$ (max)
- Input CLK accepts: LVDS, LVDS, CML, SSTL input level
- Output to Output skew: $< 20\text{ps}$
- Operating Temperature: -40°C to 85°C
- Power supply: $3.3\text{V} \pm 10\%$ or $2.5\text{V} \pm 5\%$
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green)
 - 16-pin, TQFN (ZH)

Description

The PI6C5922504 is a high-performance low-skew 1-to-4 LVDS fanout buffer. The CLK inputs accept LVPECL, LVDS, CML and SSTL signals. PI6C5922504 is ideal for clock distribution applications such as providing fanout for low noise Diodes oscillators.

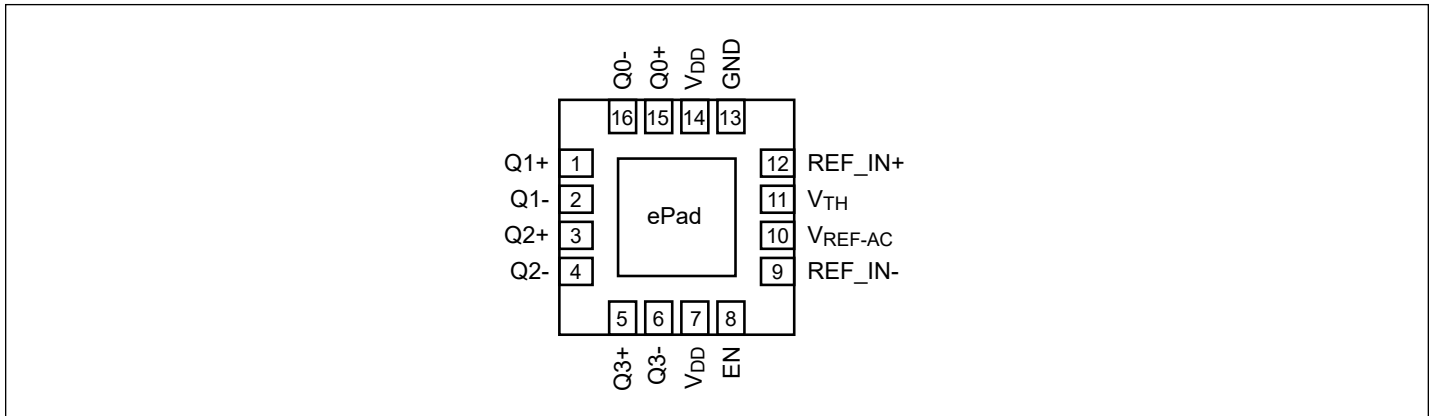
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain $< 900\text{ppm}$ bromine, $< 900\text{ppm}$ chlorine ($< 1500\text{ppm}$ total Br + Cl) and $< 1000\text{ppm}$ antimony compounds.

Pin Configuration



Pin Description

Pin #	Name	Type	Description
1, 2	Q1+, Q1-	Output	Differential output pair, LVDS interface level.
3, 4	Q2+, Q2-	Output	Differential output pair, LVDS interface level.
5, 6	Q3+, Q3-	Output	Differential output pair, LVDS interface level.
7, 14	V _{DD}	Power	Core Power Supply
8	EN	Input	Synchronous Output Enable, with internal 25kΩ pull-up resistor. Logic high selects enable, and logic low selects disable.
9	REF_IN-	Input	Differential IN negative input, AC and DC coupled
10	V _{REF-AC}	Output	Reference Voltage: Biased to V _{DD} -1.4V. Used when AC coupling inputs
11	V _{TH}	Output	Differential pair IN center-tap node. Tie to VREF-AC for AC Coupled inputs.
12	REF_IN+	Input	Differential IN positive input, AC and DC coupled
13	GND	Power	Ground
15, 16	Q0+, Q0-	Output	Differential output pair, LVDS interface level.
-	ePad	Power	Connect to GND

Functional Description

REF_IN+	REF_IN-	EN	Q+	Q-
0	1	1	0	1
1	0	1	1	0
X	X	0	0	1

Maximum Ratings

(Over operating free-air temperature range)

Storage Temperature.....	-65°C to +155°C
Junction Temperature	Max. 125°C
3.3V Core Supply Voltage	-0.5 to +4.6V
ESD Protection (HBM)	2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{DD}	Power Supply Voltage		3.0		3.6	V
			2.375		2.625	V
T _A	Ambient Temperature		-40		85	°C
I _{DD}	Power Supply Current	@3.3V± 10%, loaded		88	105	mA
		@2.5V± 5% loaded		58	75	
R _{DIFF_IN}	Differential Input Resistance (IN+ to IN-)		90	100	110	Ω
V _{IH}	Input High Voltage		1.2		V _{DD} - 0.9	V
V _{IL}	Input Low Voltage		0.4		V _{IH} -0.1	V
V _{IN}	Input Voltage Swing		0.1		V _{DD}	V
V _{DIFF_IN}	Differential Input Swing		0.2			V
V _{REF-AC}	Output Reference Voltage		V _{DD} -1.5	V _{DD} -1.3	V _{DD} -1.15	V

LVC MOS/LVTTL DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	Input High Voltage		2.0		V _{DD}	V
V _{IL}	Input Low Voltage		0		0.8	
I _{IH}	Input High Current		-125		20	μA
I _{IL}	Input Low Current		-300			μA

LVDS DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, 2.5V ±5%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{OUT}	Output Voltage Swing		250	325	400	mV
V _{DIFF_OUT}	Differential Output Voltage Swing		500	650	800	mV
V _{OCM}	Output Common Mode Voltage		1.15		1.35	V
Delta V _{OCM}	Change in Common mode Voltage		-100		100	mV

AC Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 10\%$, $2.5\text{V} \pm 5\%$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency			2.5		GHz
t_{pd}	Propagation Delay	$V_{\text{IN}} < 400\text{mV}$	370	470	570	ps
		$V_{\text{IN}} \geq 400\text{mV}$	300	410	500	
T_{sk}	Output-to-output Skew ⁽²⁾				20	ps
	Device to Device skew				200	ps
T_s	Setup time			150		ps
T_h	Hold time			150		ps
t_r/t_f	Output Rise/Fall time	20% - 80%	55		200	ps
t_{odc}	Output duty cycle	$f \leq 1\text{ GHz}$	48		52	%
		$1\text{ GHz} \leq f < 2.5\text{ GHz}$	40		60	%
V_{PP}	Output Swing	LVDS outputs	250		800	mV
t_j	Buffer additive jitter RMS	156.25MHz with 12KHz to 20MHz integration range ⁽³⁾		30		fs

Notes:

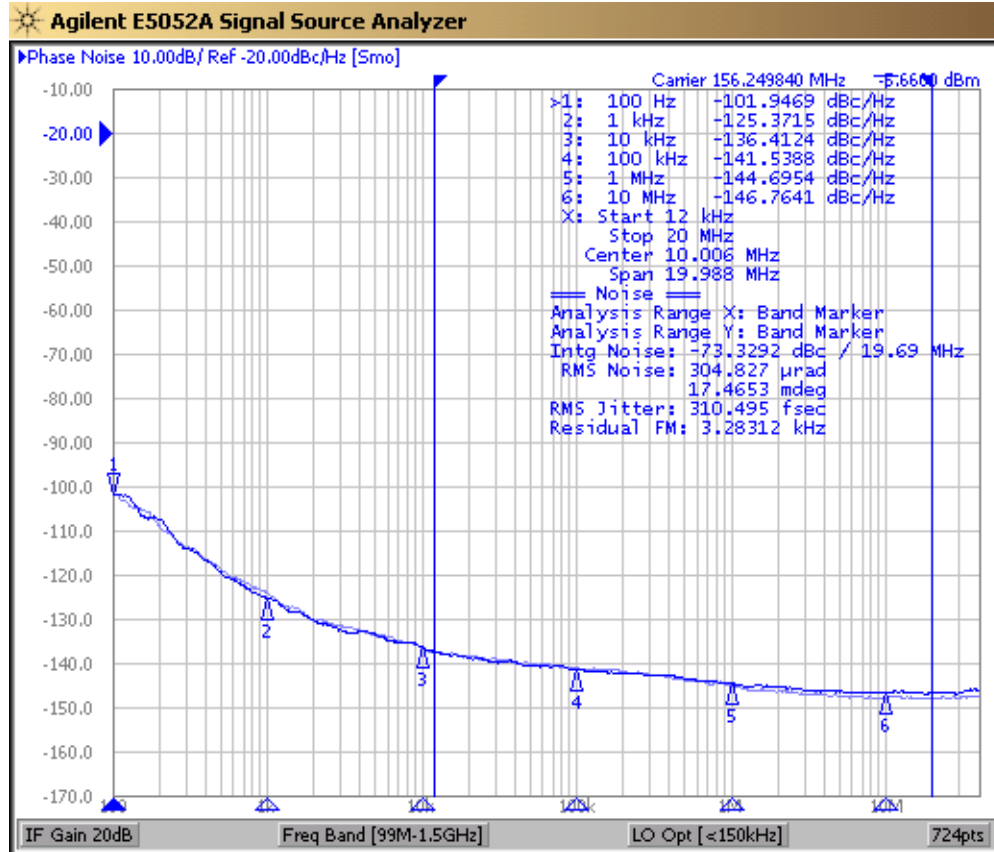
1. Measured from the differential input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point
3. Input source phase noise similar to phase noise plot in page 5

Thermal Information

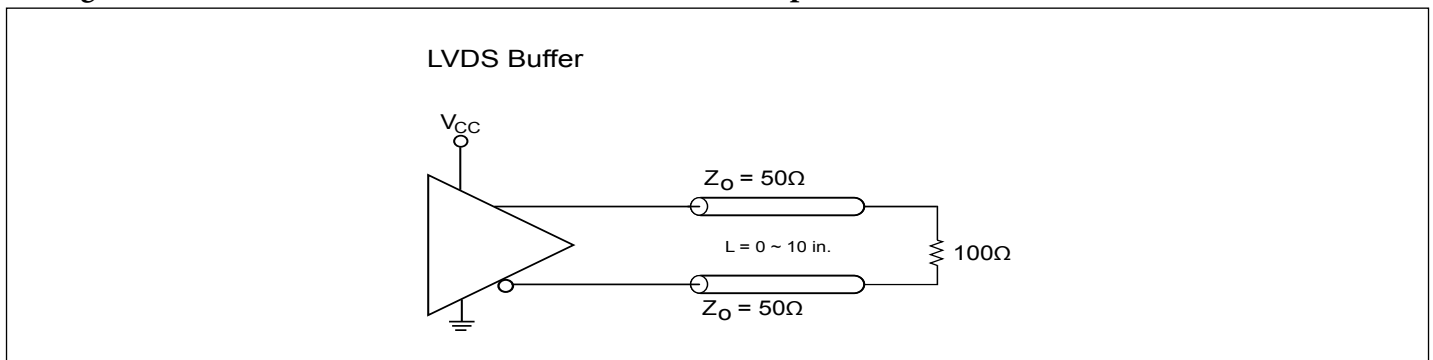
Symbol	Description	Condition	
Θ_{JA}	Junction-to-ambient thermal resistance	Still air	57.7 °C/W
Θ_{JC}	Junction-to-case thermal resistance		32.2 °C/W

Note: Thermal data accounts for ePad being connected to GND.

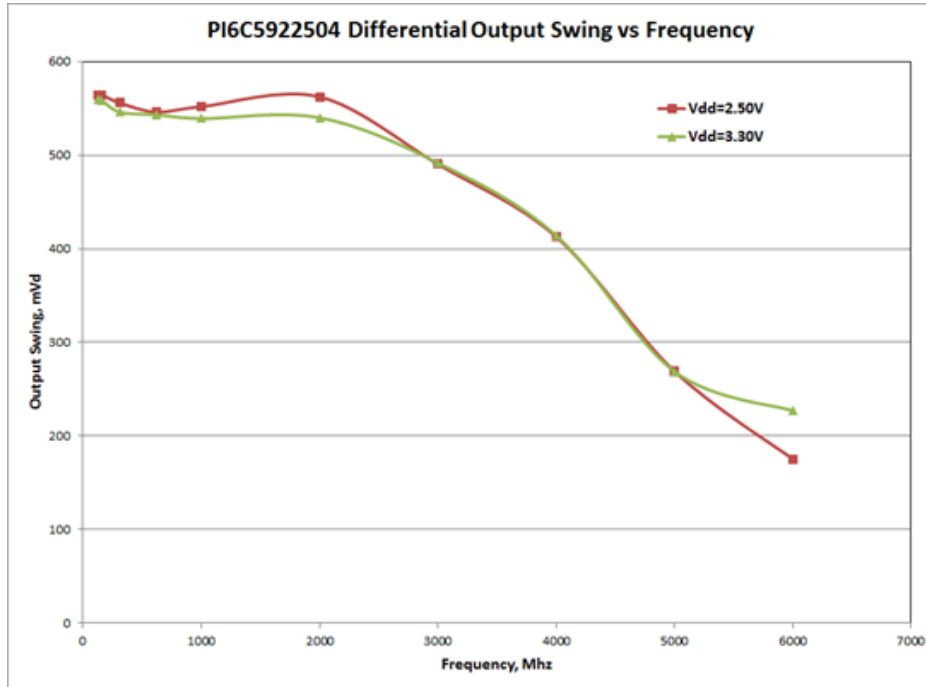
Phase Noise Plots



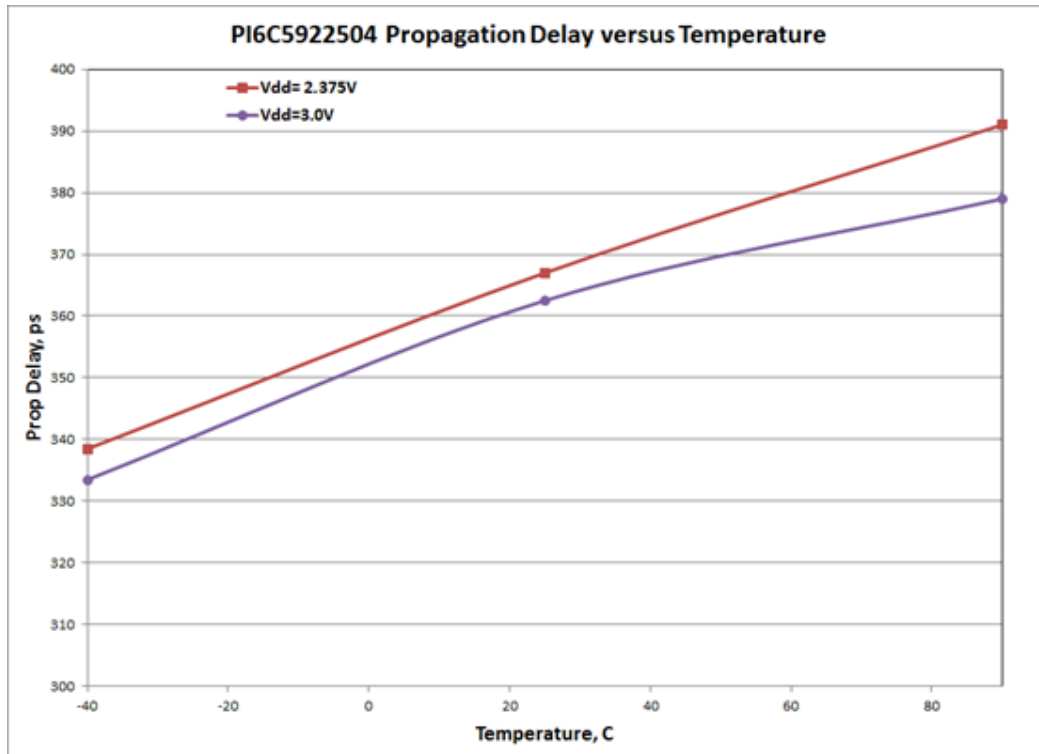
Configuration Test Load Board Termination for LVDS Outputs



Output Swing vs Frequency



Propagation Delay vs Temperature



Application Information

Suggest for Unused Inputs and Outputs

LVC MOS Input Control Pins

It is suggested to add pull-up=4.7k and pull-down=1k for LVC MOS pins even though they have internal pull-up/down but with much higher value (>=50k) for higher design reliability.

REF_IN= / REF_IN- Input Pins

They can be left floating if unused. For added reliability, connect 1kΩ to GND.

Outputs

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power supply power.

Power Decoupling & Routing

VDD Pin Decoupling

As general design rule, each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown in Fig. 1.

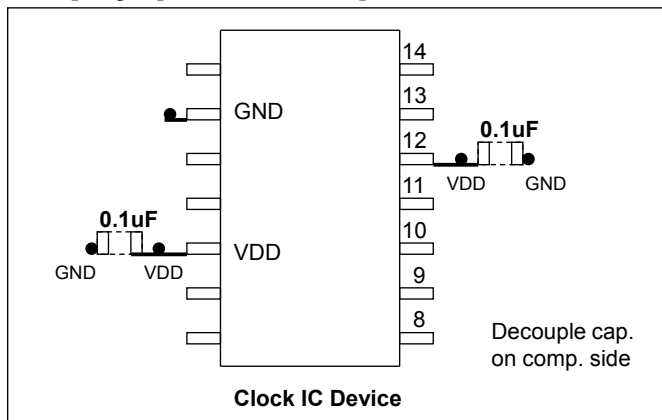


Figure 1: Placement of Decoupling Caps

Differential Clock Trace Routing

Always route differential signals symmetrically, make sure there is enough keep-out space to the adjacent trace (>20mil.). In 156.25MHz XO drives IC example, it is better routing differential trace on component side as the following Fig. 2.

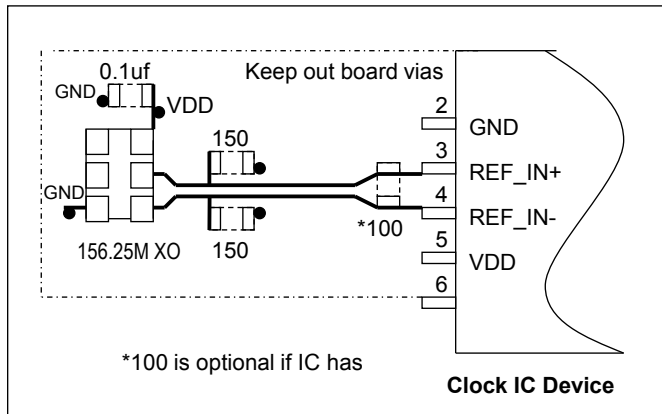


Figure 2: IC Routing for XO Drive

Clock timing is the most important component in PCB design, so its trace routing must be planned and routed as a first priority in manual routing. Some good practices are to use minimum vias (total trace vias count <4), use independent layers with good reference plane and keep other signal traces away from clock traces (>20mil.) etc.

LVPECL and LVDS Input Interface

LVPECL and LVDS DC Input

LVPECL and LVDS clock input to this IC is connected as shown in the Fig. 3.

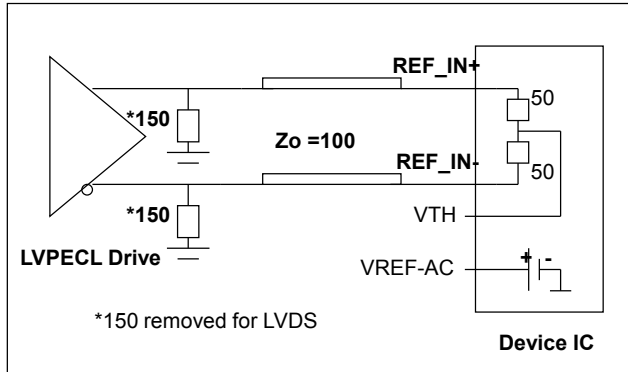


Figure 3: LVPECL/ LVDS Input

LVPECL and LVDS AC Input

LVPECL and LVDS AC drive to this clock IC requires the use of the VREF-AC output to recover the DC bias for the IC input as shown in Fig. 4

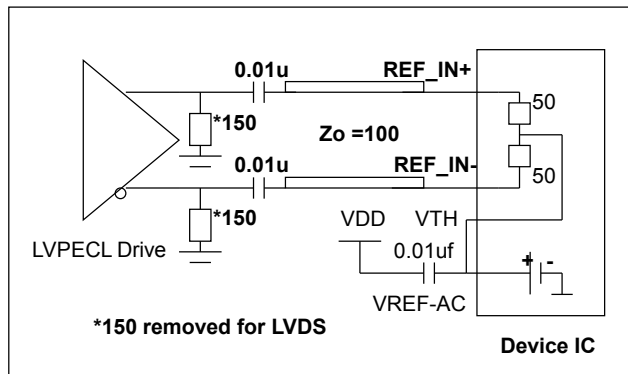


Figure 4: LVPECL/ LVDS AC Coupled Input

CML AC-Coupled Input

CML AC-coupled drive requires a connection to VREF-AC as shown in Fig. 5. The CML DC drive is not recommended as different vendors have different CML DC voltage level. CML is mostly used in AC coupled drive configuration for data and clock signals.

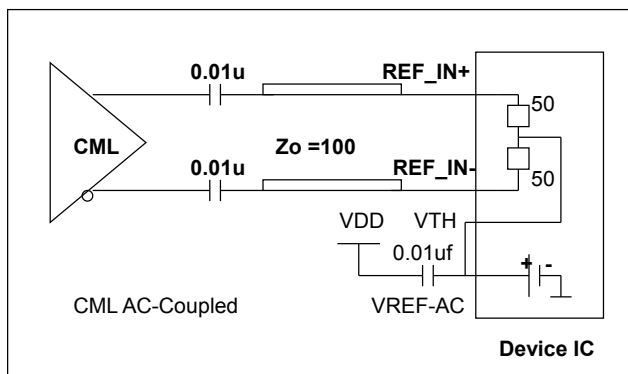


Figure 5: CML AC-Coupled Input Interface

HCSL AC-Coupled Input

It is suggested to use AC coupling to buffer PCIe HCSL 100MHz clock since its V_{cm} is relatively low at about 0.4V, as shown in Fig. 6.

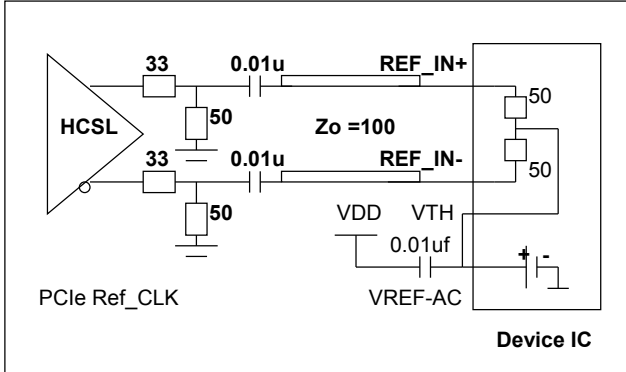


Figure 6: HCSL AC-Coupled Input Interface

CMOS Clock DC Drive Input

LVCMOS clock has voltage V_{oh} levels such as 3.3V, 2.5V, 1.8V. CMOS drive requires a V_{cm} design at the input: $V_{cm} = \frac{1}{2} (CMOS V)$ as shown in Fig. 7. $R_s = 22 \sim 33\Omega$ typically.

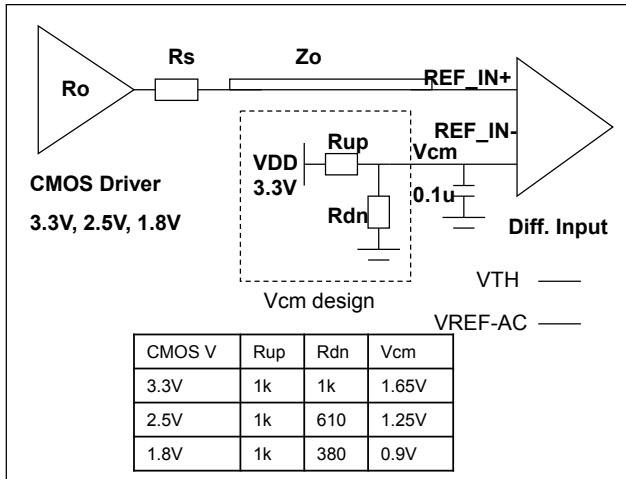


Figure 7: CMOS DC Input V_{cm} Design

Device LVPECL Output Terminations

LVPECL Output Popular Termination

The most popular LVPECL termination is 150Ω pull-down bias and 100Ω across at RX side. Please consult ASIC datasheet if it already has 100Ω or equivalent internal termination. If so, do not connect external 100Ω across as shown in Fig. 8. This popular termination's advantage is that it does not allow any bias through from V_{DD} . This prevents V_{DD} system noise coupling onto clock trace.

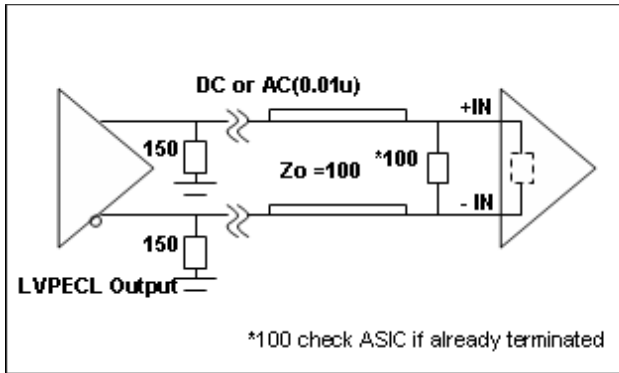


Figure. 8 LVPECL Output Popular Termination

LVPECL Output Thevenin Termination

Fig. 9 shows LVPECL output Thevenin termination which is used for shorter trace drive (<5in.), but it takes V_{DD} bias current and V_{DD} noise can get onto clock trace. It also requires more component count. So it is seldom used today.

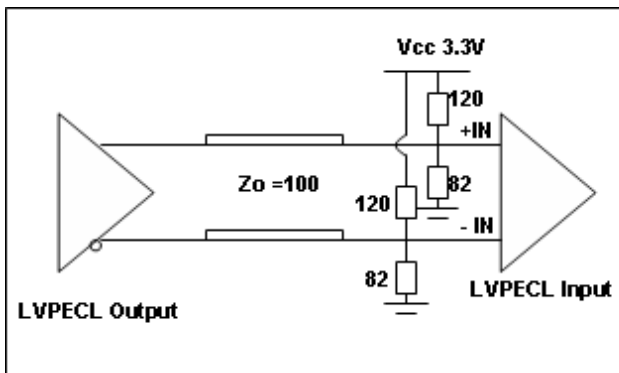


Figure. 9 LVPECL Thevenin Output Termination

LVPECL Output AC Thevenin Termination

LVPECL AC Thevenin terminations require a 150Ω pull-down before the AC coupling capacitor at the source as shown in Fig. 10. Note that pull-up/down resistor value is swapped compared to Fig. 9. This circuit is good for short trace (<5in.) application only.

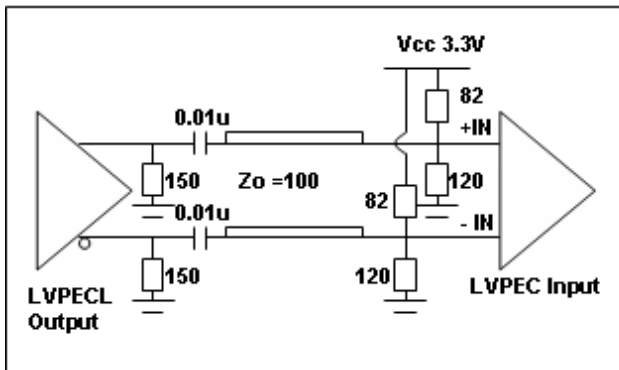


Figure. 10 LVPECL Output AC Thenvenin Termination

LVPECL Output Drive HCSL Input

Using the LVPECL output to drive a HCSL input can be done using a typical LVPECL AC Thenvenin termination scheme. Use pull-up/down 450/60Ω to generate $V_{cm}=0.4V$ for the HCSL input clock. This termination is equivalent to 50Ω load as shown in Fig. 11.

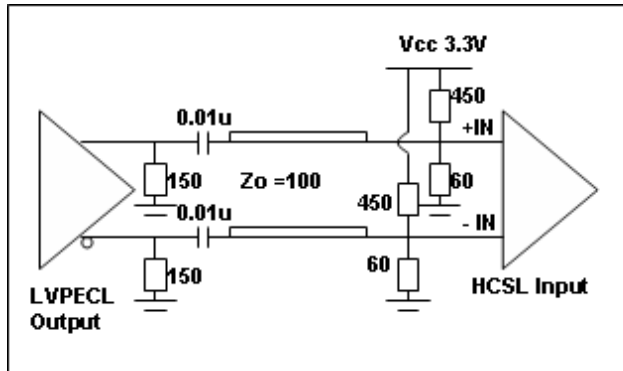


Figure. 11 LVPECL Output Drive HCSL Termination

LVPECL Output V_{swing} Adjustment

It is suggested to add another cross 100Ω at TX side to tune the LVPECL output V_{swing} without changing the optimal 150Ω pull-down bias in Fig. 12. This form of double termination can reduce the V_{swing} in 1/2 of the original at the RX side. By fine tuning the 100Ω resistor at the TX side with larger values like 150 to 200Ω, one can increase the V_{swing} by > 1/2 ratio.

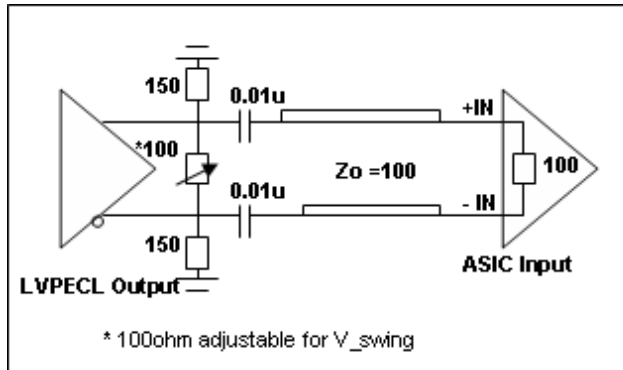


Figure. 12 LVPECL Output V_{swing} Adjustment

Clock Jitter Definitions

$$\text{Total jitter} = \text{RJ} + \text{DJ}$$

Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter: $TJ = \sqrt{RJ^2 + DJ^2}$, where $\sqrt{\quad}$ is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

Phase Jitter

Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter $\leq 1\text{ps}$ at 12k to 20MHz offset band as SONET standard specification.

Device Thermal Calculation

Fig. 13 shows the JEDEC thermal model in a 4-layer PCB.

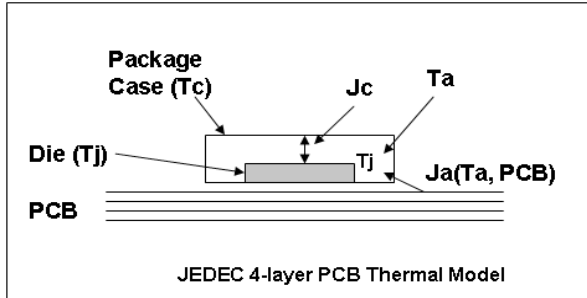


Figure. 13 JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

- 1) The power dissipation from the chip (P_{chip}) is after subtracting power dissipation from external loads. Generally it can be the no-load device I_{dd}
- 2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation
- 3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature T_j

The individual device thermal calculation formula:

$$T_j = T_a + P_{chip} \times J_a$$

$$T_c = T_j - P_{chip} \times J_c$$

J_a ___ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce J_a (still air) by 20~30%

J_c ___ Package thermal resistance from die to the package case in C/W unit

T_j ___ Die junction temperature in C (industry limit <125C max.)

T_a ___ Ambient air temperature in C

T_c ___ Package case temperature in C

P_{chip} ___ IC actually consumes power through I_{ee}/GND current

Thermal calculation example

To calculate Tj and Tc of PI6CV304 in an SOIC-8 package:

Step 1: Go to Diodes web to find Ja=157 C/W, Jc=42 C/W

<https://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Step 2: Go to device datasheet to find Idd=40mA max.

IDD	Supply Current	C _L = 33pF/33MHz	20	mA
		C _L = 33pF/60MHz	40	
		C _L = 22pF/80MHz	35	
		C _L = 15pF/100MHz	32	
		C _L = 10pF/125MHz	28	
		C _L = 10pF/155MHz	41	

Step 3: P_{total} = 3.3Vx40mA=0.132W

Step 4: If Ta=85C

$$T_j = 85 + J_a \times P_{total} = 85 + 25.9 = 105.7C$$

$$T_c = T_j + J_c \times P_{total} = 105.7 - 5.54 = 100.1C$$

Note:

The above calculation is directly using Idd current without subtracting the load power, so it is a conservative estimation. For more precise thermal calculation, use P_{unload} or P_{chip} from device I_{ee} or GND current to calculate Tj, especially for LVPECL buffer ICs that have a 150Ω pull-down and equivalent 100Ω differential RX load.

Part Marking

PI6C592
2504ZHIE
YYWWXX
○

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

IMPORTANT NOTICE

1. DIODES INCORPORATED AND ITS SUBSIDIARIES (“DIODES”) MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes products. Diodes products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of the Diodes products for their intended applications, (c) ensuring their applications, which incorporate Diodes products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes’ websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes’ website) under this document.

5. Diodes products are provided subject to Diodes’ Standard Terms and Conditions of Sale (<https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/>) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

Copyright © 2021 Diodes Incorporated

www.diodes.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View PI6C5922504ZHIEX on WIN SOURCE](#)

 [Diodes Incorporated](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management