



# THE DATASHEET OF TSM102IPWR

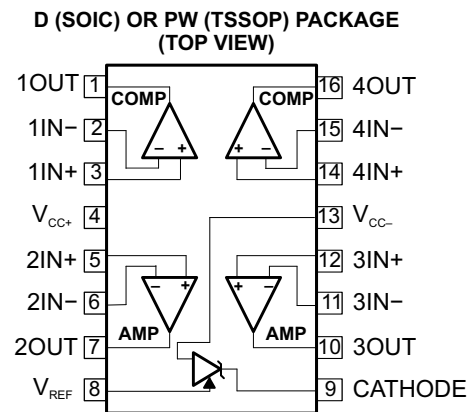


**FEATURES**

- **OPERATIONAL AMPLIFIERS**
  - Low Supply Current...200  $\mu$ A/A
  - Medium Speed...2.1 MHz
  - Low-Level Output Voltage Close to  $V_{CC}$ ...0.1 V Typ ( $R_L = 10\text{ k}\Omega$ )
  - Input Common-Mode Voltage Range Includes Ground
- **COMPARATORS**
  - Low Supply Current...200  $\mu$ A/A ( $V_{CC} = 5\text{ V}$ )
  - Input Common-Mode Voltage Range Includes Ground
  - Low Output Saturation Voltage... Typically 250 mV ( $I_{\text{sink}} = 4\text{ mA}$ )
- **VOLTAGE REFERENCE**
  - Adjustable Output Voltage... $V_{\text{REF}}$  to 36 V
  - Sink Current Capability...1 mA to 100 mA
  - 0.4% (A Grade) and 1% (Standard Grade) Precision
  - Latch-Up Immunity

**APPLICATIONS**

- Switch-Mode Power Supplies
- Battery Chargers
- Voltage and Current Sensing
- Power-Good, Overvoltage, Undervoltage, Overcurrent Detection
- Window Comparators
- Alarms, Detectors, and Sensors



**DESCRIPTION/ORDERING INFORMATION**

The TSM102 and TSM102A combine the building blocks of a dual operational amplifier, a dual comparator, and a precision voltage reference, all of which often are used to implement a wide variety of power-management functions, including overcurrent detection, undervoltage/overvoltage detection, power-good detection, window comparators, error amplifiers, etc. Additional applications include alarm and detector/sensor applications.

The TSM102A offers a tight  $V_{\text{REF}}$  tolerance of 0.4% at 25°C. The TSM102 and TSM102A are characterized for operation from –40°C to 85°C.

**ORDERING INFORMATION**

$T_A$	MAX $V_{\text{REF}}$ TOLERANCE (25°C)	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	A grade: 0.4% precision	SOIC – D	Tube of 75	TSM102AID	TSM102AI
			Reel of 2500	TSM102AIDR	
		TSSOP – PW	Tube of 90	TSM102AIPW	SN102AI
			Reel of 2000	TSM102AIPWR	
	Standard grade: 1% precision	SOIC – D	Tube of 75	TSM102ID	TSM102I
			Reel of 2500	TSM102IDR	
TSSOP – PW		Tube of 90	TSM102IPW	SN102I	
		Reel of 2000	TSM102IPWR		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# TSM102, TSM102A DUAL OPERATIONAL AMPLIFIER, DUAL COMPARATOR, AND VOLTAGE REFERENCE

SLVS602–MARCH 2006

## Absolute Maximum Ratings<sup>(1)</sup>

over free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage		36	V
$V_{ID}$	Input differential voltage		36	V
$V_I$	Input voltage range	-0.3	36	V
$I_{KA}$	Voltage reference cathode current		100	mA
$\theta_{JA}$	Package thermal impedance <sup>(2)(3)</sup>	D package		73
		PW package		108
$T_J$	Maximum junction temperature		150	°C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Selecting the maximum of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC+} - V_{CC-}$	Supply voltage	3	30	V
$V_{ID}$	Comparator differential input voltage		$V_{CC+} - V_{CC-}$	V
$V_{KA}$	Cathode-to-anode voltage	$V_{REF}$	36	V
$I_K$	Reference cathode current	1	100	mA
$T_A$	Operating free-air temperature	-40	85	°C

## Total Device Electrical Characteristics

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$I_{CC}$	Total supply current, excluding reference cathode current	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = 0\text{ V}$ , No load	25°C		0.8	1.5	mA
			Full range			2	

**Operational Amplifier Electrical Characteristics**
 $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = \text{GND}$ ,  $R_1$  connected to  $V_{CC-}/2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage		25°C		1	4.5	mV
			Full range			6.5	
$\alpha V_{IO}$	Input offset voltage drift		25°C		10		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current		25°C		5	20	nA
			Full range			40	
$I_{IB}$	Input bias current		25°C		20	100	nA
			Full range			200	
$A_{VD}$	Large-signal voltage gain	$V_{CC+} = 30\text{ V}$ , $R_1 = 10\text{ k}\Omega$ , $V_O = 5\text{ V to } 25\text{ V}$	25°C	50	100		V/mV
			Full range		25		
$k_{SVR}$	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V to } 30\text{ V}$	25°C	80	100		dB
$V_{ICM}$	Input common-mode voltage		25°C	$V_{CC-}$		$V_{CC+} - 1.8$	V
			Full range	$V_{CC-}$		$V_{CC+} - 2.2$	
CMRR	Common-mode rejection ratio	$V_{CC+} = 30\text{ V}$ , $V_{ICM} = 0\text{ V to } V_{CC+} - 1.8\text{ V}$	25°C	70	90		dB
$I_{SC}$	Short-circuit current	$V_{ID} = \pm 1\text{ V}$ , $V_O = 2.5\text{ V}$	25°C	Source	3	6	mA
				Sink	3	6	
$V_{OH}$	High-level output voltage	$V_{CC+} = 30\text{ V}$ , $R_L = 10\text{ k}\Omega$	25°C	27	28		V
			Full range		26		
$V_{OL}$	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C		130	170	mV
			Full range			200	
SR	Slew rate	$V_{CC} = \pm 15\text{ V}$ , $C_L = 100\text{ pF}$ , $V_I = \pm 10\text{ V}$ , $R_L = 10\text{ k}\Omega$	25°C	1.3	2		V/ $\mu\text{s}$
GBW	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$	25°C	1.4	2.1		MHz
$\Phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$	25°C		45		°
THD	Total harmonic distortion		25°C		0.01		%
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$	25°C		19		nV/ $\sqrt{\text{Hz}}$

# TSM102, TSM102A DUAL OPERATIONAL AMPLIFIER, DUAL COMPARATOR, AND VOLTAGE REFERENCE

SLVS602–MARCH 2006

## Comparator Electrical Characteristics

$V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = \text{GND}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	25°C			5	mV
		Full range			9	
$V_{ID}$	Comparator differential input voltage	Full range			$V_{CC+}$	V
$I_{IO}$	Input offset current	25°C			50	nA
		Full range			150	
$I_{IB}$	Input bias current	25°C			250	nA
		Full range			400	
$I_{OH}$	High-level output current	$V_{ID} = 1\text{ V}$ , $V_{CC} = V_O = 30\text{ V}$		0.1		nA
		Full range			1	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{ID} = -1\text{ V}$ , $I_{\text{sink}} = 4\text{ mA}$		250	400	mV
		Full range			700	
$A_{VD}$	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$ , $R_1 = 15\text{ k}\Omega$ , $V_O = 1\text{ V to }11\text{ V}$		200		V/mV
$I_{\text{sink}}$	Output sink current	$V_O = 1.5\text{ V}$ , $V_{ID} = -1\text{ V}$	25°C	6	16	mA
$V_{ICM}$	Input common-mode voltage range		25°C	0	$V_{CC+} - 1.5$	V
			Full range	0	$V_{CC+} - 2$	
$t_{\text{RESP}}$	Response time <sup>(1)</sup>	$R_1 = 5.1\text{ k}\Omega$ to $V_{CC+}$ , $V_{\text{REF}} = 1.4\text{ V}$	25°C		1.3	$\mu\text{s}$
$t_{\text{RESP,large}}$	Large-signal response time	$R_1 = 5.1\text{ k}\Omega$ to $V_{CC+}$ , $V_{\text{REF}} = 1.4\text{ V}$ , $V_I = \text{TTL}$	25°C		300	ns

(1) The response-time specification is for 100-mV input step with 5-mV overdrive. For larger overdrive signals, 300 ns can be obtained.

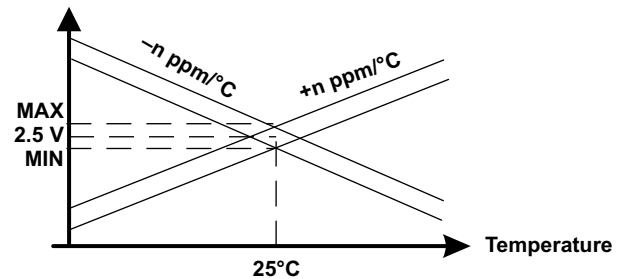
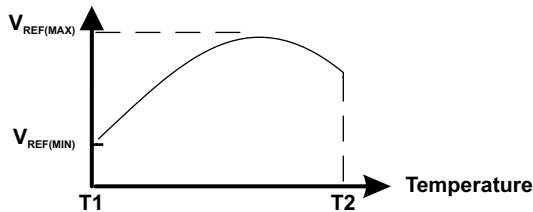
### Voltage-Reference Electrical Characteristics

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT	
V <sub>REF</sub>	Reference voltage <sup>(1)</sup>	TSM102	V <sub>KA</sub> = V <sub>REF</sub> , I <sub>K</sub> = 10 mA, See <a href="#">Figure 1</a>	25°C	2.475	2.5	2.525	V
		TSM102A		25°C	2.49	2.5	2.51	
ΔV <sub>REF</sub>	Reference input voltage deviation over temperature range <sup>(1)</sup>	V <sub>KA</sub> = V <sub>REF</sub> , I <sub>K</sub> = 10 mA, See <a href="#">Figure 1</a>	Full range		7	30	mV	
$\frac{V_{REF}}{T}$	Average temperature coefficient of reference input voltage <sup>(2)</sup>	V <sub>KA</sub> = V <sub>REF</sub> , I <sub>K</sub> = 10 mA	Full range		±22	±100	ppm/°C	
$\frac{V_{REF}}{V_{KA}}$	Ratio of change in reference voltage to change in cathode voltage	V <sub>KA</sub> = 3 V to 36 V, I <sub>K</sub> = 10 mA, See <a href="#">Figure 2</a>	25°C		-1.1	-2	mV/V	
I <sub>REF</sub>	Reference input current	I <sub>K</sub> = 10 mA, R <sub>1</sub> = 10 kΩ, R <sub>2</sub> = ∞, See <a href="#">Figure 2</a>	25°C		1.5	2.5	μA	
			Full range			3		
ΔI <sub>REF</sub>	Reference input current deviation over temperature range	I <sub>K</sub> = 10 mA, R <sub>1</sub> = 10 kΩ, R <sub>2</sub> = ∞, See <a href="#">Figure 2</a>	Full range		0.5	1	μA	
I <sub>min</sub>	Minimum cathode current for regulation	V <sub>KA</sub> = V <sub>REF</sub> , See <a href="#">Figure 1</a>	25°C		0.5	1	mA	
I <sub>K,OFF</sub>	Off-state cathode current	See <a href="#">Figure 3</a>	25°C		180	500	nA	

(1) ΔV<sub>REF</sub> is defined as the difference between the maximum and minimum values obtained over the full temperature range.

$$\Delta V_{REF} = V_{REF(MAX)} - V_{REF(MIN)}$$

(2) The temperature coefficient is defined as the slopes (positive and negative) of the voltage vs temperature limits within which the reference voltage is specified.



PARAMETER MEASUREMENT INFORMATION

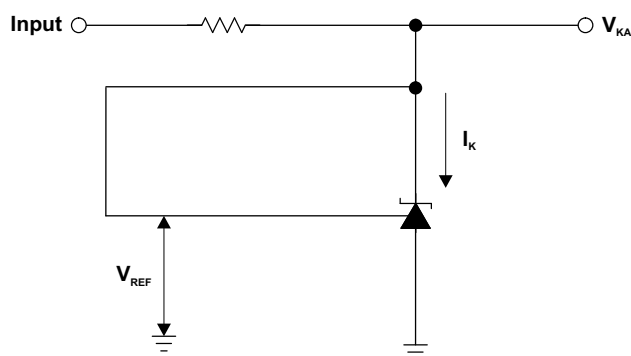


Figure 1. Test Circuit for  $V_{KA} = V_{REF}$

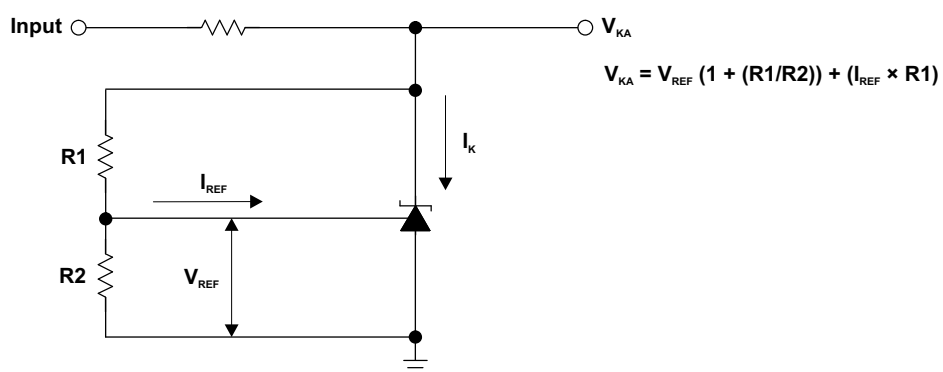


Figure 2. Test Circuit for  $V_{KA} > V_{REF}$

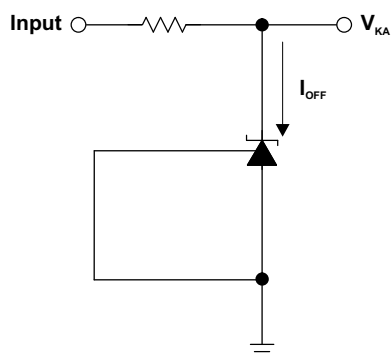


Figure 3. Test Circuit for  $I_{OFF}$

**TYPICAL CHARACTERISTICS**

**AMPLIFIER TOTAL HARMONIC DISTORTION  
VS  
FREQUENCY**

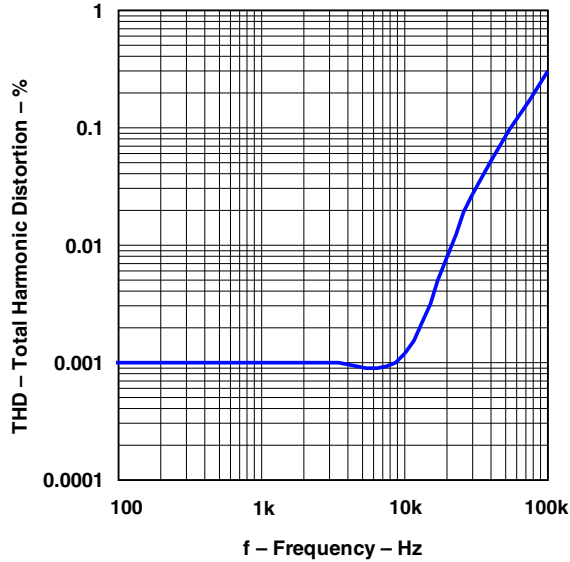


Figure 4.

**AMPLIFIER NOISE VOLTAGE  
VS  
FREQUENCY**

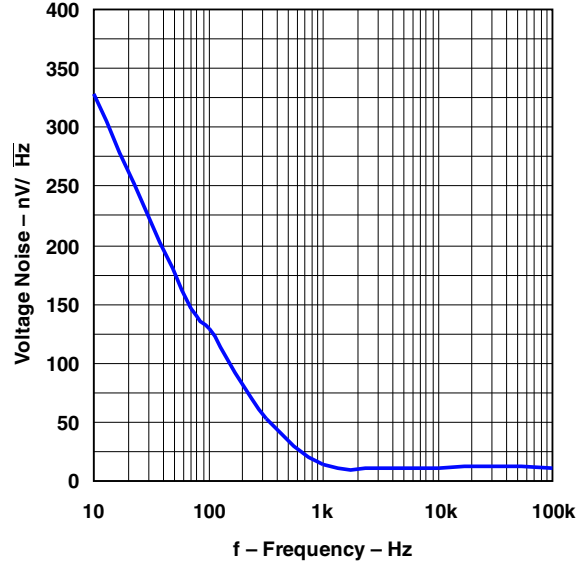


Figure 5.

**GAIN AND PHASE  
VS  
FREQUENCY**

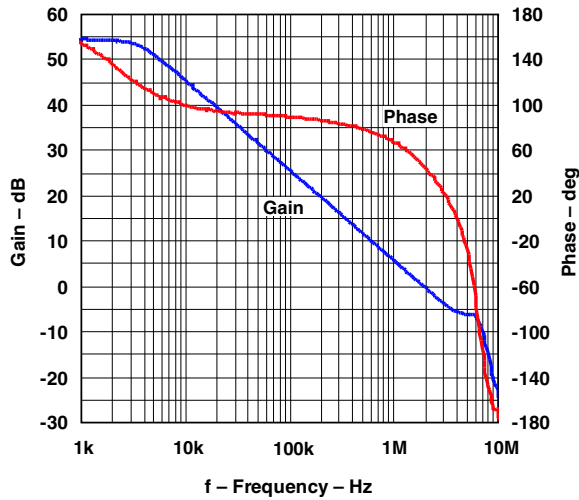


Figure 6.

**V<sub>REF</sub> STABILITY  
VS  
CAPACITANCE**

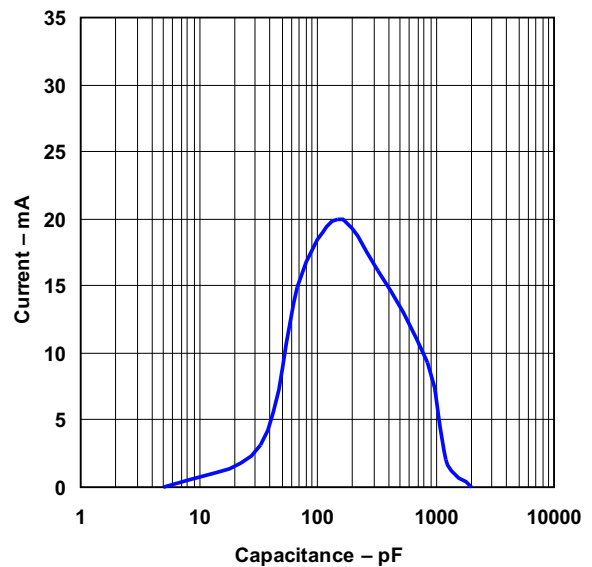


Figure 7.

TYPICAL CHARACTERISTICS (continued)

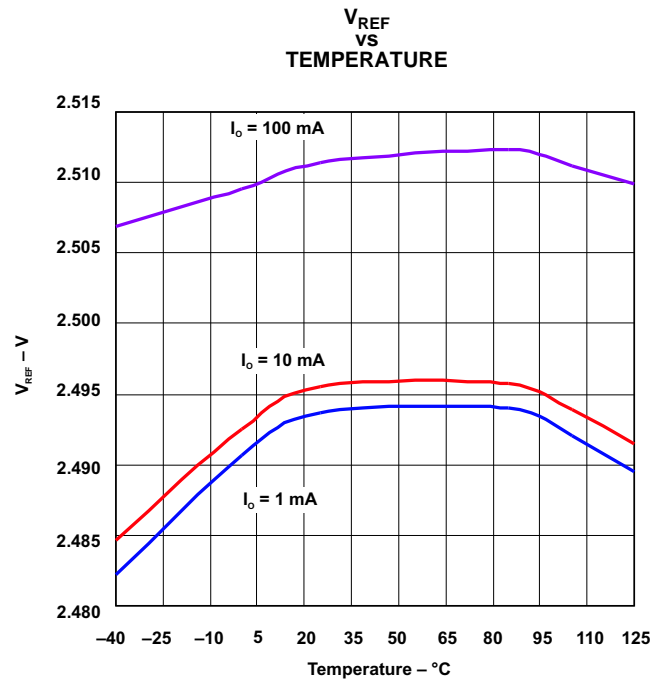


Figure 8.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSM102AIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102AI	<a href="#">Samples</a>
TSM102AIPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI	<a href="#">Samples</a>
TSM102AIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI	<a href="#">Samples</a>
TSM102ID	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I	<a href="#">Samples</a>
TSM102IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I	<a href="#">Samples</a>
TSM102IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM102AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TSM102AIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSM102IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TSM102IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSM102AIDR	SOIC	D	16	2500	356.0	356.0	35.0
TSM102AIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TSM102IDR	SOIC	D	16	2500	356.0	356.0	35.0
TSM102IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal



Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TSM102AIPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TSM102ID	D	SOIC	16	40	506.6	8	3940	4.32

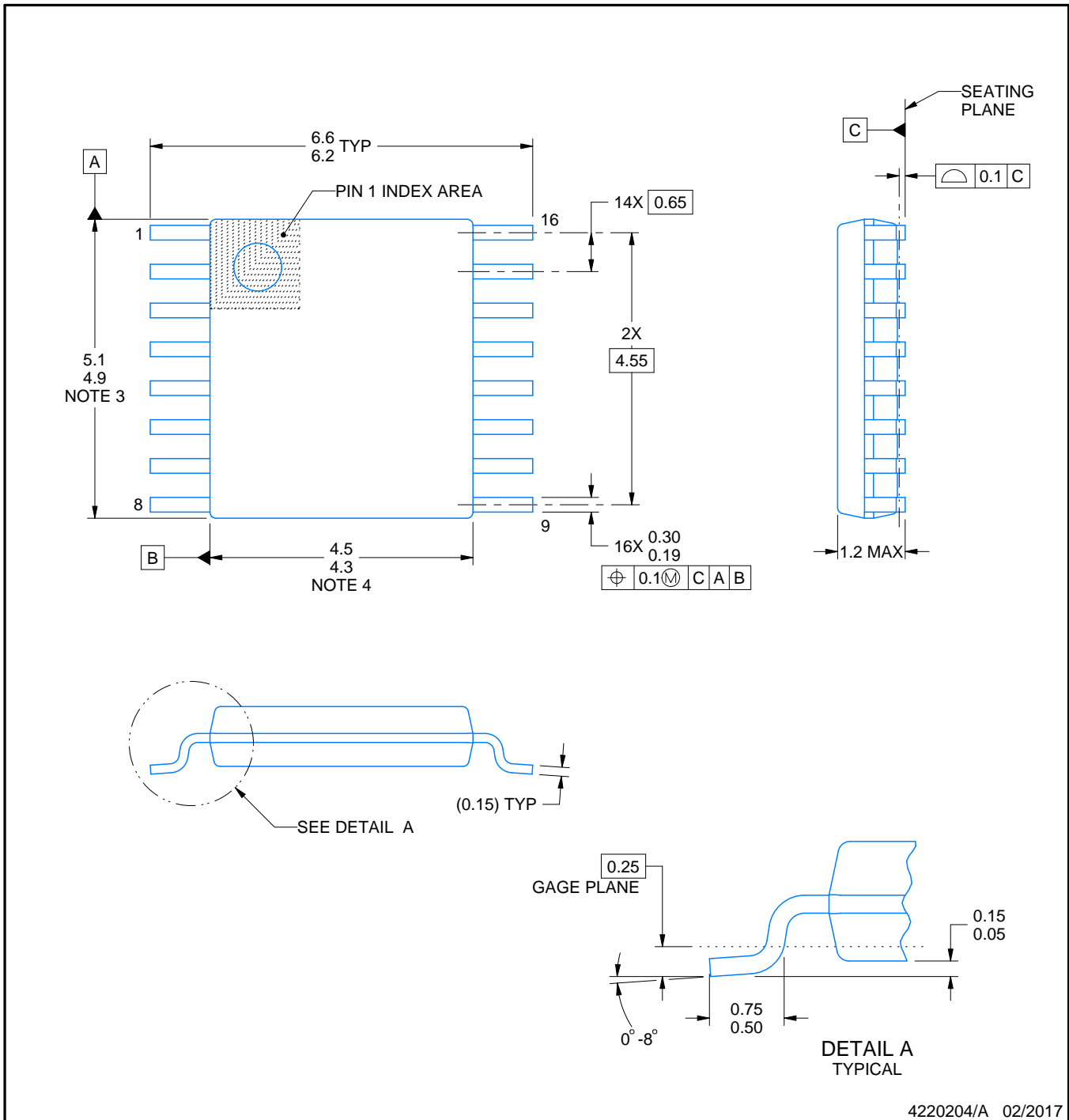
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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