THE DATASHEET OF

CYW43455XKUBGT

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CYW43455

Single-Chip 5G WiFi IEEE 802.11n/ac MAC/ Baseband/ Radio with Integrated Bluetooth 5.0

The Cypress CYW43455 single-chip device provides the highest level of integration for Internet of Things applications and handheld wireless system with integrated single-stream IEEE 802.11ac MAC/baseband/radio and, Bluetooth 5.0.

In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates of up to 433.3 Mbps. All rates specified in the IEEE 802.11a/b/g/n are supported. Included on-chip are 2.4 GHz and 5 GHz transmit amplifiers and receive low-noise amplifiers. Optional external PAs and LNAs are also supported.

The WLAN section supports the following host interface options: an SDIO v3.0 interface that can operate in 4b or 1b mode, a high-speed 4-wire UART, and a PCIe[1]Gen1 (3.0 compliant) interface. The Bluetooth section supports a high-speed 4-wire UART interface.

Using advanced design techniques and process technology to reduce active and idle power, the CYW43455 is designed to address the needs of mobile devices that require minimal power consumption and compact size. It includes a power management unit which simplifies the system power topology and allows for direct operation from a mobile platform battery while maximizing battery life.

The CYW43455 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. In addition, coexistence support for external radios (such as LTE cellular and GPS) is provided via an external interface. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a handheld system is achieved.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM43455	CYW43455
BCM43455XKUBG	CYW43455XKUBG
BCM43455HKUBG	CYW43455HKUBG
BCM4329	CYW4329
BCM4330	CYW4330

Features

IEEE 802.11x Key Features

- IEEE 802.11ac compliant.
- Support for TurboQAM® (MCS0–MCS8 86 Mbps and MCS0–MCS9 96 Mbps) HT20, 20 MHz channel bandwidth.
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- Supports explicit IEEE 802.11ac transmit beamforming.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Support for optional front-end modules (FEM) with external PAs and LNAs.
- Supports optional integrated T/R switch for 2.4 GHz band.
- Supports RF front-end architecture with a single dual-band antenna shared between Bluetooth and WLAN for lowest system cost.
- Shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.
- Internal fractional-n PLL allows support for a wide range of reference clock frequencies.
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE or GPS.

1. The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

- Supports standard SDIO v3.0 (including DDR50 mode at 50 MHz and SDR104 mode at 208 MHz, 4-bit and 1-bit) interfaces.
- Backward compatible with SDIO v2.0 host interfaces.
- PCIe[2] mode complies with PCI Express base specification revision 3.0 compliant Gen1 interface for ×1 lane and power management base specification.
- Integrated ARMCR4 processor with tightly coupled memory for complete WLAN subsystem functionality and minimizing the need to wake-up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On-chip memory includes 800KB SRAM and 704 KB ROM.

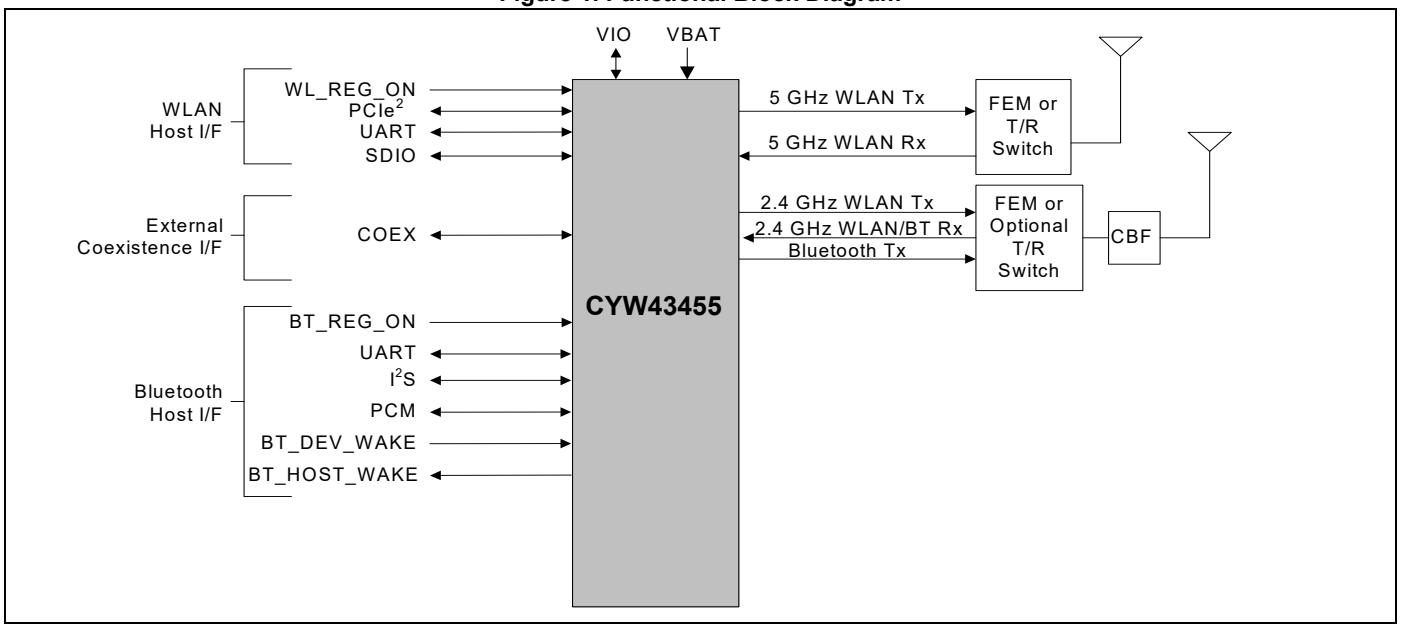
Bluetooth Key Features

- Complies with Bluetooth Core Specification v5.0 with provisions for supporting future specifications.
  - QDID:121361
  - Declaration ID: D040197
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- Interface support, host controller interface (HCI) using a high-speed UART interface and PCM for audio data.
- Low power consumption improves battery life of handheld devices.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.

General Features

- Supports battery voltage range from 3.0 V to 5.25 V supplies with internal switching regulator.
- Programmable dynamic power management
- 6 Kbit OTP for storing board parameters.
- GPIOs: 15
- 140-ball WLBGA package (4.47 mm × 5.27 mm, 0.4 mm pitch).
- Security:
  - WPA and WPA2 (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - Reference WLAN subsystem provides Cisco Compatible Extensions (CCX, CCX 2.0, CCX 3.0, and CCX 4.0)
  - Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design.

Figure 1. Functional Block Diagram



2. The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

Contents

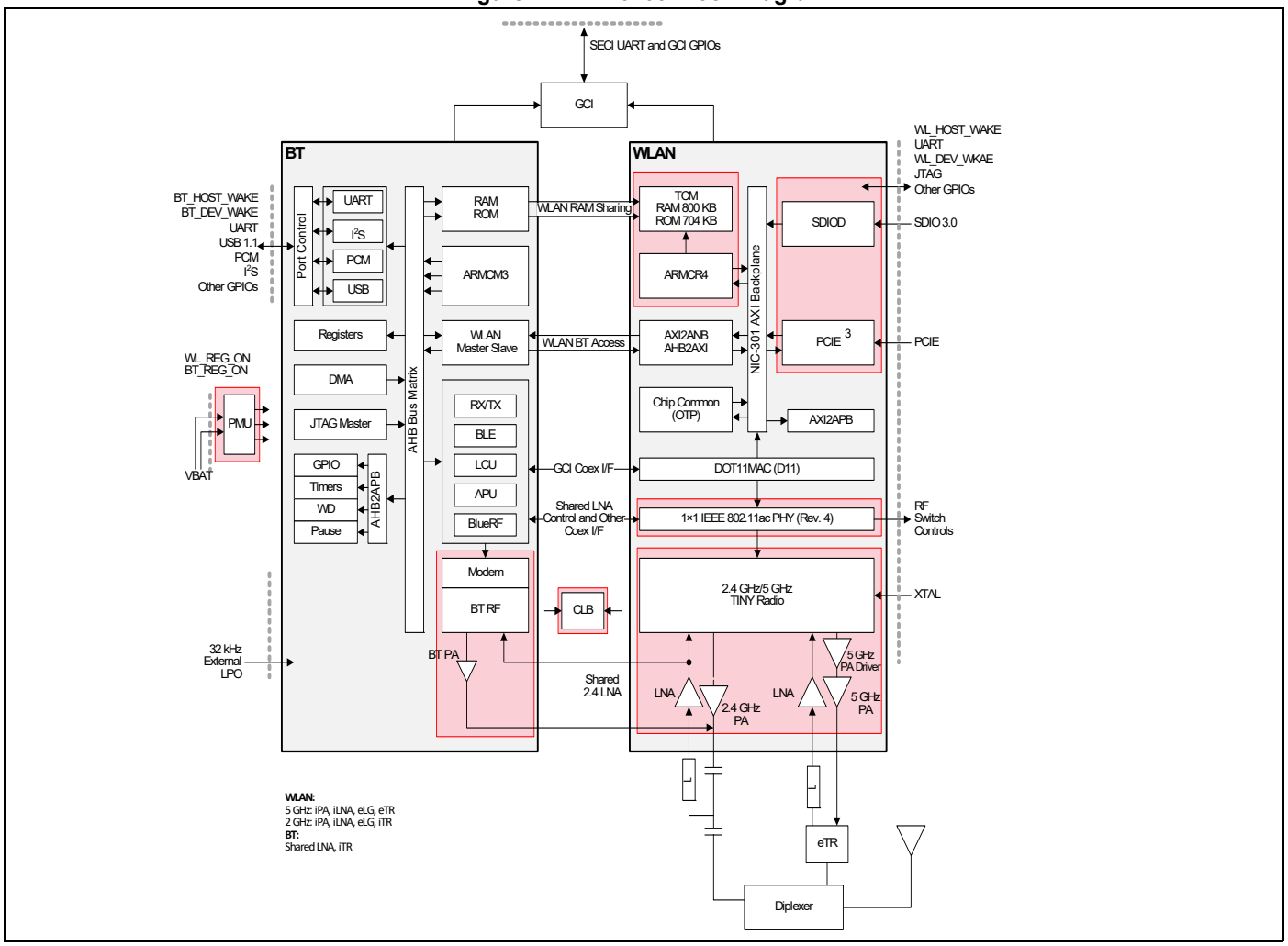
1. CYW43455 Overview

1.1 Overview

The Cypress CYW43455 single-chip device provides the highest level of integration for IoT applications handheld wireless systems, with integrated IEEE 802.1 a/b/g/n/ac MAC/baseband/radio and, Bluetooth 5.0 + EDR (Enhanced Data Rate). It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the CYW43455 and their associated external interfaces, which are described in greater detail in the following sections5 .

Figure 2. CYW43455 Block Diagram



3. The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

1.2 Standards Compliance

The CYW43455 supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0
- Bluetooth 4.2 (Bluetooth Low Energy)
- Bluetooth 5.0 compliant
- IEEE 802.11ac single-stream mandatory and optional requirements for 20, 40, and 80 MHz channels
- IEEE 802.11n (Handheld Device Class, Section 11)
- IEEE 802.11a
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i
- Security:
  - WEP
  - WPA Personal
  - WPA2 Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (hardware accelerator)
  - TKIP (hardware accelerator)
  - CKIP (software support)
- Proprietary protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
  - WFAEC
- IEEE 802.15.2 Coexistence Compliance (on-silicon solution compliant with IEEE 3-wire requirements)

The CYW43455 supports the following future drafts/standards:

- IEEE 802.11r (fast roaming between APs)
- IEEE 802.11w (secure management frames)
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS Enhancements (as per the WMM specification is already supported)
  - IEEE 802.11h 5 GHz Extensions
  - IEEE 802.11i MAC Enhancements
  - IEEE 802.11k Radio Resource Measurement

2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW43455. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth, and WLAN functions in embedded designs.

A single VBAT (3.0 V to 5.25 V6.0 V DC max.) and VIO supply (1.8 V to 3.3 V) can be used, with all additional voltages being provided by the regulators in the CYW43455.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO and LNLDO power-up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted. The CLDO and LNLDO may be turned off/on based on the dynamic demands of the digital baseband.

The CYW43455 allows for an extremely low power-consumption mode by completely shutting down the CBUCK, CLDO, and LNLDO regulators. When in this state, the LPLDO1 (which is the low-power linear regulator that is supplied by the system VIO supply) provides the CYW43455 with all required voltage, further reducing leakage currents.

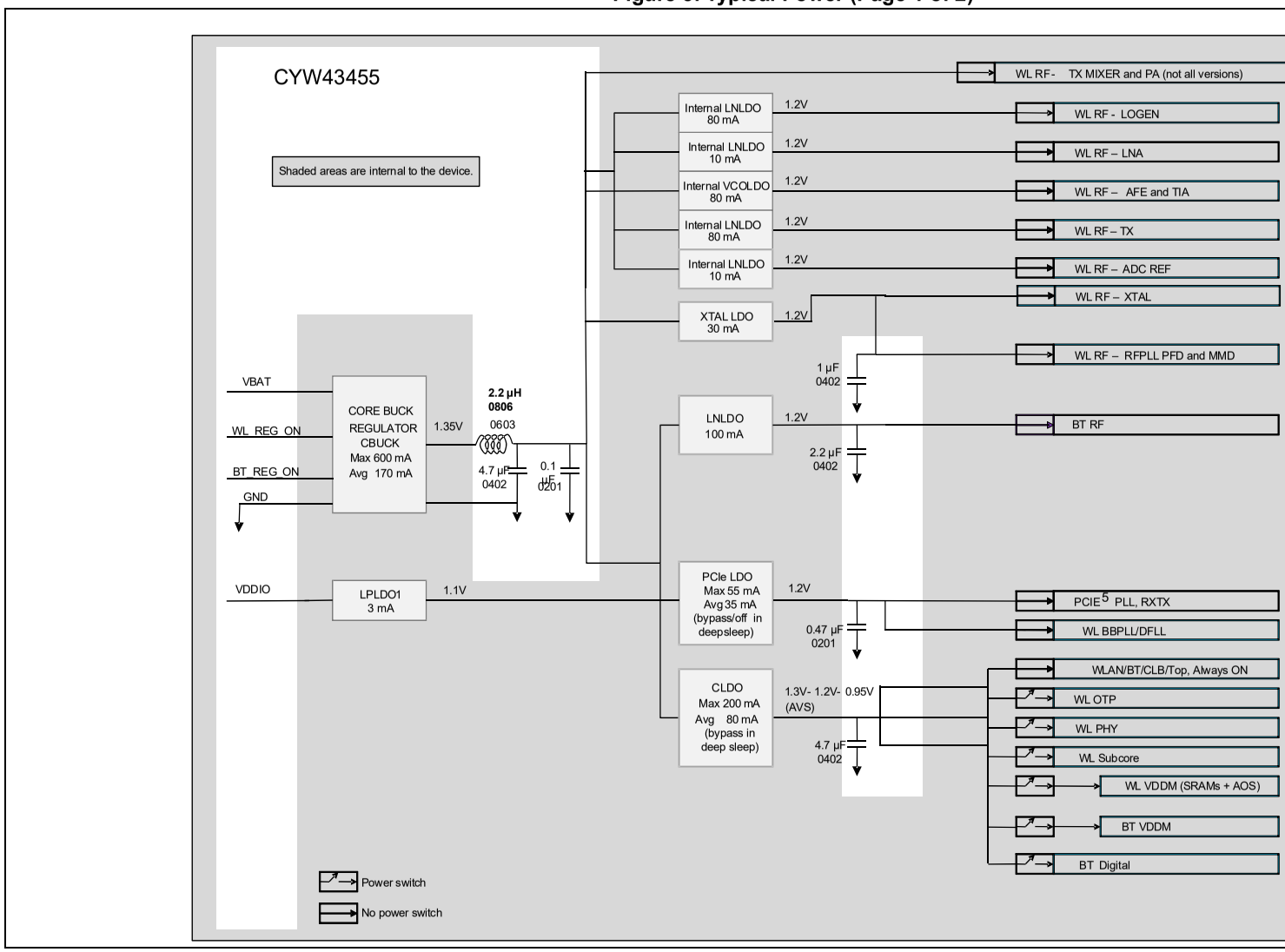
2.2 CYW43455 PMU Features

- VBAT to 1.35 Vout (170 mA nominal, 600 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3 Vout (200 mA nominal, 450 mA–850 mA maximum) LDO3P3
- VBAT to 2.5 Vout (15 mA nominal, 70 mA maximum) BTLDO2P5
- 1.35 V to 1.2 Vout (100 mA nominal, 150 mA maximum) LNLDO
- 1.35 V to 1.2 Vout (80 mA nominal, 200 mA maximum) CLDO with bypass mode for deep-sleep
- 1.35 V to 1.2 Vout (35 mA nominal, 55 mA maximum) LDO for PCIE [4]
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from extremely low power-consumption mode.

Figure 3 and Figure 4 show the regulators and a typical power topology7.

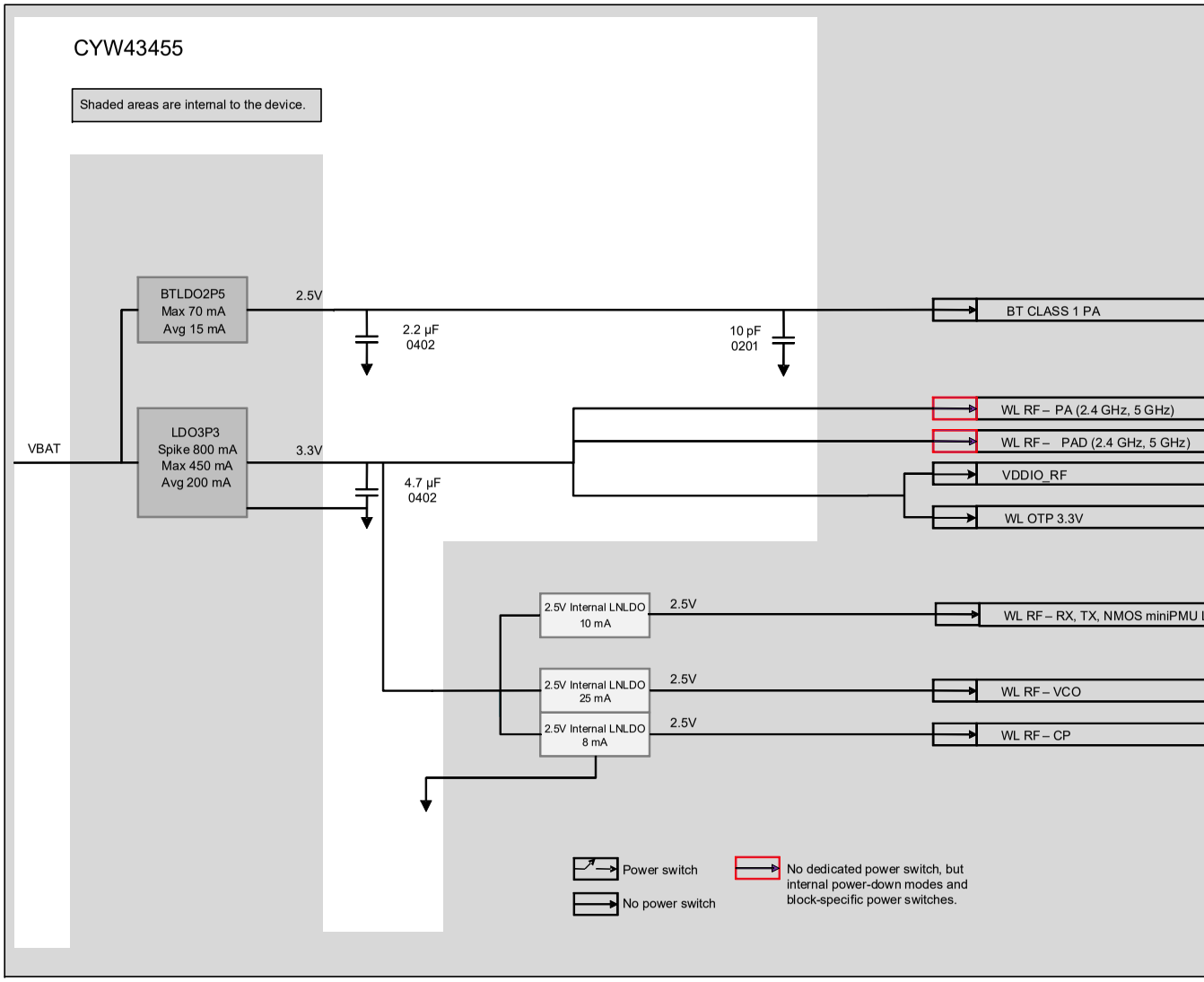
4. The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

Figure 3. Typical Power (Page 1 of 2)



5. The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

Figure 4. Typical Power Topology (Page 2 of 2)



2.3 WLAN Power Management

The CYW43455 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW43455 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW43455 includes an advanced WLAN power management unit (PM) sequencer. The PMU sequencer provides significant power savings by putting the CYW43455 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW43455 WLAN power states are described as follows:

- Active mode—All WLAN blocks in the CYW43455 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Doze mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW43455 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake-up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- Deep-sleep mode—Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the PCIe[6] bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW reinitialization.
- Power-down mode—The CYW43455 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is used to minimize system power consumption. It enables and disables various system resources based on a computation of required resources and a table that describes the relationship between resources and the time required to enable and disable them.

Resource requests may derive from several sources: clock requests from cores, the minimum resources defined in the *ResourceMin* register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states:

- enabled
- disabled
- transition_on
- transition_off

The timer contains 0 when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can transition immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can transition immediately from enabled to disabled. The terms *enable sequence* and *disable sequence* refer to either the immediate transition or the timer load-decrement sequence.

6. The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW43455 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When the CYW43455 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW43455 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the CYW43455, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW43455 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When the CYW43455 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

2.6 Power-Up/Power-Down/Reset Circuits

The CYW43455 has two signals (see Table 2) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see Section 19.: “Power-Up Sequence and Timing”.

Table 2. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW43455 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW43455 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

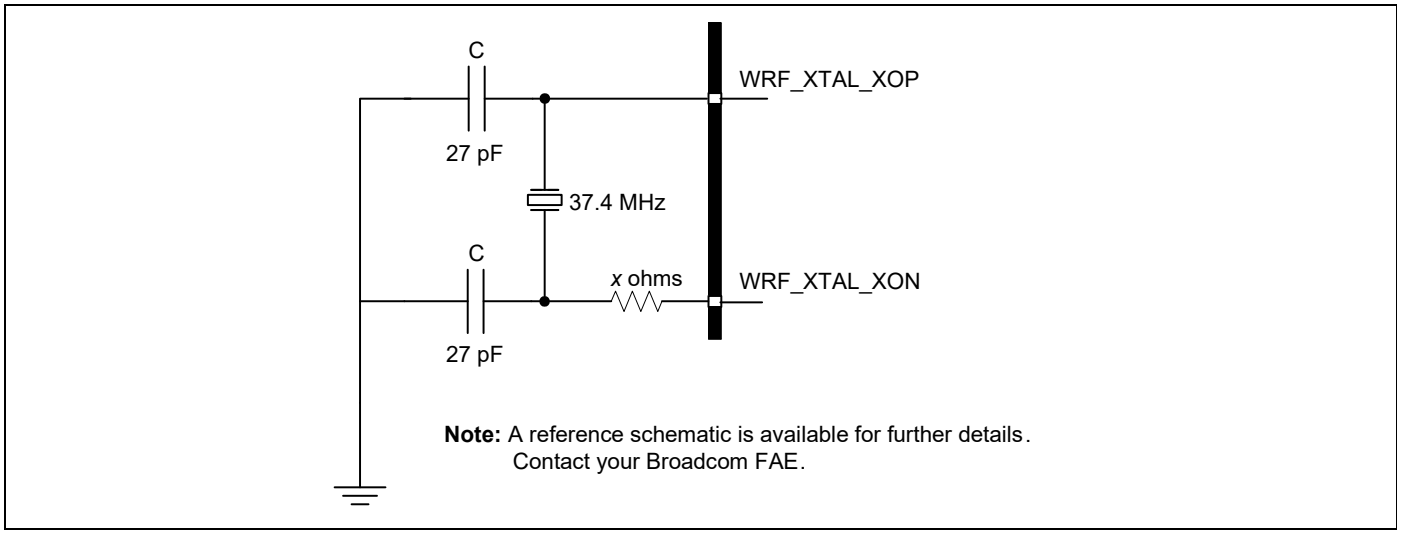
3. Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

3.1 Crystal Interface and Clock Generation

The CYW43455 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 5. Consult the reference schematics for the latest configuration.

Figure 5. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW43455 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal interface are listed in Table 3.

Note: Although the fractional-N synthesizer can support alternative reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Cypress for further details.

3.2 External Frequency Reference

As an alternative to a crystal, an external precision frequency reference can be used, provided that it meets the Phase Noise requirements listed in Table 3.

If used, the external clock should be connected to the WRF_XTAL_XOP pin through an external 1000 pF coupling capacitor, as shown in Figure 6. The internal clock buffer connected to this pin will be turned OFF when the CYW43455 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the WRF_XTAL_VDD1P35 pin.

Figure 6. Recommended Circuit to Use With an External Reference Clock

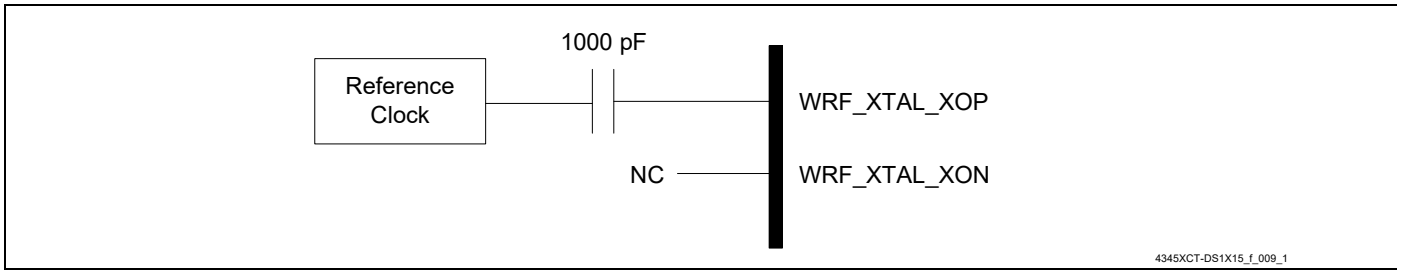


Table 3. Crystal Oscillator and External Clock—Requirements and Performance

Parameter	Conditions/Notes	Crystal[1]			External Frequency Reference[2 3]			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	2.4G and 5G bands, IEEE 802.11ac operation	35	–	52	–	52	–	MHz
Frequency	5G Band, IEEE 802.11n operation only	19	–	52	35	–	52	MHz
	2.4G band IEEE 802.11n operation, and both bands legacy IEEE 802.11a/b/g operation only	Between 19 MHz and 52 MHz [4, 5]						
Frequency tolerance over the lifetime of the equipment, including temperature[6]	Without trimming	–20	–	20	–20	–	20	ppm
Crystal load capacitance	–	–	16	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input impedance (WRF_XTAL_XOP)	Resistive	–	–	–	30k	100k	–	Ω
	Capacitive	–	–	7.5	–	–	7.5	pF
WRF_XTAL_XOP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
WRF_XTAL_XOP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_XOP input voltage (see Figure 6)	IEEE 802.11a/b/g operation only	–	–	–	400	–	1200	mV_{p-p}
WRF_XTAL_XOP input voltage (see Figure 6)	IEEE 802.11n/ac AC-coupled analog input	–	–	–	1	–	–	V_{p-p}
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[7] (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz

Table 3. Crystal Oscillator and External Clock—Requirements and Performance (continued)

Parameter	Conditions/Notes	Crystal[1]			External Frequency Reference[2 3]			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Phase Noise[7] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–144	dBc/Hz
Phase Noise[7] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase Noise[7] (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–149	dBc/Hz
Phase Noise[7] (IEEE 802.11ac, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–148	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–155	dBc/Hz

1. (Crystal) Use WRF_XTAL_XON and WRF_XTAL_XOP.
2. See "External Frequency Reference" for alternative connection methods.
3. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.
4. BT_TM6 should be tied low for a 52 MHz clock reference. For other frequencies, BT_TM6 should be tied high. Note that 52 MHz is not an auto-detected frequency using the LPO clock.
5. The frequency step size is approximately 80 Hz resolution.
6. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
7. Assumes that external clock has a flat phase noise response above 100 kHz.

3.3 Frequency Selection

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard handset reference frequencies of 19.2, 19.8, 24, 26, 33.6, 37.4, 38.4, and 52 MHz, but also other frequencies in this range, with approximately 80 Hz resolution. The CYW43455 must have the reference frequency set correctly in order for any of the UART or PCM interfaces to function correctly, since all bit timing is derived from the reference frequency.

Note: The fractional-N synthesizer can support many reference frequencies. However, frequencies other than the default require support to be added in the driver plus additional, extensive system testing. Contact Cypress for further details.

The reference frequency for the CYW43455 may be set in the following ways:

- Set the **xtalfreq=xxxxx** parameter in the nvram.txt file (used to load the driver) to correctly match the crystal frequency.
- Auto-detect any of the standard handset reference frequencies using an external LPO clock.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the CYW43455 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for auto frequency detection to work correctly, the CYW43455 must have a valid and stable 32.768 kHz LPO clock that meets the requirements listed in Table 4 and is present during power-on reset.

3.4 External 32.768 kHz Low-Power Oscillator

The CYW43455 uses a secondary low frequency clock for low-power-mode timing. An external 32.768 kHz precision oscillator is required.

Table 4. External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[1]	>100k <5	Ω pF
Clock jitter (during initial start-up)	<10,000	ppm

1. When power is applied or switched off.

4. Bluetooth Subsystem Overview

The CYW43455 is a Bluetooth 5.0 + EDR-compliant and, baseband processor with 2.4 GHz transceiver.

The CYW43455 is the optimal solution for any Bluetooth voice and/or data application. The Bluetooth subsystem presents a standard host controller interface (HCI) via a high-speed UART and PCM for audio. The CYW43455 incorporates all Bluetooth 5.0 mandatory features include secure simple pairing, sniff subrating, and encryption pause and resume.

The CYW43455 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent mobile phone temperature applications and the tightest integration into mobile handsets and portable devices. It provides full radio compatibility to operate simultaneously with GPS, WLAN, and cellular radios.

The Bluetooth transmitter also features a Class 1 power amplifier with Class 2 capability.

4.1 Features

Primary CYW43455 Bluetooth features include:

- Bluetooth 5,0 complaint and qualified
- Fully supports Bluetooth Core Specification version 4.2 + EDR features:
  - Adaptive frequency hopping (AFH)
  - Quality of service (QoS)
  - Extended synchronous connections (eSCO)—voice connections
  - Fast connect (interlaced page and inquiry scans)
  - Secure simple pairing (SSP)
  - Sniff subrating (SSR)
  - Encryption pause resume (EPR)
  - Extended inquiry response (EIR)
  - Data packet length extension
  - Link supervision timeout (LST)
  - Secure connections
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.2 + HS packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Cypress fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host Controller Power Management)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- Supports a low-power crystal, which can be used during power save mode for better timing accuracy.

4.2 Bluetooth Radio

The CYW43455 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

4.2.1 Transmit

The CYW43455 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

4.2.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

4.2.4 Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW43455 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.7 Receiver Signal Strength Indicator

The radio portion of the CYW43455 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

4.2.8 Local Oscillator Generation

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The CYW43455 uses an internal RF and IF loop filter.

4.2.9 Calibration

The CYW43455 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

5.1 Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode Bluetooth Low Energy (BT and BLE operation)
- Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure Simple Pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

5.2 Bluetooth 4.2 Features

The BBC supports all Bluetooth 4.2 features, with the following benefits:

- Dual-mode classic Bluetooth and classic low energy (BT and BLE) operation
- Low-energy physical layer
- Low-energy link layer
- Enhancements to HCI for low energy
- Low-energy direct test mode
- 128 AES-CCM secure connection for both BT and BLE
- LE Data Packet Length Extension
- LE Secure Connections

Note: The CYW43455 is compatible with the Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

5.3 Bluetooth Low Energy

The CYW43455 supports the Bluetooth Low Energy operating mode.

5.4 Bluetooth 5.0

CYW43455 is qualified for and supports the mandatory features of the Bluetooth 5.0 specification.

5.5 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

5.6 Test Mode Support

The CYW43455 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW43455 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

5.7 Bluetooth Power Management Unit

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core.

The power management functions provided by the CYW43455 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management

5.7.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.7.2 Host Controller Power Management

When running in UART mode, the CYW43455 may be configured so that dedicated signals are used for power management hand-shaking between the CYW43455 and the host. The basic power saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation. Table 5 describes the power-control handshake signals used with the UART interface.

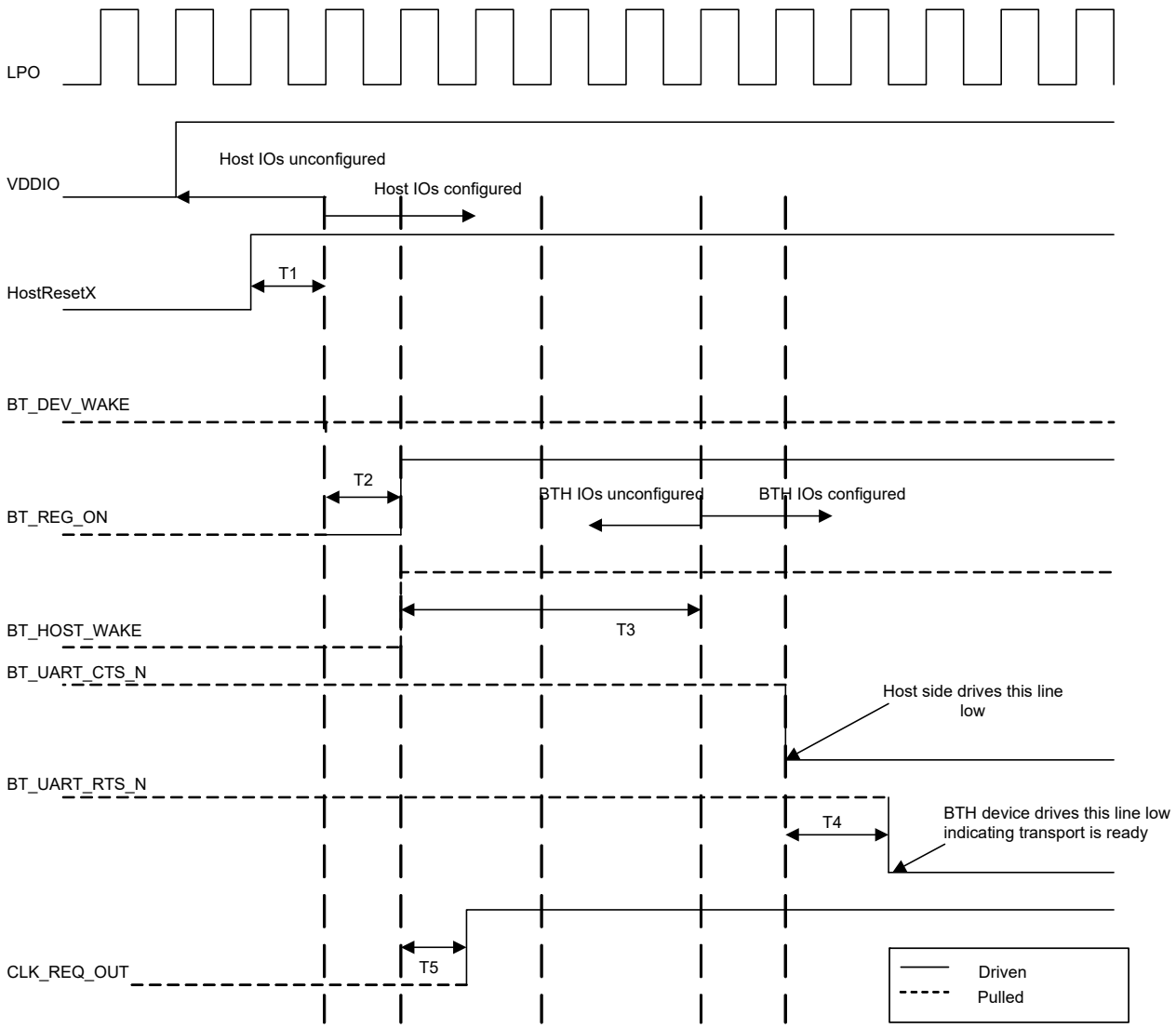
Note: Pad function Control Register is set to 0 for these pins. See ""DC Characteristics"" for more details.

Table 5. Power Control Pin Description

Signal	Mapped to Pin	Type	Description
BT_DEV_WAKE	BT_GPIO_0	I	Bluetooth device wake-up: Signal from the host to the CYW43455 indicating that the host requires attention. ■ Asserted: The Bluetooth device must wake-up or remain awake. ■ Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_HOST_WAKE	BT_GPIO_1	O	Host wake-up. Signal from the CYW43455 to the host indicating that the CYW43455 requires attention. ■ Asserted: host device must wake-up or remain awake. ■ Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
BT_CLK_REQ	BT_CLK_REQ_OUT WL_CLK_REQ_OUT	O	The CYW43455 asserts BT_CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock. The BT_CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the CYW43455 powers up or resets when VDDIO is present.

Figure 7 shows the startup signaling sequence prior to software download.

Figure 7. Startup Signaling Sequence Prior to Software Download



Notes :
T1 is the time for Host to settle it's IOs after a reset.
T2 is the time for Host to drive BT_REG_ON high after the Host IOs are configured.
T3 is the time for BTH (Bluetooth) device to settle its IOs after a reset and reference clock settling time has elapsed.
T4 is the time for BTH device to drive BT_UART_RTS_N low after the Host drives BT_UART_CTS_N low. This assumes the BTH device has already completed initialization.
T5 is the time for BTH device to drive CLK_REQ_OUT high after BT_REG_ON goes high. Note this pin is used for designs that use an external reference clock source from the Host. This pin is irrelevant for Crystal reference clock based designs where the BTH device generates it's own reference clock from an external crystal connected to it's oscillator circuit.
Timing diagram assumes VBAT is present.

5.7.3 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth-specified low-power connection modes: sniff, hold, and park. While in these modes, the CYW43455 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When the CYW43455 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the CYW43455 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O.

During the low-power shutdown state, provided VDDIO remains applied to the CYW43455, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the CYW43455 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

Two CYW43455 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the CYW43455 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

Wideband Speech

The CYW43455 provides support for wideband speech (WBS) using on-chip Cypress technology. The CYW43455 can perform subband-codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

Packet Loss Concealment

Packet Loss Concealment (PLC) improves apparent audio quality for systems with marginal link performance. Bluetooth messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream. Packet loss can be mitigated in several ways:

- Fill in zeros.
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth headsets).
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat).

These techniques cause distortion and popping in the audio stream. The CYW43455 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. Figure 8 and Figure 9 show audio waveforms with and without Packet Loss Concealment. Cypress PLC/BEC algorithms also support wideband speech.

Figure 8. CVSD Decoder Output Waveform Without PLC

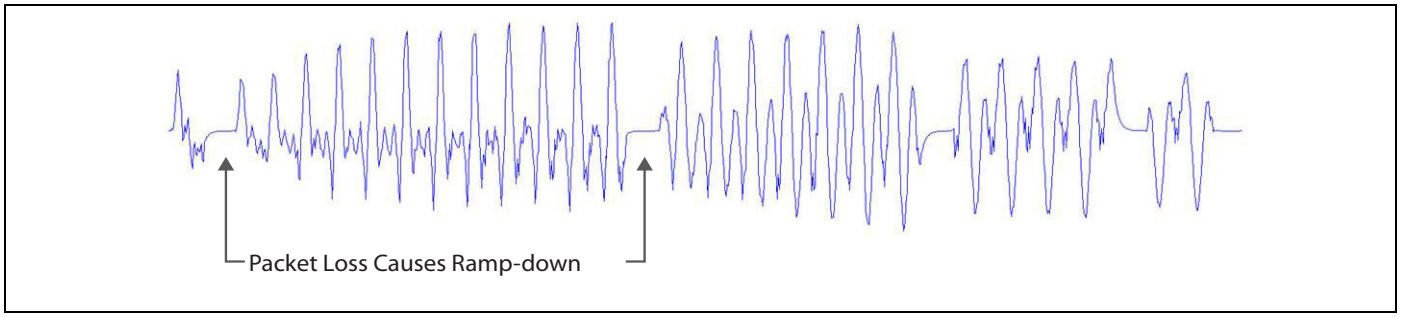
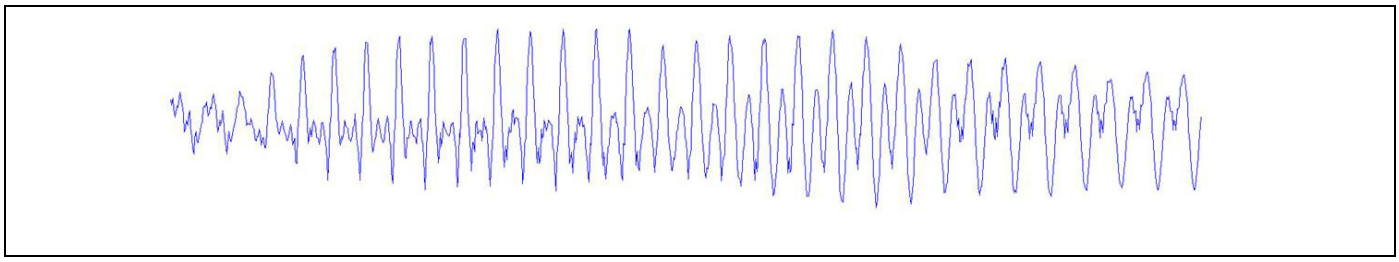


Figure 9. CVSD Decoder Output Waveform After Applying PLC



Audio Rate-Matching Algorithms

The CYW43455 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth audio data rates.

Codec Encoding

The CYW43455 can support SBC and mSBC encoding and decoding for wideband speech.

Multiple Simultaneous A2DP Audio Stream

The CYW43455 has the ability to take a single audio stream and output it to multiple Bluetooth devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

Burst Buffer Operation

The CYW43455 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

5.8 Adaptive Frequency Hopping

The CYW43455 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.9 Advanced Bluetooth/WLAN Coexistence

The CYW43455 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The CYW43455 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The CYW43455 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The CYW43455 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core’s channel information.

5.10 Fast Connection (Interlaced Page and Inquiry Scans)

The CYW43455 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

6. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the ARM Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control (LC) layer, up to the host controller interface (HCI).

The ARM core is paired with a memory unit that contains 845 KB of ROM memory for program storage and boot ROM, 270 KB of RAM for data scratchpad and patch RAM code. The internal ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the CYW43455 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the CYW4329 and CYW4330 devices.

6.1 RAM, ROM, and Patch Memory

The CYW43455 Bluetooth core has 270 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 845 KB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

6.2 Reset

The CYW43455 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

7. Bluetooth Peripheral Transport Unit

7.1 SPI Interface

The CYW43455 supports a slave SPI HCI transport with an input clock range of up to 16 MHz. Higher clock rates can be possible. The physical interface between the SPI master and the CYW43455 consists of the four SPI signals (SPI_CSB, SPI_CLK, SPI_SI, and SPI_SO) and one interrupt signal (SPI_INT). The SPI signals are muxed onto the UART signals (see Table 6). The CYW43455 can be configured to accept active-low or active-high polarity on the SPI_CSB chip select signal. It can also be configured to drive an active-low or active-high SPI_INT interrupt signal. Bit ordering on the SPI_SI and SPI_SO data lines can be configured as either little-endian or big-endian. Additionally, proprietary sleep mode and half-duplex handshaking is implemented between the SPI master and the CYW43455. The SPI_INT is required to negotiate the start of a transaction. The SPI interface does not require flow control in the middle of a payload. The FIFO is large enough to handle the largest packet size. Only the SPI master can stop the flow of bytes on the data lines, since it controls SPI_CSB and SPI_CLK. Flow control should be implemented in the higher layer protocols.

Table 6. SPI-to-UART Signal Mapping

SPI Signals	UART Signals
SPI_CLK	BT_UART_CTS_N
SPI_CSB	BT_UART_RTS_N
SPI_MISO	BT_UART_RXD
SPI_MOSI	BT_UART_TXD
SPI_INT	BT_HOST_WAKE

7.2 SPI/UART Transport Detection

The BT_HOST_WAKE (BT_GPIO1) pin is also used for BT transport detection. The transport detection occurs during the power-up sequence. It selects either UART or SPI transport operation based on the following pin state:

- If the BT_HOST_WAKE (BT_GPIO1) pin is pulled low by an external pull-down during power-up, it selects the SPI transport interface.
- If the BT_HOST_WAKE (BT_GPIO1) pin is not pulled low externally during power-up, then the default internal pull-up is detected as a high and it selects the UART transport interface.

7.3 PCM Interface

The CYW43455 supports two independent PCM interfaces that share the pins with the I2S interfaces. The PCM Interface on the CYW43455 can connect to linear PCM Codec devices in master or slave mode. In master mode, the CYW43455 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW43455.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

7.3.1 Slot Mapping

The CYW43455 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.3.2 Frame Synchronization

The CYW43455 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization

signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.3.3 Data Formatting

The CYW43455 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYW43455 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

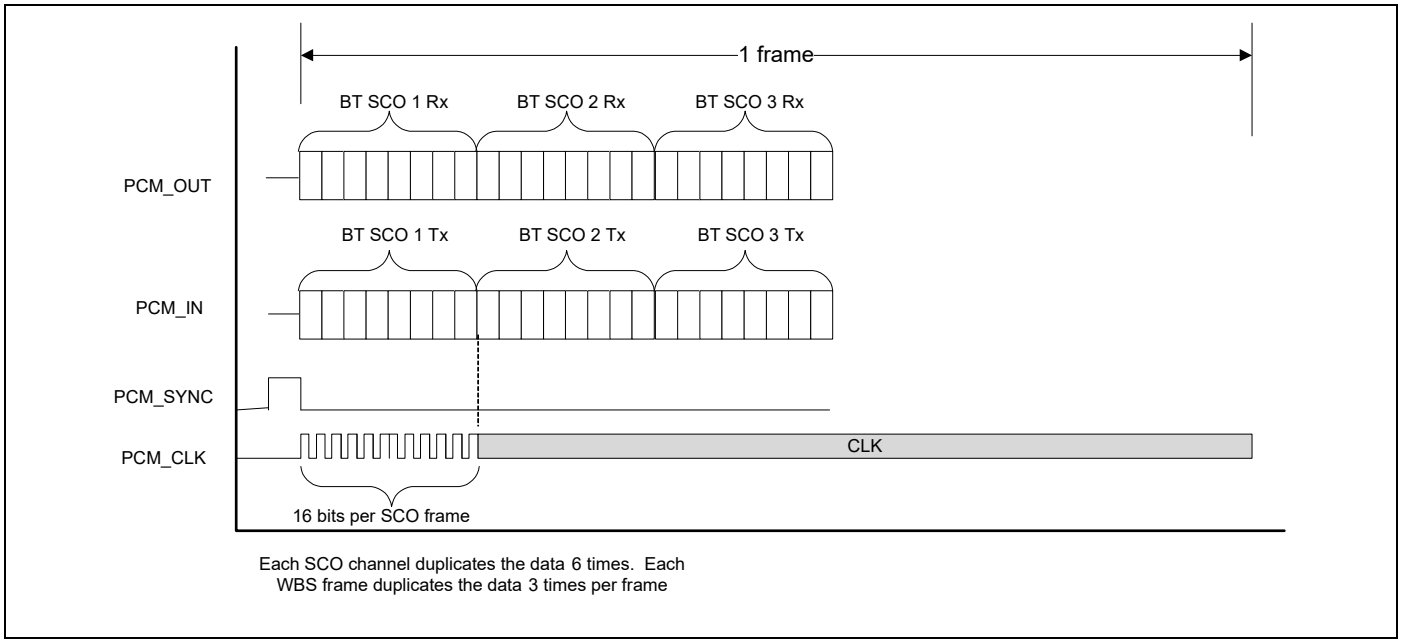
7.3.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. The CYW43455 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

7.3.5 Multiplexed Bluetooth Over PCM

Bluetooth supports multiple audio streams within the Bluetooth channel and both 16 kHz and 8 kHz streams can be multiplexed. This mode of operation is only supported when the Bluetooth host is the master. Figure 10 shows the operation of the multiplexed transport with three simultaneous SCO connections. To accommodate additional SCO channels, the transport clock speed is increased. To change between modes of operation, the transport must be halted and restarted in the new configuration.

Figure 10. Functional Multiplex Data Diagram



7.3.6 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

7.3.7 PCM Interface Timing

Short Frame Sync, Master Mode

Figure 11. PCM Timing Diagram (Short Frame Sync, Master Mode)

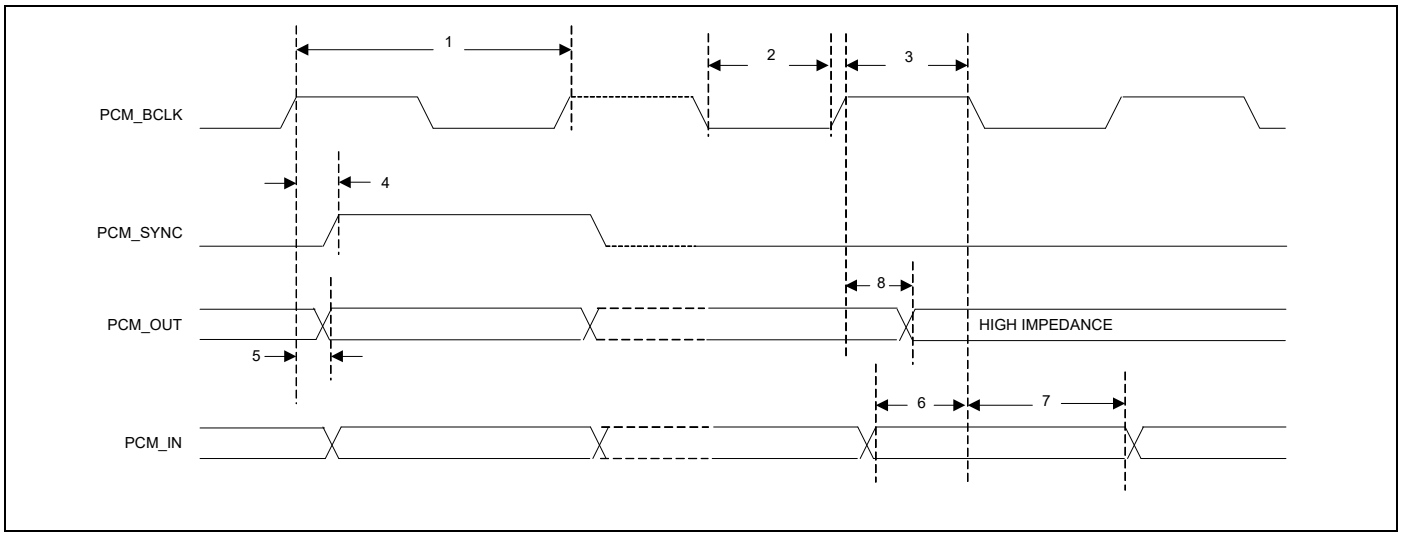


Table 7. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

Figure 12. PCM Timing Diagram (Short Frame Sync, Slave Mode)

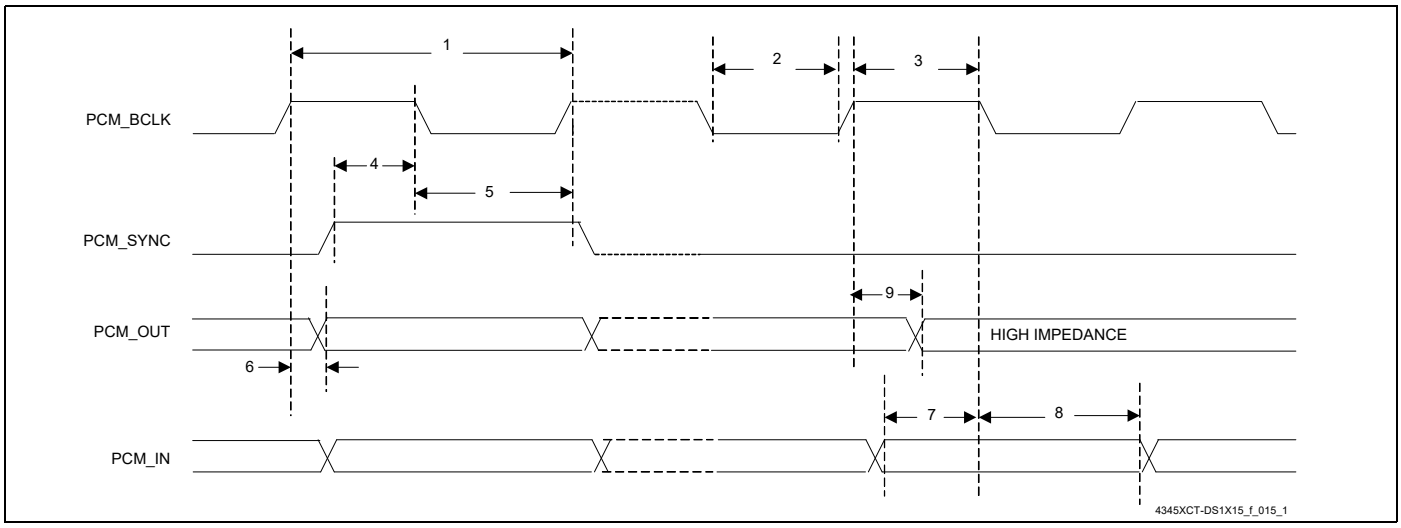


Table 8. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

Figure 13. PCM Timing Diagram (Long Frame Sync, Master Mode)

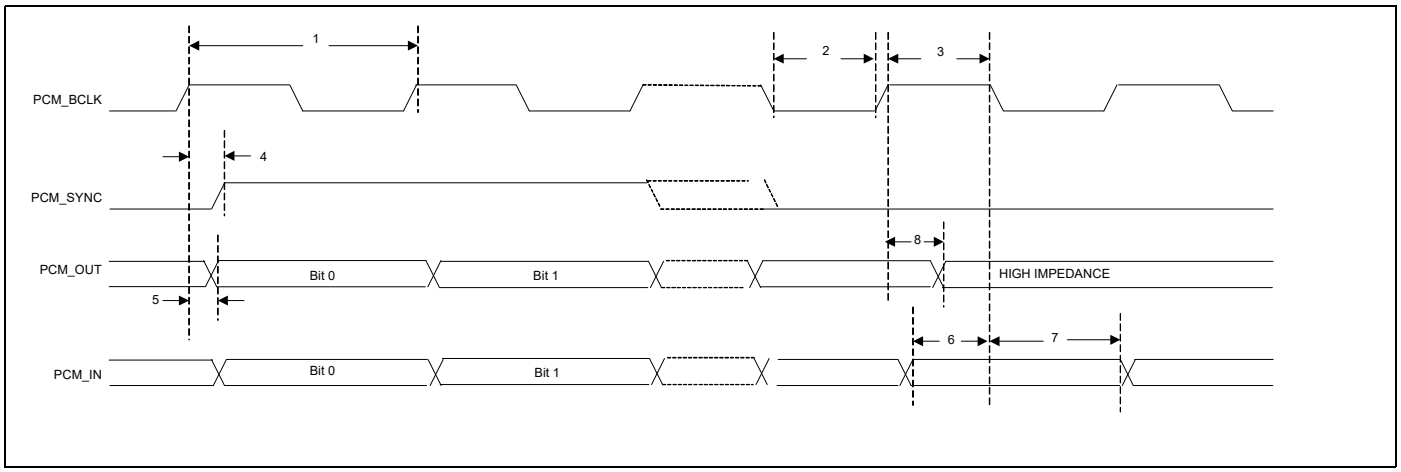


Table 9. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

Figure 14. PCM Timing Diagram (Long Frame Sync, Slave Mode)

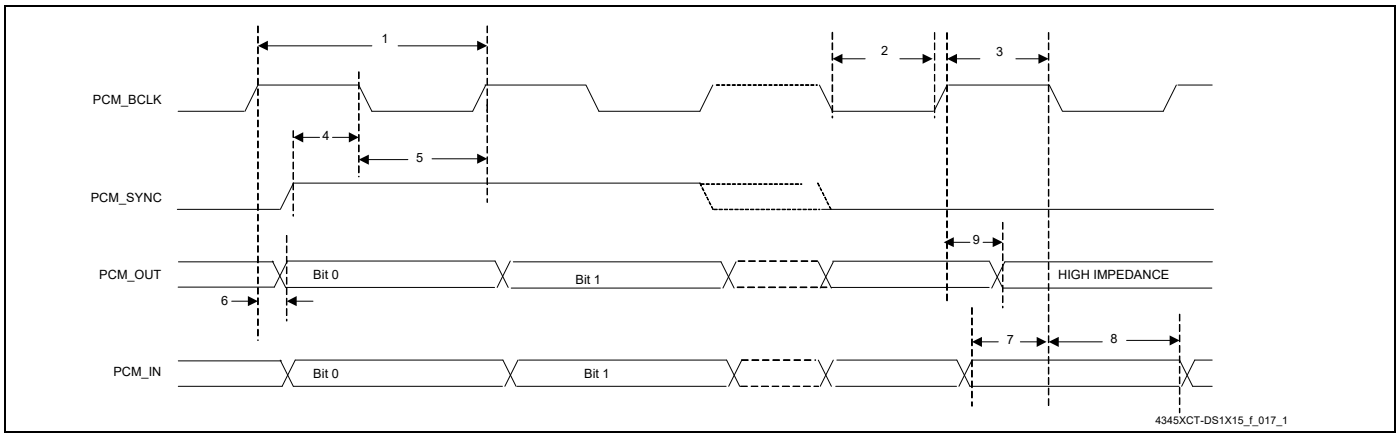


Table 10. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

Figure 15. PCM Burst Mode Timing (Receive Only, Short Frame Sync)

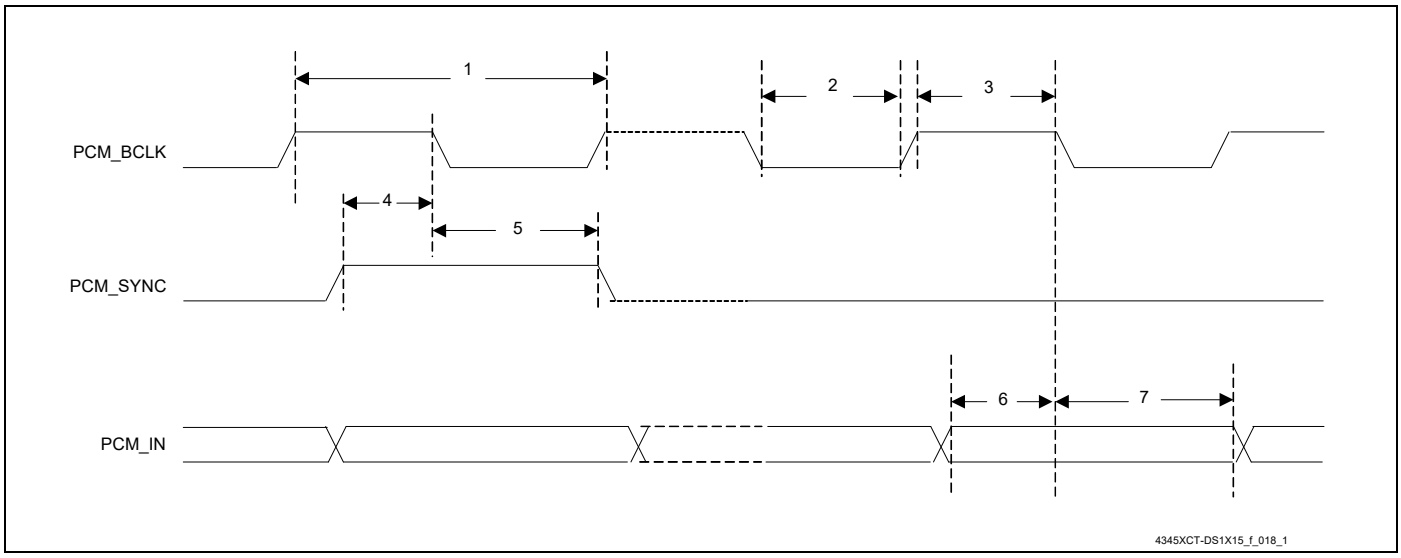


Table 11. PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

Figure 16. PCM Burst Mode Timing (Receive Only, Long Frame Sync)

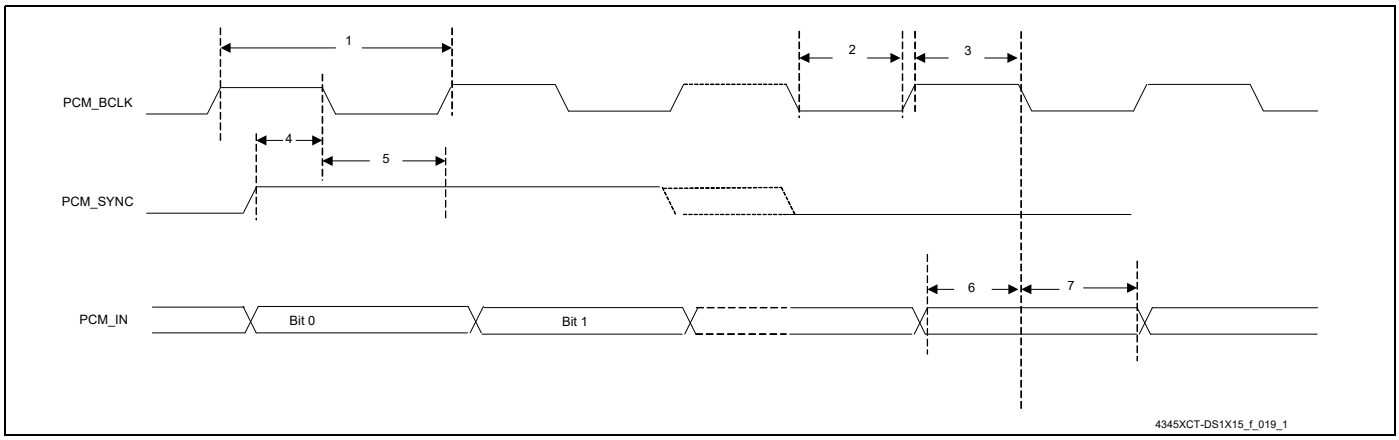


Table 12. PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

7.4 UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (*Three-wire UART Transport Layer*). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The CYW43455 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW43455 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 13. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Figure 17. UART Timing

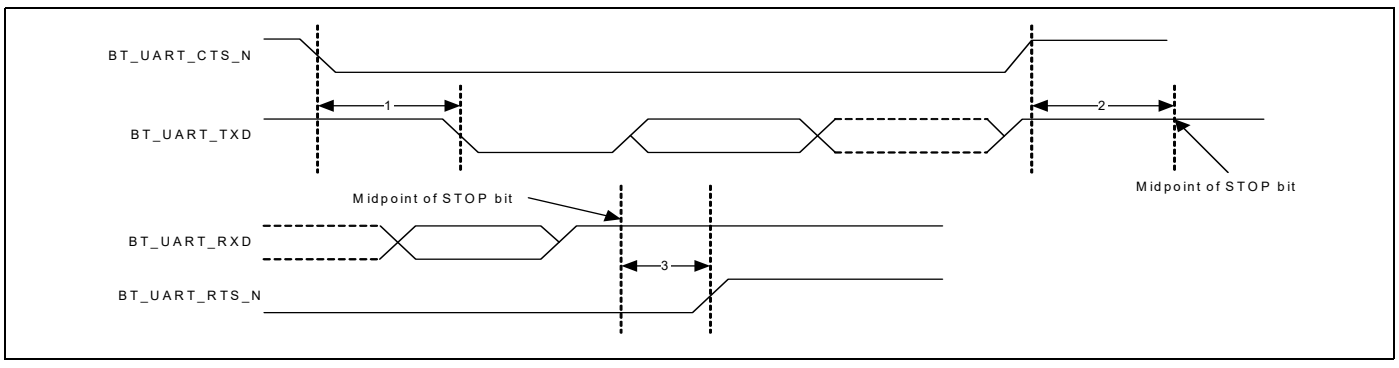


Table 14. UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

7.5 I²S Interface

The CYW43455 supports an I²S digital audio port for Bluetooth audio. The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW43455 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider. In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

7.5.1 I^2S Timing

Note: Timing values specified in Table 15 are relative to high and low threshold levels.

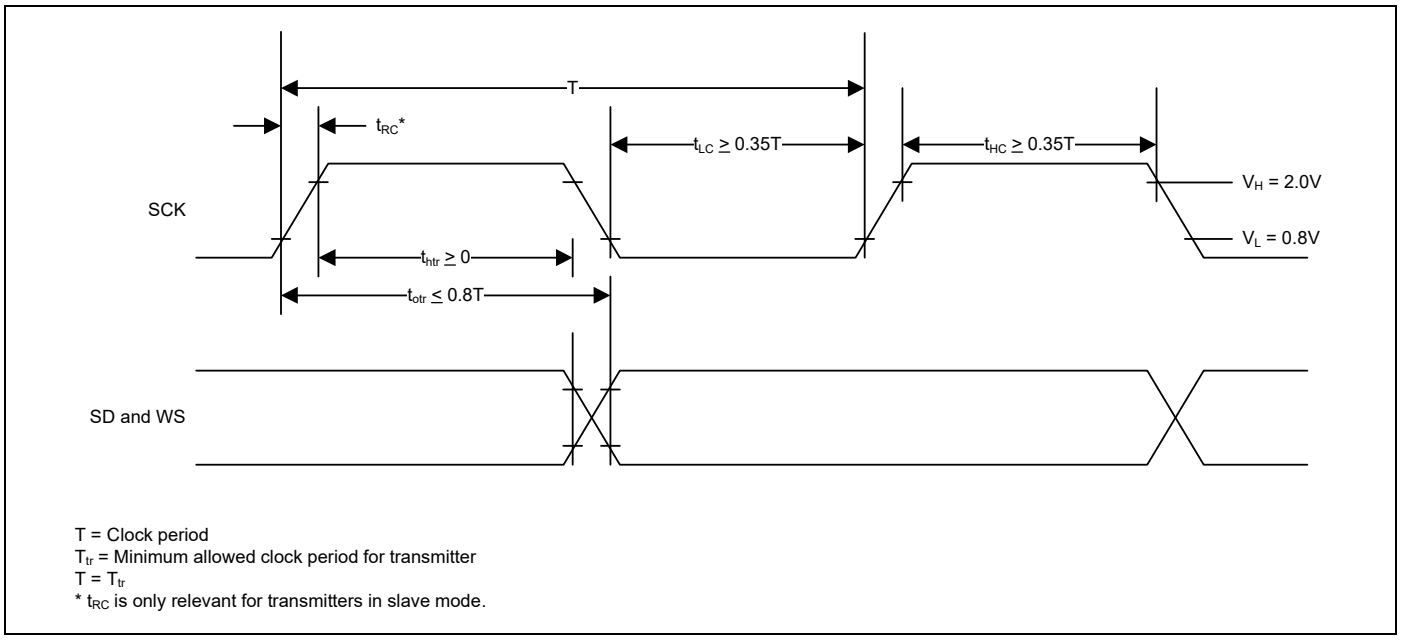
Table 15. Timing for I^2S Transmitters and Receivers

	Transmitter				Receiver				Notes
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	1
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	2
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	3
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–	–	–	4
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	5
Hold time t_{htr}	0	–	–	–	–	–	–	–	4
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	6
Hold time t_{hr}	–	–	–	–	–	0	–	–	6

1. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
2. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
3. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
4. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
5. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
6. The data setup and hold time must not be less than the specified receiver setup and hold time.

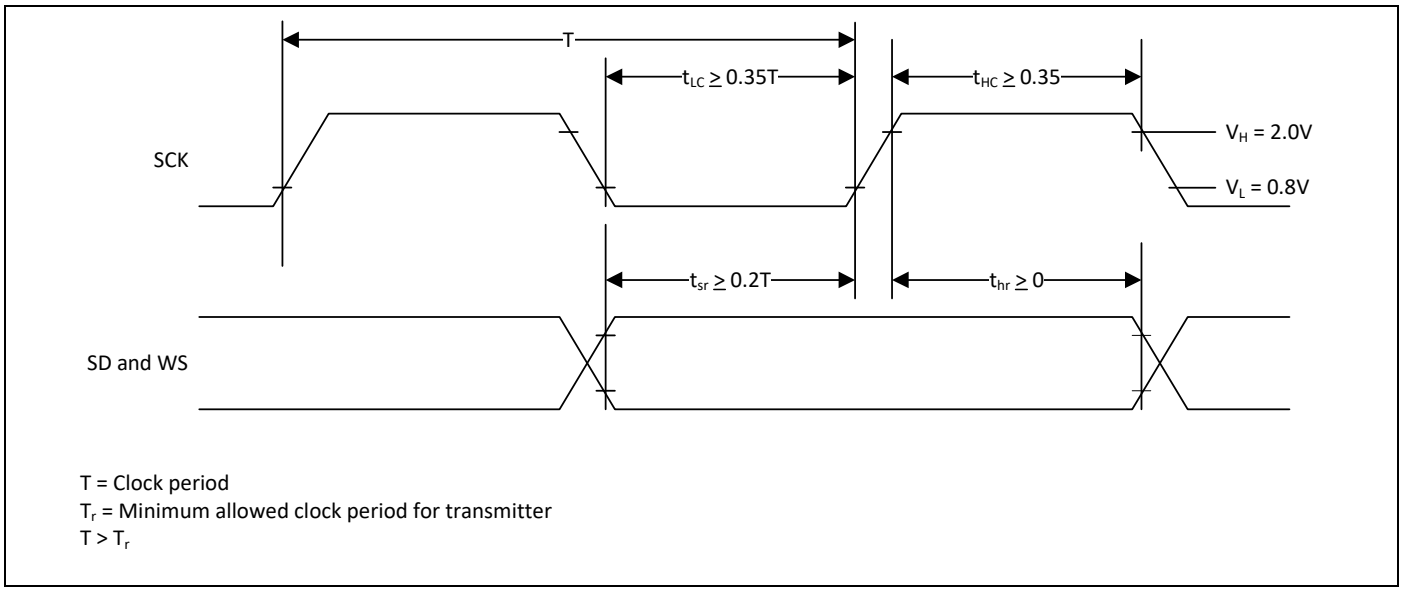
Note: The time periods specified in Figure 18 and Figure 19 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 18. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 19. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

8. WLAN Global Functions

8.1 WLAN CPU and Memory Subsystem

The CYW43455 WLAN section includes an integrated ARM Cortex-R4 32-bit processor with internal RAM and ROM. The ARM Cortex-R4 is a low-power processor that features low gate count, low interrupt latency, and low-cost debug capabilities. It is intended for deeply embedded applications that require fast interrupt response features. Delivering more than 30% performance gain over ARM7TDMI, the ARM Cortex-R4 implements the ARM v7-R architecture with support for the Thumb-2 instruction set.

At 0.19 µW/MHz, the Cortex-R4 is the most power efficient general-purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

Using multiple technologies to reduce cost, the ARM Cortex-R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (ICode/DCode and System buses), and extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 800 KB SRAM and 704 KB ROM.

8.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 6144-bit (768 bytes) One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

8.3 GPIO Interface

The following number of general-purpose I/O (GPIO) pins are available on the WLAN section of the CYW43455 that can be used to connect to various external devices:

- WLBGA package – 15 GPIOs

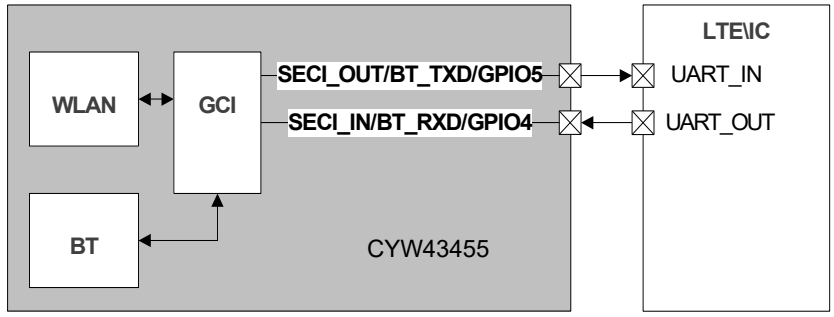
Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions.

8.4 External Coexistence Interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as GPS or LTE to manage wireless medium sharing for optimum performance.

Figure 20 shows the WCI-2 LTE coexistence interface. See Table 14 for UART baud rate.

Figure 20. Cypress GCI or BT-SIG WCI-2 LTE Coexistence Interface



NOTES:

1. SECI_OUT/BT_TXD and SECI_IN/BT_RXD on the CYW4345X are multiplexed on GPIO5 and GPIO4, respectively.
2. The 2-wire LTE coexistence interface is intended for future compatibility with the BT SIG 2-wire interface that is being standardized for Core 5.0.
3. ORing to generate ISM_RX_PRIORITY for ERCX_TXCONF or BT_RX_PRIORITY is achieved by setting the GPIO mask registers appropriately.

Figure 21 and Table 16 define an alternate 3-wire LTE coexistence interface.

Figure 21. 3-Wire LTE Coexistence Interface

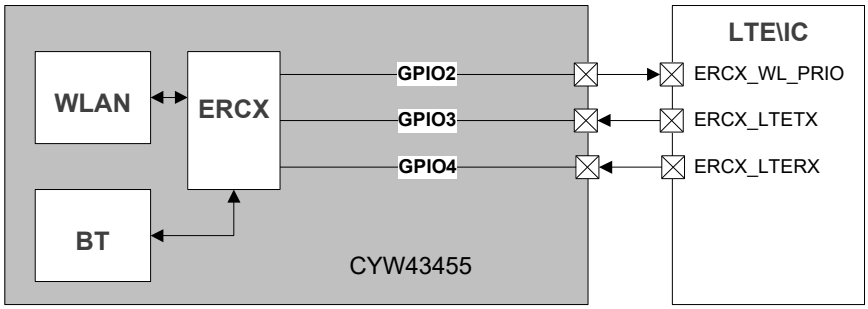


Table 16. 3-Wire External Coexistence Interface

GPIO Name	Coexistence Signal	Type	Comment
GPIO_2	ERCX_WL_PRIO	Output	Notify LTE of request to sleep
GPIO_3	ERCX_LTE_TX	Input	Notify WLAN RX of requirement to sleep
GPIO_4	ERCX_LTE_RX	Input	Notify WLAN TX to reduce TX power

8.5 UART Interface

A high-speed 4-wire CTS/RTS UART interface can be enabled by software as an alternate function on GPIO pins. Provided primarily for debugging during development, this UART enables the CYW43455 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

8.6 JTAG/SWD Interface

The CYW43455 supports IEEE 1149.1 JTAG boundary scan and reduced pin-count Serial Wire Debug (SWD) mode to access the chip's internal blocks and backplane for system bring-up and debugging. This interface allows Cypress engineers to assist customers with proprietary debug and characterization test tools. It is highly recommended that customers provide access to at least the SWD pins on all PCB designs by using either test points or a header.

The SWD interface uses two of the JTAG signals: TMS for bidirectional data (SWDIO) and TCK for the clock (SWCLK). The debug access port (DAP) embedded in the ARM processor supports both SWD and JTAG interfaces and can be switched from one to the other through a specific sequence on the TMS/SWD lines. In addition to the ARM debug interface, an internal JTAG master on the DAP allows access to test access points (TAPs) in the CYW43455 for hardware debugging.

9. WLAN Host Interfaces

9.1 SDIO v3.0

All three package options of the CYW43455 WLAN section provide support for SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3 V signaling).
- HS: High speed up to 50 MHz (3.3 V signaling).
- SDR12: SDR up to 25 MHz (1.8 V signaling).
- SDR25: SDR up to 50 MHz (1.8 V signaling).
- SDR50: SDR up to 100 MHz (1.8 V signaling).
- SDR104: SDR up to 208 MHz (1.8 V signaling)
- DDR50: DDR up to 50 MHz (1.8 V signaling).

Note: The CYW43455 is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled by strapping options. See Table 21 for strapping options.

The following three functions are supported:

- Function 0 Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B).

9.2 SDIO Pins

Table 17. SDIO Pin Description

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

Figure 22. Signal Connections to SDIO Host (SD 4-Bit Mode)

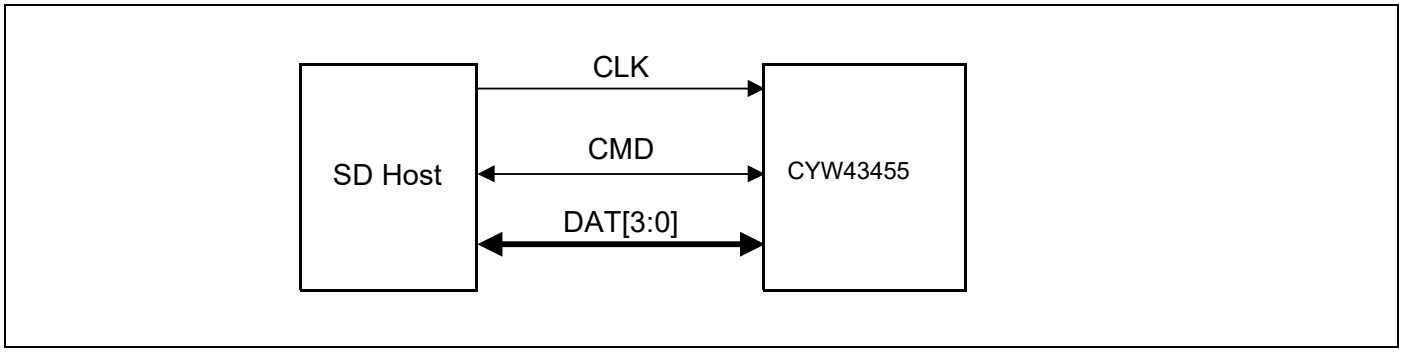
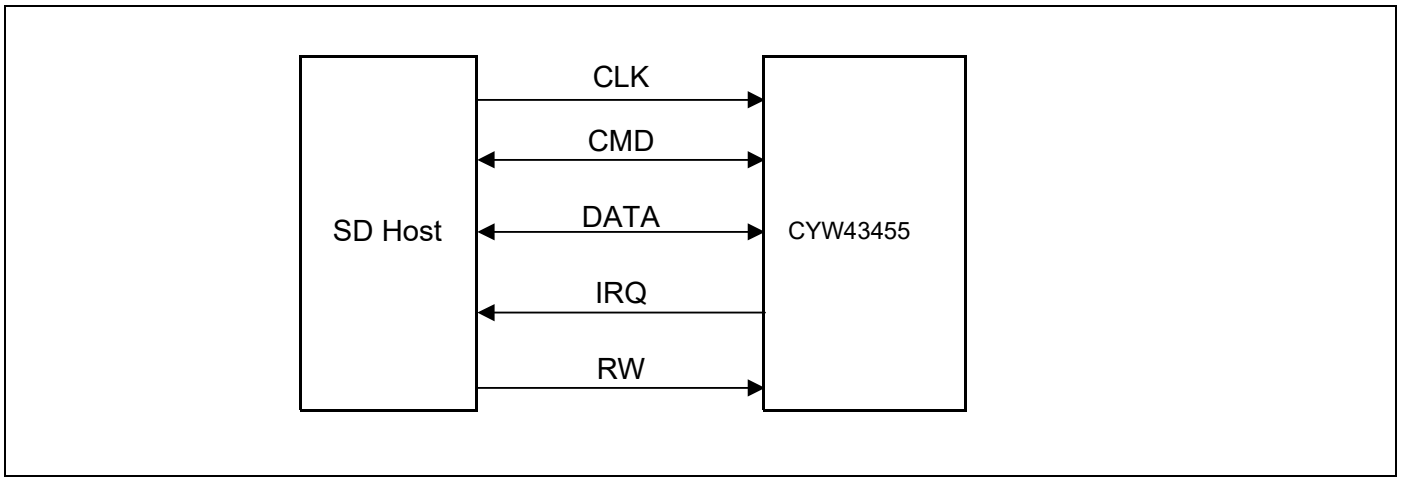


Figure 23. Signal Connections to SDIO Host (SD 1-Bit Mode)



Note: Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

9.3 PCI Express Interface

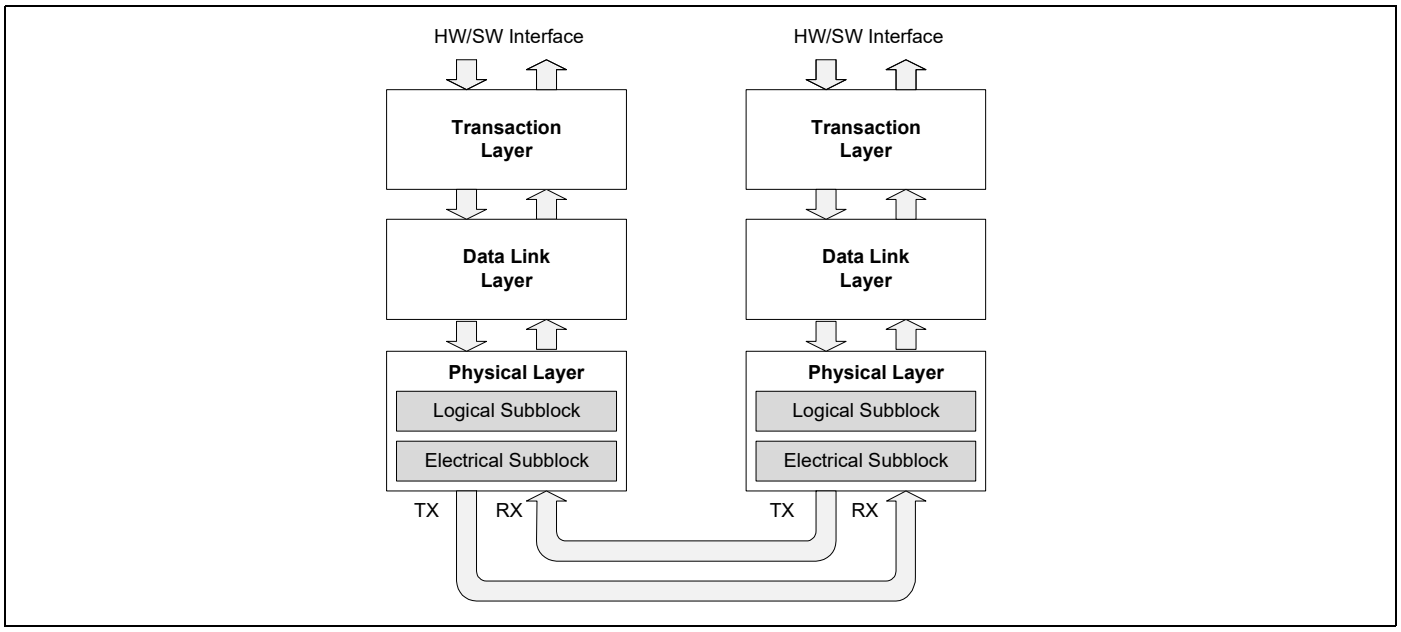
Note: The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

The PCI Express (PCIe) core on the CYW43455 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the **PCI Express Base Specification v2.0**. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 24. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and CYW43455 device. The transmit side processes outbound packets while the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

Figure 24. PCI Express Layer Model



9.4 Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and CYW43455 device, delivering new levels of performance and features. The upper layer of the PCIe is the Transaction Layer. The Transaction layer is primarily responsible for assembly and disassembly of Transaction Layer Packets (TLPs). TLP structure contains header, data payload, and End-to-End CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

9.4.1 Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

Data Link Layer Packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgment, power management, and flow control.

9.4.2 Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and CYW43455 device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

9.4.3 Logical Subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

9.4.4 Scrambler/Descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

9.4.5 8B/10B Encoder/Decoder

The PCIe core on the CYW43455 uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the twelve Special Symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. Special Symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

9.4.6 Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

9.4.7 Electrical Subblock

The high-speed signals utilize the Common Mode Logic (CML) signaling interface with on-chip termination and de-emphasis for best-in-class signal integrity. A de-emphasis technique is employed to reduce the effects of Intersymbol Interference (ISI) due to the

interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable Bit-Error Rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are de-emphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the de-emphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

9.4.8 Configuration Space

The PCIe function in the CYW43455 implements the configuration space as defined in the *PCI Express Base Specification v2.0*.

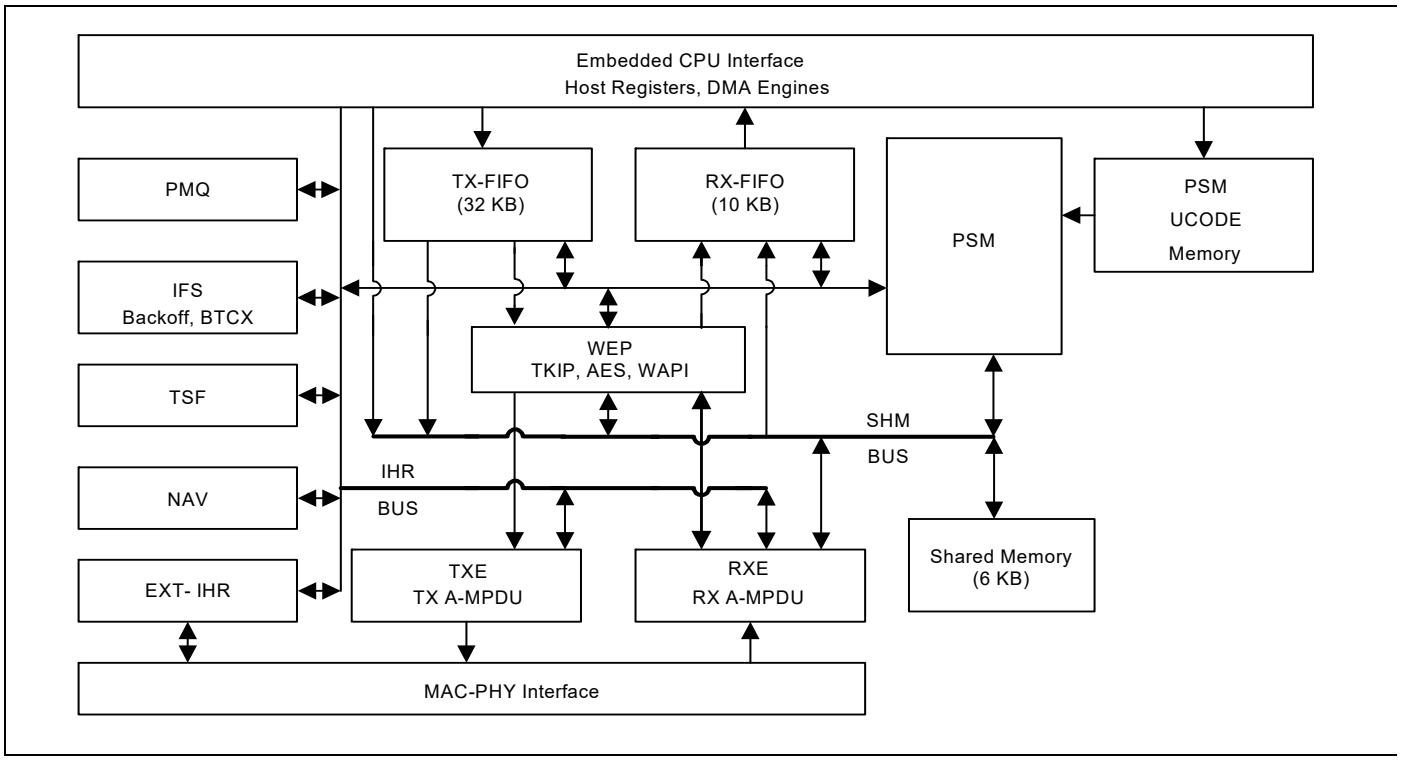
10. Wireless LAN MAC and PHY

10.1 IEEE 802.11ac MAC

The CYW43455 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 25.

The following sections provide an overview of the important modules in the MAC.

Figure 25. WLAN MAC Architecture



The CYW43455 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:

- Enhanced MAC for supporting IEEE 802.11ac features
- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

10.1.1 PSM

The programmable state machine (PSM) is a microcoded engine, which provides most of the low-level control to the hardware, to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines, by programming internal hardware registers (IHR). These IHRs are co-located with the hardware functions they control, and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

10.1.2 WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, and MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

The PSM determines, based on the frame type and association information, the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames.

10.1.3 TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

10.1.4 RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

10.1.5 IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple backoff engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The backoff engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the backoff counters. When the backoff counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple backoff counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power save mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

10.1.6 TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

10.1.7 NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

10.1.8 MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is an programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

10.2 IEEE 802.11ac PHY

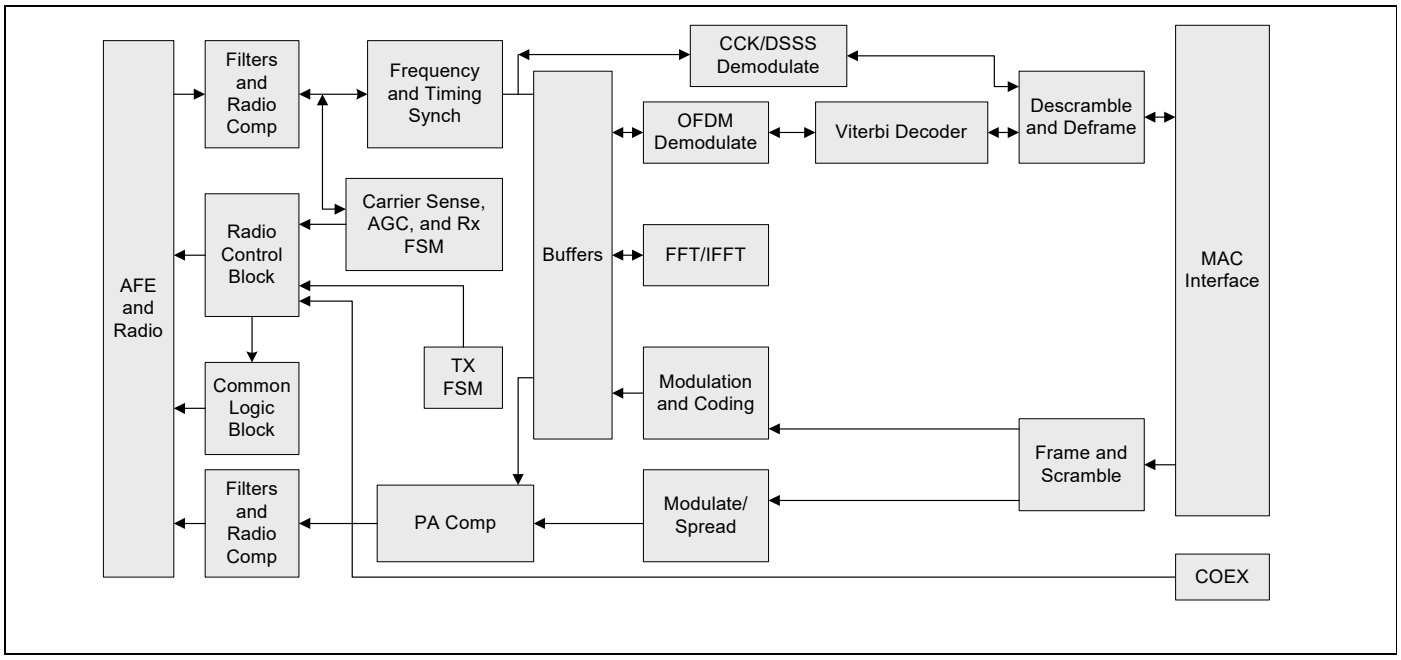
The CYW43455 WLAN Digital PHY is designed to comply with IEEE 802.11ac and IEEE 802.11a/b/g/n single-stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 433.3 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence. It has also been designed for shared single antenna systems between WL and BT to support simultaneous RX-RX.

The key PHY features include:

- Programmable data rates from MCS0–MCS9 in 20, 40, and 80 MHz channels, as specified in IEEE 802.11ac.
- Supports Optional Short GI and Green Field modes in TX and RX.
- TX and RX LDPC for improved range and power efficiency.
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.
- Supports IEEE 802.11h/k for worldwide operation.
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability.
- Algorithms to improve performance in presence of Bluetooth.
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications.
- Closed loop transmit power control.
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities.
- On-the-fly channel frequency and transmit power selection.
- Supports per-packet RX antenna diversity.
- Available per-packet channel quality and signal strength measurements.
- Designed to meet FCC and other worldwide regulatory requirements.

Figure 26. WLAN PHY Block Diagram



11. WLAN Radio Subsystem

The CYW43455 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Ten RF control signals are available to drive external RF switches and support optional external power amplifiers and low-noise amplifiers for each band. See the reference board schematics for further details.

A block diagram of the radio subsystem is shown in Figure 27. Note that integrated on-chip baluns (not shown) convert the fully differential transmit and receive paths to single-ended signal pins.

11.1 Receiver Path

The CYW43455 has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. An on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth and WLAN receivers, while the 5 GHz receive path has a dedicated on-chip LNA. Control signals are available that can support the use of optional LNAs for each band, which can increase the receive sensitivity by several dB.

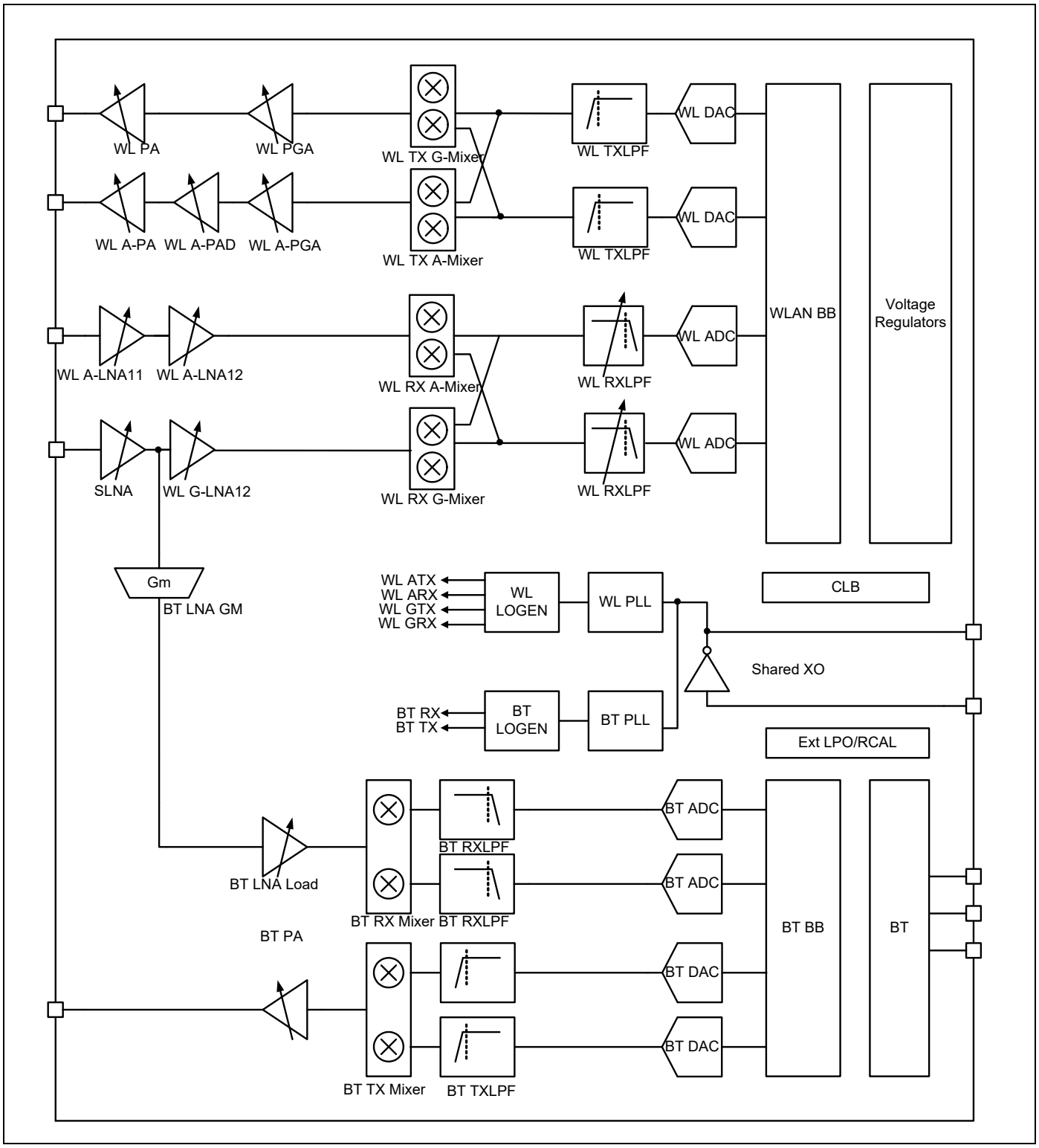
11.2 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5-GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11ac and IEEE 802.11a/b/g/n specifications without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated. As an option, external PAs can be used for even higher output power, in which case the closed-loop output power control is provided by means of a-band and g-band TSSI inputs from external power detectors.

11.3 Calibration

The CYW43455 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

Figure 27. Radio Functional Block Diagram



12. Ball Map and Pin Descriptions

12.1 Ball Map

Figure 28. 140-Ball WLBGA Map—Bottom View (Balls Facing Up)

	11	10	9	8	7	6	5	4	3	2	1	
A		PCIE_TDN	PCIE_RDN	PCIE_RDP	SDIO_CLK	SDIO_DATA_3	LDO_VDDBAT5V	VOUT_3P3	LDO_VDD1P5	SR_VDDBAT5V	SR_PVSS	A
B	PCIE_REFCLKP	PCIE_TDP	PCIE_RXTX_AVDD1P2	PCIE_CLKREQ_L	SDIO_DATA_1	SDIO_DATA_2	VOUT_BTLDO2P5	VOUT_LNLDO	VOUT_CLDO	VOUT_PCIELDO	SR_VLX	B
C	PCIE_REFCLKN	PCIE_PLL_AVDD1P2	PCIE_VSS	VDDC	SDIO_DATA_0	SDIO_CMD	VSSC	WL_REG_ON	BT_REG_ON	PMU_AVSS	GPIO_0	C
D	GPIO_13	GPIO_14	NC1	PERST_L	PCI_PME_L	VDDIO_SD	VDDIO	GPIO_2	GPIO_1	GPIO_3	GPIO_6	D
E	NC2	AVSS_BBPLL	AVDD_BBPLL	NC3	VDDIO_RF	RF_SWCTRL_8	JTAG_SEL	GPIO_4	GPIO_5	VDDC	GPIO_7	E
F	RF_SW_CTRL_0	RF_SW_CTRL_1	VSSC	VDDC	RF_SWCTRL_4	RF_SWCTRL_7	VSSC	GPIO_9	GPIO_10	BT_VDDC	LPO_IN	F
G	WRF_XTAL_XON	WRF_XTAL_GND1P2	RF_SW_CTRL_2	RF_SW_CTRL_3	RF_SWCTRL_5	RF_SWCTRL_6	GPIO_8	BT_VDDO	BT_PCM_SYNC	VSSC	BT_PCM_IN	G
H	WRF_XTAL_XOP	WRF_XTAL_VDD1P35	WRF_XTAL_VDD1P2	WRF_SYNTH_VDD3P3		BT_GPIO_3	BT_GPIO_4	NC	BT_PCM_OUT	BT_I2S_DO	BT_PCM_CLK	H
J	WRF_PMU_VDD1P35	WRF_SYNTH_VDD1P2	WRF_SYNTH_GND	WRF_VCO_GND	BT_GPIO_2	BT_UART_CTS_N	VDDC	BT_VDDC	BT_I2S_WS	BT_I2S_DI	BT_I2S_CLK	J
K	WRF_RX5G_GND	WRF_AFE_VDD1P35	WRF_GENERAL_GND	WRF_EXT_TSSIA	GPIO_15	GPIO_16	VSSC	BT_GPIO_5	BT_UART_RTS_N	BT_UART_TXD	BT_UART_RXD	K
L	WRF_RFIN_5G	WRF_GENERAL2_GND	WRF_AFE_GND	WRF_GPAIO_OUT	BT_LNAVDD1P2	BT_IFVSS	BT_PLLVSS	BT_CLK_REQ	BT_HOST_WAKE	VSSC	BT_VDDC	L
M	WRF_PAOUT_5G	WRF_PA_GND3P3	WRF_TXMIX_VDD	WRF_RX2G_GND	BT_LNAVSS	BT_PAVSS	BT_PLLVDD1P2	FM_PLLVSS	FM_RFVSS	FM_PLLVDD1P2	BT_DEV_WAKE	M
N	WRF_PA_VDD3P3		WRF_PAOUT_2G	WRF_RFIN_2G	BT_RF	BT_PAVDD2P5	BT_IFVDD1P2	FM_RFIN	FM_RFVDD1P2	FM_AOUT2	FM_AOUT1	N
	11	10	9	8	7	6	5	4	3	2	1	

12.2 Pin List by Pin Number

Table 18 lists CYW43455 pins by pin number. For a list of CYW43455 pins by pin name, see Table 19

Table 18. Pin List by Pin Number

Ball	Name
A1	SR_PVSS
A2	SR_VDDBAT5V
A3	LDO_VDD1P5
A4	VOUT_3P3
A5	LDO_VDDBAT5V
A6	SDIO_DATA_3
A7	SDIO_CLK
A8	PCIE_RDP
A9	PCIE_RDN
A10	PCIE_TDN
A11	–
B1	SR_VLX
B2	VOUT_PCIELDO
B3	VOUT_CLDO
B4	VOUT_LNLDO
B5	VOUT_BTLDO2P5
B6	SDIO_DATA_2
B7	SDIO_DATA_1
B8	PCIE_CLKREQ_L
B9	PCIE_RXTX_AVDD1P2
B10	PCIE_TDP
B11	PCIE_REFCLKP
C1	GPIO_0
C2	PMU_AVSS
C3	BT_REG_ON
C4	WL_REG_ON
C5	VSSC
C6	SDIO_CMD
C7	SDIO_DATA_0
C8	VDDC
C9	PCIE_VSS
C10	PCIE_PLL_AVDD1P2
C11	PCIE_REFCLKN
D1	GPIO_6
D2	GPIO_3
D3	GPIO_1
D4	GPIO_2

Table 18. Pin List by Pin Number (continued)

Ball	Name
D5	VDDIO
D6	VDDIO_SD
D7	PCI_PME_L
D8	PERST_L
D9	NC1
D10	GPIO_14
D11	GPIO_13
E1	GPIO_7
E2	VDDC
E3	GPIO_5
E4	GPIO_4
E5	JTAG_SEL
E6	RF_SW_CTRL_8
E7	VDDIO_RF
E8	NC3
E9	AVDD_BBPLL
E10	AVSS_BBPLL
E11	NC2
F1	LPO_IN
F2	BT_VDDC
F3	GPIO_10
F4	GPIO_9
F5	VSSC
F6	RF_SW_CTRL_7
F7	RF_SW_CTRL_4
F8	VDDC
F9	VSSC
F10	RF_SW_CTRL_1
F11	RF_SW_CTRL_0
G1	BT_PCM_IN
G2	VSSC
G3	BT_PCM_SYNC
G4	BT_VDDO
G5	GPIO_8
G6	RF_SW_CTRL_6
G7	RF_SW_CTRL_5
G8	RF_SW_CTRL_3

Table 18. Pin List by Pin Number (continued)

Ball	Name
G9	RF_SW_CTRL_2
G10	WRF_XTAL_GND1P2
G11	WRF_XTAL_XON
H1	BT_PCM_CLK
H2	BT_I2S_DO
H3	BT_PCM_OUT
H4	NC
H5	BT_GPIO_4
H6	BT_GPIO_3
H7	–
H8	WRF_SYNTH_VDD3P3
H9	WRF_XTAL_VDD1P2
H10	WRF_XTAL_VDD1P35
H11	WRF_XTAL_XOP
J1	BT_I2S_CLK
J2	BT_I2S_DI
J3	BT_I2S_WS
J4	BT_VDDC
J5	VDDC
J6	BT_UART_CTS_N
J7	BT_GPIO_2
J8	WRF_VCO_GND
J9	WRF_SYNTH_GND
J10	WRF_SYNTH_VDD1P2
J11	WRF_PMU_VDD1P35
K1	BT_UART_RXD
K2	BT_UART_TXD
K3	BT_UART_RTS_N
K4	BT_GPIO_5
K5	VSSC
K6	GPIO_16
K7	GPIO_15
K8	WRF_EXT_TSSIA
K9	WRF_GENERAL_GND
K10	WRF_AFE_VDD1P35
K11	WRF_RX5G_GND
L1	BT_VDDC
L2	VSSC
L3	BT_HOST_WAKE

Table 18. Pin List by Pin Number (continued)

Ball	Name
L4	BT_CLK_REQ
L5	BT_PLLVSS
L6	BT_IFVSS
L7	BT_LNAVDD1P2
L8	WRF_GPAIO_OUT
L9	WRF_AFE_GND
L10	WRF_GENERAL2_GND
L11	WRF_RFIN_5G
M1	BT_DEV_WAKE
M2	FM_PLLVDD1P2
M3	FM_RFVSS
M4	FM_PLLVSS
M5	BT_PLLVDD1P2
M6	BT_PAVSS
M7	BT_LNAVSS
M8	WRF_RX2G_GND
M9	WRF_TXMIX_VDD
M10	WRF_PA_GND3P3
M11	WRF_PAOUT_5G
N1	FM_AOUT1
N2	FM_AOUT2
N3	FM_RFVDD1P2
N4	FM_RFIN
N5	BT_IFVDD1P2
N6	BT_PAVDD2P5
N7	BT_RF
N8	WRF_RFIN_2G
N9	WRF_PAOUT_2G
N10	–
N11	WRF_PA_VDD3P3

12.3 Pin List by Pin Name

Table 19 lists CYW43455 pins by pin name. For a list of CYW43455 pins by pin number, see Table 18.

Table 19. Pin List by Pin Name

Name	Ball
AVDD_BBPLL	E9
AVSS_BBPLL	E10
BT_CLK_REQ	L4
BT_DEV_WAKE	M1
BT_GPIO_2	J7
BT_GPIO_3	H6
BT_GPIO_4	H5
BT_GPIO_5	K4
BT_HOST_WAKE	L3
BT_I2S_CLK	J1
BT_I2S_DI	J2
BT_I2S_DO	H2
BT_I2S_WS	J3
BT_IFVDD1P2	N5
BT_IFVSS	L6
BT_LNAVDD1P2	L7
BT_LNAVSS	M7
BT_PAVDD2P5	N6
BT_PAVSS	M6
BT_PCM_CLK	H1
BT_PCM_IN	G1
BT_PCM_OUT	H3
BT_PCM_SYNC	G3
BT_PLLVDD1P2	M5
BT_PLLVSS	L5
BT_REG_ON	C3
BT_RF	N7
BT_UART_CTS_N	J6
BT_UART_RTS_N	K3
BT_UART_RXD	K1
BT_UART_TXD	K2
BT_VDDC	F2
BT_VDDC	J4
BT_VDDC	L1
BT_VDDO	G4
FM_AOUT1	N1
FM_AOUT2	N2

Table 19. Pin List by Pin Name (continued)

Name	Ball
FM_PLLVDD1P2	M2
FM_PLLVSS	M4
FM_RFIN	N4
FM_RFVDD1P2	N3
FM_RFVSS	M3
GPIO_0	C1
GPIO_1	D3
GPIO_2	D4
GPIO_3	D2
GPIO_4	E4
GPIO_5	E3
GPIO_6	D1
GPIO_7	E1
GPIO_8	G5
GPIO_9	F4
GPIO_10	F3
GPIO_13	D11
GPIO_14	D10
GPIO_15	K7
GPIO_16	K6
JTAG_SEL	E5
LDO_VDD1P5	A3
LDO_VDDBAT5V	A5
LPO_IN	F1
NC	H4
NC1	D9
NC2	E11
NC3	E8
PCIE_CLKREQ_L	B8
PCIE_PLL_AVDD1P2	C10
PCIE_RDN	A9
PCIE_RDP	A8
PCIE_REFCLKN	C11
PCIE_REFCLKP	B11
PCIE_RXTX_AVDD1P2	B9
PCIE_TDN	A10
PCIE_TDP	B10

Table 19. Pin List by Pin Name (continued)

Name	Ball
PCIE_VSS	C9
PCI_PME_L	D7
PERST_L	D8
PMU_AVSS	C2
RF_SW_CTRL_0	F11
RF_SW_CTRL_1	F10
RF_SW_CTRL_2	G9
RF_SW_CTRL_3	G8
RF_SW_CTRL_4	F7
RF_SW_CTRL_5	G7
RF_SW_CTRL_6	G6
RF_SW_CTRL_7	F6
RF_SW_CTRL_8	E6
SDIO_CLK	A7
SDIO_CMD	C6
SDIO_DATA_0	C7
SDIO_DATA_1	B7
SDIO_DATA_2	B6
SDIO_DATA_3	A6
SR_PVSS	A1
SR_VDDBAT5V	A2
SR_VLX	B1
VDDC	C8
VDDC	E2
VDDC	F8
VDDC	J5
VDDIO	D5
VDDIO_RF	E7
VDDIO_SD	D6
VOUT_3P3	A4
VOUT_BTLDO2P5	B5
VOUT_CLDO	B3
VOUT_LNLDO	B4
VOUT_PCIELDO	B2
VSSC	C5
VSSC	F5
VSSC	F9
VSSC	G2
VSSC	K5

Table 19. Pin List by Pin Name (continued)

Name	Ball
VSSC	L2
WL_REG_ON	C4
WRF_AFE_GND	L9
WRF_AFE_VDD1P35	K10
WRF_EXT_TSSIA	K8
WRF_GENERAL2_GND	L10
WRF_GENERAL_GND	K9
WRF_GPAIO_OUT	L8
WRF_PAOUT_2G	N9
WRF_PAOUT_5G	M11
WRF_PA_GND3P3	M10
WRF_PA_VDD3P3	N11
WRF_PMU_VDD1P35	J11
WRF_RFIN_2G	N8
WRF_RFIN_5G	L11
WRF_RX2G_GND	M8
WRF_RX5G_GND	K11
WRF_SYNTH_GND	J9
WRF_SYNTH_VDD1P2	J10
WRF_SYNTH_VDD3P3	H8
WRF_TXMIX_VDD	M9
WRF_VCO_GND	J8
WRF_XTAL_GND1P2	G10
WRF_XTAL_VDD1P2	H9
WRF_XTAL_VDD1P35	H10
WRF_XTAL_XON	G11
WRF_XTAL_XOP	H11
–	A11
–	H7
–	N10

12.4 Pin Descriptions

The signal name, type, and description of each pin in the CYW43455 is listed in Table 20. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 20. Signal Descriptions

Signal Name	WLBGA Ball		Type	Description
WLAN and Bluetooth Receive RF Signal Interface				
WRF_RFIN_2G	N8		I	2.4 GHz Bluetooth and WLAN receiver shared input.
WRF_RFIN_5G	L11		I	5 GHz WLAN receiver input.
WRF_PAOUT_2G	N9		O	2.4 GHz WLAN PA output.
WRF_PAOUT_5G	M11		O	5 GHz WLAN PA output.
WRF_EXT_TSSIA	K8		I	5 GHz TSSI input from an optional external power amplifier/power detector.
WRF_GPAIO_OUT	L8		I/O	GPIO or 2.4 GHz TSSI input from an optional external power amplifier/power detector.
RF Switch Control Lines				
RF_SW_CTRL_0	F11		O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
RF_SW_CTRL_1	F10		O	
RF_SW_CTRL_2	G9		O	
RF_SW_CTRL_3	G8		O	
RF_SW_CTRL_4	F7		O	
RF_SW_CTRL_5	G7		O	
RF_SW_CTRL_6	G6		O	
RF_SW_CTRL_7	F6		O	
RF_SW_CTRL_8	E6		O	
WLAN PCI Express Interface **Note:** The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.				
PCIE_CLKREQ_L	B8		OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
PERST_L	D8		I (PU)	PCIe System Reset. This input is the PCIe reset as defined in the *PCIe Base Specification Version 1.1*.
PCIE_RDN	A9		I	Receiver differential pair (×1 lane).
PCIE_RDP	A8		I	
PCIE_REFCLKN	C11		I	PCIe differential clock inputs (negative and positive), 100 MHz differential.
PCIE_REFCLKP	B11		I	
PCIE_TDN	A10		O	Transmitter differential pair (×1 lane).
PCIE_TDP	B10		O	

Table 20. Signal Descriptions (continued)

Signal Name	WLBGA Ball		Type	Description
PCI_PME_L	D7		OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the *PCI Bus Local Bus Specification, Revision 2.3*.
WLAN SDIO Bus Interface **Note:** These signals can also have alternate functionality depending on package and host interface mode.				
SDIO_CLK	A7		I	SDIO clock input.
SDIO_CMD	C6		I/O	SDIO command line.
SDIO_DATA_0	C7		I/O	SDIO data line 0.
SDIO_DATA_1	B7		I/O	SDIO data line 1.
SDIO_DATA_2	B6		I/O	SDIO data line 2.
SDIO_DATA_3	A6		I/O	SDIO data line 3.
WLAN GPIO Interface **Note:** The GPIO signals can be multiplexed via software and the JTAG_SEL pin to behave as various specific functions.				
GPIO_0	C1		I/O	Programmable GPIO pins: GPIO_2 is TCK/SWCLK if JTAG_SEL = 1 GPIO_3 is TMS/SWDIO if JTAG_SEL = 1 GPIO_4 is TDIO if JTAG_SEL = 1 GPIO_5 is TDO if JTAG_SEL = 1 GPIO_6 is TRST_L if JTAG_SEL = 1
GPIO_1	D3		I/O	
GPIO_2	D4		I/O	
GPIO_3	D2		I/O	
GPIO_4	E4		I/O	
GPIO_5	E3		I/O	
GPIO_6	D1		I/O	
GPIO_7	E1		I/O	
GPIO_8	G5		I/O	
GPIO_9	F4		I/O	
GPIO_10	F3		I/O	
GPIO_13	D11		I/O	
GPIO_14	D10		I/O	
GPIO_15	K7		I/O	
GPIO_16	K6		I/O	

Table 20. Signal Descriptions (continued)

Signal Name	WLBGA Ball		Type	Description
JTAG/SWD Interface				
JTAG_SEL	E5		I/O	JTAG select. This pin must be connected to ground if the JTAG/SWD interface is not used. It must be high to select SWD OR JTAG. When JTAG_SEL = 1: GPIO_2 is TCK/SWCLK GPIO_3 is TMS/SWDIO GPIO_4 is TDIO GPIO_5 is TDO GPIO_6 is TRST_L
Clocks				
WRF_XTAL_XOP	H11		I	XTAL oscillator input.
WRF_XTAL_XON	G11		O	XTAL oscillator output.
LPO_IN	F1		I	External sleep clock input (32.768 kHz).
BT_CLK_REQ	L4		O	Reference clock request (shared by BT and WLAN).
Bluetooth/FM Transceiver				
BT_RF	N7		O	Bluetooth PA output.
FM_RFIN	N4		I	FM radio antenna port.
FM_AOUT1	N1		O	FM DAC output 1.
FM_AOUT2	N2		O	FM DAC output 2.
Bluetooth PCM				
BT_PCM_CLK	H1		I/O	PCM or SLIMbus clock; can be master (output) or slave (input).
BT_PCM_IN	G1		I	PCM data input or SLIMbus transport sensing.
BT_PCM_OUT	H3		O	PCM data output.
BT_PCM_SYNC	G3		I/O	PCM sync; can be master (output) or slave (input), or SLIMbus data.
Bluetooth UART				
BT_UART_CTS_N	J6		I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
BT_UART_RTS_N	K3		O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
BT_UART_RXD	K1		I	UART serial input. Serial data input for the HCI UART interface. BT RF disable pin 2.
BT_UART_TXD	K2		O	UART serial output. Serial data output for the HCI UART interface.
Bluetooth/FM/I^2S				
BT_I2S_CLK	J1		I/O	I^2S clock, can be master (output) or slave (input).

Table 20. Signal Descriptions (continued)

Signal Name	WLBGA Ball		Type	Description
BT_I2S_DI	J2		I/O	I^2S data input.
BT_I2S_DO	H2		I/O	I^2S data output.
BT_I2S_WS	J3		I/O	I^2S WS; can be master (output) or slave (input).
Bluetooth GPIO				
BT_GPIO_2	J7		I/O	Bluetooth general-purpose I/O.
BT_GPIO_3	H6		I/O	Bluetooth general-purpose I/O.
BT_GPIO_4	H5		I/O	Bluetooth general-purpose I/O.
BT_GPIO_5	K4		I/O	Bluetooth general-purpose I/O.
Miscellaneous				
WL_REG_ON	C4		I	Used by PMU to power-up or power down the internal CYW43455 regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	C3		I	Used by PMU to power-up or power down the internal CYW43455 regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_DEV_WAKE	M1		I/O	Bluetooth DEV_WAKE.
BT_HOST_WAKE	L3		I/O	Bluetooth HOST_WAKE.
Integrated Voltage Regulators				
SR_VDDBAT5V	A2		I	VBAT.
SR_VLX	B1		O	CBUCK switching regulator output. Refer to Table 44 for details of the inductor and capacitor required on this output.
LDO_VDD1P5	A3		I	LNLDO input.
LDO_VDDBAT5V	A5		I	LDO VBAT.
WRF_XTAL_VDD1P35	H10		I	XTAL LDO input (1.35V).
WRF_XTAL_VDD1P2	H9		O	XTAL LDO output (1.2V).
VOUT_LNLDO	B4		O	Output of LNLDO.
VOUT_CLDO	B3		O	Output of core LDO.
VOUT_BTLDO2P5	B5		O	Output of BT LDO.
VOUT_3P3	A4		O	LDO 3.3 V output.
Bluetooth Supplies				
BT_PAVDD2P5	N6		PWR	Bluetooth PA power supply.
BT_LNAVDD1P2	L7		PWR	Bluetooth LNA power supply.
BT_IFVDD1P2	N5		PWR	Bluetooth IF block power supply.

Table 20. Signal Descriptions (continued)

Signal Name	WLBGA Ball		Type	Description
BT_PLLVDD1P2	M5		PWR	Bluetooth RF PLL power supply.
FM Transceiver Supplies				
FM_RFVDD1P2	N3		PWR	FM RF power supply.
FM_PLLVDD1P2	M2		PWR	FM PLL power supply.
WLAN Supplies				
WRF_SYNTH_VDD3P3	H8		PWR	Synthesizer VDD 3.3 V supply.
WRF_PA_VDD3P3	N11		PWR	2 GHz and 5 GHz PA 3.3 V VBAT supply.
WRF_PMU_VDD1P35	J11		PWR	PMU 1.35 V supply.
WRF_TXMIX_VDD	M9		PWR	3.3 V supply for the TX Mix.
WRF_SYNTH_VDD1P2	J10		PWR	1.2 V supply for the synthesizer.
WRF_AFE_VDD1P35	K10		PWR	1.35 V supply for the AFE.
Miscellaneous Supplies				
VDDC	C8, E2, F8, J5		PWR	1.2 V core supply for the WLAN.
VDDIO	D5		PWR	1.8 V–3.3 V VDDIO supply for the WLAN. Must be directly connected to PMU_VDDO and BT_VDDO on the PCB.
BT_VDDC	F2, J4, L1		PWR	1.2 V core supply for the BT.
BT_VDDO	G4		PWR	1.8 V–3.3 V VDDIO supply for the BT. Must be directly connected to PMU_VDDO and VDDIO on the PCB.
VDDIO_SD	D6		PWR	1.8 V–3.3 V supply for the SDIO pads.
VDDIO_RF	E7		PWR	IO supply for the RF switch control pads (3.3 V).
AVDD_BBPLL	E9		PWR	1.2 V supply for the baseband PLL.
PCIE_PLL_AVDD1P2	C10		PWR	1.2 V supply for the PCIe PLL.
VOUT_PCIELDO	B2		PWR	1.2 V supply for the PCIe.
PCIE_RXTX_AVDD1P2	B9		PWR	1.2 V supply for the PCIe TX/RX.
Ground				
WRF_VCO_GND	J8		GND	VCO/LOGEN ground.
WRF_AFE_GND	L9		GND	AFE ground.
WRF_XTAL_GND1P2	G10		GND	XTAL ground.
WRF_RX2G_GND	M8		GND	RX 2 GHz ground.
WRF_RX5G_GND	K11		GND	RX 5 GHz ground.
WRF_PA_GND3P3	M10		GND	PA ground.
WRF_GENERAL_GND	K9		GND	General ground.
WRF_GENERAL2_GND	L10		GND	General ground.
WRF_SYNTH_GND	J9		GND	Ground.
VSSC	C5, F5, F9, G2, K5, L2		GND	Core ground for WLAN and BT.
SR_PVSS	A1		GND	Power ground.

Table 20. Signal Descriptions (continued)

Signal Name	WLBGA Ball		Type	Description
PMU_AVSS	C2		GND	Quiet ground.
BT_PAVSS	M6		GND	Bluetooth PA ground.
BT_LNAVSS	M7		GND	Bluetooth LNA ground.
BT_IFVSS	L6		GND	Bluetooth IF block ground.
BT_PLLVSS	L5		GND	Bluetooth PLL ground.
FM_PLLVSS	M4		GND	FM PLL ground.
FM_RFVSS	M3		GND	FM RF ground.
AVSS_BBPLL	E10		GND	Baseband PLL ground.
PCIE_VSS	C9		GND	PCIe ground.
No Connect				
NC1	D9		–	No connect.
NC2	E11			
NC3	E8			
NC	H4		–	No connect.
Depopulated Pins				
–	A11, H7, N10		–	–

12.5 WLAN GPIO Signals and Strapping Options

This section describes WLAN GPIO signals and strapping options. The pins are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 21. Strapping Options

Pin Name	Strap	WLBGA Ball		Default Internal Pull During Strap	Description
GPIO_7	sdio_padvddio	E1		1	Default pull = 1. SDIO interface voltage. 1 = 1.8 V, 0 = 3.3 V. Default is 1.8 V.
GPIO_16	host_iface_sdio	K6		0	Default is PCIe. Pull high during POR to select SDIO.

12.5.1 Multiplexed Bluetooth GPIO Signals

The Bluetooth GPIO pins (BT_GPIO_0 to BT_GPIO_7) are multiplexed pins and can be programmed to be used as GPIOs or for other Blue
I^2S. The specific function for a given BT_GPIO_X pin is chosen by programming the Pad Function Control register for that specific pin. Table
for each BT_GPIO_X pin. Note that each BT_GPIO_X pin's Pad Function Control register setting is independent (BT_GPIO_5 can be set to
that BT_GPIO_3 is set to pad function 0). When the Pad Function Control register is set to 0, the BT_GPIOs do not have specific functions a
generic GPIOs. The A_GPIO_X pins described below are multiplexed behind the CYW43455's PCM and I^2S interface pins.

Table 22. GPIO Multiplexing Matrix

Pin Name	Pad Function Control Register Setting							
	0	1	2	3	4	5	6	
BT_UART_CTS_N	UART_CTS_N	–	–	–	–	–	–	A
BT_UART_RTS_N	UART_RTS_N	–	–	–	–	–	–	A
BT_UART_RXD	UART_RXD	–	–	–	–	–	–	G
BT_UART_TXD	UART_TXD	–	–	–	–	–	–	G
BT_PCM_IN	A_GPIO[3]	PCM_IN	PCM_IN	HCLK	–	–	–	I2
BT_PCM_OUT	A_GPIO[2]	PCM_OUT	PCM_OUT	LINK_IND	–	I2S_MSDO	–	I2
BT_PCM_SYNC	A_GPIO[1]	PCM_SYNC	PCM_SYNC	HCLK	–	I2S_MWS	–	I2
BT_PCM_CLK	A_GPIO[0]	PCM_CLK	PCM_CLK	–	–	I2S_MSCK	–	I2
BT_I2S_DO	A_GPIO[5]	PCM_OUT	–	–	I2S_SSDO	I2S_MSDO	–	S
BT_I2S_DI	A_GPIO[6]	PCM_IN	–	HCLK	I2S_SSDI/MSDI	–	–	T
BT_I2S_WS	GPIO[7]	PCM_SYNC	–	LINK_IND	–	I2S_MWS	–	I2
BT_I2S_CLK	GPIO[6]	PCM_CLK	–	–	–	I2S_MSCK	–	I2
BT_GPIO_5	GPIO[5]	HCLK	–	I2S_MSCK	I2S_SSCK	–	–	C
BT_GPIO_4	GPIO[4]	LINK_IND	–	I2S_MSDO	I2S_SSDO	–	–	–
BT_GPIO_3	GPIO[3]	–	–	I2S_MWS	I2S_SWS	–	–	–
BT_GPIO_2	GPIO[2]	–	–	–	I2S_SSDI/MSDI	–	–	–
BT_CLK_REQ	WL/BT_CLK_REQ	–	–	–	–	–	–	A

The multiplexed GPIO signals are described in Table 23.

Table 23. Multiplexed GPIO Signals

Pin Name	Type	Description
UART_CTS_N	I	Host UART clear to send.
UART_RTS_N	O	Device UART request to send.
UART_RXD	I	Device UART receive data.
UART_TXD	O	Host UART transmit data.
PCM_IN	I	PCM data input.
PCM_OUT	O	PCM data output.
PCM_SYNC	I/O	PCM sync signal, can be master (output) or slave (input).
PCM_CLK	I/O	PCM clock, can be master (output) or slave (input).
GPIO[7:0]	I/O	General-purpose I/O.
A_GPIO[7:0]	I/O	A group general-purpose I/O.
I2S_MSDO	O	I^2S master data output.
I2S_MWS	O	I^2S master word select.
I2S_MSCK	O	I^2S master clock.
I2S_SSCK	I	I^2S slave clock.
I2S_SSDO	O	I^2S slave data output.
I2S_SWS	I	I^2S slave word select.
I2S_SSDI/MSDI	I	I^2S slave/master data input.
STATUS	O	Signals Bluetooth priority status.
TX_CON_FX	I	WLAN-BT coexist. Transmission confirmation; permission for BT to transmit.
RF_ACTIVE	O	WLAN-BT coexist. Asserted (logic high) during local BT RX and TX slots.
LINK_IND	O	BT receiver/transmitter link indicator.
CLK_REQ	O	WLAN/BT clock request output.
SF_SPI_CLK	O	SFlash SCLK: serial clock (output from master).
SF_MISO	I	SFlash MISO; SOMI: master input, slave output (output from slave).
SF_MOSI	O	SFlash MOSI; SIMO: master output, slave input (output from master).
SF_SPI_CSN	O	SFlash SS: slave select (active low, output from master).

12.6 I/O States

The following notations are used in Table 24:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Table 24. I/O States

Name	I/O	Keeper[1]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[2] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_R BT_R VDD
WL_REG_ON	I	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input;
BT_REG_ON	I	N	Input; PD (pull down can be disabled)	Input; PD (pull down can be disabled)	Input; PD (of 200K)	Input; PD (of 200K)	Input;
BT_CLK_REQ	I/O	Y	Open drain or push-pull (programmable). Active high.	Open drain or push-pull (programmable). Active high	High-Z, NoPull	Open drain. Active high	Open
BT_HOST_WAKE	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input,
BT_DEV_WAKE	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input,
BT_GPIO_2, BT_GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input,
BT_GPIO_4, BT_GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input,
BT_UART_CTS_N	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; PU	Input;
BT_UART_RTS_N	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input;
BT_UART_RXD	I	Y	Input; PU	Input; NoPull	High-Z, NoPull	Input; PU	Input;
BT_UART_TXD	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU	Input;

Table 24. I/O States (continued)

Name	I/O	Keeper[1]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[2] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_R BT_R VDD
SDIO_DATA[0:3]	I/O	N	Input/Output; PU (SDIO Mode)	Input; PU (SDIO Mode)	High-Z, NoPull	Input; PU (SDIO Mode)	Input;
SDIO_CMD	I/O	N	Input/Output; PU (SDIO Mode)	Input; PU (SDIO Mode)	High-Z, NoPull	Input; PU (SDIO Mode)	Input;
SDIO_CLK	I	N	Input; NoPull	Input; noPull	High-Z, NoPull	Input; noPull	Input;
BT_PCM_CLK	I/O	Y	Input; NoPull[3]	Input; NoPull[3]	High-Z, NoPull	Input, PD	Input,
BT_PCM_IN	I/O	Y	Input; NoPull[3]	Input; NoPull[3]	High-Z, NoPull	Input, PD	Input,
BT_PCM_OUT	I/O	Y	Input; NoPull[3]	Input; NoPull[3]	High-Z, NoPull	Input, PD	Input,
BT_PCM_SYNC	I/O	Y	Input; NoPull [3]	Input; NoPull[3]	High-Z, NoPull	Input, PD	Input,
BT_I2S_WS	I/O	Y	Input; NoPull[4]	Input; NoPull[4]	High-Z, NoPull	Input, PD	Input,
BT_I2S_CLK	I/O	Y	Input; NoPull[4]	Input; NoPull[4]	High-Z, NoPull	Input, PD	Input,
BT_I2S_DI	I/O	Y	Input; NoPull[4]	Input; NoPull[4]	High-Z, NoPull	Input, PD	Input,
BT_I2S_DO	I/O	Y	Input; NoPull[4]	Input; NoPull[4]	High-Z, NoPull	Input, PD	Input,
GPIO_0	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input;
GPIO_1	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;
GPIO_2	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;
GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input;
GPIO_4	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;

Table 24. I/O States (continued)

Name	I/O	Keeper[1]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[2] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_R BT_R VDD
GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input;
GPIO_6	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;
GPIO_7	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;
GPIO_8	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])[5]	Input/Output; PU, PD, NoPull (programmable [Default: PD])[5]	High-Z, NoPull	Input; PD[5]	Input;
GPIO_9	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD	Input;
GPIO_10	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;
GPIO_13	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;
GPIO_14	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;
GPIO_15	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;
GPIO_16	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull	Input;

Table 24. I/O States (continued)

Name	I/O	Keeper[1]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[2] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON High)	(WL_R BT_R VDD
RF_SW_CTRL [0:8]	I/O	Y	Output; NoPull	Output; NoPull	High-Z	Output; NoPull	Outpu

1. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in power-down state. If there is no keeper, and it is an input pad should be driven to prevent leakage due to floating pad (SDIO_CLK, for example).
2. In the power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.
3. Depending on whether the PCM interface is enabled and the configuration of PCM is in master or slave mode, it can be either output or input.
4. Depending on whether the I^2S interface is enabled and the configuration of I^2S is in master or slave mode, it can be either output or input.
5. NoPull when in SDIO mode.

13. DC Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

13.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 25 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 25. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for the VBAT and PA driver supply	VBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO	–0.5 to 3.9	V
DC supply voltage for RF switch I/Os	VDDIO_RF	–0.5 to 3.9	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 1.575	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
WRF_TCXO_VDD	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O[1]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[1]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C

1. Duration not to exceed 25% of the duty cycle.

13.2 Environmental Ratings

The environmental ratings are shown in Table 26.

Table 26. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to +85	°C	Functional operation[1]
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

1. Functionality is guaranteed across this ambient temperature range. Optimal RF performance specified in the data sheet, however, is guaranteed only for –20°C to 75°C.

13.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 27. ESD Specifications

Pin Type	Symbol	Condition	Minimum ESD Rating	Unit
ESD Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1	kV
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V

13.4 Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 28. Operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Note: For DC absolute maximum rating (AMR), see Table 25.

Table 28. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.0[1]	–	5.25[2]6.0	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for TCXO input buffer	WRF_TCXO_VDD	1.62	1.8	1.98	V
DC supply voltage for digital I/O	VDDIO	1.62	–	3.63	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V
Other Digital I/O Pins					
For VDDIO = 1.8 V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
For VDDIO = 3.3V:					
Input high voltage	VIH	2.00	–	–	V
Input low voltage	VIL	–	–	0.80	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low Voltage @ 2 mA	VOL	–	–	0.40	V
RF Switch Control Output Pins[3]					
For VDDIO_RF = 3.3 V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Output capacitance	C_{OUT}	–	–	5	pF

1. The CYW43455 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2 V < VBAT < 4.8 V.
2. The maximum continuous voltage is 5.25 V.
3. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

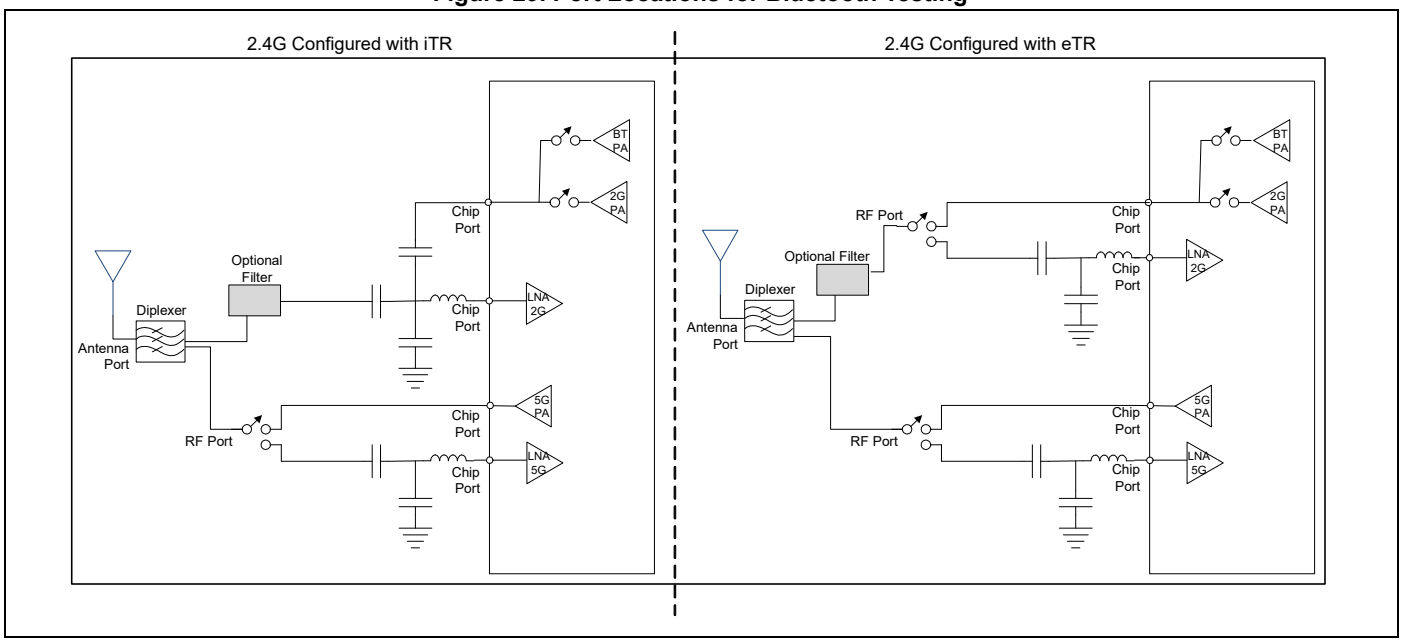
14. Bluetooth RF Specifications

Note: Values in this data sheet are design goals and are subject to change based on device characterization results.

Unless otherwise stated, limit values apply for the conditions specified in Table 26 and Table 28. Typical values apply for the following conditions:

- VBAT = 3.6 V
- Ambient temperature +25°C

Figure 29. Port Locations for Bluetooth Testing



Note: All Bluetooth specifications are measured at the chip port, unless otherwise defined.

Note: The specifications in Table 28 are measured at the chip port input, unless otherwise defined.

Table 29. Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity[1]	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Input IP3	–	–16	–	–	dBm
Maximum input at RF port	–	–	–	–20	dBm
RX LO Leakage					
2.4 GHz band	–	–	–	–90	dBm
Interference Performance[2]					
C/I co-channel	GFSK, 0.1% BER	–	–	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9	dB

Table 29. Bluetooth Receiver RF Specifications (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
C/I 1-MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20	dB
C/I co-channel	π/4-DQPSK, 0.1% BER	–	–	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–30	dB
C/I ≥ 3 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–40	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–	–7	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–	–20	dB
C/I co-channel	8-DPSK, 0.1% BER	–	–	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13	dB
Out-of-Band Blocking Performance (CW)					
30–2000 MHz	0.1% BER	–	–10	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer					
GFSK (1 Mbps) [3]					
698–716 MHz	WCDMA	–	–14	–	dBm
776–849 MHz	WCDMA	–	–14	–	dBm
824–849 MHz	GSM850	–	–14	–	dBm
824–849 MHz	WCDMA	–	–14	–	dBm
880–915 MHz	E-GSM	–	–13	–	dBm
880–915 MHz	WCDMA	–	–13	–	dBm
1710–1785 MHz	GSM1800	–	–18	–	dBm
1710–1785 MHz	WCDMA	–	–17	–	dBm
1850–1910 MHz	GSM1900	–	–20	–	dBm
1850–1910 MHz	WCDMA	–	–19	–	dBm
1880–1920 MHz	TD-SCDMA	–	–20	–	dBm
1920–1980 MHz	WCDMA	–	–20	–	dBm
2010–2025 MHz	TD–SCDMA	–	–20	–	dBm
2500–2570 MHz	WCDMA	–	–23	–	dBm
2500–2570 MHz[4]	Band 7	–	–25	–	dBm
2300–2400 MHz[5]	Band 40	–	–35.2	–	dBm
2570–2620 MHz[6]	Band 38	–	–21	–	dBm
2545–2575 MHz[7]	XGP Band	–	–22	–	dBm
π/4-DPSK (2 Mbps) [3]					
698–716 MHz	WCDMA	–	–10	–	dBm
776–794 MHz	WCDMA	–	–10	–	dBm
824–849 MHz	GSM850	–	–11	–	dBm

Table 29. Bluetooth Receiver RF Specifications (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
824–849 MHz	WCDMA	–	–11	–	dBm
880–915 MHz	E-GSM	–	–10	–	dBm
880–915 MHz	WCDMA	–	–10	–	dBm
1710–1785 MHz	GSM1800	–	–16	–	dBm
1710–1785 MHz	WCDMA	–	–16	–	dBm
1850–1910 MHz	GSM1900	–	–17	–	dBm
1850–1910 MHz	WCDMA	–	–16	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18	–	dBm
1920–1980 MHz	WCDMA	–	–17	–	dBm
2010–2025 MHz	TD-SCDMA	–	–19	–	dBm
2500–2570 MHz	WCDMA	–	–23	–	dBm
2500–2570 MHz[d]	Band 7	–	–24.4	–	dBm
2300–2400 MHz[e]	Band 40	–	–36.5	–	dBm
2570–2620 MHz[f]	Band 38	–	–21	–	dBm
2545–2575 MHz[g]	XGP Band	–	–22	–	dBm
8-DPSK (3 Mbps) [3]					
698-716 MHz	WCDMA	–	–13	–	dBm
776-794 MHz	WCDMA	–	–13	–	dBm
824-849 MHz	GSM850	–	–13	–	dBm
824-849 MHz	WCDMA	–	–14	–	dBm
880-915 MHz	E-GSM	–	–13	–	dBm
880-915 MHz	WCDMA	–	–13	–	dBm
1710-1785 MHz	GSM1800	–	–18	–	dBm
1710-1785 MHz	WCDMA	–	–17	–	dBm
1850-1910 MHz	GSM1900	–	–19	–	dBm
1850-1910 MHz	WCDMA	–	–19	–	dBm
1880-1920 MHz	TD-SCDMA	–	–19	–	dBm
1920-1980 MHz	WCDMA	–	–19	–	dBm
2010-2025 MHz	TD-SCDMA	–	–20	–	dBm
2500-2570 MHz	WCDMA	–	–23	–	dBm
2500–2570 MHz[d]	Band 7	–	–24.7	–	dBm
2300–2400 MHz[e]	Band 40	–	–36.7	–	dBm
2570–2620 MHz[f]	Band 38	–	–21	–	dBm
2545–2575 MHz[g]	XGP Band	–	–22	–	dBm

Table 29. Bluetooth Receiver RF Specifications (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Spurious Emissions					
30 MHz–1 GHz		–	–95	–62	dBm
1–12.75 GHz		–	–70	–47	dBm
851–894 MHz		–	–147	–	dBm/Hz
925–960 MHz		–	–147	–	dBm/Hz
1805–1880 MHz		–	–147	–	dBm/Hz
1930–1990 MHz		–	–147	–	dBm/Hz
2110–2170 MHz		–	–147	–	dBm/Hz

1. Dirty TX is off.
2. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.1 specification.
3. 3 dB receiver desense.
4. 2560 MHz performance is used.
5. 2360 MHz performance is used.
6. 2580 MHz performance is used.
7. 2555 MHz performance is used.

Table 30. Bluetooth Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the Bluetooth chip port output, unless otherwise defined.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth		–	12	–	dBm
QPSK TX Power at Bluetooth		–	8	–	dBm
8PSK TX Power at Bluetooth		–	8	–	dBm
Power control step	–	2	4	8	dB
Note: Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–31	–20	dBm
|M – N| ≥ 2.5 MHz[1]		–	–43	–40	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36 [2, 3]	dBm
1 GHz to 12.75 GHz	–	–	–	–30 [b, 4, 5]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47	dBm
GPS Band Spurious Emissions					
Spurious emissions	–	–	–103	–	dBm

Table 30. Bluetooth Transmitter RF Specifications (continued)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Out-of-Band Noise Floor [6]					
65–108 MHz	FM RX	–	–147	–	dBm/Hz
776–794 MHz	CDMA2000	–	–146	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–146	–	dBm/Hz
925–960 MHz	E-GSM	–	–146	–	dBm/Hz
1570–1580 MHz	GPS	–	–146	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–144	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–143	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–137	–	dBm/Hz
2500–2570 MHz	Band 7	–	–130	–	dBm/Hz
2300–2400 MHz	Band 40	–	–130	–	dBm/Hz
2570–2620 MHz	Band 38	–	–132	–	dBm/Hz
2545–2575 MHz	XGP Band	–	–135	–	dBm/Hz

1. The typical number is measured at ± 3 MHz offset.
2. The maximum value represents the value required for Bluetooth qualification as defined in the v4.1 specification.
3. The spurious emissions during Idle mode are the same as specified in Table 30.
4. Specified at the Bluetooth Antenna port.
5. Meets this specification using a front-end band-pass filter.
6. Transmitted power in cellular and FM bands at the antenna port. See Figure 29 for location of the port.

Table 31. Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	±25	±75	kHz
Frequency Drift				
DH1 packet	–	±8	±25	kHz
DH3 packet	–	±8	±40	kHz
DH5 packet	–	±8	±40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[1]	140	155	175	kHz
10101010 sequence in payload[2]	115	140	–	kHz
Channel spacing	–	1	–	MHz

1. This pattern represents an average deviation in payload.
2. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 32. BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	–	2402	–	2480	MHz
RX sense[1]	GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
TX power[2]	–	–	8.5	–	dBm
Mod Char: delta F1 average	–	225	255	275	kHz
Mod Char: delta F2 max.[3]	–	230	–	–	%
Mod Char: ratio	–	0.8	1	–	%

1. Dirty TX is Off.
2. The BLE TX power cannot exceed 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.
3. At least 99.9% of all delta F2 max. frequency values recorded over 10 packets must be greater than 185 kHz.

15. WLAN RF Specifications

15.1 Introduction

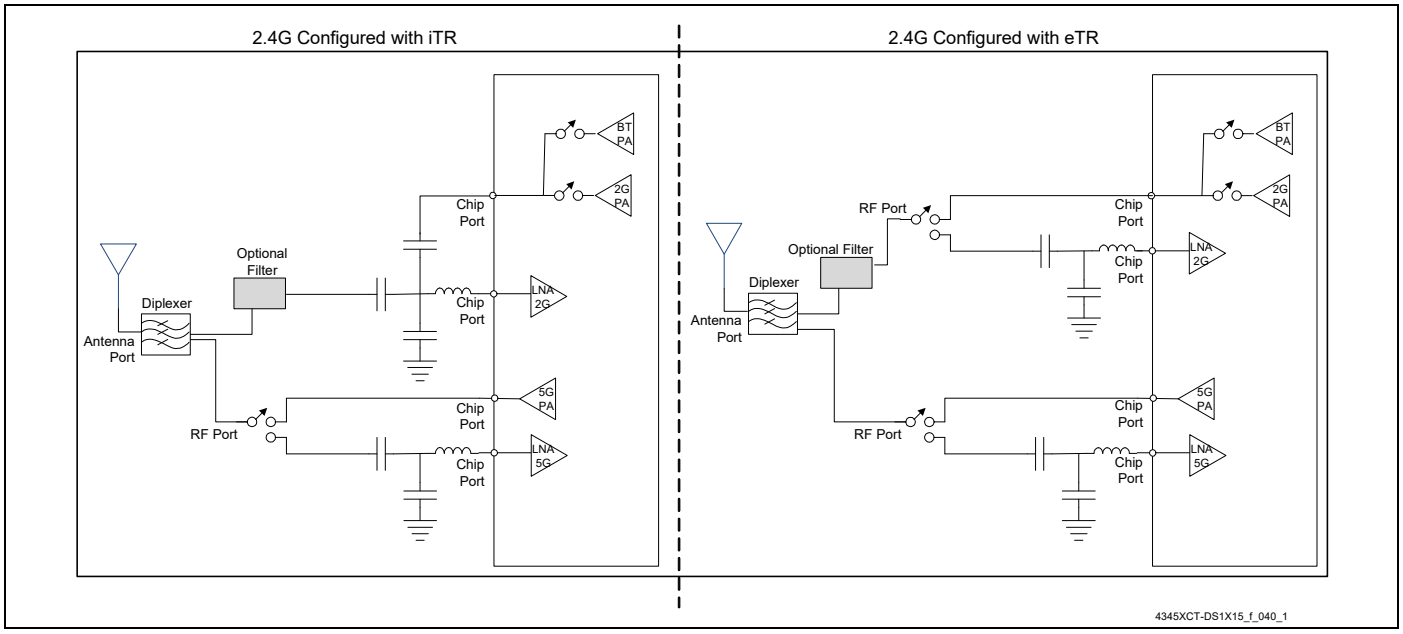
The CYW43455 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radio.

Note: Values in this section of the data sheet are design goals and are subject to change based on device characterization results.

Unless otherwise stated, limit values apply for the conditions specified in Table 26 and Table 28. Typical values apply for the following conditions:

- VBAT = 3.6 V
- Ambient temperature +25°C

Figure 30. Port Locations for WLAN Testing



Note: Unless otherwise defined, all WLAN specifications are provided at the chip port.

15.2 2.4 GHz Band General RF Specifications

Table 33. 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	<2	µs

15.3 WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications shown in the following table are provided at the chip port, unless otherwise defined.

Table 34. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	–	–98.7	–	dBm
	2 Mbps DSSS	–	–96.0	–	dBm
	5.5 Mbps DSSS	–	–94.4	–	dBm
	11 Mbps DSSS	–	–90.7	–	dBm
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–	–95.3	–	dBm
	9 Mbps OFDM	–	–94.3	–	dBm
	12 Mbps OFDM	–	–93.5	–	dBm
	18 Mbps OFDM	–	–90.9	–	dBm
	24 Mbps OFDM	–	–87.7	–	dBm
	36 Mbps OFDM	–	–84.4	–	dBm
	48 Mbps OFDM	–	–79.6	–	dBm
	54 Mbps OFDM	–	–78.2	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) [1] Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–94.8	–	dBm
	MCS1	–	–92.3	–	dBm
	MCS2	–	–89.8	–	dBm
	MCS3	–	–86.4	–	dBm
	MCS4	–	–83.3	–	dBm
	MCS5	–	–78.6	–	dBm
	MCS6	–	–76.7	–	dBm
	MCS7	–	–74.7	–	dBm
RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) [2] Defined for default parameters: 800 ns GI and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0	–	–95.0	–	dBm
	MCS1	–	–92.3	–	dBm
	MCS2	–	–90.1	–	dBm
	MCS3	–	–87.0	–	dBm
	MCS4	–	–83.6	–	dBm
	MCS5	–	–78.7	–	dBm
	MCS6	–	–76.8	–	dBm
	MCS7	–	–75.9	–	dBm
	MCS8	–	–71.5	–	dBm
RX sensitivity IEEE 802.11ac with LDPC (10% PER for 4096 octet PSDU) at RF port. Defined for default parameters: 800 ns GI, LDPC coding, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS7	–	–77.8	–	dBm
	MCS8	–	–74.0	–	dBm
	MCS9	–	–72.0	–	dBm

Table 34. WLAN 2.4 GHz Receiver Performance Specifications (continued)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Blocking level for 3 dB RX sensitivity degradation (without external filtering)[3]	776–794 MHz (CDMA2000):				
	Blocker frequency = 794 MHz	–	–16	–	dBm
	824–849 MHz[4] (cdmaOne):				
	Blocker frequency = 849 MHz	–	–11	–	dBm
	824–849 MHz (GSM850):				
	Blocker frequency = 849 MHz	–	–11	–	dBm
	880–915 MHz (E-GSM):				
	Blocker frequency = 915 MHz	–	–11	–	dBm
	1710–1785 MHz (GSM1800):				
	Blocker frequency = 1785 MHz	–	–12	–	dBm
	1850–1910 MHz (GSM1900):				
	Blocker frequency = 1910 MHz	–	–13	–	dBm
	1850–1910 MHz (cdmaOne):				
	Blocker frequency = 1910 MHz	–	–5	–	dBm
	1850–1910 MHz (WCDMA):				
	Blocker frequency = 1910 MHz	–	–19	–	dBm
	1920–1980 MHz (WCDMA):				
	Blocker frequency = 1980 MHz	–	–19	–	dBm
	2300–2400 MHz (LTE band 40)				
	Blocker frequency = 2300 MHz	–	–29	–	dBm
	Blocker frequency = 2365 MHz	–	–35	–	dBm
	2500–2570 MHz (LTE band 7):				
	Blocker frequency = 2505 MHz	–	–39	–	dBm
	Blocker frequency = 2565 MHz	–	–35	–	dBm
	2570–2620 MHz (LTE band 38):				
	Blocker frequency = 2575 MHz	–	–35	–	dBm
	2496-2690 MHz (LTE band 41):				
	Blocker frequency = 2501 MHz	–	–42	–	dBm
	Blocker frequency = 2685 MHz	–	–17	–	dBm
	2545–2575 MHz (XGP Band):				
	Blocker frequency = 2550 MHz	–	–33	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max. input level)	–80	–	–	dBm
Input In-Band IP3	Maximum LNA gain	–	–10	–	dBm
	Minimum LNA gain	–	15	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)	–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)	–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)	–9.5	–	–	dBm
	@ MCS0–MCS7 rates (10% PER, 4095 octets)	–9.5	–	–	dBm
	@ MCS8–MCS9 rates (10% PER, 4095 octets)	–11.5	–	–	dBm

Table 34. WLAN 2.4 GHz Receiver Performance Specifications (continued)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	Desired and interfering signal 30 MHz apart					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Adjacent channel rejection MCS0–MCS9 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS0	–79 dBm	16	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS7	–61 dBm	–2	–	–	dB
	MCS8	–59 dBm	–4	–	–	dB
	MCS9	–57 dBm	–6	–	–	dB
Maximum receiver gain	–	–	–	70	–	dB
Gain control step	–	–	–	3	–	dB
RSSI accuracy[5]	Range –95[6] dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		10	11.5	13	dB
Receiver cascaded noise figure	At maximum gain		–	4	–	dB

1. Sensitivity degradations for alternate settings in MCS modes. SGI: 2 dB drop.
2. Sensitivity degradations for alternate settings in MCS modes. SGI: 2 dB drop.
3. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
4. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
5. The minimum and maximum values shown have a 95% confidence level.
6. –95 dBm with calibration at time of manufacture, –92 dBm without calibration.

15.4 WLAN 2.4 GHz Transmitter Performance Specifications

Note: Unless otherwise noted, the values shown in the following table are provided at the WLAN chip port output.

Table 35. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
Transmitted power in cellular and FM bands (at +21 dBm, 100% duty cycle, 1 Mbps CCK) [1]	776-794 MHz (CDMA2000)	–	–164	–	dBm/Hz
	869–960 MHz (cdmaOne, GSM850)	–	–163	–	dBm/Hz
	1450–1495 (DAB)	–	–153.6	–	dBm/Hz
	1570–1580 MHz (GPS)	–	–151.2	–	dBm/Hz
	1592–1610 MHz (GLONASS)	–	–150.4	–	dBm/Hz
	1710–1800 (DSC-1800-Uplink)	–	–145	–	dBm/Hz
	1805–1880 MHz (GSM 1800)	–	–139	–	dBm/Hz
	1850–1910 MHz (GSM 1900)	–	–139	–	dBm/Hz
	1910–1930 MHz (TDSCDMA,LTE)	–	–140	–	dBm/Hz
	1930–1990 MHz (GSM1900, cdmaOne, WCDMA)	–	–128	–	dBm/Hz
	2010–2075 MHz (TDSCDMA)	–	–131	–	dBm/Hz
	2110–2170 MHz (WCDMA)	–	–125	–	dBm/Hz
	2305–2370 (LTE band 40)	–	–95	–	dBm/Hz
	2370–2400 (LTE band 40)	–	–80	–	dBm/Hz
	2496-2530 (LTE band 41)	–	–90	–	dBm/Hz
	2530-2560 (LTE band 41)	–	–110	–	dBm/Hz
	2570-2690 (LTE band 41)	–	–116	–	dBm/Hz
	5000-5900 (WLAN 5G)	–	–155	–	dBm/Hz
EVM Does Not Exceed					
TX power at the chip port for highest power level setting at 25°C and VBAT = 3.6V with spectral mask and EVM compliance	802.11b (DSSS/CCK) –9 dB	–	20.5	–	dBm
	OFDM, BPSK –8 dB	–	20	–	dBm
	OFDM, 64QAM –25 dB	–	19	–	dBm
	MCS7 –27 dB	–	19	–	dBm
	MCS8 –30 dB	–	17	–	dBm
Phase noise	37.4 MHz crystal, integrated from 10 kHz to 10 MHz	–	0.45	–	Degrees
TX power control dynamic range	–	10	–	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies to 10 dBm to 20 dBm output power range.	–	–	±1.5	dB
Carrier suppression	–	15	–	–	dBc
Gain control step	–	–	0.25	–	dB
Return loss at Chip port TX	Z_o = 50Ω	–	6	–	dB

1. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

15.5 WLAN 5 GHz Receiver Performance Specifications

Note: Unless otherwise noted, the values shown in the following table are provided at the chip port input.

Table 36. WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	4900	–	5845	MHz
RX sensitivity [1] IEEE 802.11a (10% PER for 1000 octet PSDU)	6 Mbps OFDM	–	–94.5	–	dBm
	9 Mbps OFDM	–	–93.5	–	dBm
	12 Mbps OFDM	–	–92.7	–	dBm
	18 Mbps OFDM	–	–90.1	–	dBm
	24 Mbps OFDM	–	–86.9	–	dBm
	36 Mbps OFDM	–	–83.6	–	dBm
	48 Mbps OFDM	–	–78.6	–	dBm
	54 Mbps OFDM	–	–77.4	–	dBm
RX sensitivity [1] IEEE 802.11n (10% PER for 4096 octet PSDU) Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–94.0	–	dBm
	MCS1	–	–91.5	–	dBm
	MCS2	–	–89.0	–	dBm
	MCS3	–	–85.6	–	dBm
	MCS4	–	–82.5	–	dBm
	MCS5	–	–77.8	–	dBm
	MCS6	–	–75.9	–	dBm
	MCS7	–	–73.9	–	dBm
RX sensitivity [1] IEEE 802.11n (10% PER for 4096 octet PSDU) Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS0	–	–92.0	–	dBm
	MCS1	–	–89.0	–	dBm
	MCS2	–	–86.5	–	dBm
	MCS3	–	–83.2	–	dBm
	MCS4	–	–79.9	–	dBm
	MCS5	–	–75.3	–	dBm
	MCS6	–	–73.8	–	dBm
	MCS7	–	–72.2	–	dBm
RX sensitivity [1] IEEE 802.11ac (10% PER for 4096 octet PSDU) Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–	–94.2	–	dBm
	MCS1	–	–91.5	–	dBm
	MCS2	–	–89.3	–	dBm
	MCS3	–	–86.2	–	dBm
	MCS4	–	–82.8	–	dBm
	MCS5	–	–77.9	–	dBm
	MCS6	–	–76.0	–	dBm
	MCS7	–	–75.1	–	dBm
	MCS8	–	–70.7	–	dBm

Table 36. WLAN 5 GHz Receiver Performance Specifications (continued)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
RX sensitivity [1] IEEE 802.11ac (10% PER for 4096 octet PSDU) Defined for default parameters: 800 ns GI and non-STBC.	40 MHz channel spacing for all MCS rates					
	MCS0		–	–92.3	–	dBm
	MCS1		–	–89.3	–	dBm
	MCS2		–	–86.9	–	dBm
	MCS3		–	–83.6	–	dBm
	MCS4		–	–80.2	–	dBm
	MCS5		–	–75.6	–	dBm
	MCS6		–	–74.0	–	dBm
	MCS7		–	–72.6	–	dBm
	MCS8		–	–68.3	–	dBm
	MCS9		–	–66.7	–	dBm
RX sensitivity [1] IEEE 802.11ac (10% PER for 4096 octet PSDU) Defined for default parameters: 800 ns GI and non-STBC.	80 MHz channel spacing for all MCS rates					
	MCS0		–	–89.0	–	dBm
	MCS1		–	–86.0	–	dBm
	MCS2		–	–83.3	–	dBm
	MCS3		–	–80.1	–	dBm
	MCS4		–	–76.8	–	dBm
	MCS5		–	–72.2	–	dBm
	MCS6		–	–70.9	–	dBm
	MCS7		–	–69.2	–	dBm
	MCS8		–	–65.2	–	dBm
	MCS9		–	–63.6	–	dBm
RX sensitivity [1] IEEE 802.11ac 20/40/80 MHz channel spacing with LDPC (10% PER for 4096 octet PSDU) at RF port. Defined for default parameters: 800 ns GI, LDPC coding and non-STBC.	MCS7	20 MHz	–	–76.8	–	dBm
	MCS8	20 MHz	–	–72.9	–	dBm
	MCS9	20 MHz	–	–70.7	–	dBm
	MCS7	40 MHz	–	–74.8	–	dBm
	MCS8	40 MHz	–	–70.9	–	dBm
	MCS9	40 MHz	–	–68.9	–	dBm
	MCS7	80 MHz	–	–71.5	–	dBm
	MCS8	80 MHz	–	–67.6	–	dBm
	MCS9	80 MHz	–	–65.5	–	dBm

Table 36. WLAN 5 GHz Receiver Performance Specifications (continued)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Blocking level for 3 dB RX sensitivity degradation (without external filtering)[2]	776–794 MHz (CDMA2000):				
	Blocker frequency = 794 MHz	–	–21	–	dBm
	824–849 MHz[3] (cdmaOne):				
	Blocker frequency = 849 MHz	–	–20	–	dBm
	824–849 MHz (GSM850):				
	Blocker frequency = 849 MHz	–	–10	–	dBm
	880–915 MHz (E-GSM):				
	Blocker frequency = 915 MHz	–	–12	–	dBm
	1710–1785 MHz (GSM1800):				
	Blocker frequency = 1785 MHz	–	–13	–	dBm
	1850–1910 MHz (GSM1900):				
	Blocker frequency = 1910 MHz	–	–13	–	dBm
	1850–1910 MHz (cdmaOne):				
	Blocker frequency = 1910 MHz	–	–18	–	dBm
	1850–1910 MHz (WCDMA):				
	Blocker frequency = 1910 MHz	–	–20	–	dBm
	1920–1980 MHz (WCDMA):				
	Blocker frequency = 1980 MHz	–	–20	–	dBm
	2300–2400 MHz (LTE band 40)				
	Blocker frequency = 2395 MHz	–	–19	–	dBm
	2500–2570 MHz (LTE band 7):				
	Blocker frequency = 2565 MHz	–	–16	–	dBm
	2570–2620 MHz (LTE band 38):				
	Blocker frequency = 2615 MHz	–	–16	–	dBm
	2496-2690 MHz (LTE band 41):				
	Blocker frequency = 2685 MHz	–	–16	–	dBm
	2545–2575 MHz (XGP Band):				
	Blocker frequency = 2570 MHz	–	–18	–	dBm
Input In-Band IP3	Maximum LNA gain	–	–11	–	dBm
	Minimum LNA gain	–	5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps	–9.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps	–14.5	–	–	dBm

Table 36. WLAN 5 GHz Receiver Performance Specifications (continued)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[4] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
	65 Mbps OFDM	–60.5 dBm	14	–	–	dB
Maximum receiver gain	–		–	65	–	dB
Gain control step	–		–	3	–	dB
RSSI accuracy[5]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω, across the dynamic range		10	–	13	dB
Receiver cascaded noise figure	At maximum gain		–	4	–	dB

1. For PCIE derate 5G RX sensitivity by 1.5 dB
2. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
3. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)
4. For 65 Mbps, the size is 4096.
5. The minimum and maximum values shown have a 95% confidence level.

15.6 WLAN 5 GHz Transmitter Performance Specifications

Note: Unless otherwise noted, the values shown in the following table are provided at the WLAN chip port output.

Table 37. WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
Transmitted power in cellular and FM bands (at +18.5 dBm, 100% duty cycle, 6 Mbps OFDM) [1]	776–794 MHz (CDMA2000)		–	–164	–	dBm/Hz
	869–960 MHz (cdmaOne, GSM850)		–	–166	–	dBm/Hz
	1450–1495 (DAB)		–	–166	–	dBm/Hz
	1570–1580 MHz (GPS)		–	–166	–	dBm/Hz
	1592–1610 MHz (GLONASS)		–	–165.5	–	dBm/Hz
	1710–1800(DSC-1800-Uplink)		–	–135	–	dBm/Hz
	1805–1880 MHz (GSM 1800)		–	–165	–	dBm/Hz
	1850–1910 MHz (GSM 1900)		–	–165	–	dBm/Hz
	1910–1930 MHz (TDSCDMA, LTE)		–	–165	–	dBm/Hz
	1930–1990 MHz (GSM1900, cdmaOne, WCDMA)		–	–165	–	dBm/Hz
	2010–2075 MHz (TDSCDMA)		–	–164.5	–	dBm/Hz
	2110–2170 MHz (WCDMA)		–	–164	–	dBm/Hz
	2305–2370 (LTE band 40)		–	–160	–	dBm/Hz
	2370–2400 (LTE band 40)		–	–163	–	dBm/Hz
	2400–2500 (WLAN 2G)		–	–160	–	dBm/Hz
	2496–2530 (LTE band 41)		–	–161.5	–	dBm/Hz
	2530–2560 (LTE band 41)		–	–161.5	–	dBm/Hz
	2570–2690 (LTE band 41)		–	–161	–	dBm/Hz
EVM Does Not Exceed						
TX power at the chip port for highest power level setting at 25°C and VBAT = 3.6V with spectral mask and EVM compliance	OFDM, BPSK	–8 dB	–	21.5	–	dBm
	OFDM, 64QAM	–25 dB	–	19	–	dBm
	MCS7	–27 dB	–	19	–	dBm
	MCS9	–32 dB	–	16	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
TX power control dynamic range	–		10	–	–	dB
Closed loop TX power variation at highest power level setting	Across full-temperature and voltage range. Applies across 10 to 20 dBm output power range.		–	–	±2.0	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Z_o = 50Ω		–	6	–	dB

1. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

15.7 General Spurious Emissions Specifications

This section provides the TX and RX spurious emissions specifications for both the WLAN 2.4 GHz and 5 GHz bands. The recommended spectrum analyzer settings for the spurious emissions specifications are provided in Table 38.

Table 38. Recommended Spectrum Analyzer Settings

Parameter	Setting
Resolution Bandwidth (RBW):	1 MHz
Video Bandwidth (VBW):	1 MHz
Sweep:	Auto
Span:	100 MHz
Detector:	Maximum Peak
Trace:	Maximum Hold
Modulation:	OFDM (Orthogonal Frequency-division Multiplexing)

15.7.1 Transmitter Spurious Emissions Specifications

The TX spurious emissions specifications in this subsection are based on the following definitions:

- AFE = VCO/16 for 2G channels
- AFE = VCO/18 for 5G 20 MHz channels
- AFE = VCO/9 for 5G 40 MHz channels
- AFE = VCO/6 for 5G 80 MHz channels
- LO = Channel frequency

2.4 GHz Band Spurious Emissions

20 MHz Channel Spacing

Note: Possible AFE combinations are as follows. The AFE=VCO/16 specifications for channel 2442 are listed in Table 39.

Table 39. 2.4 GHz Band, 20 MHz Channel Spacing TX Spurious Emissions Specifications[1]

Spurious Frequency	Power (dBm)	Frequency (Fch; MHz) Channel 2442	
		Typical (dBm)	Maximum (dBm)
HD2	21	–22.78	–
HD3	21	–19.54	–
HD4	21	–41.79	–
HD5	21	–61.78	–
VCO – LO	21	–55.13	–
VCO + LO	21	–63.40	–
VCO	21	–48.56	–
LO + AFE	21	–59.2	–
LO-AFE	21	–59.3	–
LO + AFE × 2	21	–68.2	–
LO – AFE × 2	21	–67.4	–
LO + XTAL × 2	21	–56.2	–
LO – XTAL × 2	21	–56.3	–
LO + XTAL × 4	21	–57.5	–
LO – XTAL × 4	21	–56.7	–
LO + XTAL × 8	21	–59.1	–
LO – XTAL × 8	21	–67.2	–

1. VCO = 1.5 × Fch, where Fch is the center frequency of the channel.

5 GHz Band Spurious Emissions

20 MHz Channel Spacing

Note: Possible AFE combinations are as follows. The AFE=VCO/18 specifications for channels 5180, 5500, and 5825 are listed in Table 40.

Table 40. 5 GHz Band, 20 MHz Channel Spacing TX Spurious Emissions Specifications

Spurious Frequency	Power (dBm)	CH5180[1]		CH5500[1]		CH5825[1]	
		Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)
HD2	19	–29.33	–	–32.56	–	–33.14	–
HD3	19	–39.71	–	–38.93	–	–39.87	–
VCO	19	–49.03	–	–48.35	–	–46.70	–
VCO × 2	19	–55.64	–	–60.40	–	–64.77	–
LO + VCO	19	–63.94	–	–62.80	–	–62.16	–
LO – VCO	19	–81.58	–	–72.56	–	–70.58	–
LO – AFE	19	–62.1	–	–63.3	–	–60.4	–
LO + AFE	19	–57.8	–	–59.6	–	–60.6	–
LO – XTAL × 4	19	–60.1	–	–60.1	–	–58.7	–
LO + XTAL × 4	19	–57.2	–	–57.4	–	–58.2	–
LO – XTAL × 6	19	–63.4	–	–59.3	–	–61.1	–
LO + XTAL × 6	19	–60.2	–	–58.9	–	–60.8	–
LO – XTAL × 8	19	–66.1	–	–67.3	–	–63.8	–
LO + XTAL × 8	19	–64.2	–	–63.8	–	–65.8	–
AFE × 12	19	–	–	–	–	–	–

1. VCO = (2/3) × Fch, where Fch is the center frequency of the channel.

40 MHz Channel Spacing

Note: Possible AFE combinations are as follows. The AFE=VCO/9 specifications for channels 5190, 5510, and 5795 are listed in Table 41.

Table 41. 5 GHz Band, 40 MHz Channel Spacing TX Spurious Emissions Specifications

Spurious Frequency	Power (dBm)	CH5190m[1]		CH5510m[1]		CH5795m[1]	
		Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)
HD2	19	–33.43	–	–35.53	–	–36.49	–
HD3	19	–41.81	–	–42.13	–	–42.33	–
VCO	19	–48.36	–	–47.65	–	–46.93	–
VCO × 2	19	–55.87	–	–59.26	–	–64.45	–
LO + VCO	19	–65.58	–	–64.96	–	–	–
LO – VCO	19	–	–	–	–	–	–
LO – AFE	19	–65.3	–	–67.2	–	–65.2	–
LO + AFE	19	–63.2	–	–64.3	–	–67.3	–
LO – XTAL × 4	19	–59.3	–	–59.7	–	–59.6	–
LO + XTAL × 4	19	–58.3	–	–57.4	–	–57.9	–
LO – XTAL × 6	19	–64.1	–	–63.4	–	–63.2	–
LO + XTAL × 6	19	–61.5	–	–59.4	–	–61.2	–
LO – XTAL × 8	19	–66.3	–	–67.1	–	–64.3	–
LO + XTAL × 8	19	–63.8	–	–64.7	–	–61.2	–
AFE × 12	19	–65.2	–	–66.3	–	–65.4	–

1. VCO = (2/3) × Fch, where Fch is the center frequency of the channel.

80 MHz Channel Spacing

Note: Possible AFE combinations are as follows. The AFE=VCO/6 specifications for channels 5210, 5530, and 5775 are listed in Table 42.

Table 42. 5 GHz Band, 80 MHz Channel Spacing TX Spurious Emissions Specifications

Spurious Frequency	Power (dBm)	CH5210q[1]		CH5530q[1]		CH5775q[1]	
		Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)	Typ. (dBm)	Max. (dBm)
HD2	19	–36.28	–	–39.59	–	–41.02	–
HD3	19	–45.00	–	–44.82	–	–46.10	–
VCO	19	–48.00	–	–47.34	–	–46.01	–
VCO × 2	19	–57.04	–	–62.82	–	–66.84	–
LO + VCO	19	–66.66	–	–66.11	–	–66.40	–
LO – VCO	19	–	–	–	–	–	–
LO – AFE	19	–68.5	–	–67.8	–	–66.9	–
LO + AFE	19	–63.8	–	–66.3	–	–68.6	–
LO – XTAL × 4	19	–	–	–	–	–	–
LO + XTAL × 4	19	–	–	–	–	–	–
LO – XTAL × 6	19	–	–	–	–	–	–
LO + XTAL × 6	19	–	–	–	–	–	–
LO – XTAL × 8	19	–	–	–	–	–	–
LO + XTAL × 8	19	–	–	–	–	–	–
AFE × 12	19	–	–	–	–	–	–

1. VCO = (2/3) × Fch, where Fch is the center frequency of the channel.

15.7.2 Receiver Spurious Emissions Specifications

Table 43. 2G and 5G General Receiver Spurious Emissions

Band	Frequency Range	Typical	Maximum	Unit
2G	2.4 GHz < f < 2.5 GHz	–92	–	dBm
	3.6 GHz < f < 3.8 GHz	–75.16	–	dBm
5G	5150 MHz < f < 5850 MHz	–70.4	–	dBm
	3.45 GHz < f < 3.9 GHz	–59.2	–	dBm

16. Internal Regulator Electrical Specifications

16.1 Core Buck Switching Regulator

Note: Values in this data sheet are design goals and are subject to change based on device characterization results.
Note: Functional operation is not guaranteed outside of the specification limits provided in this section.

Table 44. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Unit
Input supply voltage (DC)	DC voltage range inclusive of disturbances.	3.0	3.6	5.25[1]6.0	V
PWM mode switching frequency	CCM, Load > 100 mA VBAT = 3.6V	–	4	–	MHz
PWM output current	–	–	–	600	mA
Output current limit	–	–	1400	–	mA
Output voltage range	Programmable, 30 mV steps. Default = 1.35V	1.2	1.35	1.5	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM mode.	–4	–	4	%
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. Max. Ripple based on VBAT = 3.6V, Vout = 1.35V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH, Cap + Board total-ESR < 20 mΩ, C_{out} > 1.9 µF, ESL<200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load	78	86	–	%
PFM mode efficiency	10 mA load current	70	80	–	%
Start-up time from power down	VIO already ON and steady. Time from REG_ON rising edge to CLDO reaching 1.2V.	–	400	500	µs
External inductor	0806 size, 2.2 µH, DCR=0.11Ω, ACR=1.18Ω @ 4 MHz	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, 4.7 µF ±20%, 6.3V	2.0	4.7	10[2]	µF
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0603, ESR < 30 mΩ at 4 MHz, ±4.7uF ±20%, 6.3V	0.67[2]	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

1. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
2. Total capacitance includes those connected at the far end of the active load.

16.2 3.3V LDO (LDO3P3)

Table 45. LDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = V_o + 0.2V = 3.5V dropout voltage requirement must be met under maximum load for performance specifications.	3.0	3.6	5.25[1] 6.0	V
Output current	–	0.001	–	450	mA
Nominal output voltage, V_o	Default = 3.3V	–	3.3	–	V
Dropout voltage	At max. load.	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	–	100	µA
Line regulation	V_{in} from (V_o + 0.2V) to 5.25V, max. load	–	–	3.5	mV/V
Load regulation	load from 1 mA to 450 mA	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 3.3V, C_o = 4.7 µF, Max. load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	160	250	µs
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5 mΩ–240 mΩ), ± 10%, 10V	1.0[2]	4.7	10	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) Ceramic, X5R, 0402, (ESR: 30m-200 mΩ), ± 10%, 10V. Not needed if sharing VBAT capacitor 4.7 µF with SR_VDDBATP5V.	–	4.7	–	µF

1. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
2. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

16.3 2.5V LDO (BTLDO2P5)

Table 46. BTLDO2P5 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage	Min. = 2.5V + 0.2V = 2.7V. Dropout voltage requirement must be met under maximum load for performance specifications.	3.0	3.6	5.25[1] 6.0	V
Nominal output voltage	Default = 2.5V.	–	2.5	–	V
Output voltage programmability	Range	2.2	2.5	2.8	V
	Accuracy at any step (including line/load regulation), load > 0.1 mA.	–5	–	5	%
Dropout voltage	At maximum load.	–	–	200	mV
Output current	–	0.1	–	70	mA
Quiescent current	No load.	–	8	16	µA
	Maximum load at 70 mA.	–	660	700	µA
Leakage current	Power-down mode.	–	1.5	5	µA
Line regulation	V_{in} from (V_o + 0.2V) to 5.25V, maximum load.	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 70 mA, V_{in} = 3.6V.	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2V, V_o = 2.5V, C_o = 2.2 µF, maximum load, 100 Hz to 100 kHz.	20	–	–	dB
LDO turn-on time	Chip already powered up.	–	–	150	µs
In-rush current	$V_{in} = V_o$ + 0.15V to 5.25V, C_o = 2.2 µF, No load.	–	–	250	mA
External output capacitor, C_o	Ceramic, X5R, 0402, (ESR: 5m–240 mΩ), ±10%, 10V	0.7[2]	2.2	2.64	µF
External input capacitor	For SR_VDDBATA5V pin (shared with Bandgap) ceramic, X5R, 0402, (ESR: 30–200 mΩ), ±10%, 10V. Not needed if sharing VBAT 4.7 µF capacitor with SR_VDDBATP5V.	–	4.7	–	µF

1. The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.
2. The minimum value refers to the residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

16.4 CLDO

Table 47. CLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, V_{in}	Min. = 1.2 + 0.15V = 1.35V dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output current	–	0.2	–	200	mA
Output voltage, V_o	Programmable in 10 mV steps. Default = 1.2.V	0.95	1.2	1.26	V
Dropout voltage	At max. load	–	–	150	mV
Output voltage DC accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	13	–	µA
	200 mA load	–	1.24	–	mA
Line Regulation	V_{in} from (V_o + 0.15V) to 1.5V, maximum load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 300 mA	–	0.02	0.05	mV/mA
Leakage Current	Power down	–	5	20	µA
	Bypass mode	–	1	3	µA
PSRR	@1 kHz, Vin ≥ 1.35V, C_o = 4.7 µF	20	–	–	dB
Start-up Time of PMU	VIO up and steady. Time from the REG_ON rising edge to the CLDO reaching 1.2V.	–	–	700	µs
LDO Turn-on Time	LDO turn-on time when rest of the chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR: 5 mΩ–240 mΩ	1.1[1]	2.2	–	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

1. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

16.5 LNLDO

Table 48. LNLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. $V_{IN} = V_O + 0.15V = 1.35V$ (where V_O = 1.2V)dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output Current	–	0.1	–	150	mA
Output Voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout Voltage	At maximum load	–	–	150	mV
Output Voltage DC Accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	44	–	µA
	Max. load	–	970	990	µA
Line Regulation	V_{in} from (V_o + 0.1V) to 1.5V, 150 mA load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 150 mA	–	0.02	0.05	mV/mA
Leakage Current	Power-down	–	–	10	µA
Output Noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO Turn-on Time	LDO turn-on time when rest of chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.5[1]	2.2	4.7	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	2.2	µF

1. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

16.6 PCIe LDO

Note: The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

Table 49. PCIe LDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. $V_{IN} = V_O + 0.15V = 1.35V$ (where $V_O = 1.2V$)dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Output Current	Peak load=80 mA. Average load=35 mA	0.1	–	55	mA
Output Voltage, V_o	Programmable in 25 mV steps. Default = 1.2V	1.1	1.2	1.275	V
Dropout Voltage	At maximum load	–	–	150	mV
Output Voltage DC Accuracy	Includes line/load regulation	–4	–	+4	%
Quiescent current	No load	–	10	12	µA
	55 mA load	–	550	570	µA
Line Regulation	V_{IN} from (V_O + 0.1V) to 1.5V, 150 mA load	–	–	5	mV/V
Load Regulation	Load from 1 mA to 150 mA	–	0.02	0.05	mV/mA
Leakage Current	Power-down	–	5	20	µA
	Bypass mode	–	0.02	1.5	µA
Output Noise	@30 kHz, 60–150 mA load C_o = 2.2 µF @100 kHz, 60–150 mA load C_o = 2.2 µF	–	–	60 35	nV/rt Hz nV/rt Hz
PSRR	@ 1kHz, Input > 1.35V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO Turn-on Time	LDO turn-on time when balance of chip is up	–	140	180	µs
External Output Capacitor, C_o	Total ESR (trace/capacitor): 5 mΩ–240 mΩ	0.27[1]	0.47	–	µF
External Input Capacitor	Only use an external input capacitor at the VDD_LDO pin if it is not supplied from CBUCK output. Total ESR (trace/capacitor): 30 mΩ–200 mΩ	–	1	2.2	µF

1. Minimum capacitor value refers to the residual capacitor value after taking into account the part-to-part tolerance, DC-bias, temperature, and aging.

17. System Power Consumption

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.
Note: Unless otherwise stated, these values apply for the conditions specified in Table 28: "Recommended Operating Conditions and DC Characteristics".

17.1 WLAN Current Consumption

The tables in this subsection show the typical, total current consumed by the CYW43455. All values shown are with the Bluetooth core in reset mode with Bluetooth off.

17.1.1 2.4 GHz Mode

Table 50. 2.4 GHz Mode WLAN Power Consumption

Mode	V_{BAT} = 3.6V, V_{DDIO} = 1.8V, T_A25°C	
	$V_{BAT, mA}$	$V_{IO, uA}$ [1]
Sleep Modes		
Radio off [2]	0.006	5
Sleep [3]	0.020	200
IEEE Power Save: DTIM = 1, single RX [4]	1.25	200
IEEE Power Save: DTIM = 3, single RX	0.45	200
Active RX Modes		
Continuous RX mode: MCS7, HT20, 1SS [5, 6]	55	60
CRS: HT20 [7]	50	60
Active TX Modes – Internal PA		
Continuous TX mode: 1 Mbps @ 21.5 dBm [8]	400	60
Continuous TX mode: MCS7, HT20, 1SS, 1 TX @ 19 dBm [8]	350	60

1. VIO is specified with all pins idle (not switching) and not driving any loads.
2. WL_REG_ON and BT_REG_ON are both low. All supplies are present.
3. Idle, not associated, or inter-beacon.
4. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3× DTIM intervals.
5. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
6. Measured using packet engine test mode.
7. Carrier sense (CCA) when no carrier present.
8. Duty cycle is 100%.

17.1.2 5 GHz Mode

Table 51. 5 GHz Mode WLAN Power Consumption

Mode	V_{BAT} = 3.6V, V_{DDIO} = 1.8V, T_A25°C	
	V_{BAT} , mA	V_{IO}, uA [1]
Sleep Modes		
Radio off [2]	0.006	5
Sleep [3]	0.025	200
IEEE Power Save: DTIM = 1, single RX [4]	1.1	200
IEEE Power Save: DTIM = 3, single RX	0.4	200
Active RX Modes		
Continuous RX mode: MCS7, HT20, 1SS [5, 6]	74	60
Continuous RX mode: MCS7, HT40, 1SS [5, 6]	82	60
Continuous RX mode: MCS9, HT40, 1SS [5, 6]	86	60
Continuous RX mode: MCS9, HT80, 1SS [5, 6]	117	60
CRS: HT20 [7]	70	60
CRS: HT40 [7]	79	60
CRS: HT80 [7]	100	60
Active TX Modes – Internal PA		
Continuous TX mode: MCS7, HT20, 1SS, 1 TX @ 19 dBm [8]	330	60
Continuous TX mode: MCS7, HT40, 1SS, 1 TX @ 19 dBm [8]	345	60
Continuous TX mode: MCS9, HT40, 1SS, 1 TX @ 16 dBm [8]	320	60
Continuous TX mode: MCS9, HT80, 1SS, 1 TX @ 16 dBm [8]	340	60

1. V_{IO} is specified with all pins idle (not switching) and not driving any loads.
2. WL_REG_ON and BT_REG_ON are both low. All supplies present.
3. Idle, not associated, or inter-beacon.
4. Beacon Interval = 102.4 ms. Beacon duration = 1ms @ 1Mbps. Average current over 3x DTIM intervals.
5. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.
6. Measured using packet engine test mode.
7. Carrier sense (CCA) when no carrier present.
8. Duty cycle is 100%.

17.2 Bluetooth Current Consumption

The Bluetooth and BLE current consumption measurements are shown in Table 52.

Note: The WLAN core is in reset (WLAN_REG_ON = low) for all measurements provided in Table 52.
Note: The BT current consumption numbers are measured based on GFSK TX output power = 10 dBm.

Table 52. Bluetooth and BLE Current Consumption

Operating Mode	VBAT	VDDIO	Units
Sleep	6	133	µA
Standard 1.28s Inquiry Scan	165	130	µA
500 ms Sniff Master	168	127	µA
DM1/DH1 Master	25.8	0.057	mA
DM3/DH3 Master	32.1	0.071	mA
DM5/DH5 Master	33.2	0.074	mA
3DH5/3DH1 Master	27.7	0.143	mA
SCO HV3 Master	12.2	0.113	mA
BLE Scan[1]	179	132	µA
BLE Adv—Unconnectable 1.00 sec	73	131	µA
BLE Connected 1 sec	62	130	µA

1. No devices present. A 1.28 second interval with a scan window of 11.25 ms.

18. Interface Timing and AC Characteristics

18.1 SDIO Timing

18.1.1 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 31 and Table 53.

Figure 31. SDIO Bus Timing (Default Mode)

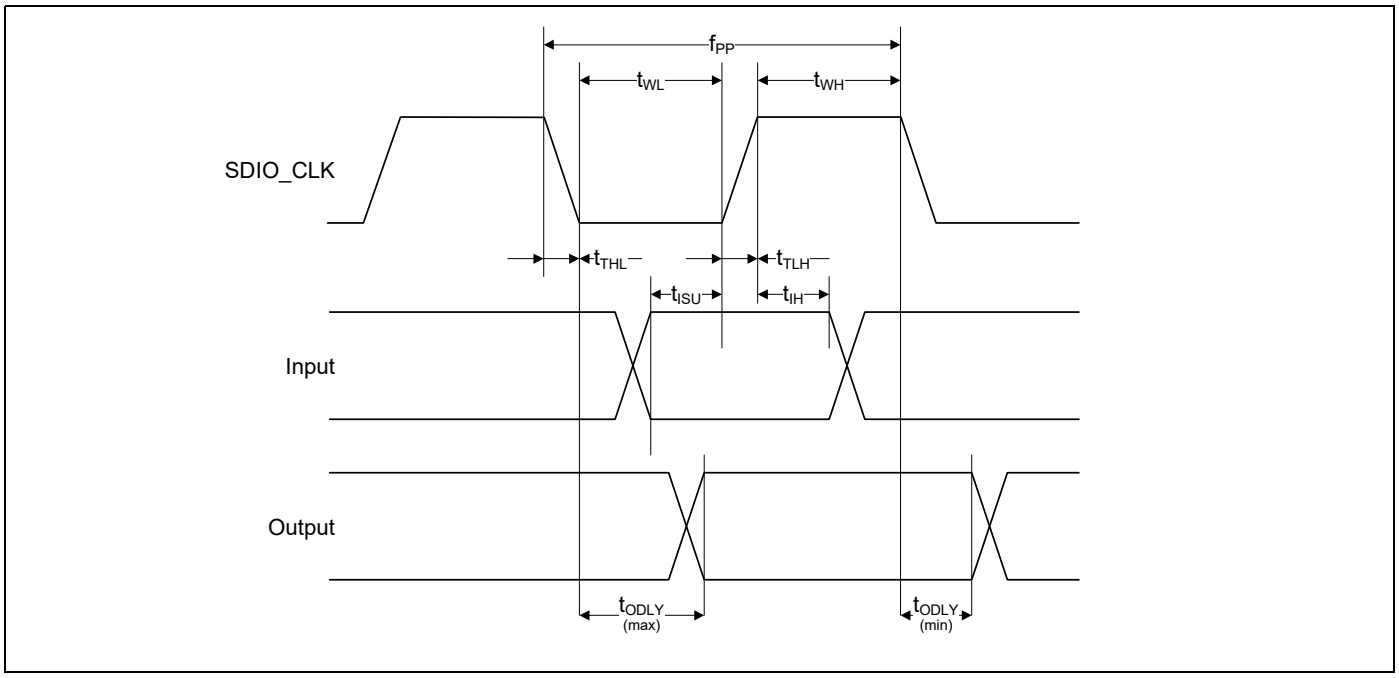


Table 53. SDIO Bus Timing[1] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

1. Timing is based on CL ≤ 40 pF load on CMD and Data.
2. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

18.2 SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 32 and Table 54.

Figure 32. SDIO Bus Timing (High-Speed Mode)

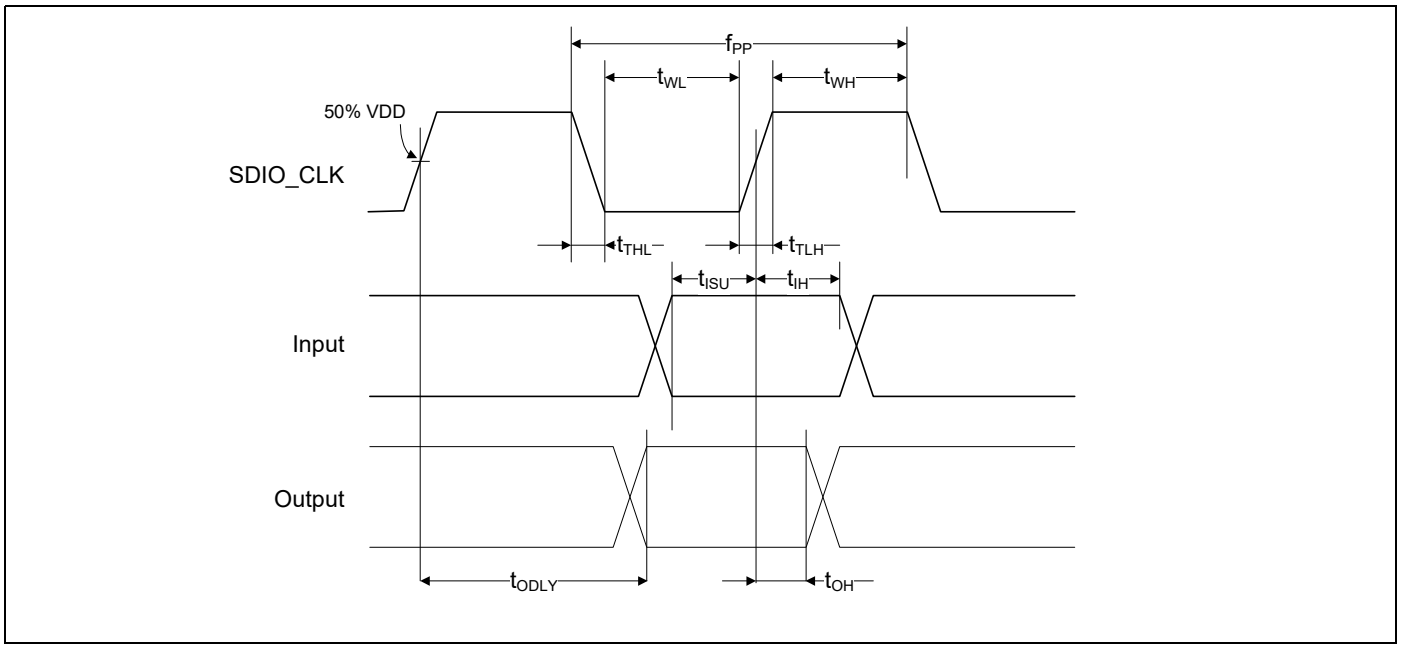


Table 54. SDIO Bus Timing[1] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)	–	–	–	–	–
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)	–	–	–	–	–
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

1. Timing is based on CL ≤ 40 pF load on CMD and Data.
2. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

18.2.1 SDIO Bus Timing Specifications in SDR Modes

Clock Timing

Figure 33. SDIO Clock Timing (SDR Modes)

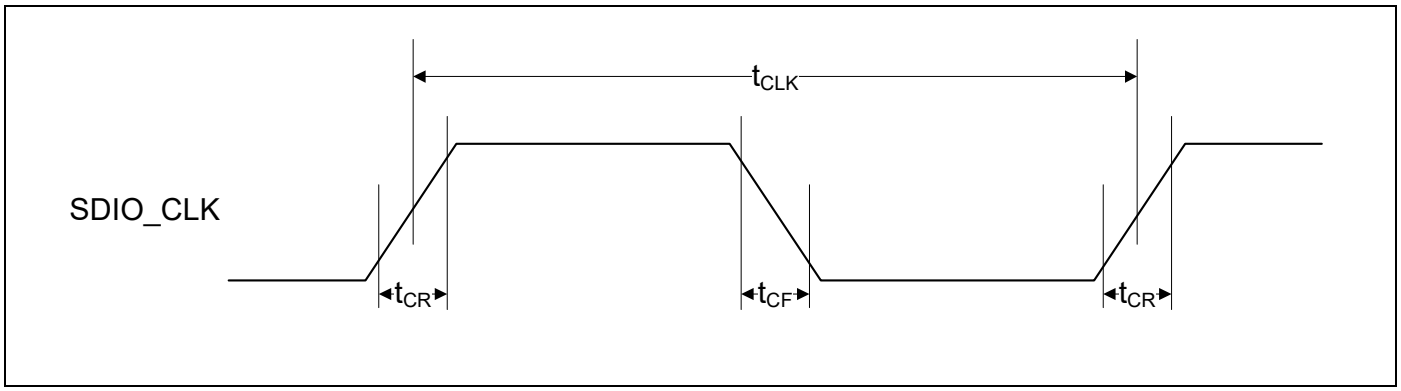


Table 55. SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @ 100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @ 208 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	30	70	%	–

Card Input Timing

Figure 34. SDIO Bus Input Timing (SDR Modes)

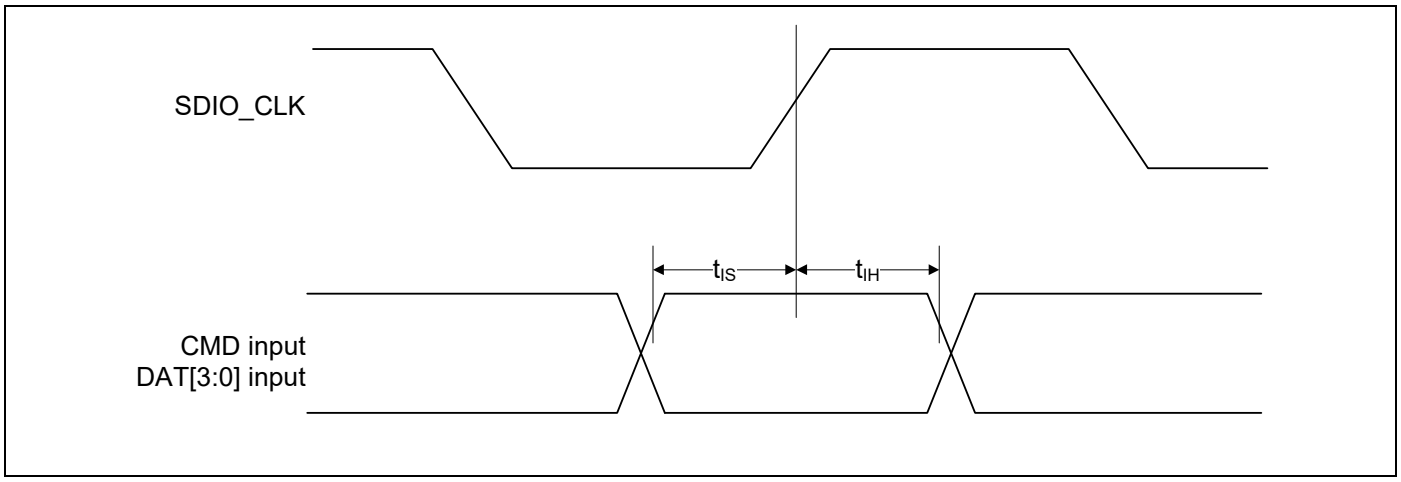


Table 56. SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

Card Output Timing

Figure 35. SDIO Bus Output Timing (SDR Modes up to 100 MHz)

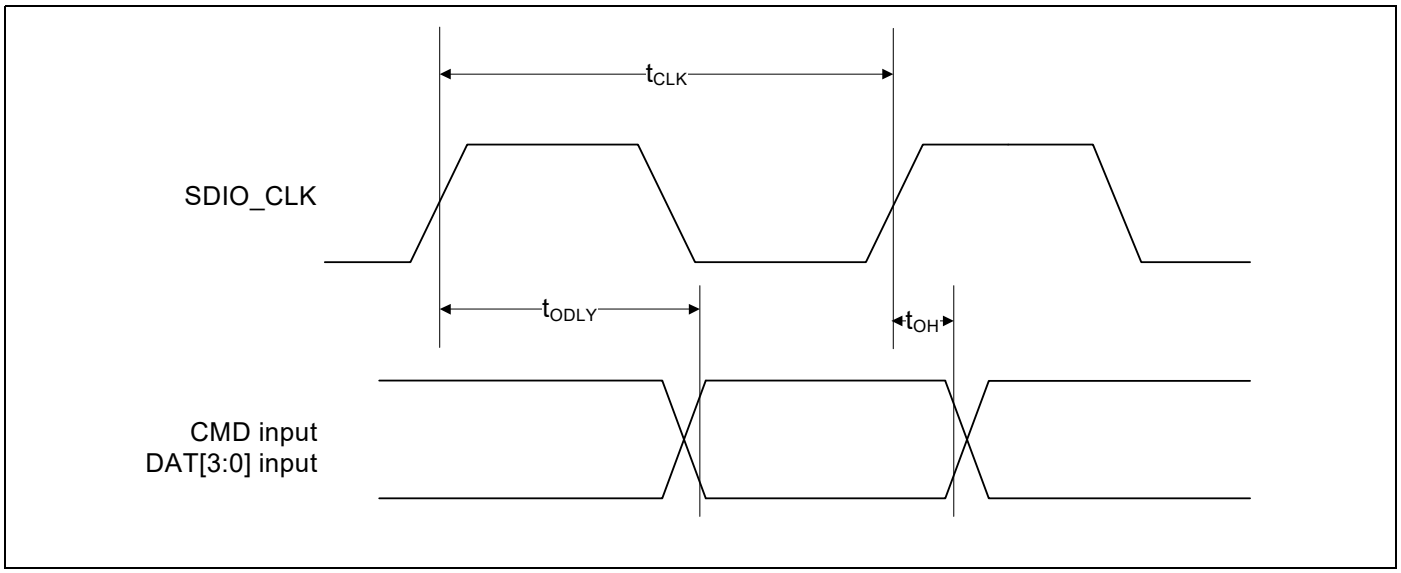


Table 57. SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK} ≥ 10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L= 15 pF

Figure 36. SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

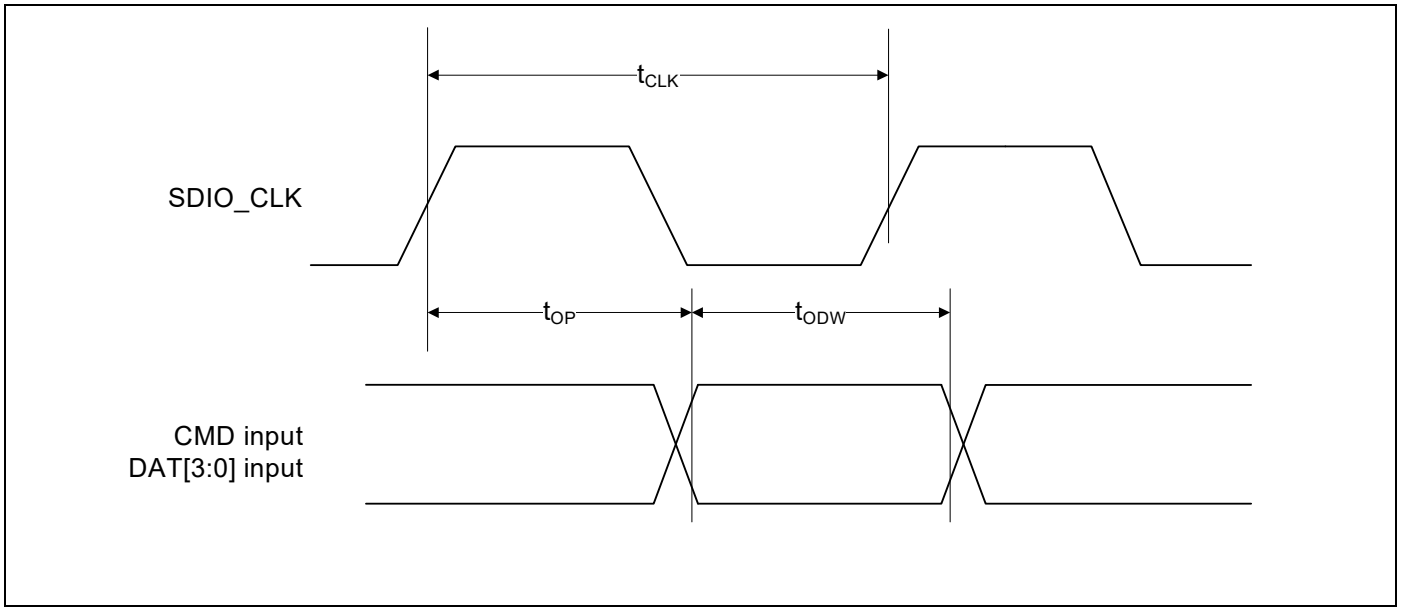
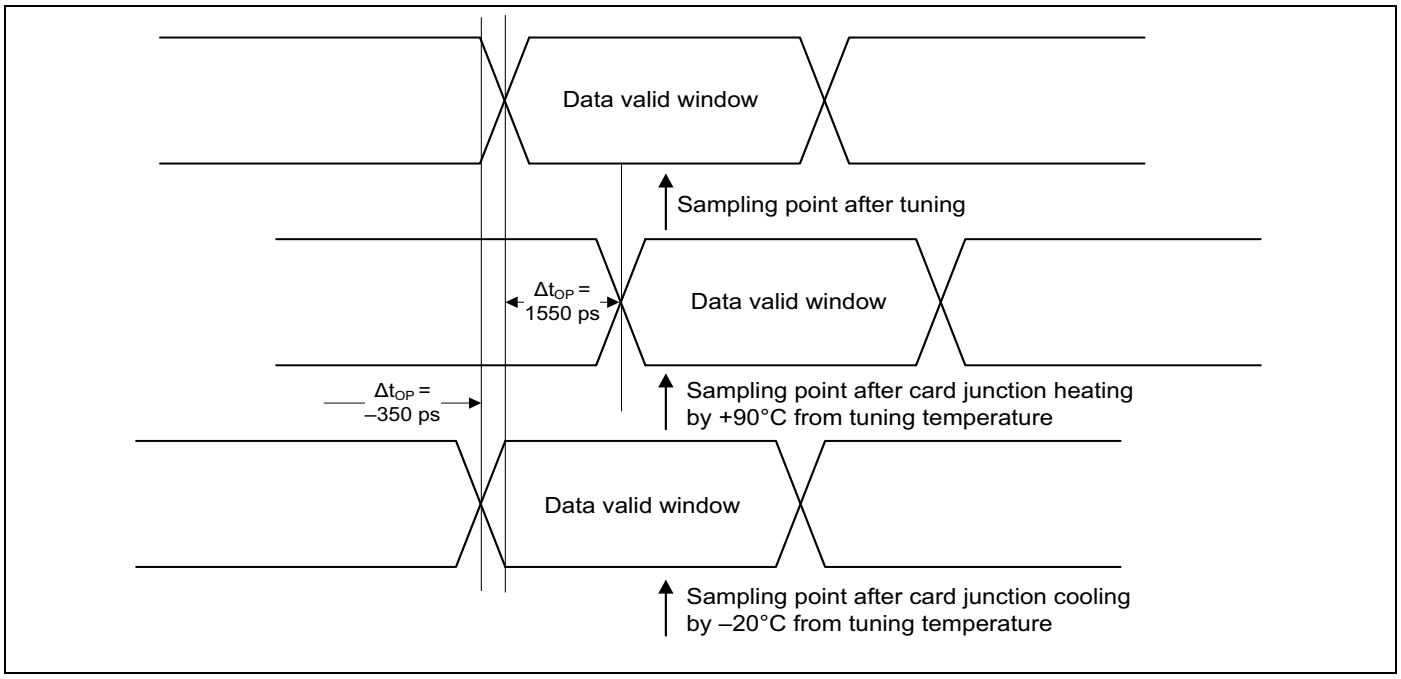


Table 58. SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW} = 2.88 ns @ 208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90°C during operation.
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20°C during operation.
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20°C to +125°C during operation.

Figure 37. Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)



18.2.2 SDIO Bus Timing Specifications in DDR50 Mode

Figure 38. SDIO Clock Timing (DDR50 Mode)

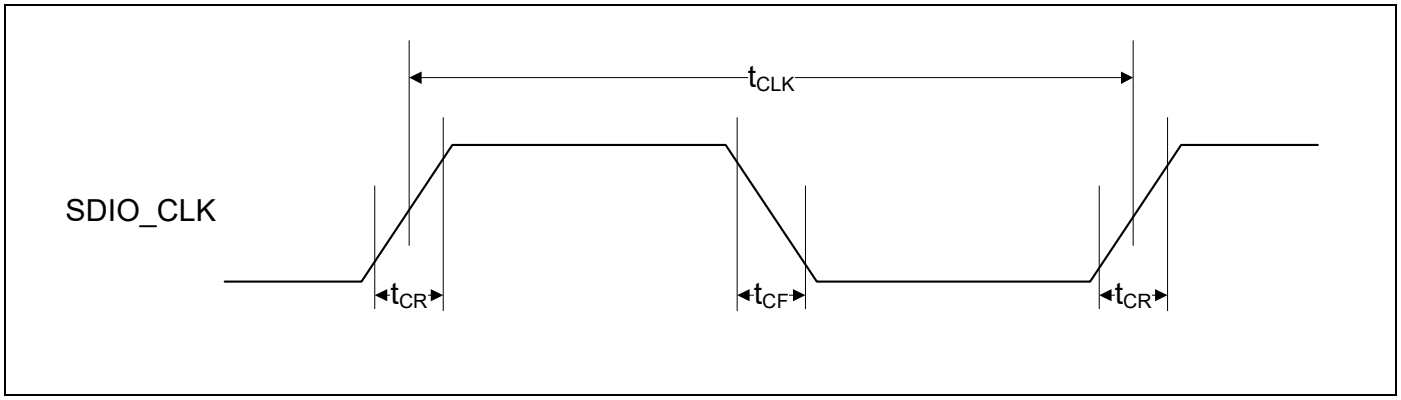


Table 59. SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	45	55	%	–

Data Timing

Figure 39. SDIO Data Timing (DDR50 Mode)

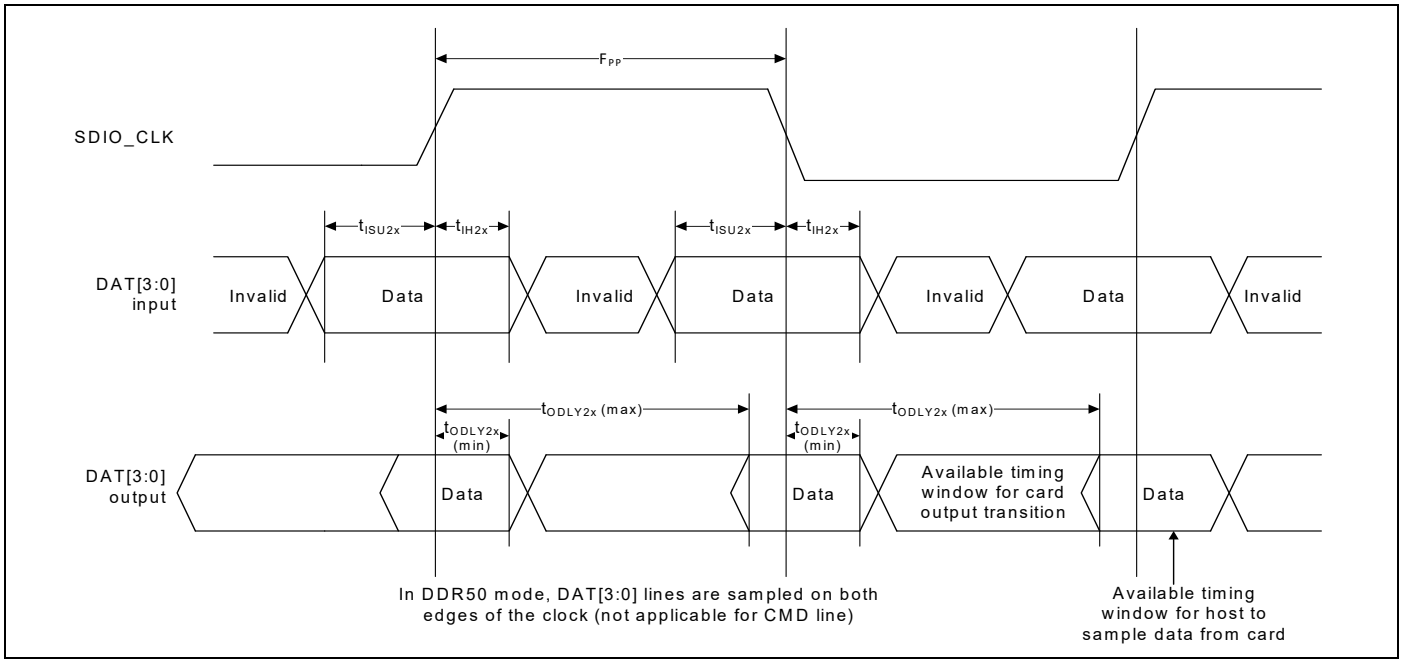


Table 60. SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

18.3 PCI Express Interface Parameters

Note: The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

Table 61. PCI Express Interface Parameters

Parameter	Symbol	Comments	Minimum	Typical	Maximum	Unit
General						
Baud rate	BPS	–	–	5	–	Gbaud
Reference clock amplitude	Vref	LVPECL, AC coupled	1	–	–	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	–	–	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	–	–	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	–	–	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	–	–	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	–	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	–	–	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20	mV

Table 61. PCI Express Interface Parameters (continued)

Parameter	Symbol	Comments	Minimum	Typical	Maximum	Unit
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV
Absolute delta of DC common-model voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	–	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min.) for 0.05: 1.25 GHz 8 (min.) for 1.25: 2.5 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI

18.4 JTAG Timing

Table 62. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
JTAG_TRST	250 ns	–	–	–	–

18.5 SWD Timing

The probe outputs data to SWDIO on the falling edge of SWDCLK and captures data from SWDIO on the rising edge of SWDCLK. The target outputs data to SWDIO on the rising edge of SWDCLK and captures data from SWDIO on the rising edge of SWDCLK. SWD timing is defined through the combination of Figure 40 and Table 63.

Figure 40. SWD Read and Write Timing

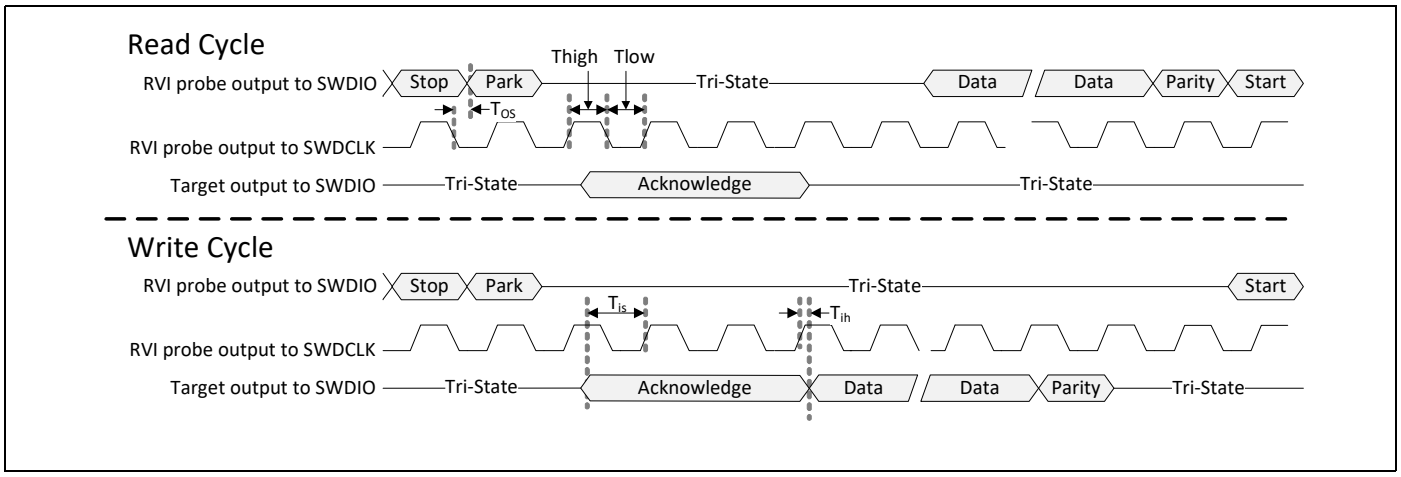


Table 63. SWD Read and Write Timing Parameters

Parameter	Description	Min.	Max.	Units
Tcyc	SWDCLK cycle time	125	–	ns
Thigh	SWDCLK high period	50	–	ns
Tlow	SWDCLK low period	50	–	ns
T_{os}	SWDIO output skew to the falling edge of SWDCLK	–5	5	ns
T_{is}	Input setup time between SWDIO and the rising edge of SWDCLK	20	–	ns
T_{ih}	Input hold time between SWDIO and the rising edge of SWDCLK	0	100	ns

19. Power-Up Sequence and Timing

19.1 Sequencing of Reset and Regulator Control Signals

The CYW43455 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 41, Figure 42, and Figure 43 and Figure 44). The timing values indicated are minimum required values; longer delays are also acceptable.

19.1.1 Description of Control Signals

- **WL_REG_ON:** Used by the PMU to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW43455 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON**: Used by the PMU (OR-gated with WL_REG_ON) to power-up the internal CYW43455 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

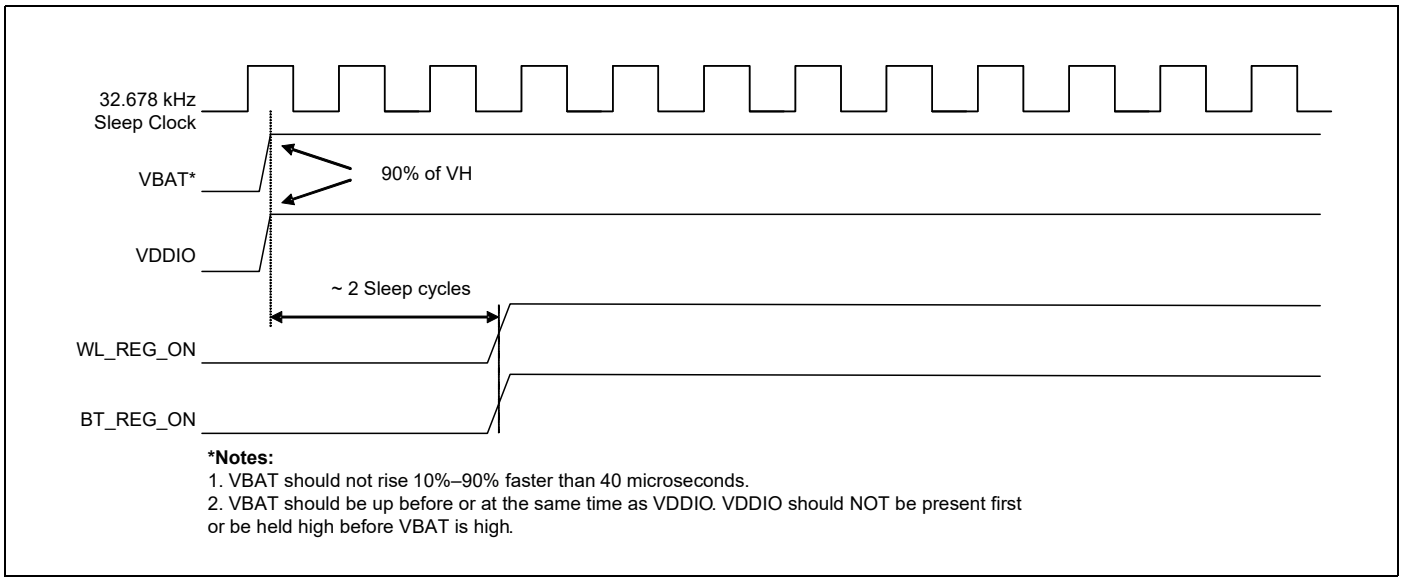
Note: For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10 ms time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

Note: The CYW43455 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating PCIe[7] accesses.

Note: VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

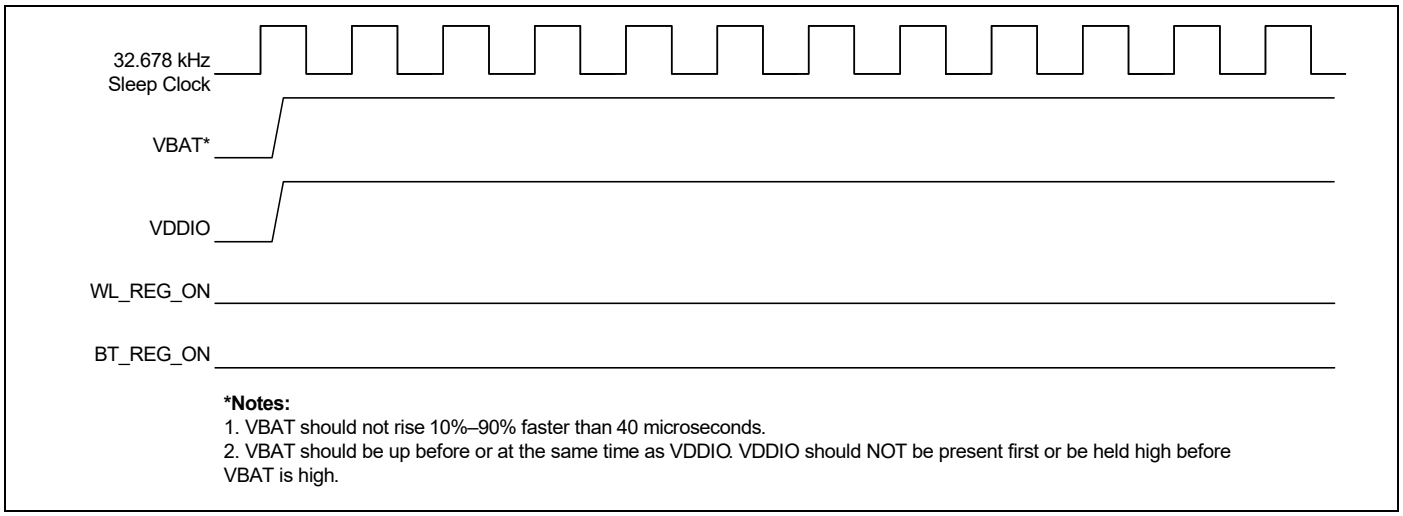
19.1.2 Control Signal Timing Diagrams

Figure 41. WLAN = ON, Bluetooth = ON



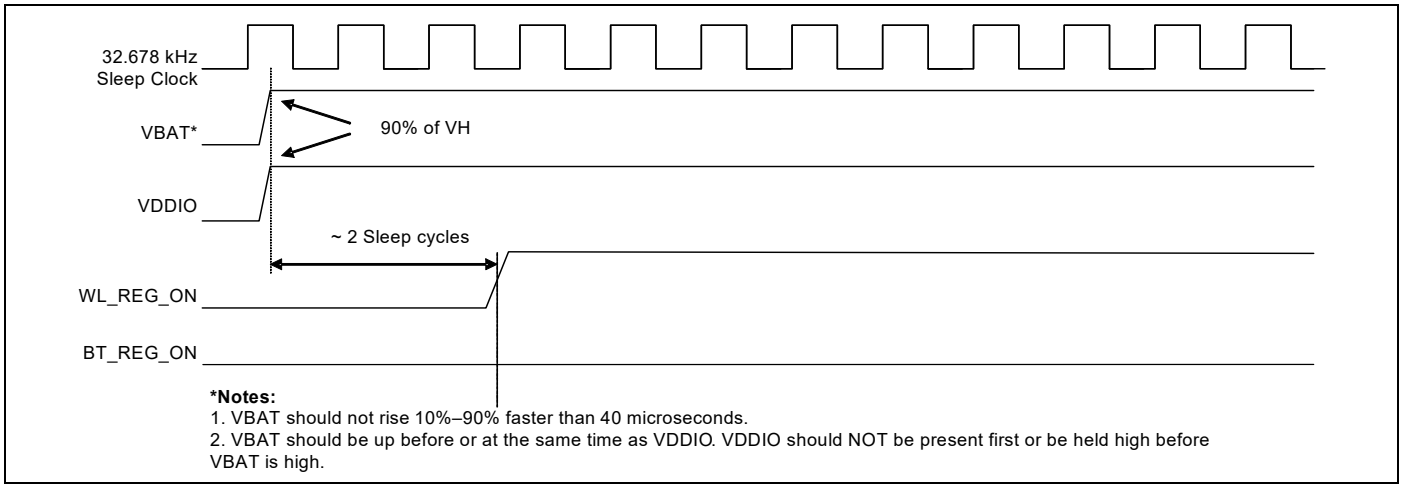
7. The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface.

Figure 42. WLAN = OFF, Bluetooth = OFF



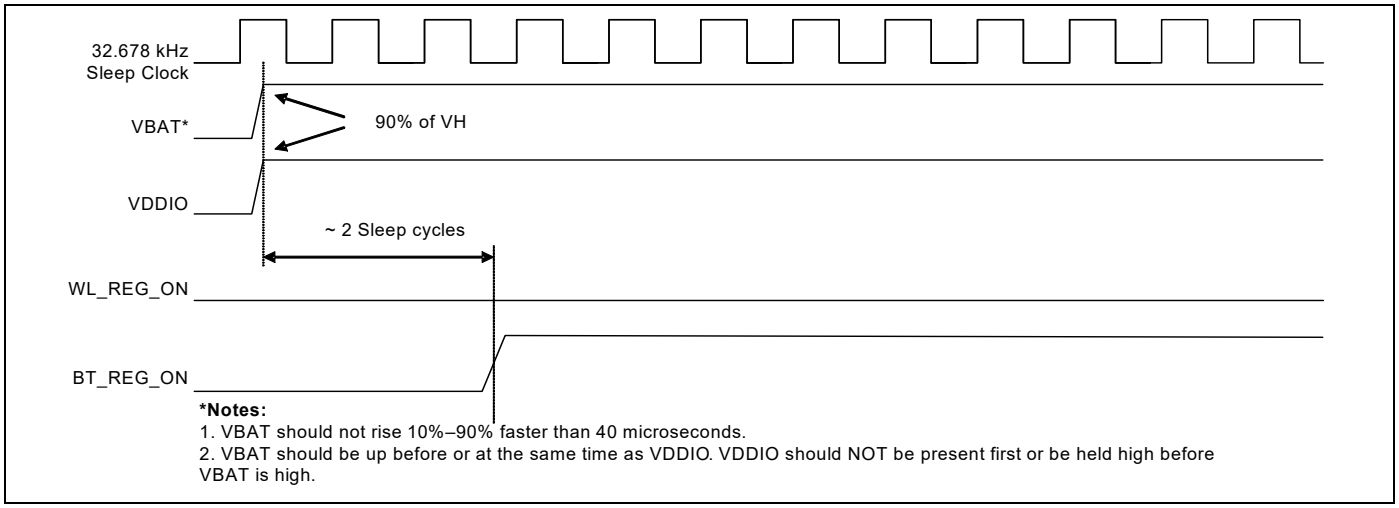
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 43. WLAN = ON, Bluetooth = OFF



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 44. WLAN = OFF, Bluetooth = ON



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

20. Package Information

20.1 Package Thermal Characteristics

Table 64. Package Thermal Characteristics[1]

Characteristic	WLBGA
θ_{JA} (°C/W) (value in still air)	38.73
θ_{JB} (°C/W)	1.97
θ_{JC} (°C/W)	3.16
Ψ_{JT} (°C/W)	9.3
Ψ_{JB} (°C/W)	16.21
Maximum Junction Temperature T_j (°C)	123.6
Maximum Power Dissipation (W)	1.38

1. No heat sink, TA = 70°C. This is an estimate, based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm × 101.6 mm × 1.6 mm) and P = 1.119W continuous dissipation.

20.2 Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

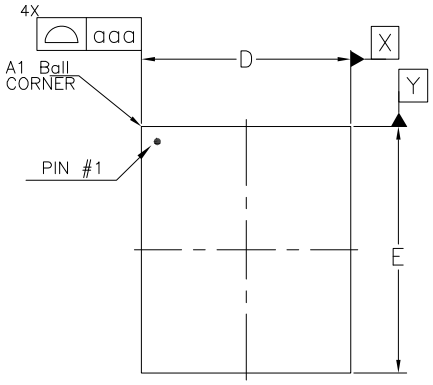
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

20.3 Environmental Characteristics

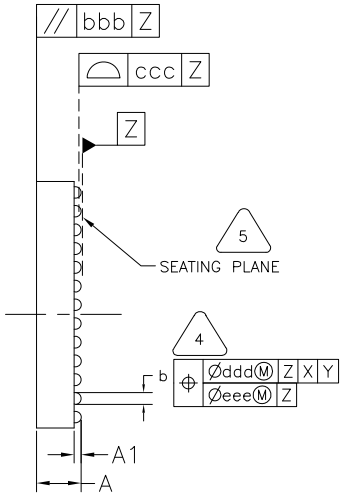
For environmental characteristics data, see Table 26.

21. Mechanical Information

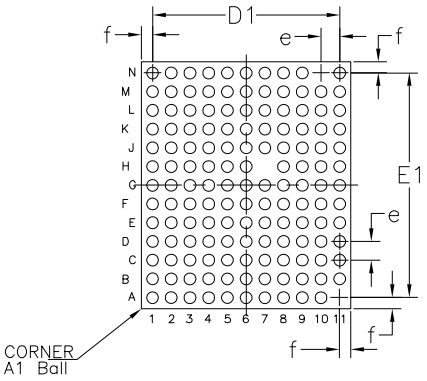
Figure 45. 140-Ball WLBGA Package Mechanical Information



TOP VIEW



SIDE VIEW



BOTTOM VIEW
(140 SOLDER BALLS)

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	0.55	0.60
A1	0.160	0.190	0.220
D	4.43	4.47	4.51
D1		4.00 REF.	
E	5.23	5.27	5.31
E1		4.80 REF.	
b	0.20	0.25	0.30
e		0.40 BSC	
f		0.235 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD01839 Rev: 000

6. REFER TO BROADCOM APPLICATION NOTE "WAFER-LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

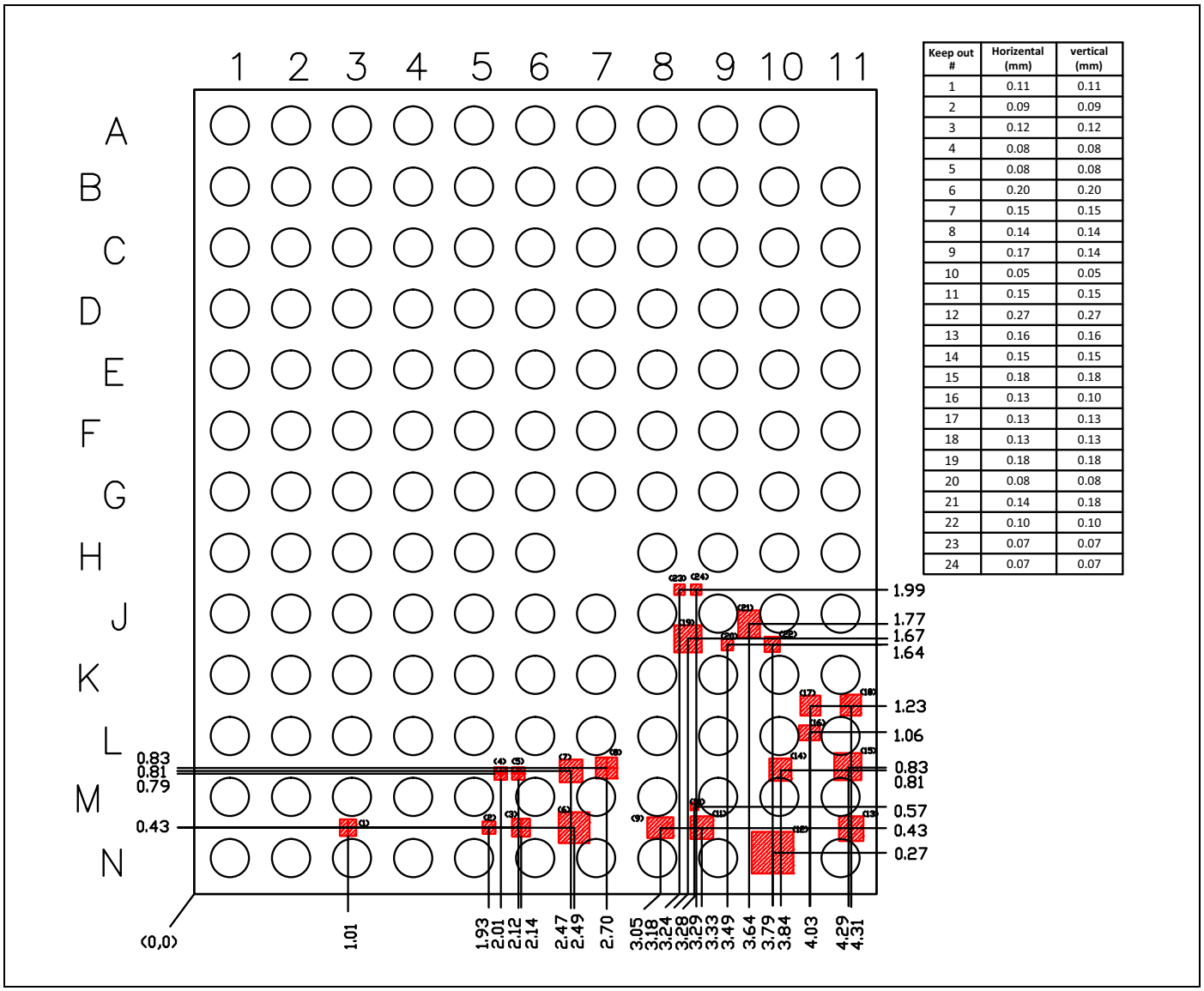
3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 46. 140-Balls WLBGA Keep-out Areas for PCB Layout—Top View with Balls Facing Down



Keep out #	Horizental (mm)	vertical (mm)
1	0.11	0.11
2	0.09	0.09
3	0.12	0.12
4	0.08	0.08
5	0.08	0.08
6	0.20	0.20
7	0.15	0.15
8	0.14	0.14
9	0.17	0.14
10	0.05	0.05
11	0.15	0.15
12	0.27	0.27
13	0.16	0.16
14	0.15	0.15
15	0.18	0.18
16	0.13	0.10
17	0.13	0.13
18	0.13	0.13
19	0.18	0.18
20	0.08	0.08
21	0.14	0.18
22	0.10	0.10
23	0.07	0.07
24	0.07	0.07

Note: No top-layer metal is allowed in keep-out areas.

Note: A DXF file for the WLBGA keep-out area is available for importation into a layout program. Contact Cypress for more information.

22. Ordering Information

Table 65. Part Ordering Information

Part Number	Package	Description	Operating Ambient Temperature
CYW43455XKUBG	140-ball WLBGA (4.47 mm × 5.27 mm, 0.4 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN+ BT 4.1	–30°C to +85°C

23. Additional Information

23.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

23.2 References

The references in this section may be used in conjunction with this document.

Note: Cypress provides customer access to technical documentation and software through its Customer Support Portal and Downloads & Support site (see IoT Resources).

For Cypress documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Bluetooth MWS Coexistence 2-wire Transport Interface Specification	–	www.bluetooth.com
PCI Bus Local Bus Specification, Revision 2.3	–	www.pcisig.com
PCIe Base Specification Version 1.1	–	www.pcisig.com

23.3 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (https://community.cypress.com/)

Document History Page

Document Title: CYW43455 Single-Chip 5G WiFi IEEE 802.11n/ac MAC/Baseband/ Radio with Integrated Bluetooth 5.0 Document Number: 002-15051				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	10/27/2014	43455-DS100-R Initial release.
*A	–	–	11/06/2014	43455-DS101-R See the pertinent document for the revision history.
*B	–	–	11/20/2014	43455-DS102-R See the pertinent document for the revision history.
*C	–	–	02/04/2015	43455-DS103-R See the pertinent document for the revision history.
*D	–	–	03/31/2015	43455-DS104-R See the pertinent document for the revision history.
*E	–	–	04/06/2015	43455-DS105-R See the pertinent document for the revision history.
*F	–	–	07/09/2015	43455-DS106-R See the pertinent document for the revision history.
*G	–	–	07/29/2015	43455-DS107-R See the pertinent document for the revision history.
*H	–	–	09/25/2015	43455-DS108-R See the pertinent document for the revision history.
*I	–	–	11/05/2015	43455-DS109-R • Table 35. WLAN 2.4 GHz Transmitter Performance Specifications. • Table 37. WLAN 5 GHz Transmitter Performance Specifications. • Table 51. 5 GHz Mode WLAN Power Consumption.
*J	–	–	01/04/2016	43455-DS110-R Updated: • Table 52. Bluetooth and BLE Current Consumption
*K	5450777	UTSV	10/5/2016	43455-DS111-R Updated: • Table 18. WLBGA Pin List by Pin Number. • Table 19. WLBGA Pin List by Pin Name. • Table 20. Signal Descriptions. Updated in Cypress template. Added Cypress Part Numbering Scheme.
*L	5675342	UTSV	03/28/2016	Updated with new logo. FM related sections are removed from this document.
*M	5770411	TLAU	05/22/2017	Updated Title Bluetooth 4.1 to 4.2 throughout the Datasheet. Added: LE Data Packet Length Extension LE Secure Connections to “Bluetooth 4.2 Features” on page 20. Changed Table 20: VDDIO Description to VDDIO can be 1.8V and 3.3V.
*N	5947698	UTSV	11/02/2017	Removed the Empty box in the Figure 2. Updated contents in the “External 32.768 kHz Low-Power Oscillator” on page 15. Replaced “LPO/Ext LPO/RCAL” to “Ext LPO/RCAL” in the Figure 27. Updated Table 22 on page 64.

Document Title: CYW43455 Single-Chip 5G WiFi IEEE 802.11n/ac MAC/Baseband/ Radio with Integrated Bluetooth 5.0 Document Number: 002-15051				
*O	6440968	UTSV	03/22/2019	Updated the title as “Single-Chip 5G WiFi IEEE 802.11n/ac MAC/Baseband/ Radio with Integrated Bluetooth 5.0 “. Added footnote for references of PCIe as “The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface”. Changed Bluetooth 4.2 to “Bluetooth 5.0” throughout the document. Updated Bluetooth Key Features. Added “Bluetooth 5.0 compliant” in Standards Compliance section. Added Bluetooth 5.0 section. Added Note “The PCIe interface is not brought up on CYW43455 and Cypress's firmware and drivers do not support this interface” in the following sections: PCI Express Interface, Pin Descriptions (Table 20), PCI Express Interface Parameters.

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