THE DATASHEET OF

TLE4966V1KHTSA1

TLE4966V-1K

In Plane Sensing with Vertical Dual Hall Effect Latch
for Automotive Applications

Data Sheet

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Sense & Control

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Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2014-05-13	

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1 Product Description

1.1 Target Applications

The TLE4966V-1K is specifically designed to detect the rotation direction and the rotation speed of a pole wheel.The sensing direction is **in-plane** to the sensor surface. Even at high distances to the hall elements the direction will be detected correctly.

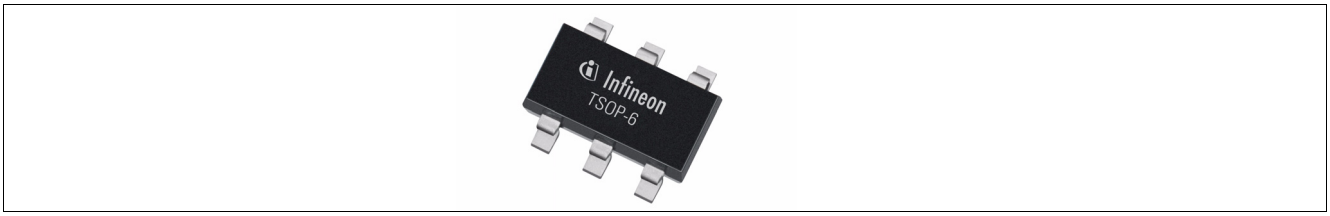

Figure 1-1 Image of TLE4966V in the PG-TSOP6-6-5 package

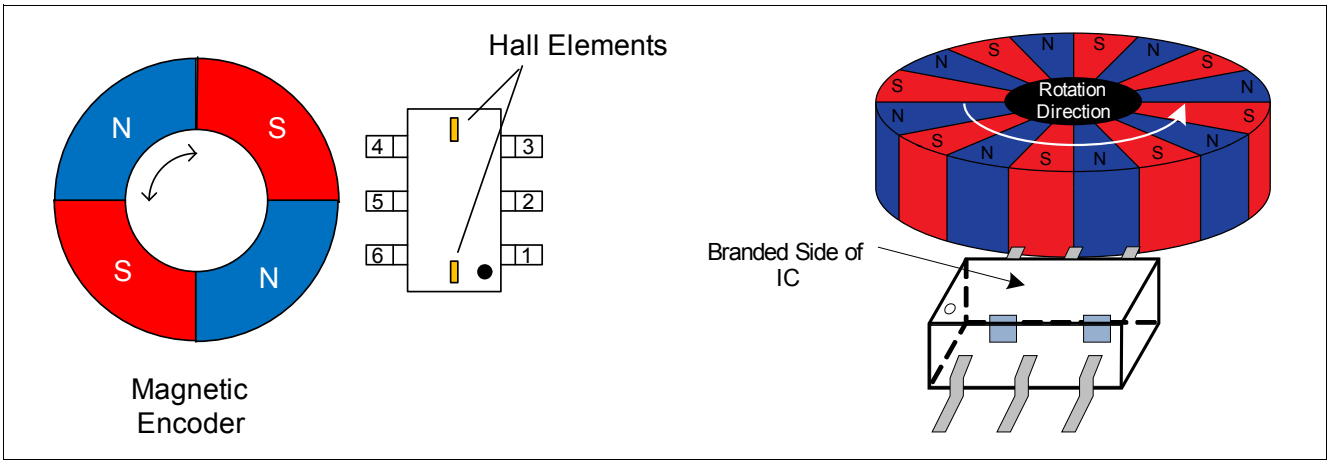

Figure 1-2 Target Application (top and side view): Sensing Direction parallel to target wheel

1.2 Features

- **In-Plane Sensing** for parallel mounting of magnetic encoder and sensor
- Low current consumption
- Direction Detection
- Speed output for index counting applications
- 3.5V to 32V operating supply voltage
- Operating from unregulated power supply
- Reverse polarity protection (-18V)
- Over voltage capability up to 42V without external resistor
- Output over current and over temperature protection
- High robustness to mechanical stress by Active Error Compensation
- Low drift of magnetic thresholds
- Low jitter (typ. 0.3us)
- SMD package PG-TSOP6-6-5

Table 1-1 Ordering Information

Product Name	Product Type	Ordering Code	Package
TLE4966V-1K	Dual Vertical Hall Latch	SP000997990	TSOP6-6-5

2 Functional Description

The TLE4966V-1K is specifically designed to detect the direction and rotational speed of a pole wheel as shown in **Figure 1-2**.

2.1 General

The new Infineon Vertical Double Hall Switch TLE4966V-1K has integrated the functionality of detecting speed and direction of a rotating magnet, commonly known as pole wheel.

Note: Completely new is the in plane field direction which will be detected with the TLE4966V-1K *shown in* **Figure 2-1** *which enables completely new application layouts.*

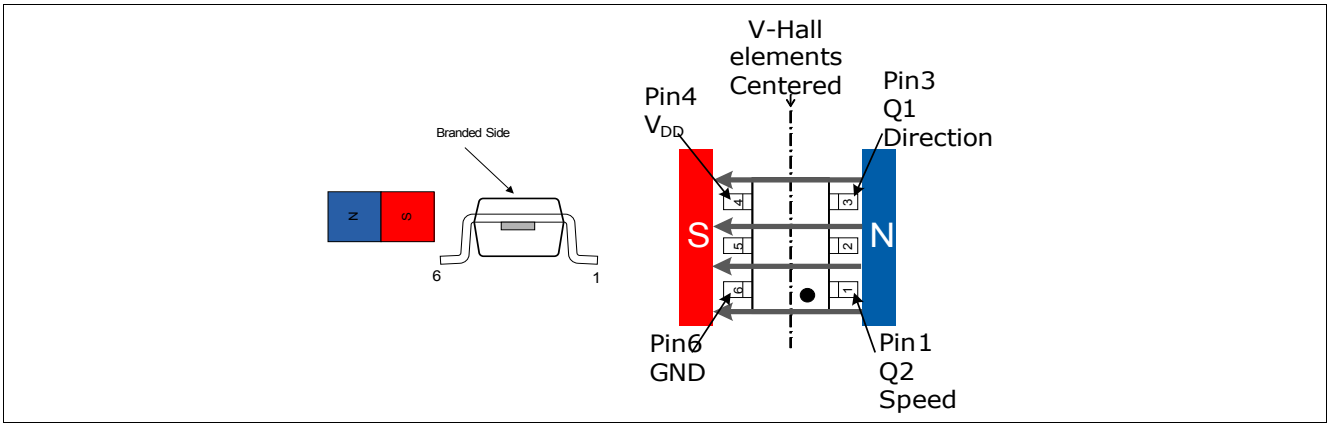

Figure 2-1 Target Application: Side view and top view for In-Plane Sensing

The sensor provides a speed output at Q2 with the status (high or low) corresponding to the magnetic field value. For positive magnetic fields (south pole) exceeding the threshold B_{OP} the output is low, whereas for negative magnetic fields (north pole) lower than B_{RP} the output switches to high. The output Q1 can be either high or low depending on the direction of rotation of the pole wheel. This direction information is calculated internally. (see **Table 2-2**)

Designed in a new technology, this device offers high voltage capabilities with very small current consumption. The product can be operated from unregulated power supplies which offers our customers unique freedom of design for their system.

This product is AEC Q100 certified and enables our customers to build systems for the highest automotive quality requirements. The product has a TSOP6 package, which is RoHs compliant and fulfills the usual automotive environmental guidelines.

Application Examples are:

- Window lifter (index counting)
- Power closing (index counting)
- All applications with the need of speed and direction detection.

Figure 2-2 and **Table 2-1** show the mapping of a pole wheel with the two corresponding output signals of the device.

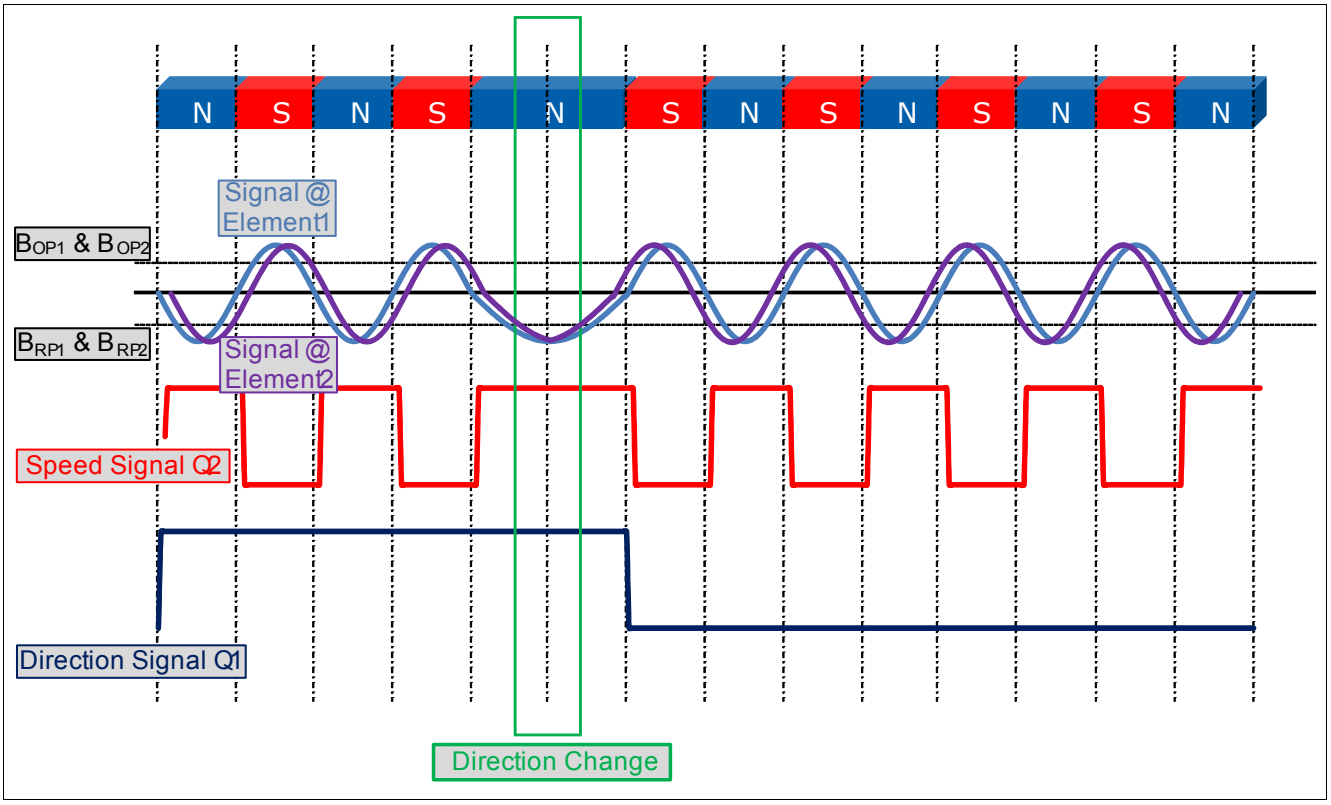

Figure 2-2 Magnetic field signal with the corresponding speed & direction output including the definition of the direction signal

Table 2-1 Output Pin Q1 Direction Signals

Rotation direction	State of direction output Q1
Counterclockwise	Low
Clockwise	High

2.2 Pin Configuration (top view)

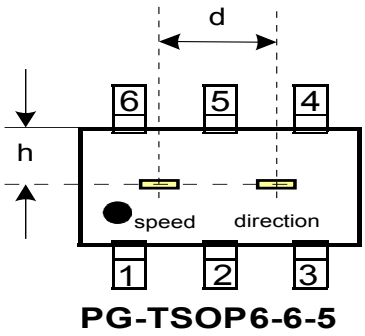

Figure 2-3 PG-TSOP6-6-5 Pin Configuration and sensitive area (d = 1.25mm) (see table 2-2)

Table 2-2 Pin Description PG-TSOP6-6-5

Pin No.	Symbol	Function
1	Q2	Speed
2	GND	Recommended connection to GND
3	Q1	Direction
4	V_{DD}	Supply voltage
5	GND	Recommended connection to GND
6	GND	Ground

The sensitive elements are placed in an optimized distance (d) to guarantee the direction detection. To compensate package stress the sensitive elements are placed in the middle of the package (h).

2.3 Block Diagram

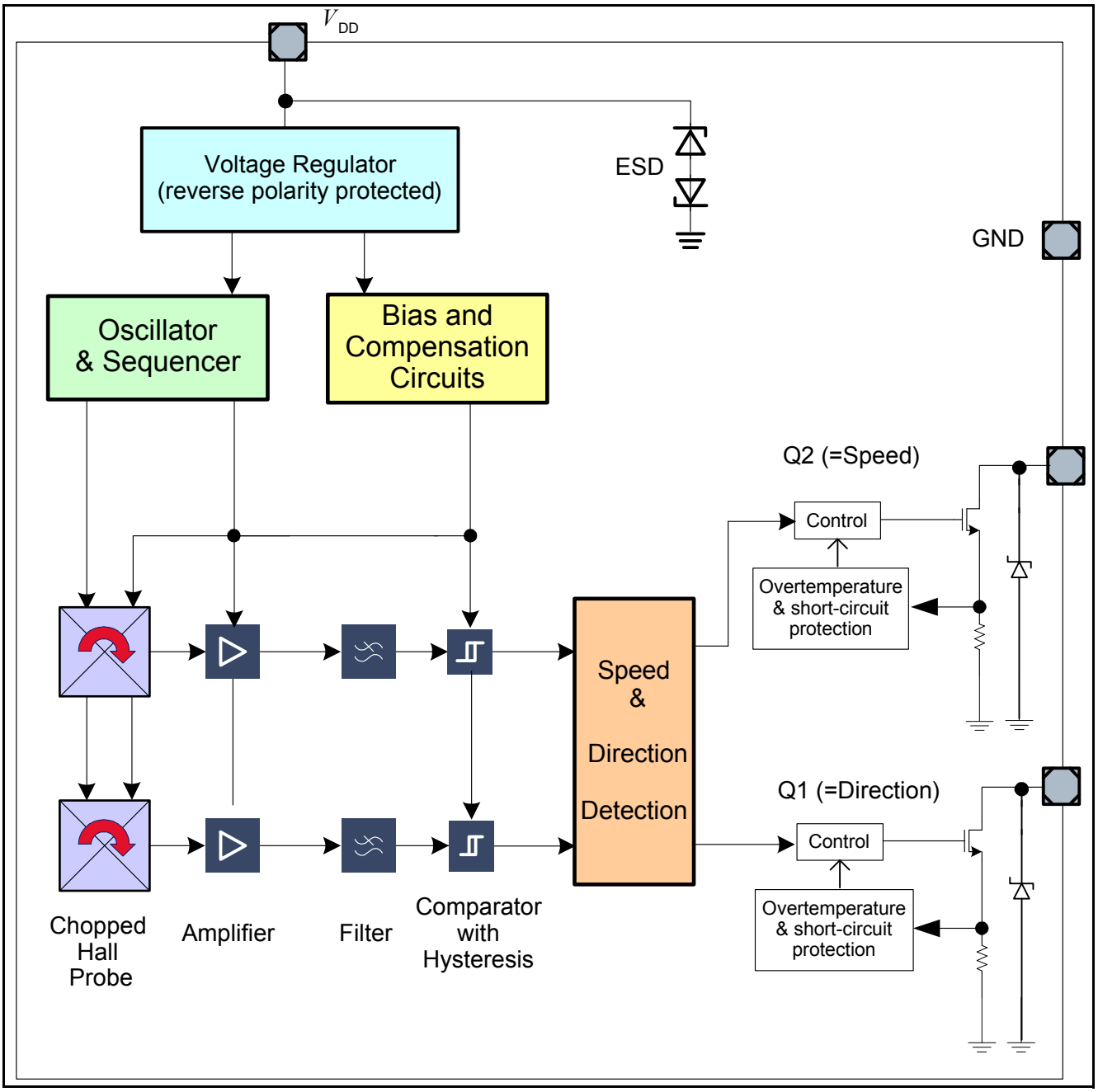

Figure 2-4 Functional Block Diagram of the TLE4966V-1K

The chopped Dual Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensations (chopping technique) rejects offsets in the signal path. Therefore the influence of mechanical stress to the Hall elements caused by molding and soldering processes and other thermal stress in the package is minimized. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds. The output transistor has an integrated over current and over temperature protection to prevent the device from destruction.

2.4 Start-up Behavior

The magnetic threshold exhibit a hysteresis Bhys = Bop - Brp. In case of a power-on with a magnetic field B within hysteresis (B_{rp} < B < B_{op}) the output of the sensor is set to the pull up voltage level "V_q" per default. After the first crossing of B_{op} or B_{rp} of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

V_{DDA} is the internal supply voltage which is following the external supply voltage V_{DD}.

This means for B > B_{op} the output is switching for B > B_{rp} and B_{op} > B > Brp the output stays at V_Q

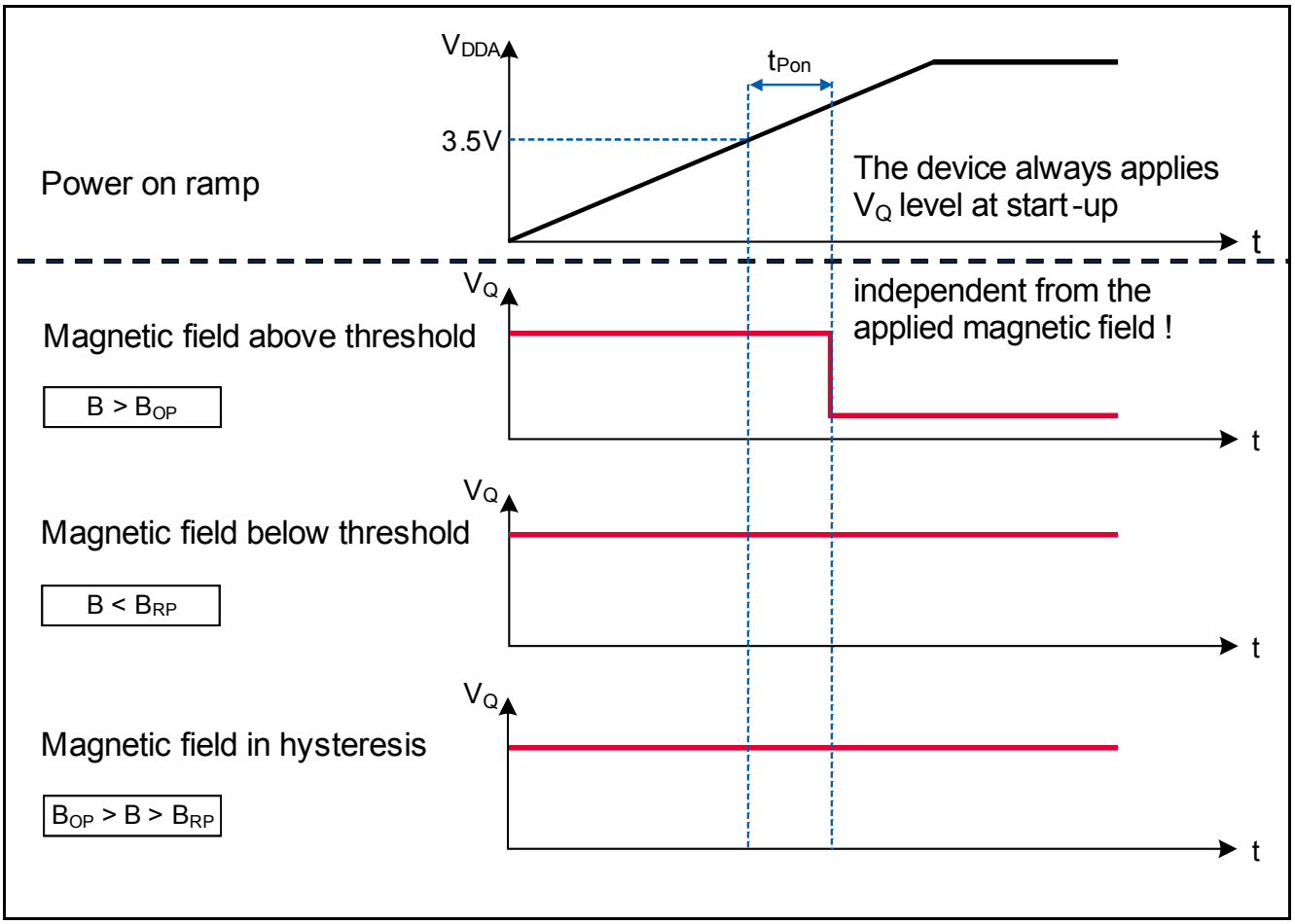

Figure 2-5 Start-up behavior of the at different magnetic start conditions

2.5 Application Circuit

The **Figure 2-6** below shows the basic option of an application circuit. The Resistor Rq has to be in a dimension to match the applied Vs to keep Iq limited to the operating range of maximal 10mA.

For example: Vs = 12V, Iq = 10mA --> R = 12V / 0.01A = 1.2kΩ.

In **Figure 2-7** the additional ESD Diodes are optional to achieve an increased ESD robustness at the Q pins. Additional with the (optional) 47nF between Vdd and GND a high system level robustness is achieved.

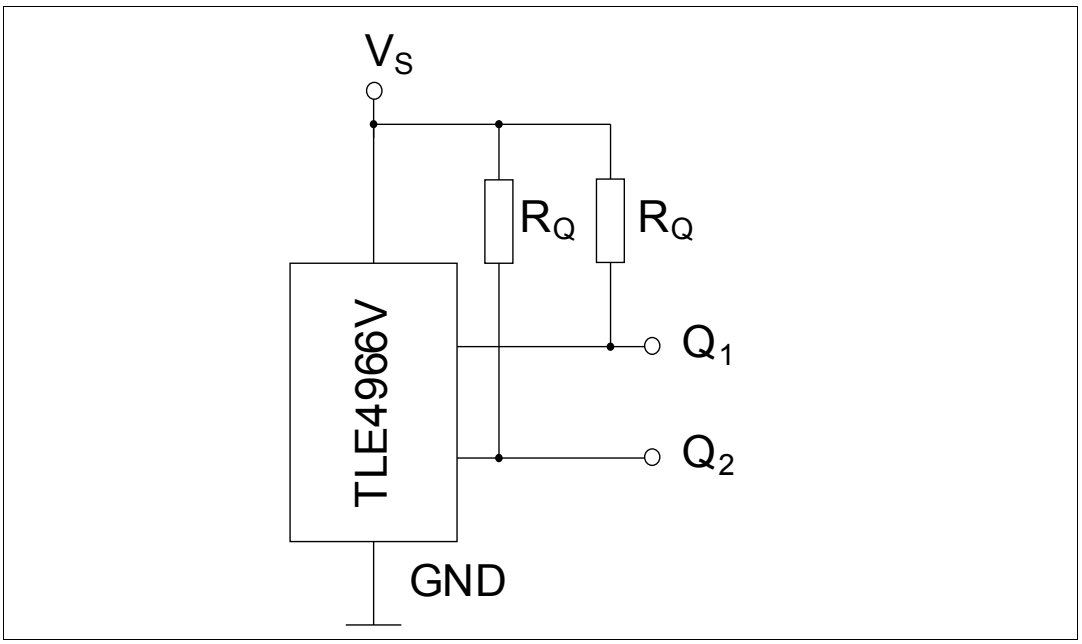

Figure 2-6 Basic Application Circuit

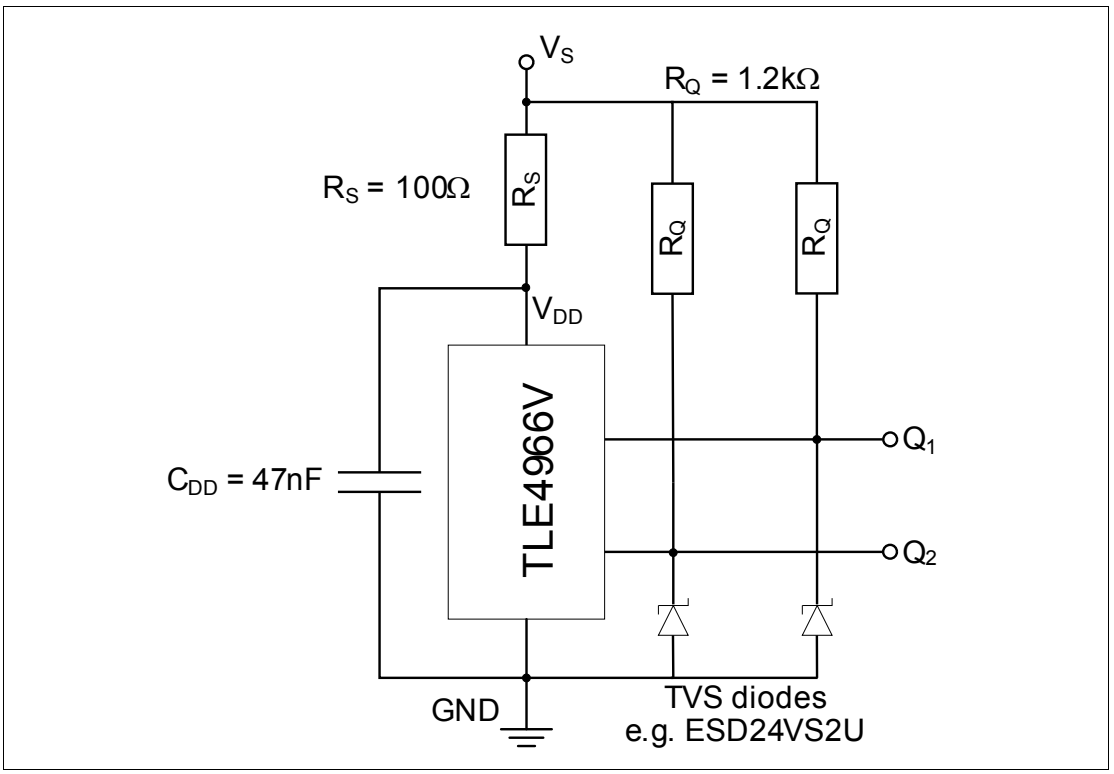

Figure 2-7 Enhanced Application Circuit for very high ESD robustness on system level

3 Specification

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Note / Test Condition
		Min.	Max.		
Supply voltage	V_{DD}	-18	32 42	V	 10h, no external resistor required
Output voltage	V_Q	-0.5	32	V	
Reverse output current	I_Q	-35		mA	
Junction temperature	T_J	-40	155 165 175	°C	for 2000h (not additive) for 1000h (not additive) for 168h (not additive)
Storage temperature	T_S	-40	150	°C	
Thermal resistance Junction ambient	R_{thJA}		200	K/W	for PG-TSOP6-6-5
Thermal resistance Junction lead	R_{thJL}		100	K/W	for PG-TSOP6-6-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Calculation of the dissipated power P_{DIS} and junction temperature T_J of the chip (TSPOP6 example):
e.g for: V_{DD} = 12 V, I_S = 10mA, V_{QSAT} = 0.5 V, I_Q = 10mA
Power dissipation: P_{DIS} = 12 V x 10mA + 2 x (0.5 V x 10mA) = 120mW + 10mW = 130mW
Temperature $\Delta T = R_{thJA} \times P_{DIS}$ = 200K/W x 130mW = 26K
For T_A = 100°C: $T_J = T_A + \Delta T$ = 100°C + 26K = 126°C

Table 3-2 ESD Protection[1] (TA = 25°C)

Parameter	Symbol	Limit Values		Unit	Note / Test Condition
		Min.	Max.		
ESD voltage (HBM)[2]	V_{ESD}	-2	+2	kV	R = 1.5kΩ, C = 100pF
System level test		-6	+6	kV	Figure 2-7 [3]

1) Characterization of ESD is carried out on a sample basis.
2) Human Body Model (HBM) tests according to EIA/JESD22-A114
3) Gun test (2kΩ/330pF or 330Ω/150pF) according to ISO 10605-2008

3.2 Operating Range

Attention: The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4966V-1K. All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

Table 3-3 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.5		32[1)]	V	
Output voltage	V_Q	-0.3		32	V	
Junction temperature	T_j	-40		150	°C	
Output current	I_Q	0		10	mA	
Magnetic signal input frequency[2)]	f_{mag}	0		5	kHz	

1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.

2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3dB corner frequency of the internal low-pass filter in the signal path.

3.3 Electrical Characteristics

Table 3-4 General Electrical Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	I_S	3.9	5.8	7.5	mA	
Reverse current	I_{SR}	-	0.05	1	mA	for V_{DD} = -18V
Output saturation voltage	V_{QSAT}	-	0.2	0.5	V	I_Q = 10mA
Output leakage current	I_{QLEAK}	-	-	5.0	µA	T=150°C, 12V
Output current limitation	I_{QLIMIT}	20	30	40	mA	internally limited & thermal shutdown
Output fall time[1)]	t_f	0.1	0.2	1	µs	1.2kΩ[2)]/ 50pF, see **Figure 4-1**
Output rise time[1)]	t_r	0.1	0.2	1	µs	1.2kΩ[2)]/ 50pF, see **Figure 4-1**
Output jitter[3)1)]	t_{QJ}		0.3	1	µs	For square wave signal with 1kHz
Effective noise value of the magnetic switching points[4)1)]	B_{Neff}		45		μT_{RMS}	
Delay time[5)1)]	t_d	8	20	30	µs	B_{peak}=10mT, Ramp=500mT/s; see **Figure 4-1**
Signal Count Delay[1)]	t_{dc}	50	400	1000	ns	1.2kΩ/50pF @ Vq=12V, Direction before Speed Signal, 50% to 50%
Power-on time[6)1)]	t_{PON}	48	84	120	µs	V_{DD} = 3.5 V, B ≤ B_{RP} - 0.5 mT or B ≥ B_{OP} + 0.5 mT
Chopper frequency[1)]	f_{OSC}		1300		kHz	

1) Not subject to production test, verified by design/characterization
2) Current limitation has to be taken into consideration for Vs > 12V in order not to exceed 10mA
3) Output jitter is the 1σ value of the output switching distribution.
4) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents a the rms-value and corresponds therefore to a 1 σ probability of normal distribution. Consequently a 3 σ value corresponds to 0.3% probability of appearance.
5) Systematic delay between magnetic threshold reached and output switching.
6) Time from applying V_{DD} = 3.0 V to the sensor until the output is valid.

3.4 Magnetic Characteristics

Table 3-5 Magnetic Characteristics

Parameter	Symbol	T (°C)	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Operating point	B_{OP}	-40	1.1	2.8	4.5	mT	
		25	0.9	2.5	4.1		
		150	0.4	1.9	3.3		
Release point	B_{RP}	-40	-4.5	-2.8	-1.1	mT	
		25	-4.1	-2.5	-0.9		
		150	-3.3	-1.9	-0.4		
Hysteresis	B_{Hys}	-40	3.6	5.3	7.4	mT	
		25	3.4	5.0	6.8		
		150	2.5	3.7	5.2		
Magnetic Matching	B_{Match}		-1.0		+1.0	mT	for (Bop1 - Bop2) and (Brp1 - Brp2); -40..125°C
			-1.5		+1.5		-40..150°C
Magnetic Offset	B_{Off}		-1.0		+1.0	mT	(Bop + Brp) / 2; -40..125°C
			-1.5		+1.5	mt	(Bop + Brp) / 2; -40..150°C
Temperature Compensation[1)]	TC			-1700		ppm/K	ferrite magnet

1) Not subject to production test, verified by design/characterization

The initial status of Q1 and Q2 after power on is Vq high (=OFF)!

3.5 Electro Magnetic Compatibility

Characterization of Electro Magnetic Compatibility is carried out on a sample basis from one qualification lot. Not all specification parameters have been monitored during EMC exposure.

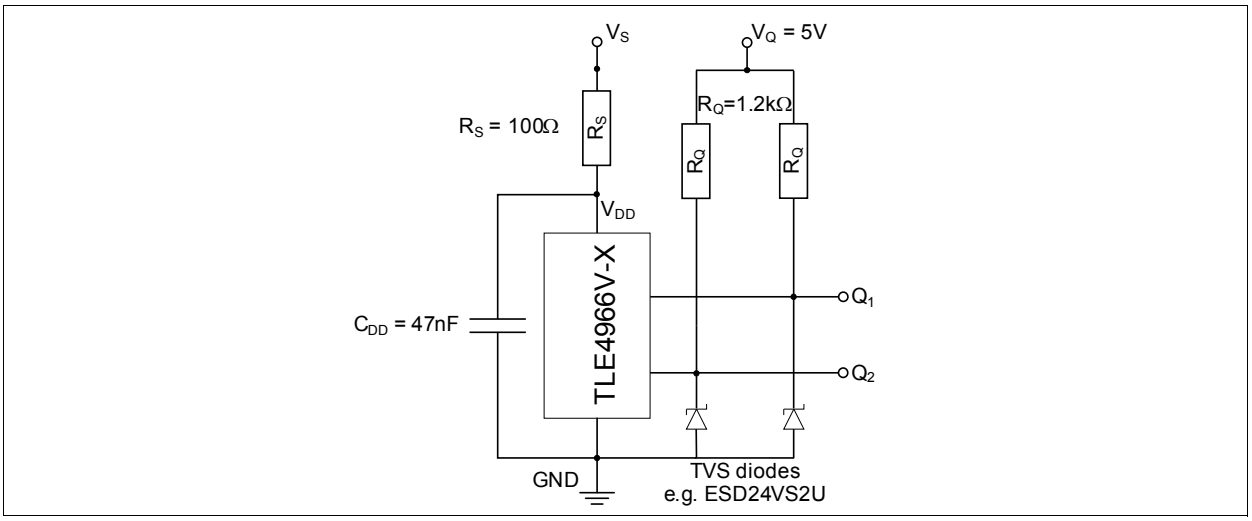

Figure 3-1 EMC test circuit

Ref: ISO 7637-2 (Version 2004), test circuit Figure 3-1 (with external resistor, Rs = 100Ω)

Table 3-6 Magnetic Compatibility

Parameter	Symbol	Level / Type	Status
Testpulse 1	V_{EMC}	-90V	C
Testpulse 2a[1)]		60V/110V	A/C
Testpulse 2b		10V	C
Testpulse 3a		-150V	A
Testpulse 3b		100V	A
Testpulse 4[2)]		-7V / -5.5V	A
Testpulse 5b[3)]		U_S = 86.5 V / U_S* = 28.5 V	A

1) ISO 7637-2 (2004) describes internal resistance = 2Ω (former 10Ω).
2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V +/- 0.2 V.
3) A central load dump protection of 42 V is used. U_S* = 42 V-13.5V.

Ref: ISO 7637-2 (Version 2004), test circuit **Figure 3-1** (without external resistor, R_S = 0Ω)

Table 3-7 Electro Magnetic Compatibility

Parameter	Symbol	Level / Type	Status
Testpulse 1	V_{EMC}	-50V	C
Testpulse 2a[1)]		45V	A
Testpulse 2b		10V	C
Testpulse 3a		-150V	A
Testpulse 3b		100V	A
Testpulse 4[2)]		-7V / 5.5 V	A
Testpulse 5b[3)]		U_S = 86.5 V / U_S* = 28.5 V	A

1) ISO 7637-2 (2004) describes internal resistance = 2Ω (former 10Ω).
2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V +/- 0.2 V.
3) A central load dump protection of 42 V is used. U_S* = 42 V-13.5V.

4 Timing Diagrams for the Speed and Direction Output

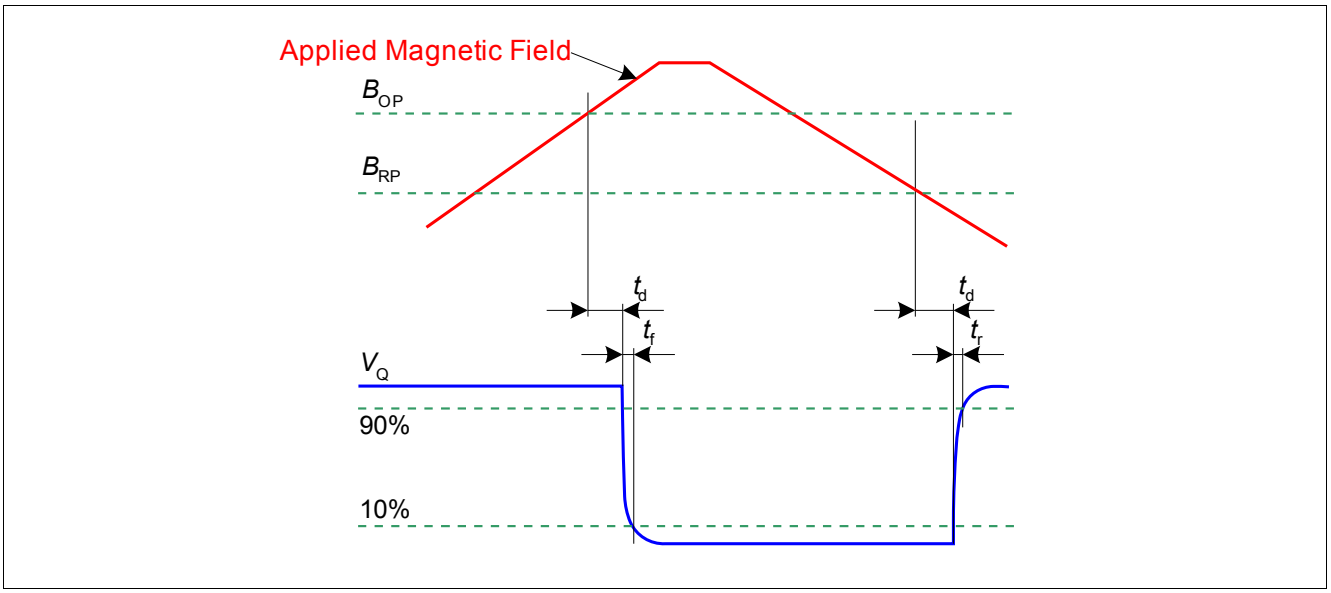

Figure 4-1 Timing Diagram TLE4966V

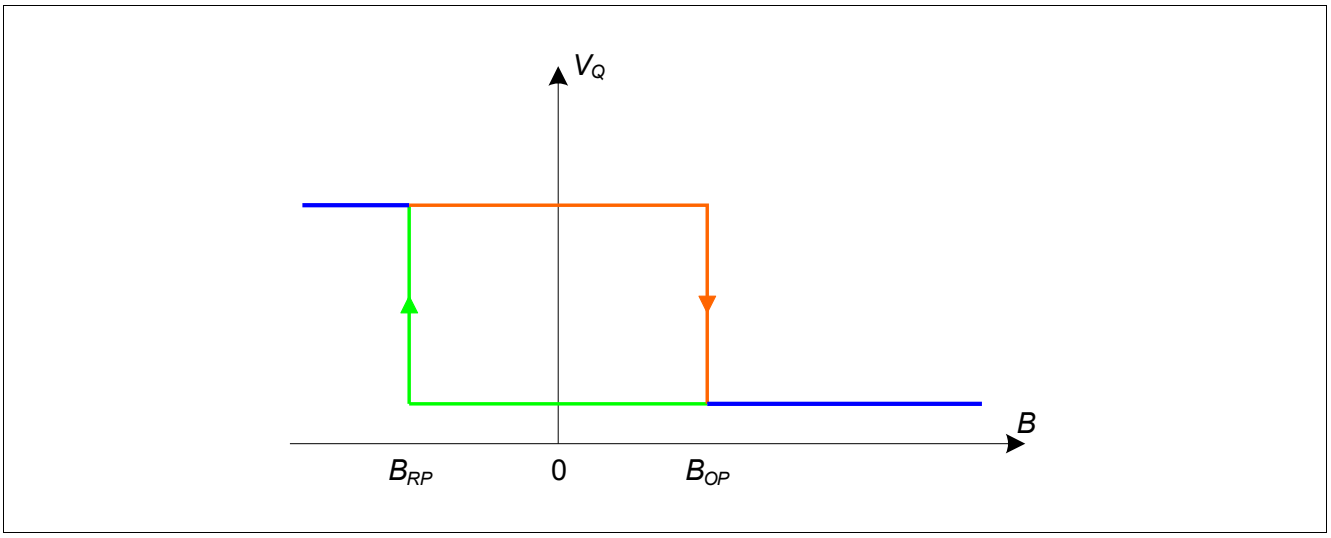

Figure 4-2 TLE4966V - Output Voltage Signal over applied magnetic Field

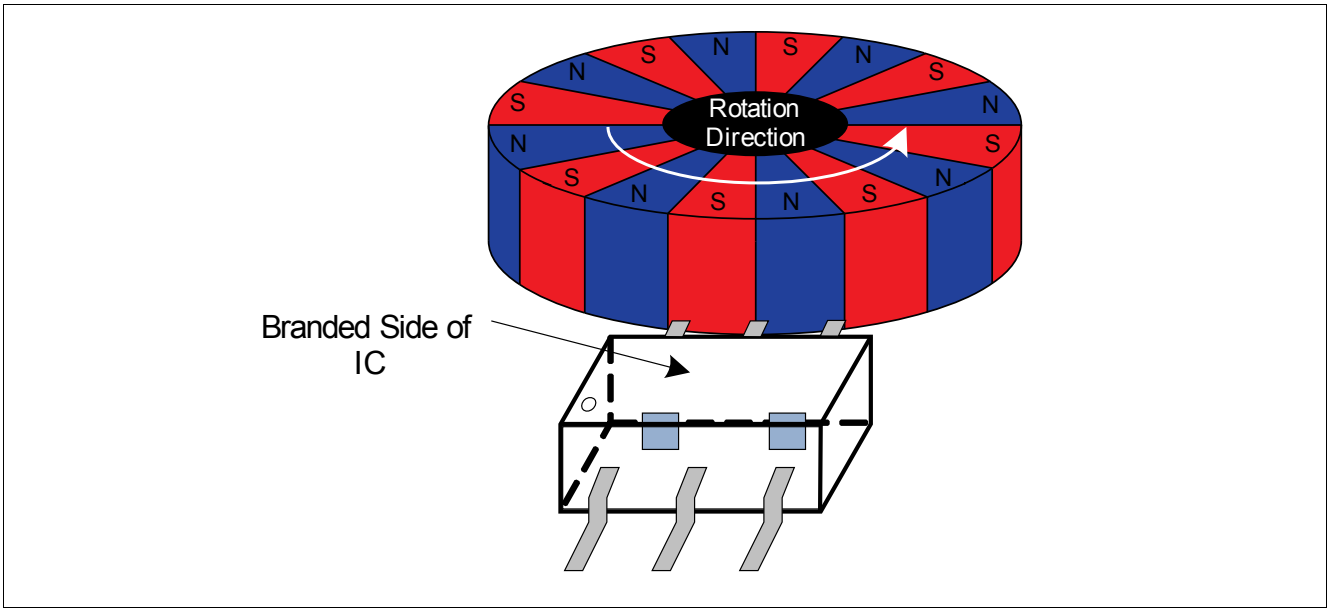

Figure 4-3 TLE4966V - Definition of the direction signal

Table 4-1 Output Pin Q1 Direction Signals

Rotation direction	State of direction output Q1
Counterclockwise	Low
Clockwise	High

5 Package Information

Figure 5-1 Image of TLE4966V in the PG-TSOP6-6-5 package

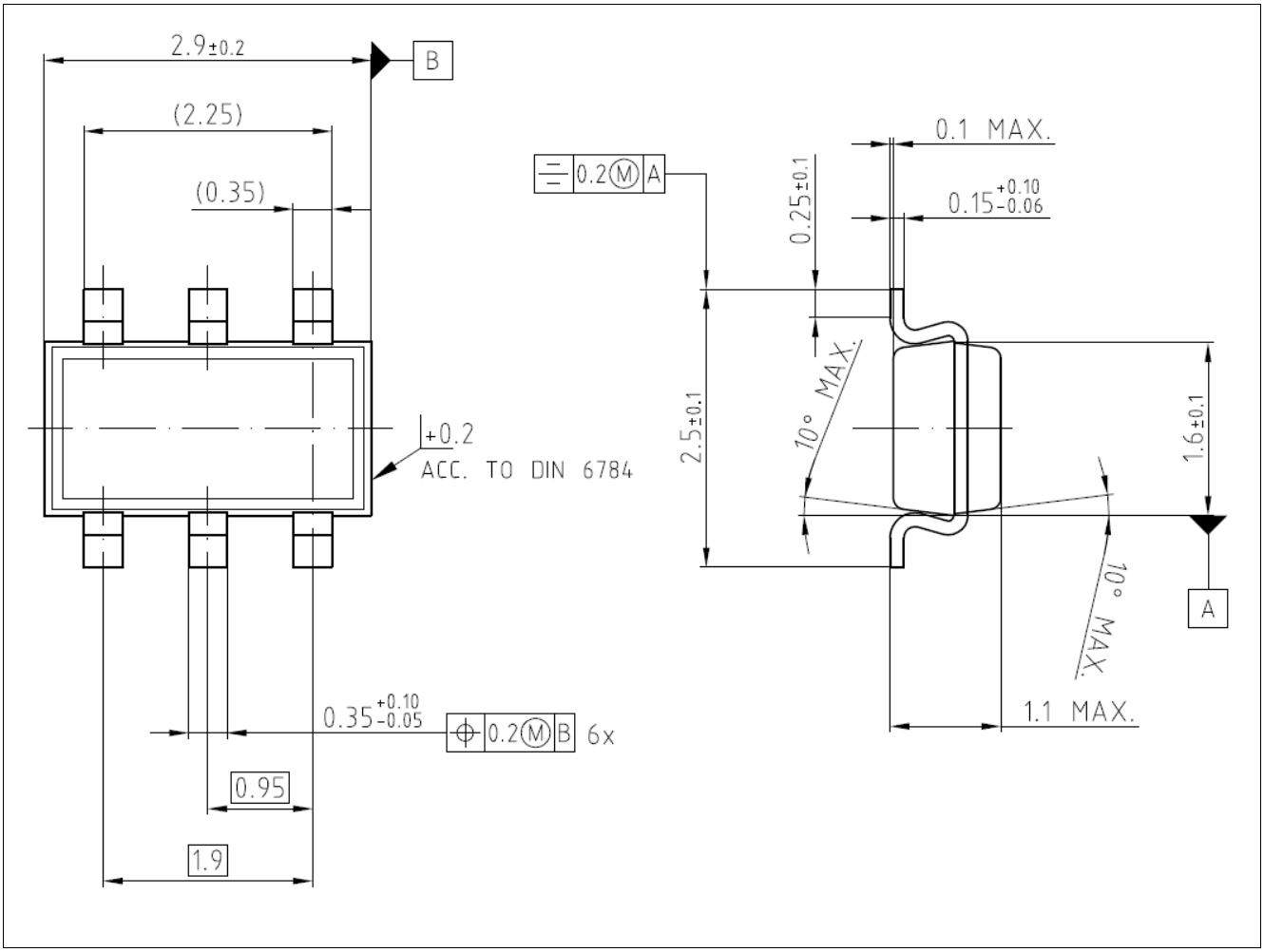

Figure 5-2 PG-TSOP6-6-5 Package Outline (All dimensions in mm)

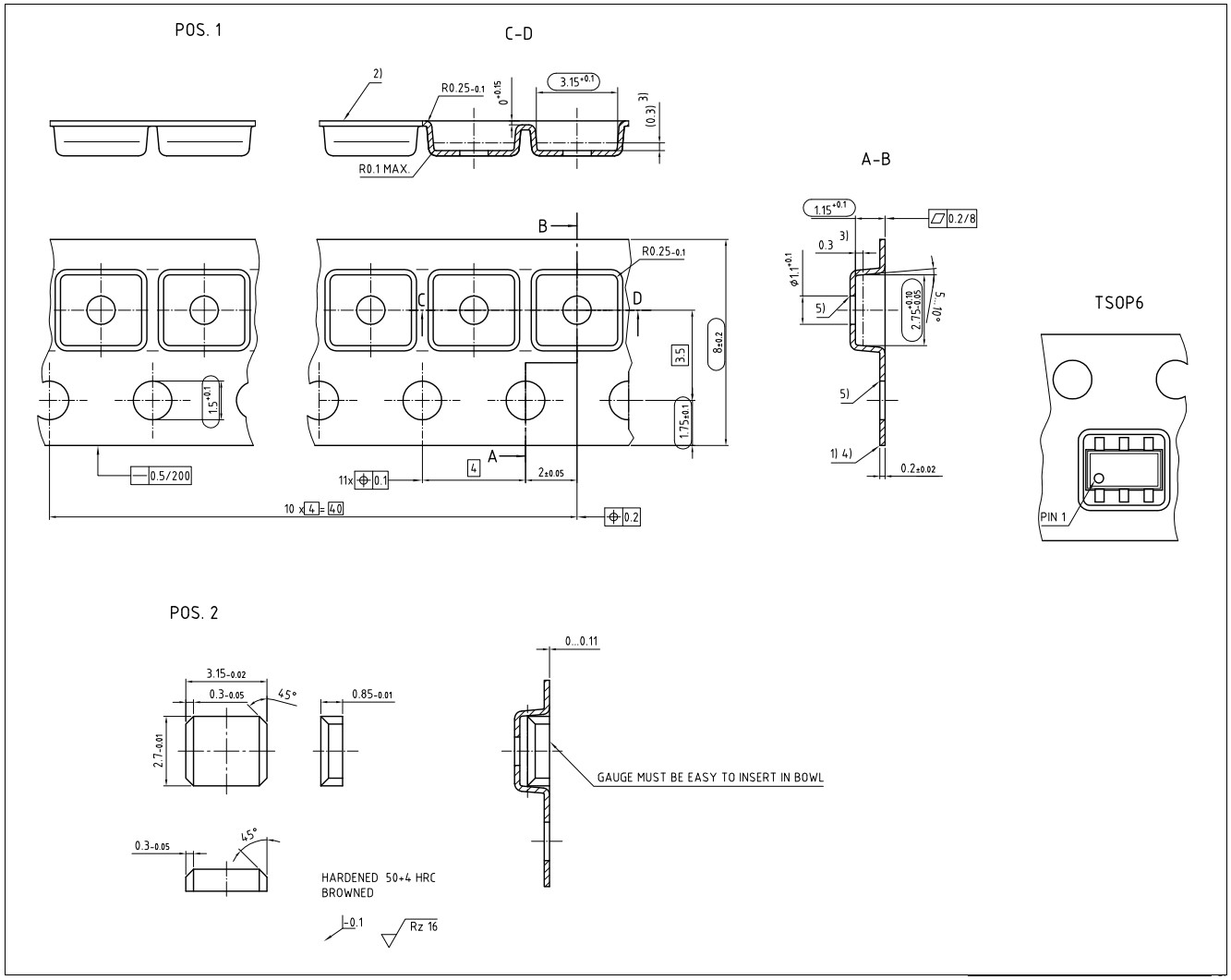

Figure 5-3 PG-TSOP6-6-5 Packing (All dimensions in mm)

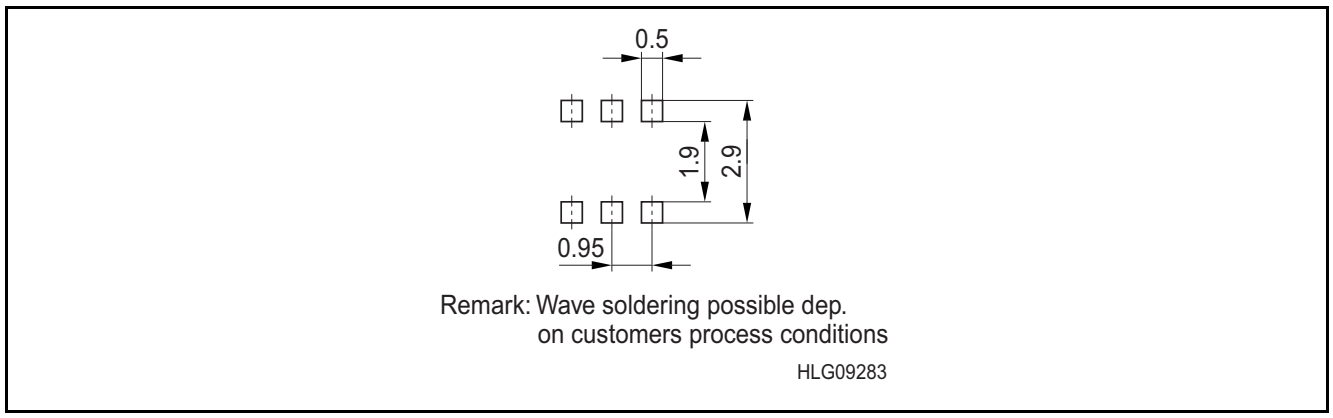

Figure 5-4 Footprint of PG-TSOP-6-6-5

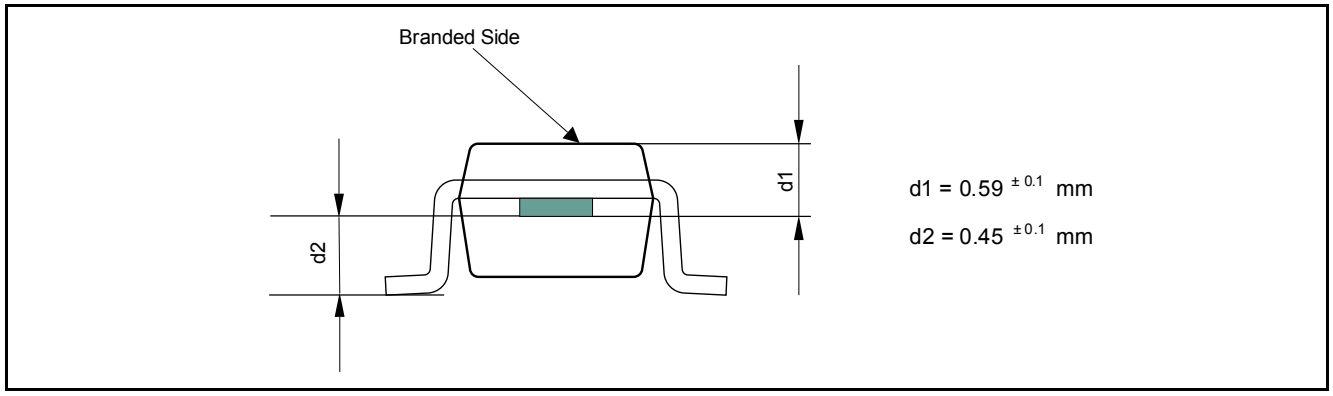

Figure 5-5 Distance between chip and package

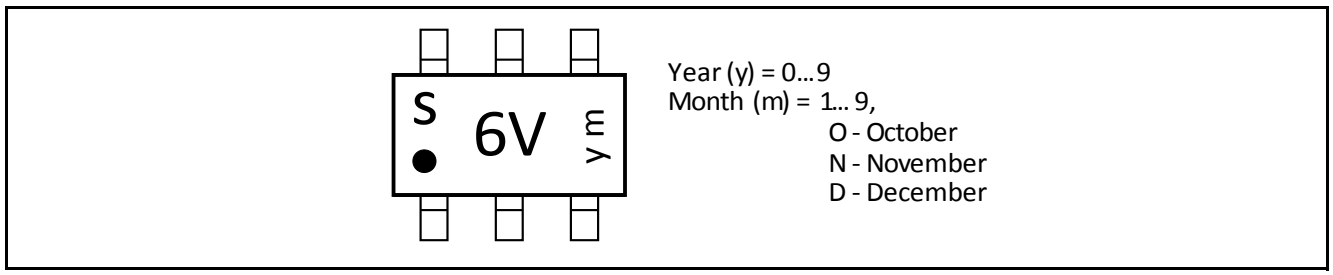

Figure 5-6 Marking of TLE4966V

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