Structure: Silicon Monolithic IC

Product Name: 4-wire resistive touch screen controller IC

Product No: BU21023GUL

Features

1) 4-wire resistive touch screen interface
2) 3.0V single power supply
3) 4-wire SPI interface / 2-wire serial interface
4) Selectable download way of CPU firmware (Host or EEPROM)
5) Two points and gesture detection

●Absolute maximum rating

Parameter	Symbol	Rating	Unit	Remarks
Power supply voltage	VDD	−0.3 ～ 4.5	V	
Voltage applied to pins	VIN	VSS−0.3 ～ VDD+0.3	V	
Power dissipation	Pd	830	mW	
Storage temperature range	Tstg	−50 ～ 125	℃	

*1 This is the power dissipation per IC unit. Reduce to 8.30 mW /℃ when Ta = 25℃ or above.

●Operating conditions

Parameter	Symbol	Rating			Unit	Remarks
		MIN	TYP	MAX		
Power supply	VDD	2.70	3.00	3.60	V	
Digital CORE power supply	DVDD	1.62	1.80	1.98	V	DVDD_EXT=H
Operating temperature	Topr	−20	25	85	℃	

This chip is not designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Application example

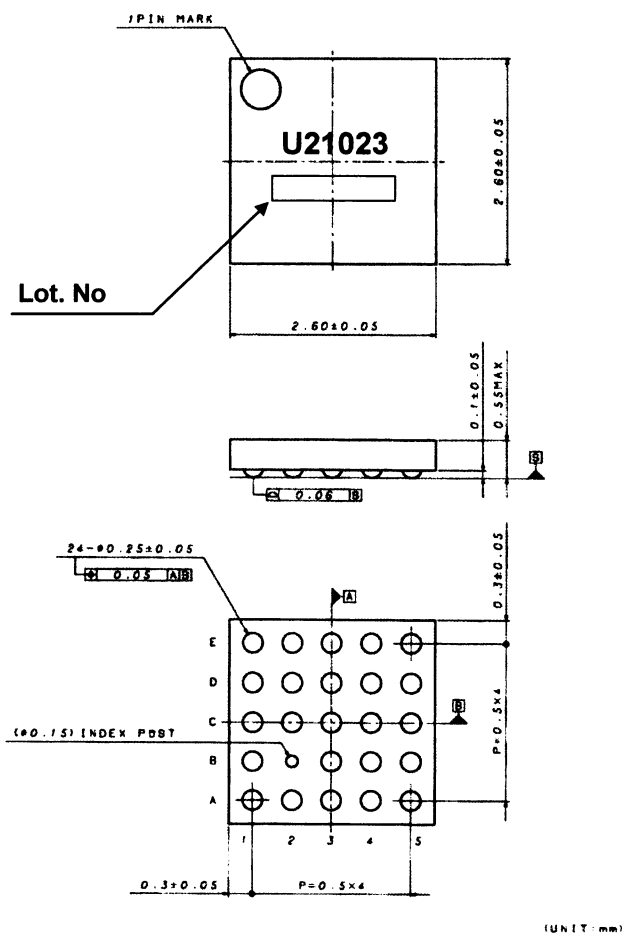
- ROHM cannot provide adequate confirmation of patents.
- The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
  Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.
- ROHM assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

●Electrical characteristics (Ta=25℃,VDD=3.00V)

Parameter	Symbol	Rating			Unit	Remarks
		MIN	TYP	MAX		
Low-level input voltage	VIL	-0.5	-	0.2xVDD	V	
High-level input voltage	VIH	0.8xVDD	-	VDD+0.5	V	
Low-level output voltage	VOL	-	-	VSS+0.4	V	
High-level output voltage	VOH	VDD-0.4	-	-	V	
Stop current	Ist	-	-	1	uA	RSTB=L
Standby current 1	Icc1	-	60	100	uA	DVDD_EXT=L
Standby current 2	Icc2	-	10	20	uA	DVDD_EXT=H
Operating current	Idd	-	4	6	mA	Load none
OSC frequency	Freq	18	20	22	MHz	
Resolution	Ad	1024 x 1024			Bit	
Differential non line accurate	DNL	-3.0	-	+3.0	LSB	
Integrate non line accurate	INL	-3.0	-	+3.0	LSB	

●Package outline drawing

(VCSP50L2)



●Terminal list

Ball	name	IN/OUT	function
D1	YN	I/O	Panel interface
C1	XN	I/O	Panel interface
C2	YP	I/O	Panel interface
B1	XP	I/O	Panel interface
A1	T4	I/O	Test pin
A2	PVDD	O	Regulator output (for supply panel voltage)
B3	AVDD	O	Regulator output (for supply analog block)
A3	DVDD	I/O	Regulator output (for supply digital block) or supply digital voltage (DVDD_EXT="H")
B4	DVDD_EXT	I	Digital voltage enable (H=output , L=Hi-Z)
A4	VDD	-	Supply voltage
A5	VSS	-	Ground
C3	RSTB	I	H/W reset
B5	CLK_EXT	I	Supply external clock for debug
C4	T1	I	Test pin
C5	T2	I	Test pin
D4	T3	I	Test pin
D5	IFSEL	I	Intereface select pin (L=SPI, H=2wire serial)
D3	SO	O	SPI: Serila data output / 2wire: -
E5	INT	O	Interrupt output
D2	SEL_CSB	I	SPI: Chip select / 2wire: Chip select
E4	SDA_SI	I	SPI: Serial data input / 2wire: Serial data in-out
E3	SCL_SCK	I	SPI: Serial clock input / 2wire: Serial clock input
E2	EDA	I/O	EEPROM SDA
E1	ECL	O	EEPROM SCL

(*1) Please connect AVDD and DVDD with 1.0uF connected with GND, and use the terminal PVDD with no connection.

(*2) DVDD_EXT="L ", the terminal DVDD can be supplied digital CORE power supply.

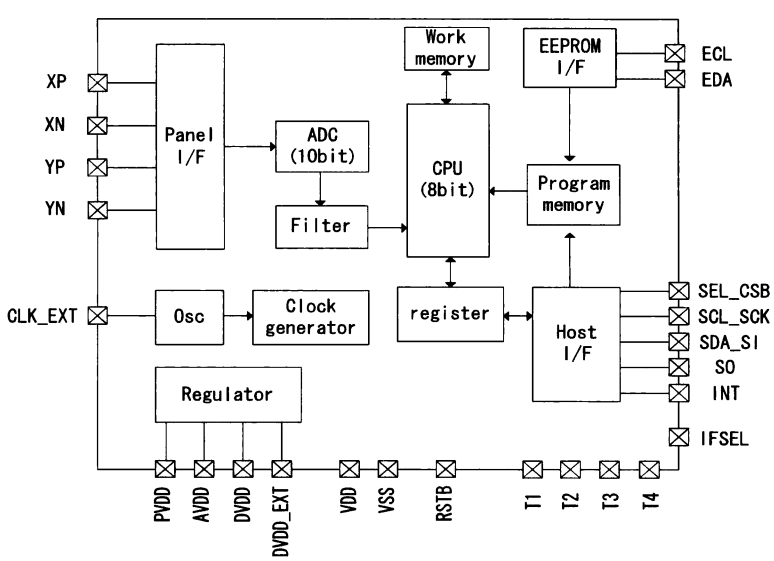
(*3) Please pull up the ECL, EDA, and INT by 10k ohm. Please connect T4 with 1.0uF connected with GND.
Please connect direct with GND when not use.

(*4) When use 2 wire serial interface, please pull up the SCL_SCK, SDA_SI by 10k ohm, and the terminal SO with no connection.

(*5) Each constant is a recommended value, and no guarantee value.

(*6) It must not RSTB="H" when supply VDD voltage.

●Block diagram



●Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.

Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Rush current

The IC with some power supplies has a capable of rush current due to procedure and delay at power-on. Pay attention to the capacitance of the coupling condensers and the wiring pattern width and routing of the power supply and the GND lines.

(13) Others

In case of use this LSI, please peruse some other detail documents, we called, Technical note, Functional description, Application note.

- Jisso Information -

Package : VCSP50L2

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1. Structure and materials

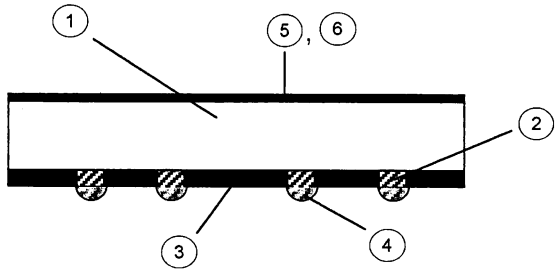


Fig. 1 Structure

No.	Item	Materials
1	Die	Silicon
2	Cu Post	Cu
3	Mold Compound	Epoxy Resin
4	Ext. terminal	Sn-3Ag-0.5Cu Solder
5	Mold Compound	Polyamide-imide Resin
6	Marking	Laser Marking

Dehydrated weight : 6.8mg

2. Tape and Reel information

2. 1. Packing specification

Tape	Embossed carrier tape
Quantity	3,000pcs/Reel
Direction of feed	E2 (See Fig. 2)

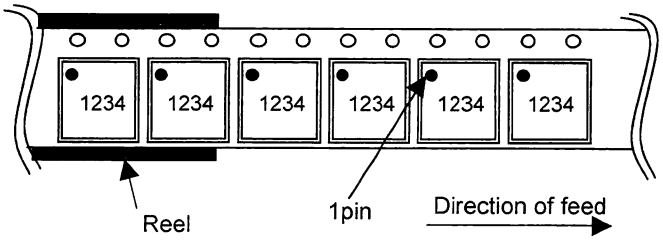


Fig. 2 Typical Tape and Reel configuration

2. 2. Tape and Reel specification

2. 2. 1. Tape and reel dimensions (See the table on page 2/4)

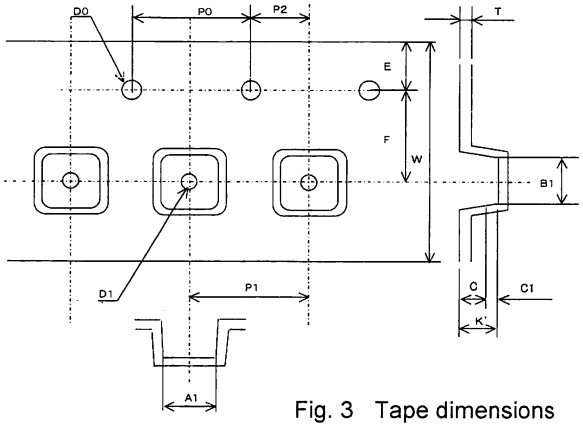


Fig. 3 Tape dimensions

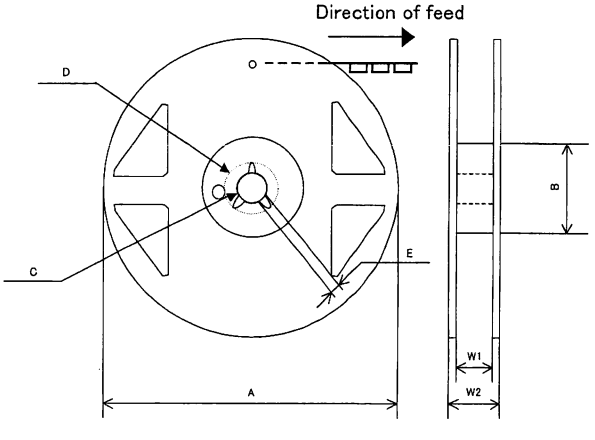


Fig. 4 Reel dimensions

(Tape dimensions)

A1	B1	C	C1	D0	D1	E	F	K'	P0	P1	P2	T	W
3.01 ±0.1	3.04 ±0.1	(0.6)	(0.25)	φ1.5 +0.1 -0	φ0.5 ±0.1	1.75 ±0.1	3.5 ±0.1	0.85 ±0.1	4.0 ±0.1	4.0 ±0.1	2.0 ±0.1	0.3 ±0.05	8.0 ±0.3

(Reel dimensions)

A	B	C	D	E	W1	W2
φ180 +0 -1.5	60 MIN	φ13.0 ±0.2	φ20.2 MIN	1.5 MIN	9.0 +1.0 -0	11.4 ±1.0

(Unit : mm)

2. 3. Leader and Trailer

2. 3. 1. Leader

No component pockets are 100 pockets(400mm) or more.

2. 3. 2. Trailer

No component pockets are 40 pockets(160mm) or more.

Tape is free from reel.

2. 4. Label for Reel and Box

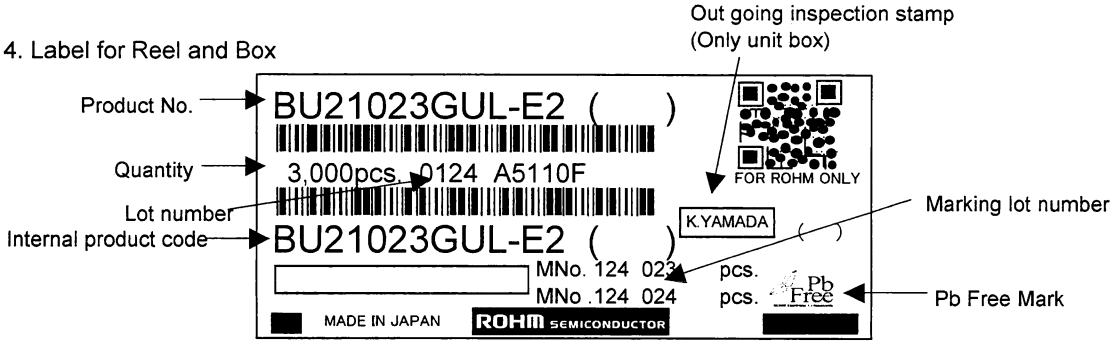


Fig. 5 Label example

2. 5. Packing style

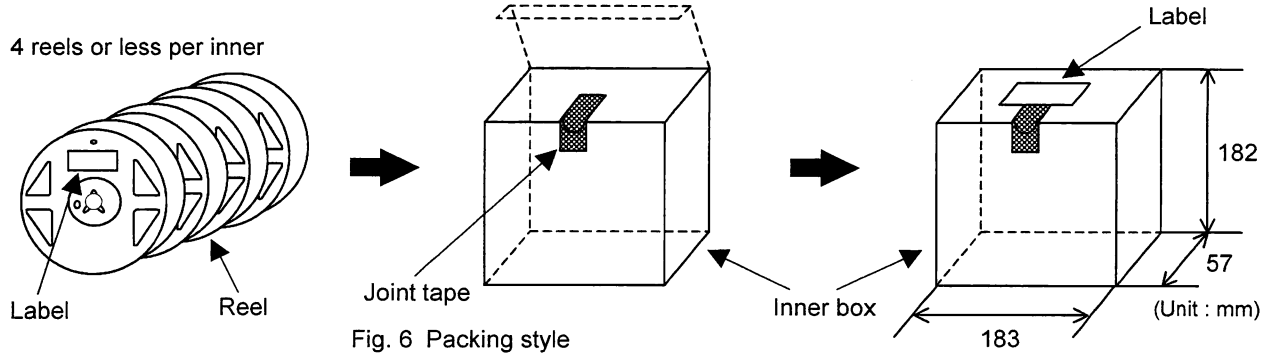
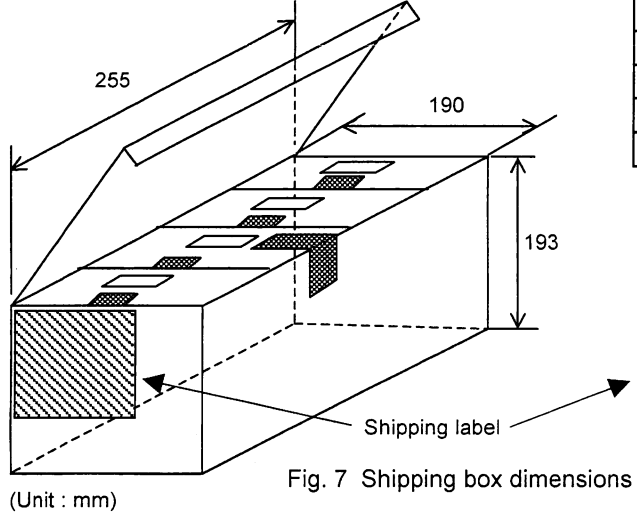


Fig. 6 Packing style

2. 6. Shipping style

4 unit boxes or less per shipping box.

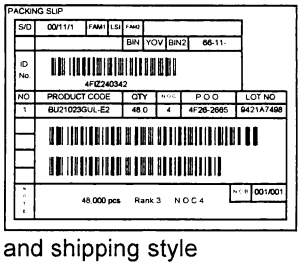


(Unit : mm)

2.7. Packing materials

Item	Material	Antistatic
Embossed carrier tape	PS	Yes
Cover tape	PET + PE	Yes
Reel	PS	Yes
Unit box	Cardboard	None
Shipping box	Cardboard	None

<Ex.>



<Shipping label>

1. Product code
2. Q' TY
3. N.O.C
4. LOT No.

Fig. 7 Shipping box dimensions and shipping style

2. 8. Others

2. 8. 1. Peelback strength

Cover tape peelback strength is 0.2 to 0.7N.

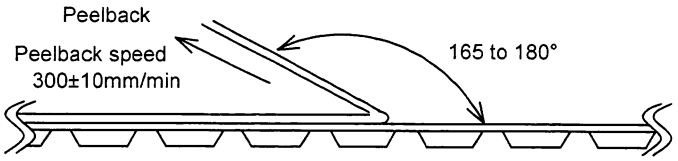


Fig. 8 Test method

2. 8. 2. Missing ICs

(1) No consecutive dropouts.

(2) A maximum 0.1% of specified number of products in each packing may be missing.

3. Storage conditions

3. 1. Storage environment

Recommended storage conditions are as follows :

-Temperature : 5 to 30°C

-Humidity : 40 to 70% RH

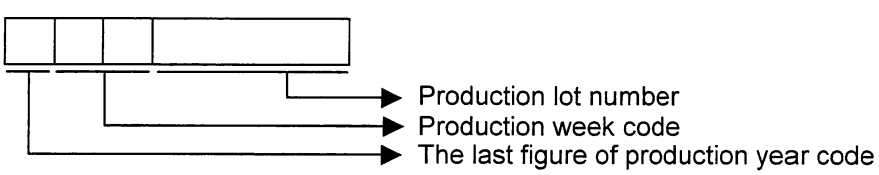
3. 2. Storage period

-Specified storage period : 1 year

3. 3. Specified storage period until soldering

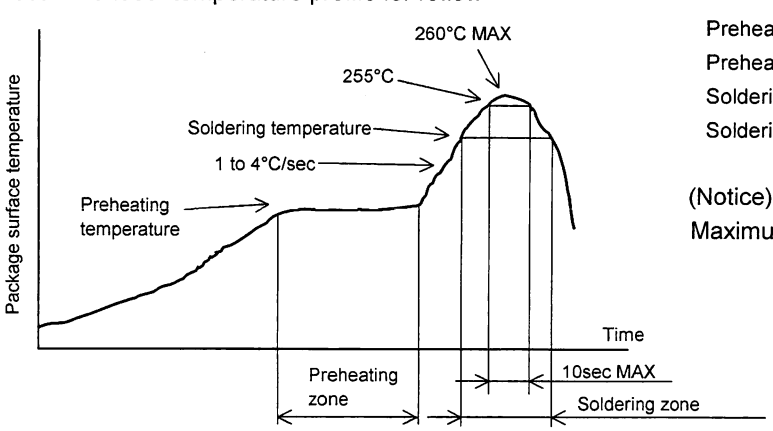
This package dose not require additional drying treatment as long as the moisture condition at the mounting process is within our recommended mounting condition.

4. Marking lot number



5. Soldering conditions

5. 1. Recommended temperature profile for reflow



Preheating temperature ; 130°C to 190°C
Preheating zone ; 120sec MAX
Soldering temperature ; 220°C to 230°C
Soldering zone ; 60sec MAX

(Notice)
Maximum 3-times soldering

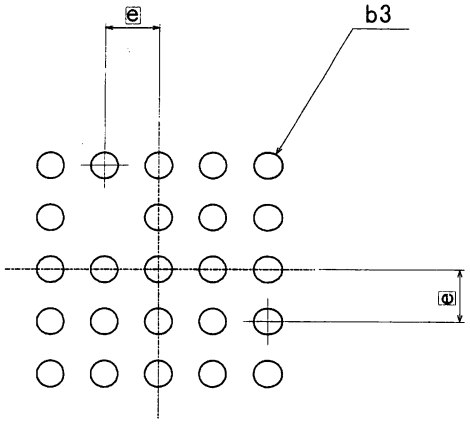
5. 2. About mounting with Sn-Pb solder paste.

Mounting with Sn-Pb solder paste is not recommended because it has a possibility of reducing reliability to connect with Sn-3.0Ag-0.5Cu solder balls.

5. 3. The wave soldering method is not supported.

5. 4. Partial heat supply method (by soldering iron) is not supported.

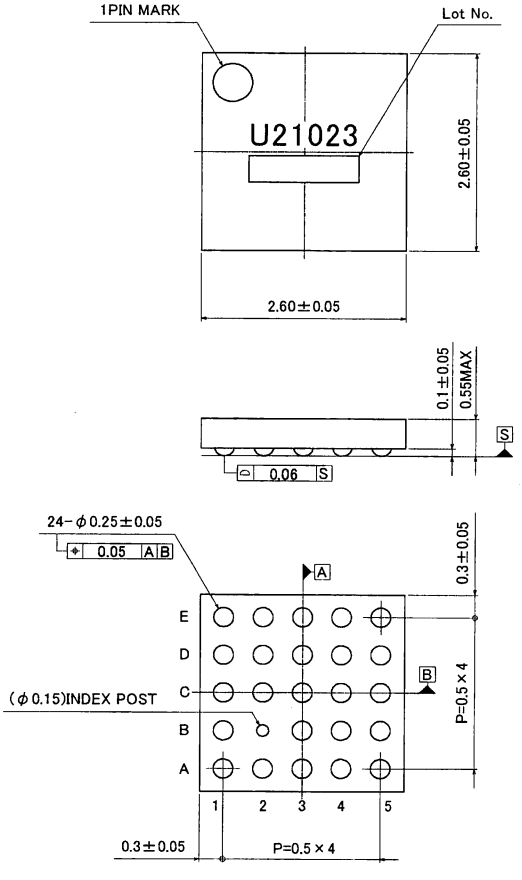
6. Footprint dimensions (Optimize footprint dimensions to the board design and soldering condition)



Symbol	Reference Value
e	0.50
b3	Φ0.25

(Unit : mm)

7. External dimensions



(Unit : mm)

8. Precautions

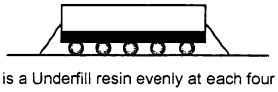
8. 1. Caution for handling

Silicon substrate surface is exposing to the side of this package.
Therefore, please pay careful attention to chip and crack, and handle without touching the side of package.

8. 2. Regarding the underfill material

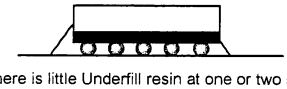
In some case, the underfill material is applied in order to reinforce the solder junction of package.
Since there is a case that solder joint reliability may deteriorate according to the resin material or coating condition, please evaluate it sufficiently for its application. In term of the coating condition, it is preferable that there is an enough material beyond the each four sides of package.

<Preferable example>



(There is a Underfill resin evenly at each four sides.)

<Non preferable example>



(There is little Underfill resin at one or two sides.)

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