



# THE DATASHEET OF IRL60HS118



## Target Applications

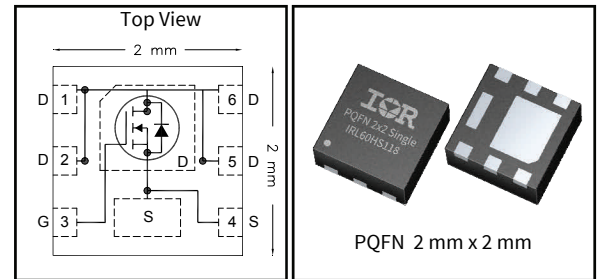
- Wireless charging
- Adapter
- Telecom

## Benefits

- Higher power density designs
- Higher switching frequency
- Uses OptiMOS™5 Chip
- Reduced parts count wherever 5V supplies are available
- Driven directly from microcontrollers (slow switching)
- System cost reductions

Typical values (unless otherwise specified)

$V_{DS}$	$V_{GS}$	$R_{DS(on)}$ (max.)
60V min.	± 20V max	17mΩ @ 10V
$Q_{g\ tot}$	$Q_{gd}$	$V_{gs(th)}$
5.3nC	2.1nC	1.7V



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack Form		Orderable Part Number
		Form	Quantity	
IRL60HS118	PQFN 2mm x 2mm	Tape and Reel	4000	IRL60HS118

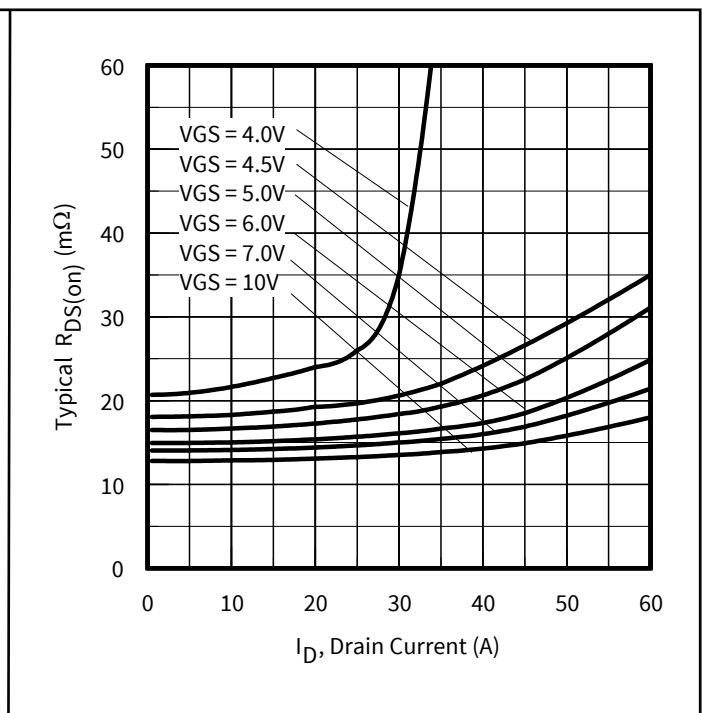
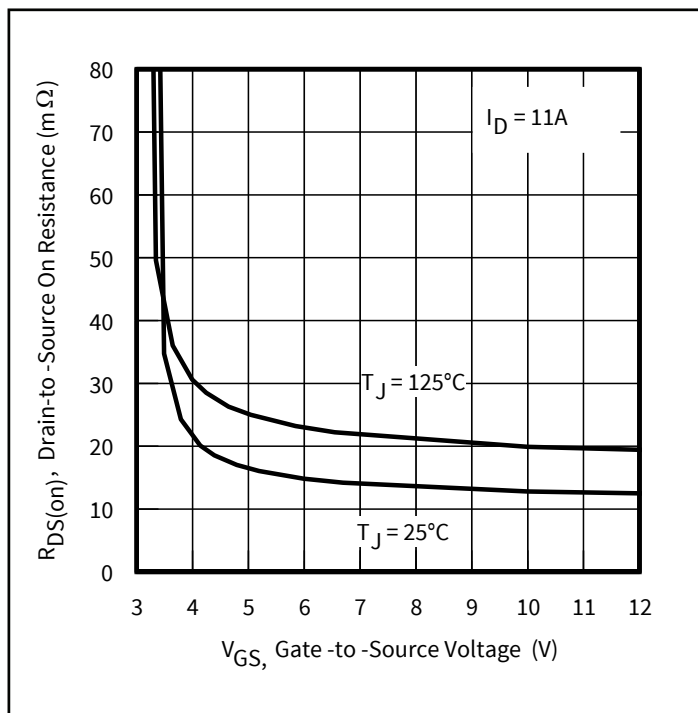


Figure 1 Typical On-Resistance vs. Gate Voltage

Figure 2 Typical On-Resistance vs. Drain Current

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# 1 Parameters

**Table1 Key performance parameters**

<b>Parameter</b>	<b>Values</b>	<b>Units</b>
$V_{DS}$	60	V
$R_{DS(on) \max}$	17	m $\Omega$
$I_D @ T_C = 25^\circ\text{C}$	18.5	A
$I_D @ T_A = 25^\circ\text{C}$	10	A

## 2 Maximum ratings and thermal characteristics

**Table 2 Maximum ratings (at  $T_J = 25^\circ\text{C}$ , unless otherwise specified)**

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current (Silicon Limited) ⑥ ⑦	$I_D$	$T_{C(\text{Bottom})} = 25^\circ\text{C}, V_{GS} @ 10\text{V}$	18.5	A
Continuous Drain Current (Silicon Limited) ⑥	$I_D$	$T_{C(\text{Bottom})} = 100^\circ\text{C}, V_{GS} @ 10\text{V}$	13	
Continuous Drain Current (Silicon Limited) ⑦ (Source Bonding Technologies Limited)	$I_D$	$T_{C(\text{Bottom})} = 25^\circ\text{C}, V_{GS} @ 10\text{V}$	17	
Continuous Drain Current (Silicon Limited) ⑤	$I_D$	$T_A = 25^\circ\text{C}, V_{GS} @ 10\text{V}$	10	
Pulsed Drain Current ①	$I_{DM}$	$T_{C(\text{Bottom})} = 25^\circ\text{C}$	56	W
Maximum Power Dissipation	$P_D$	$T_{C(\text{Bottom})} = 25^\circ\text{C}$	11.5	
Maximum Power Dissipation	$P_D$	$T_{C(\text{Bottom})} = 100^\circ\text{C}$	5.8	
Maximum Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$	2.5	V
Gate-to-Source Voltage	$V_{GS}$	-	$\pm 20$	
Peak Soldering Temperature	$T_P$	-	270	$^\circ\text{C}$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-	-55 to + 175	

**Table 3 Thermal characteristics**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case (Bottom) ④	$R_{\theta JC}$	-	-	-	13	$^\circ\text{C}/\text{W}$
Junction-to-Case (Top) ④	$R_{\theta JC}$	-	-	-	90	
Junction-to-Ambient ⑤	$R_{\theta JA}$	-	-	-	60	
Junction-to-Ambient ⑤	$R_{\theta JA} (<10\text{s})$	-	-	-	42	

**Table 4 Avalanche characteristics**

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy ②	$E_{AS}$	22	mJ
Avalanche Current ②	$I_{AR}$	11	A

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.36\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 11\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on a 1 inch square PCB (FR-4). Please refer to AN-994 for more details.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to 17A by source bonding technology.

### 3 Electrical characteristics

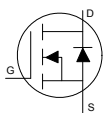
**Table 5 Static characteristics**

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, $I_D = 1mA$	-	28	-	mV/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 11A$ ③	-	13.3	17	mΩ
		$V_{GS} = 4.5V, I_D = 5.5A$ ③	-	18.3	23.5	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 10\mu A$	1.1	1.7	2.3	V
Gate Threshold Voltage Temp. Coefficient	$\Delta V_{GS(th)}/\Delta T_J$		-	-6.8	-	mV°/C
Drain-to-Source Leakage Current	$I_{DSS}$	$V_{DS} = 48V, V_{GS} = 0V$	-	-	1.0	μA
Gate-to-Source Forward Leakage	$I_{GSS}$	$V_{GS} = 20V$	-	-	100	nA
	$I_{GSS}$	$V_{GS} = -20V$	-	-	100	
Gate Resistance	$R_G$	-	-	1.2	-	Ω

**Table 6 Dynamic characteristics**

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Forward Trans conductance	gfs	$V_{DS} = 10V, I_D = 11A$	17	-	-	S
Total Gate Charge	$Q_g$	$I_D = 11A$ $V_{DS} = 30V$ $V_{GS} = 4.5V$ See Fig.8	-	5.3	8.0	nC
Pre-Vth Gate-to-Source Charge	$Q_{gs1}$		-	1.5	-	
Post-Vth Gate-to-Source Charge	$Q_{gs2}$		-	0.6	-	
Gate-to-Drain Charge	$Q_{gd}$		-	2.1	-	
Gate Charge Overdrive	$Q_{godr}$		-	1.1	-	
Switch Charge ( $Q_{gs2} + Q_{gd}$ )	$Q_{sw}$		-	2.7	-	
Output Charge	$Q_{oss}$	$V_{DS} = 30V, V_{GS} = 0V$	-	11	-	nC
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30V$	-	8.4	-	ns
Rise Time	$t_r$	$I_D = 11A$	-	21	-	
Turn-Off Delay Time	$t_{d(off)}$	$R_G = 2.7\Omega$	-	9.0	-	
Fall Time	$t_f$	$V_{GS} = 4.5V$ ③	-	5.0	-	
Input Capacitance	$C_{iss}$	$V_{GS} = 0V$	-	660	-	pF
Output Capacitance	$C_{oss}$	$V_{DS} = 25V$	-	180	-	
Reverse Transfer Capacitance	$C_{rss}$	$f = 1.0MHz$	-	14	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$	-	550	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz$	-	110	-	

**Table 7 Reverse Diode**

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous Source Current (Body Diode) ⑥ ⑦	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	17	A
Pulsed Source Current (Body Diode) ①	$I_{SM}$		-	-	56	
Diode Forward Voltage	$V_{SD}$	$T_J = 25^\circ C, I_S = 11A, V_{GS} = 0V$ ③	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ C, I_F = 11A, V_{DD} = 30V$	-	21	-	ns
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100A/\mu s$	-	12	-	nC

### 4 Electrical characteristic diagrams

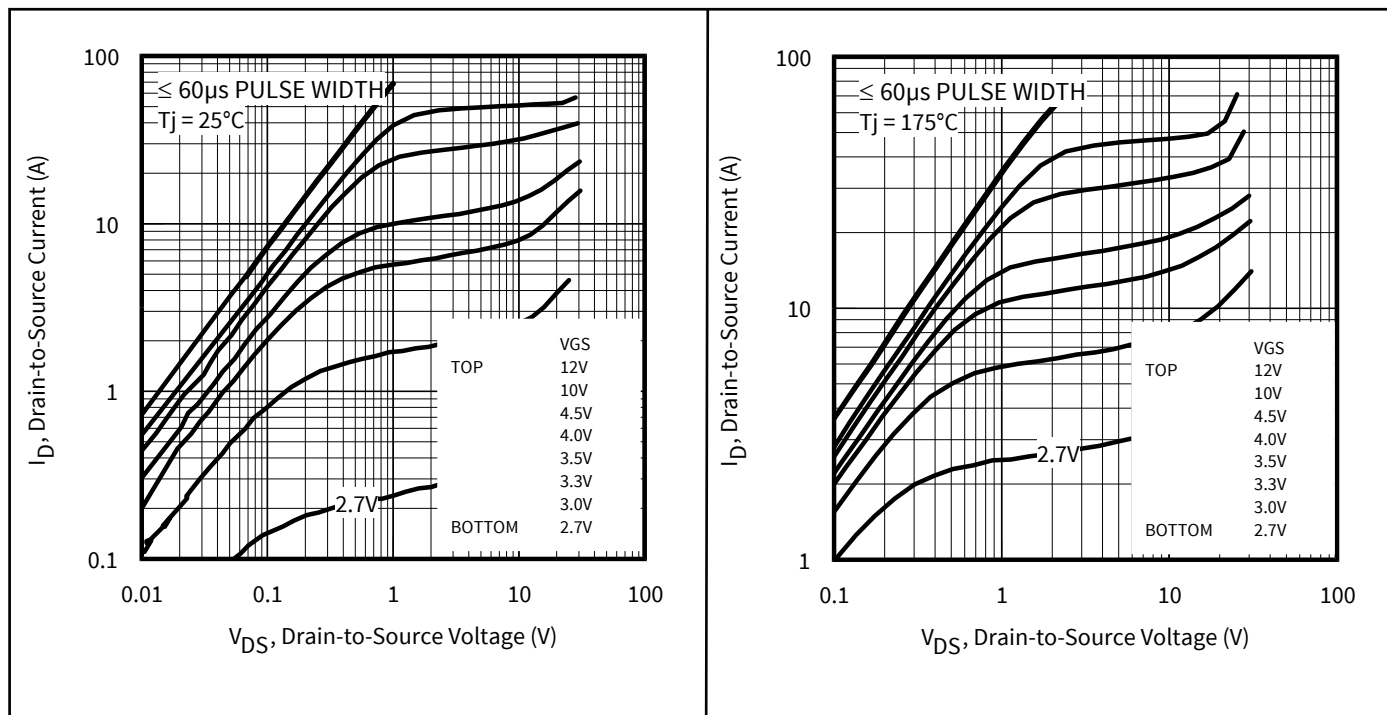


Figure 3 Typical Output Characteristics

Figure 4 Typical Output Characteristics

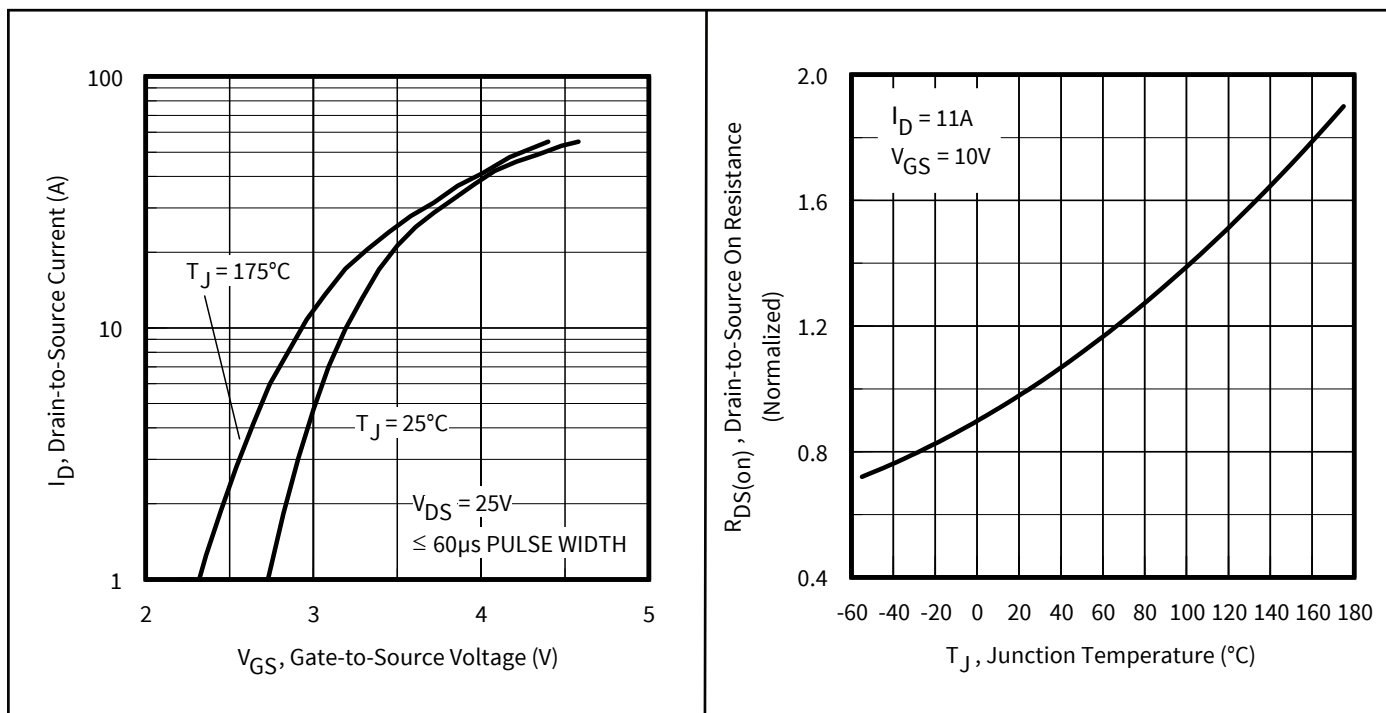
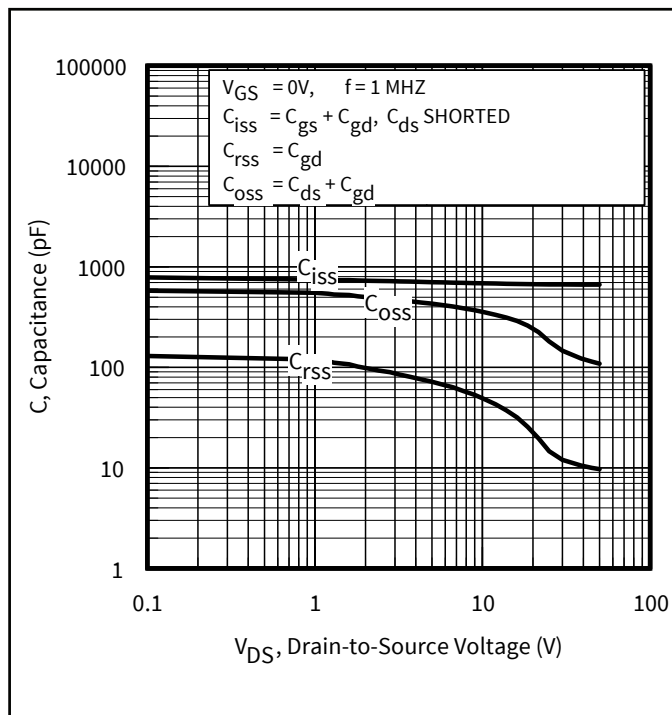
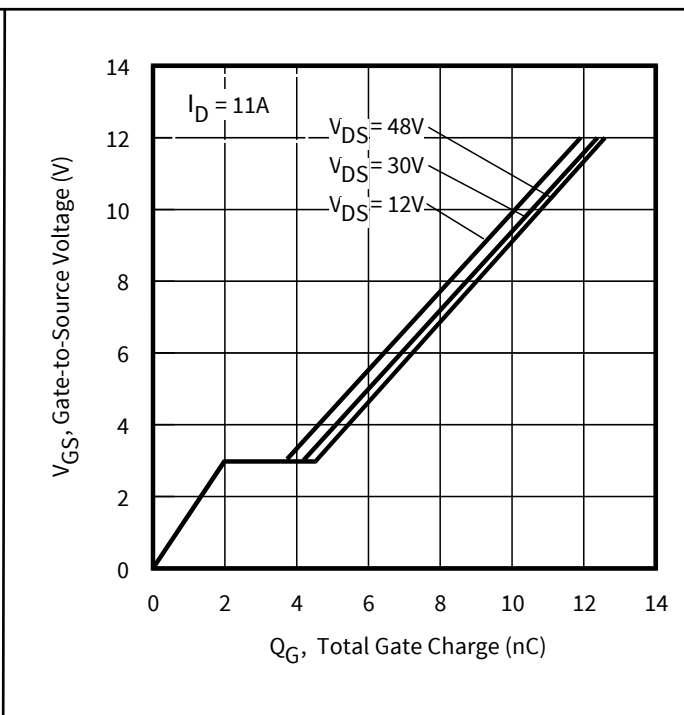
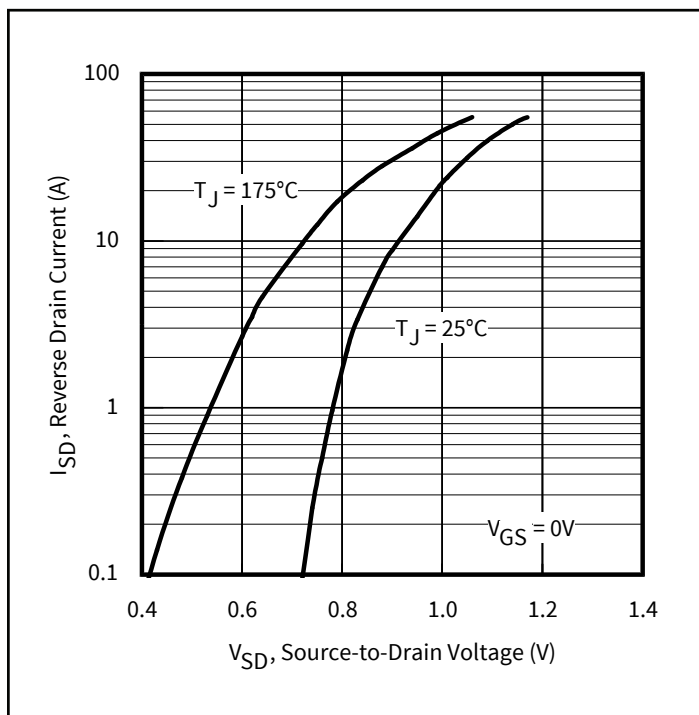
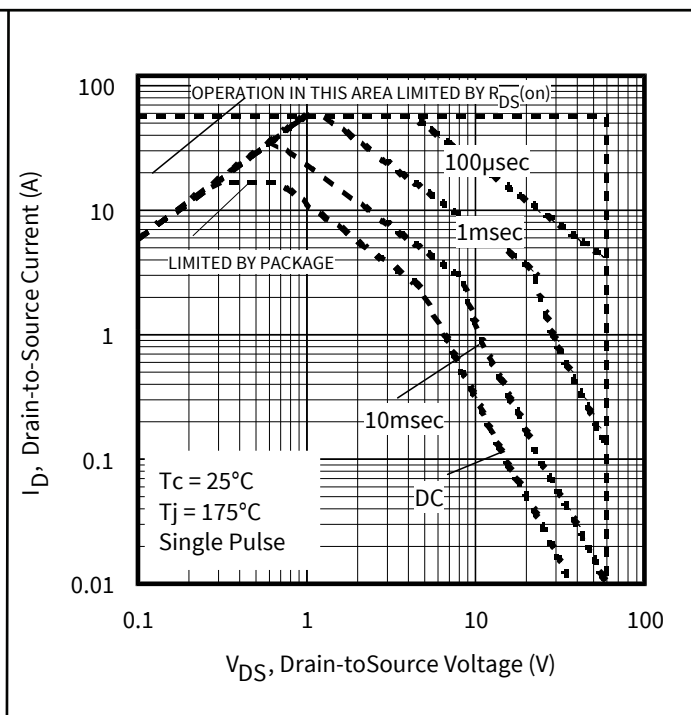


Figure 5 Typical Transfer Characteristics

Figure 6 Normalized On-Resistance vs. Temperature


**Figure 7 Typical Capacitance vs. Drain-to-Source Voltage**

**Figure 8 Typical Gate Charge vs. Gate-to-Source Voltage**

**Figure 9 Typical Source-Drain Diode Forward Voltage**

**Figure 10 Maximum Safe Operating Area**

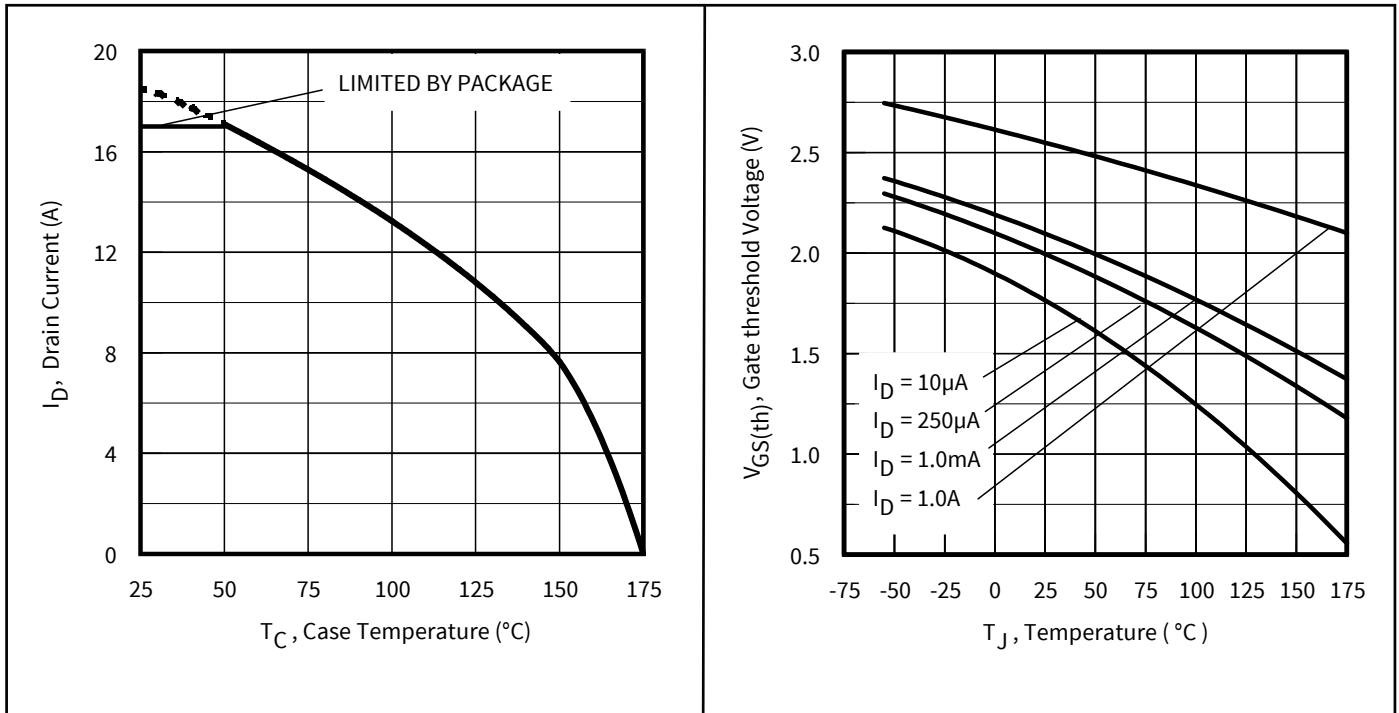


Figure 11 Maximum Drain Current vs. Case Temperature

Figure 12 Typical Threshold Voltage vs. Junction Temperature

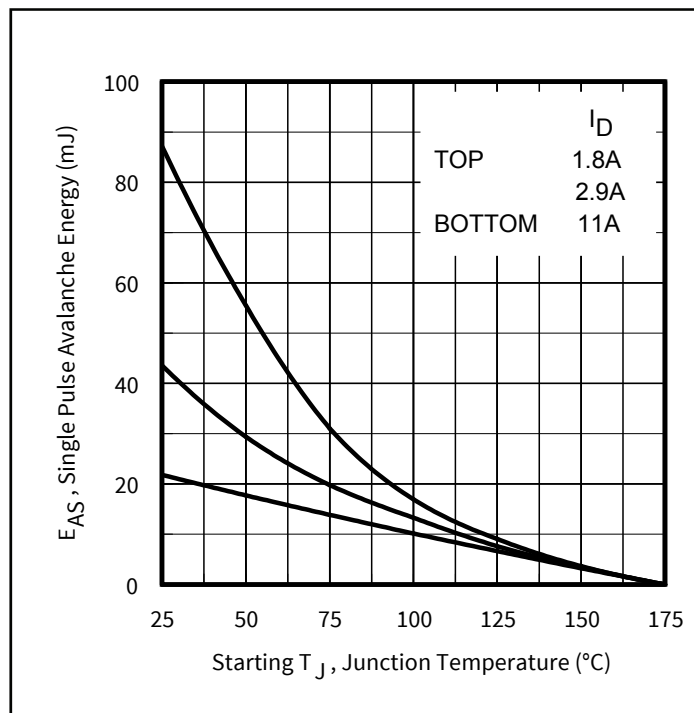


Figure 13 Maximum Avalanche Energy vs. Drain Current

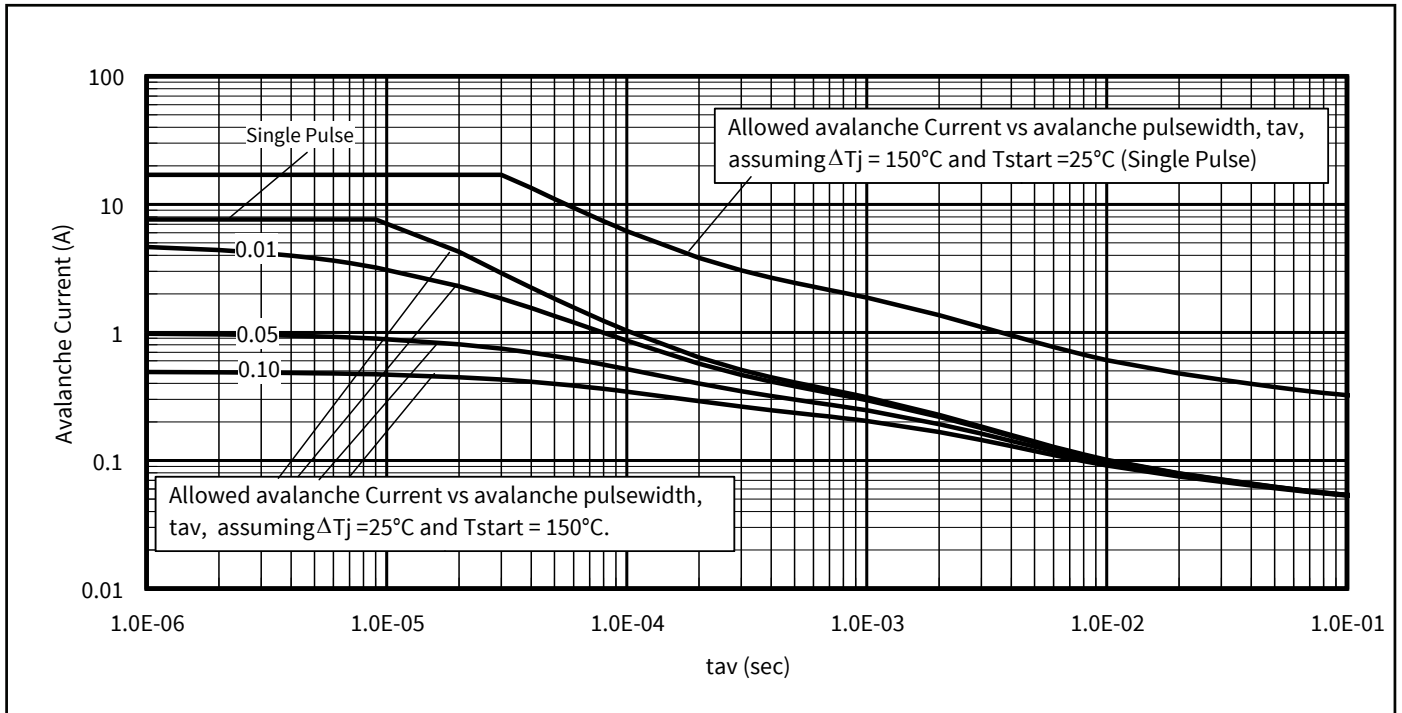


Figure 14 Typical Avalanche Current vs. Pulse Width

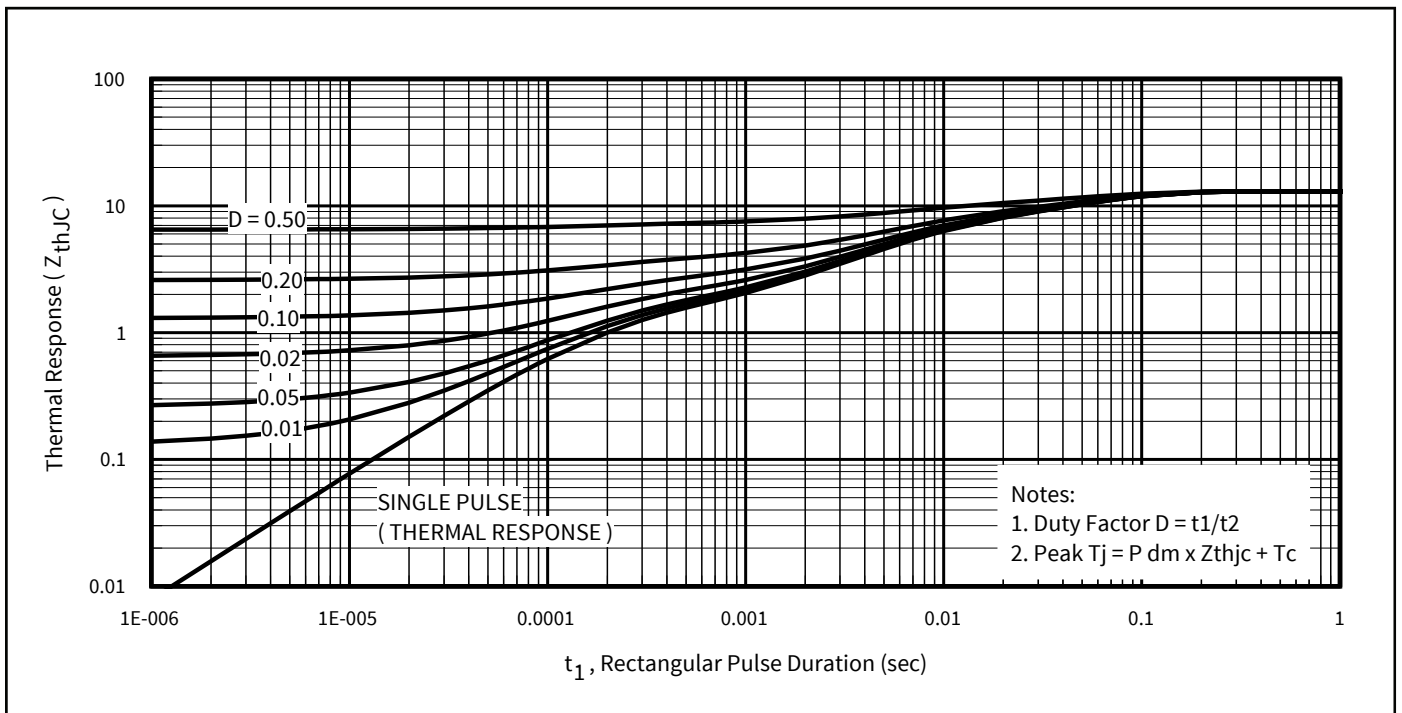


Figure 15 Maximum Effective Transient Thermal Impedance, Junction-to-Case

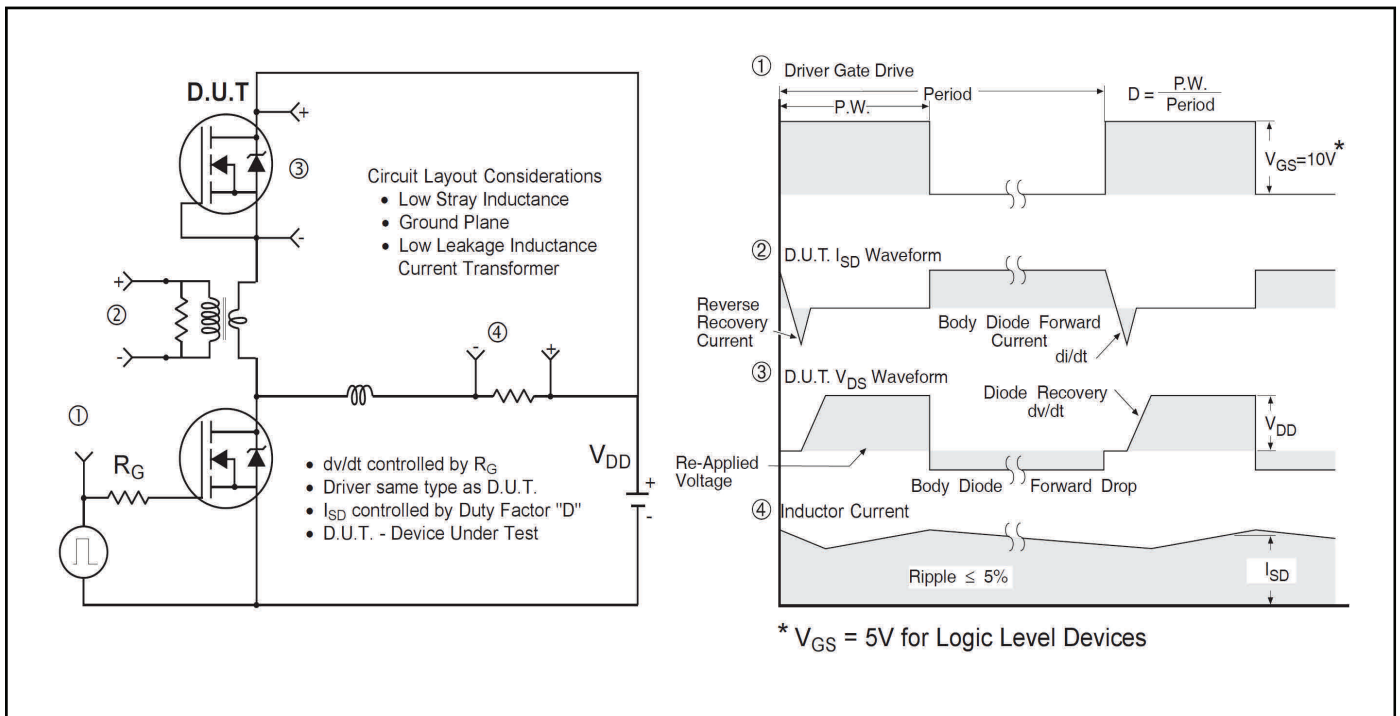


Figure 16 Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel Power MOSFETs

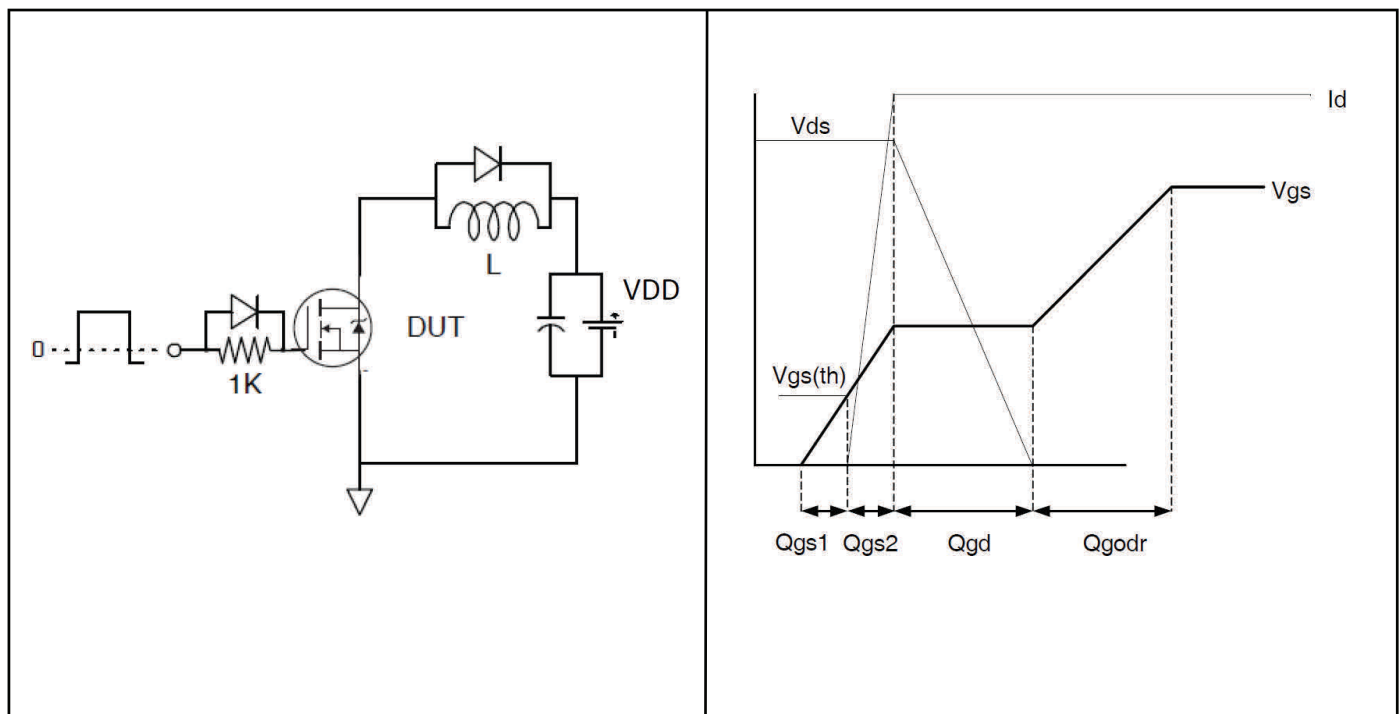
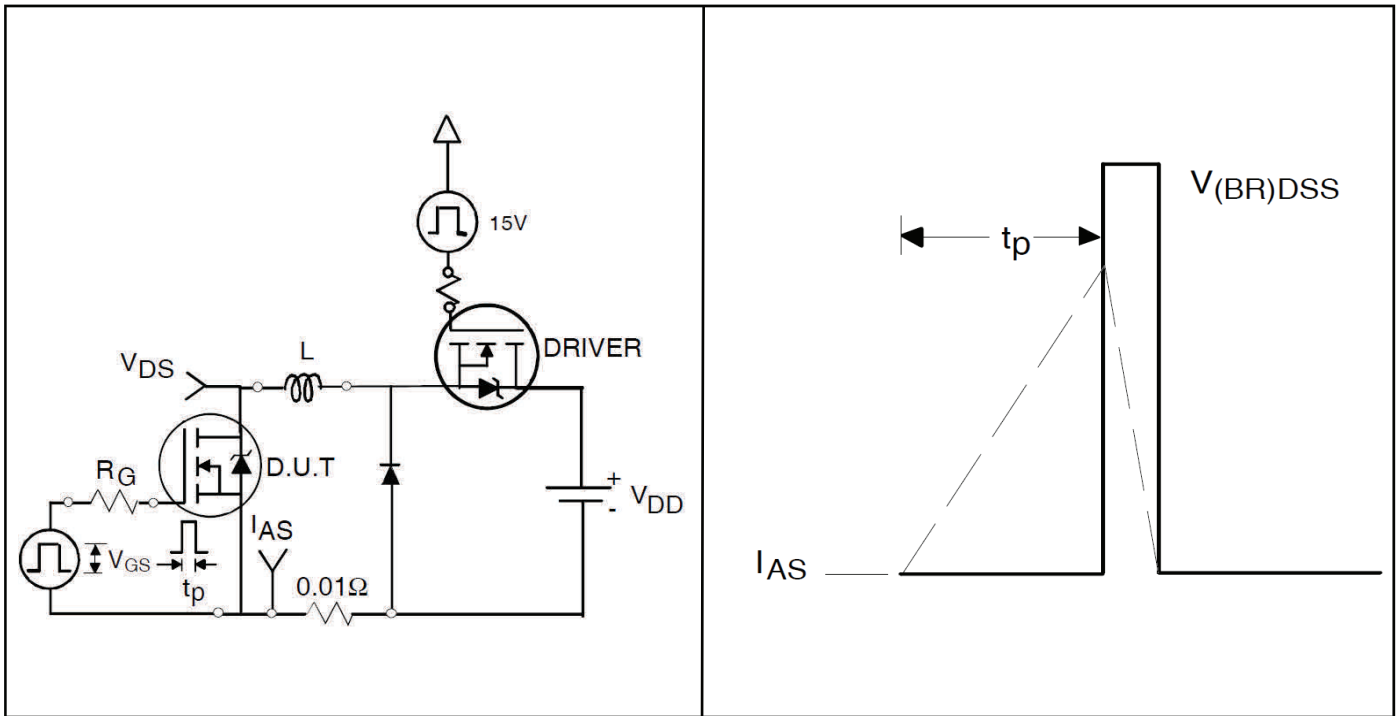


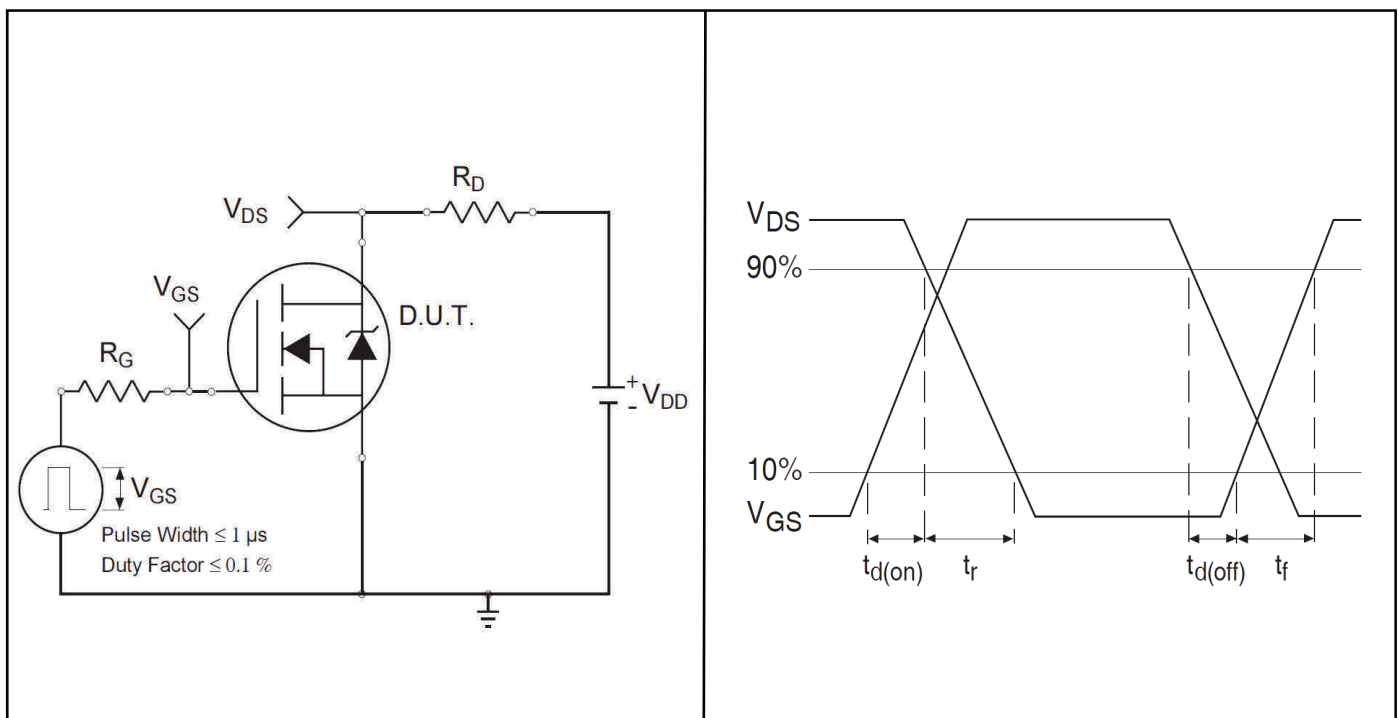
Figure 17a Gate Charge Test Circuit

Figure 17b Gate Charge Waveform



**Figure 18a Unclamped Inductive Test Circuit**

**Figure 18b Unclamped Inductive Waveforms**

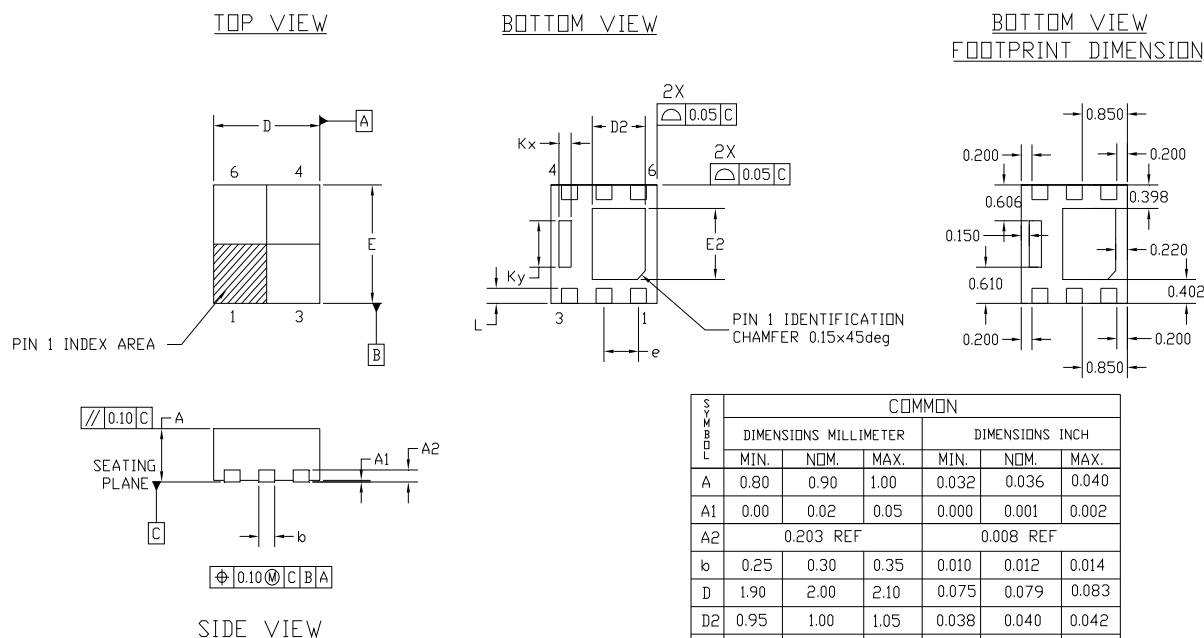


**Figure 19a Switching Time Test Circuit**

**Figure 19b Switching Time Waveforms**

## 5 Package Information

### PQFN 2 x 2 Outline Package Details



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.036	0.040
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.203 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	0.95	1.00	1.05	0.038	0.040	0.042
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	1.15	1.20	1.25	0.046	0.048	0.050
e	0.65 BSC			0.026 BSC		
L	0.20	0.25	0.30	0.008	0.010	0.012
Kx	0.23 REF			0.010 REF		
Ky	0.785 REF			0.031 REF		

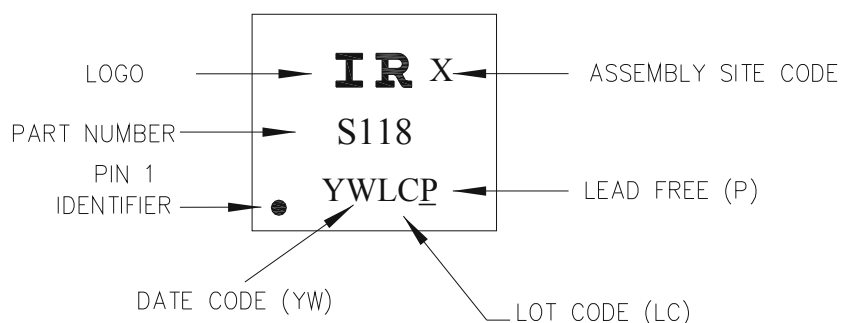
NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm. FROM TERMINAL TIP.

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.infineon.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.infineon.com/technical-info/appnotes/an-1154.pdf>

### PQFN 2 x 2 Part Marking



Note: For the most current drawing please refer to website at : [www.irf.com/package/](http://www.irf.com/package/)

# IRL60HS118

## Package Information

### PQFN 2 x 2 Tape and Reel

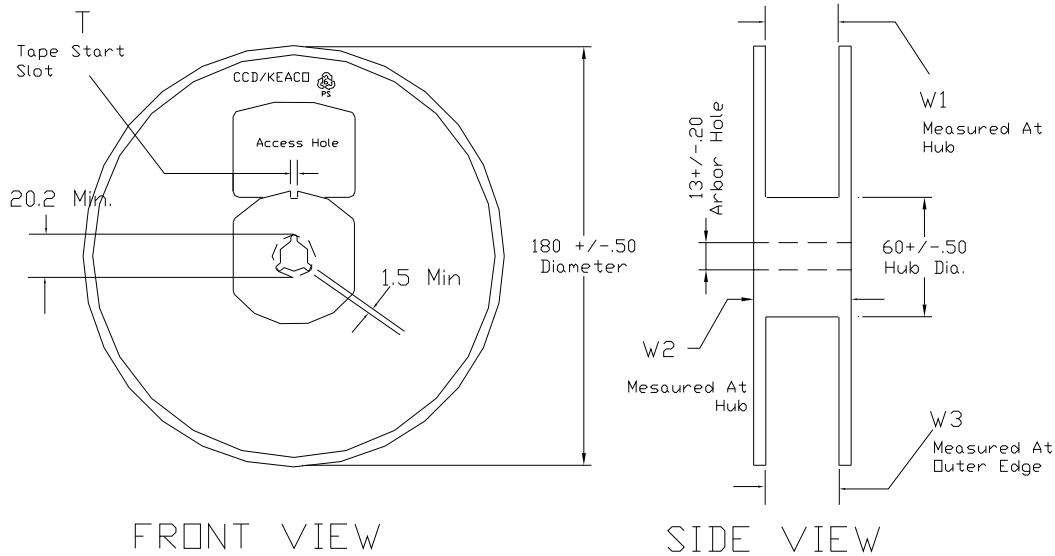
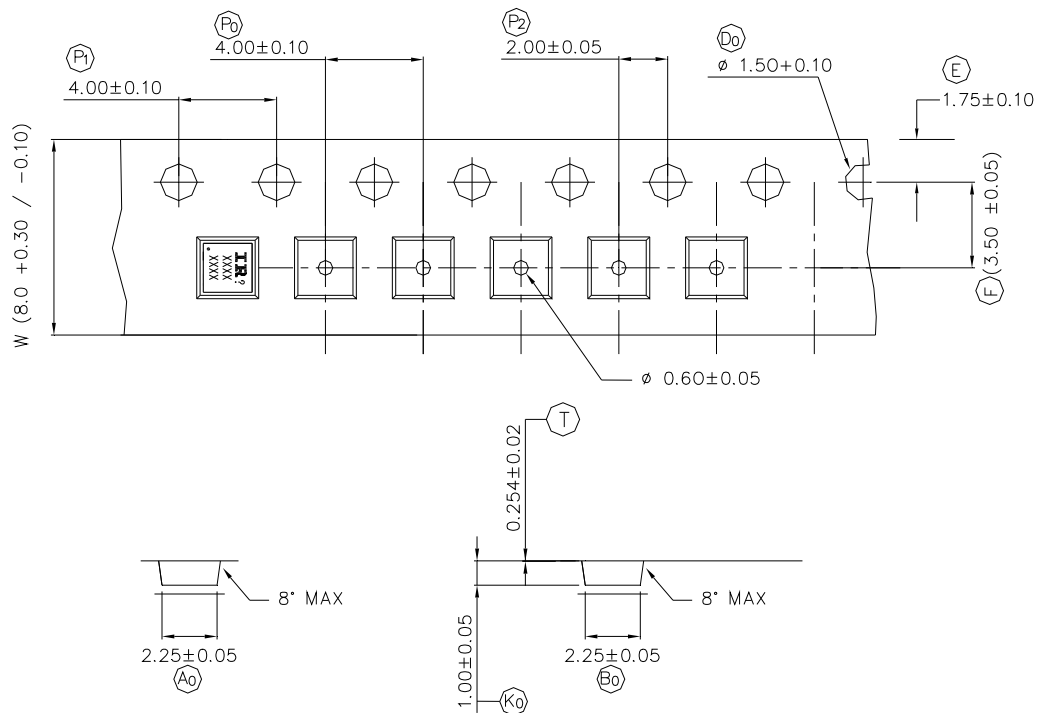


TABLE 1: REEL DETAILS

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is  $\geq 1 \times 10^5$  but  $< 1 \times 10^{12}$  ohm/sq.



NOTE: The Surface Resistivity is  $10^4 - 10^8$  OHM/SQ

Note: For the most current drawing please refer to website at : [www.irf.com/package/](http://www.irf.com/package/)

## 6 Qualification Information

**Qualification Information**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) †	
<b>Moisture Sensitivity Level</b>	PQFN 2 mm x 2 mm	MSL1 (per JEDEC J-STD-020D)†
<b>RoHS Compliant</b>	Yes	

† Applicable version of JEDEC standard at the time of product release.

## Revision History

### Major changes since the last revision

Page or Reference	Revision	Date	Description of changes
All pages	1.0	2016-09-16	<ul style="list-style-type: none"> <li>First release data sheet as Provisional.</li> </ul>
All pages	1.1	2016-10-17	<ul style="list-style-type: none"> <li>Added Switch Time test data.</li> <li>Datasheet released as Provisional.</li> </ul>
All page	2.0	2017-03-29	<ul style="list-style-type: none"> <li>Parts tested as Unique datasheet with revised current and all other tests</li> <li>Updated datasheet in new Infineon Template .</li> </ul>
All page	2.1	2018-05-08	<ul style="list-style-type: none"> <li>Corrected typo on part marking from “60HS118” to “S118” to matched actual marking on the devices –page12.</li> </ul>
All page	2.2	2019-12-13	<ul style="list-style-type: none"> <li>Features-Corrected from “IR MOSFET /OptiMOS™5” to “OptiMOS™5” to in line with the technology positioning of product –page 1.</li> </ul>

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**Edition 2015-05-06**  
**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

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