ROHM SEMICONDUCTOR

Technical Note

GPIO ICs

Keyencoder IC

BU1852GUW, BU1852GXW

No.11098EBT04

●Description

Keyencoder IC BU1852 can monitor up to 8x12 matrix (96 keys), which means to be adaptable to Qwerty keyboard. We adopt the architecture that the information of the only key which status is changed, like push or release, is encoded into the 8 bits data. This can greatly reduce the CPU load which tends to become heavier as the number of keys increase. (Previously, all key's status is stored in the registers.) When the number of keys is small, the extra ports can be used as GPIO. Furthermore, auto sleep function contributes to low power consumption, when no keys are pressed. It is also equipped with the various functions such as ghost key rejection, N-key Rollover, Built-in power on reset and oscillator.

●Features

1) Monitor up to 96 matrix keys.
2) Under 3µA Stand-by Current
3) Built-in Power on Reset.
4) Ghost key rejection.
5) Keyscan / GPIO selectable
6) 3 volt tolerant Input

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Conditions
Supply Voltage	VDD	-0.3 ~ +2.5	V	VDD≦VDDIO
	VDDIO	-0.3 ~ +4.5	V	
Input voltage	VI1	-0.3 ~ VDD +0.3※1	V	XRST, XI, TW, PORENB
	VI2	-0.3 ~ VDDIO +0.3※1	V	ADR
	VIT	-0.3 ~ +4.5	V	XINT, SCL, SDA, COL[11:0], ROW[7:0]
Storage temperature range	Tstg	-55 ~ +125	℃	
Package power	PD	272※2	mW	

※ This IC is not designed to be X-ray proof.
※1 It is prohibited to exceed the absolute maximum ratings even including +0.3 V.
※2 Package dissipation will be reduced each 2.72mW/℃ when the ambient temperature increases beyond 25℃.

●Operating conditions

Parameter	Symbol	Ratings			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage range (VDD)	VDD	1.65	1.80	1.95	V	
Supply voltage range (VDDIO)	VDDIO	1.65	1.80	3.60	V	
Input voltage range	VI1	-0.2	-	VDD+0.2	V	XRST, XI, TW, PORENB
	VI2	-0.2	-	VDDIO+0.2	V	ADR
	VIT	-0.2	-	3.60	V	XINT, SCL, SDA, COL[11:0], ROW[7:0]
Operating temperature range	Topr	-30	25	+85	℃	

●Electrical characteristics

1. DC characteristics (VDD=1.8V, VDDIO=1.8V, Ta=25℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Input H Voltage1	V_{IH1}	0.8xVDD	-	3.6	V	※1
Input H Voltage2	V_{IH2}	0.8xVDD	-	VDD+0.2	V	※2
Input H Voltage3	V_{IH3}	0.8xVDDIO	-	3.6	V	COL[11:0]
Input H Voltage4	V_{IH4}	0.8xVDDIO	-	VDDIO+0.2	V	ADR
Input L Voltage1	V_{IL1}	-0.2	-	0.2xVDD	V	※3
Input L Voltage2	V_{IL2}	-0.2	-	0.2xVDDIO	V	ADR, COL[11:0]
Input H Current1	I_{IH1}	-1.0	-	1.0	µA	V_{IN}=3.60V※4 Pull-down/up OFF
Input H Current2	I_{IH2}	-1.0	-	1.0	µA	V_{IN}=1.80V※5
Input L Current	I_{IL}	-1.0	-	1.0	µA	V_{IN}=0V Pull-down/up OFF
Output H Voltage1	V_{OH1}	0.75xVDD	-	-	V	I_{OH}=-2mA, ROW[7:0]
Output H Voltage2	V_{OH2}	0.75xVDDIO	-	-	V	I_{OH}=-2mA, COL[11:0]
Output L Voltage1	V_{OL1}	-	-	0.25xVDD	V	I_{OL}=2mA, ※6
Output L Voltage2	V_{OL2}	-	-	0.25xVDDIO	V	I_{OL}=2mA, COL[11:0]

※1 XINT,SCL,SDA,ROW[7:0]
※2 XRST,XI,TW,PORENB
※3 XINT,SCL,SDA,ROW[7:0],XRST,XI,TW,PORENB
※4 XINT,SCL,SDA,ROW[7:0],COL[11:0]
※5 XRST,XI,TW,PORENB,ADR
※6 XINT,SDA,ROW[7:0]

2. Circuit Current (VDD=1.8V, VDDIO=1.8V, Ta=25℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Power Down Current (VDD)	I_{PD}	-	-	1.0	µA	XRST=VSS
Power Down Current (VDDIO)	I_{PDIO}	-	-	1.0	µA	
Standby Current1 (VDD)	I_{STBY1}	-	-	3.0	µA	XRST=VDD, PORENB=VSS, SCL=VDD, SDA=VDD
Standby Current1 (VDDIO)	$I_{STBYIO1}$	-	-	1.0	µA	
Standby Current2 (VDD)	I_{STBY2}	-	-	1.0	µA	XRST=VDD, PORENB=VDD, SCL=VDD, SDA=VDD
Standby Current2 (VDDIO)	$I_{STBYIO2}$	-	-	1.0	µA	
Operating Current (VDD)	I_{OP}	-	50	110	µA	Internal oscillator is used. one key is pressed.

3. I²C AC Characteristics

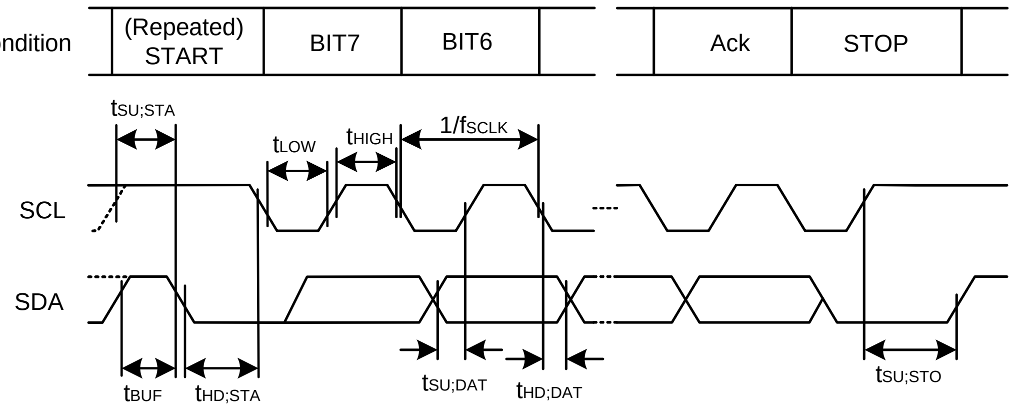


Fig.1 I²C AC timing

VDD=1.8V, VDDIO=1.8V, Topr=25℃, TW=VSS

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
SCL Clock Frequency	f_{SCL}	-	-	400	kHz	
Bus free time	t_{BUF}	1.3	-	-	µs	
(Repeated) START Condition Setup Time	$t_{SU;STA}$	0.6	-	-	µs	
(Repeated) START Condition Hold Time	$t_{HD;STA}$	0.6	-	-	µs	
SCL Low Time	t_{LOW}	1.3	-	-	µs	
SCL High Time	t_{HIGH}	0.6	-	-	µs	
Data Setup Time	$t_{SU;DAT}$	100	-	-	ns	
Data Hold Time	$t_{HD;DAT}$	0	-	-	ns	
STOP Condition Setup Time	$t_{SU;STO}$	0.6	-	-	µs	

4. GPIO AC Characteristics

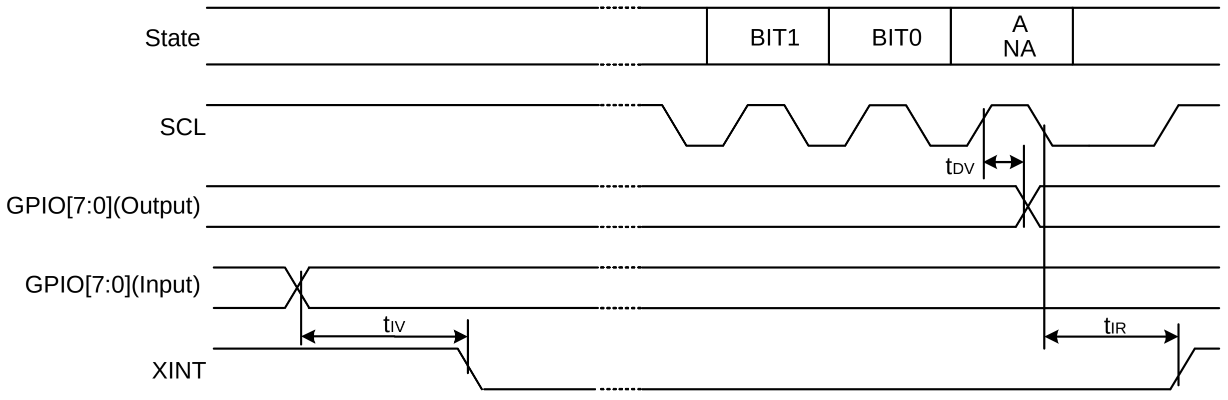


Fig.2 GPIO AC timing

VDD=1.8V, VDDIO=1.8V, Topr=25℃, TW=VSS

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Output Data Valid Time	t_{DV}	-	-	0.8	μs	
Interrupt Valid Time	t_{IV}	-	-	5	μs	
Interrupt Reset Time	t_{IR}	-	-	5	μs	

5. Startup sequence

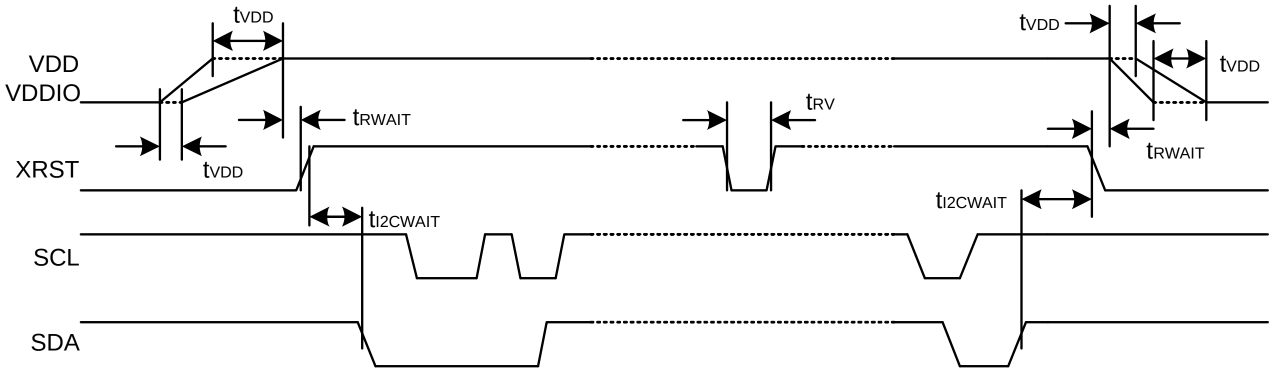


Fig.3 Start Sequence timing

VDD=1.8V, VDDIO=1.8V, Topr=25℃, TW=VSS

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
VDD Stable Time	t_{VDD}	-	-	5	ms	VDD and VDDIO are ON at the same time.
Reset Wait Time	t_{RWAIT}	0	-	-	µs	XRST controlling※1
Reset Valid Time	t_{RV}	10	-	-	µs	
I²C Wait Time	$t_{I2CWAIT}$	10	-	-	µs	

※1 Even if XRST port is not used, it operates because Power On Reset is built in.
In this case, connect XRST port with VDD on the set PCB.

Note) At VDD=0V, when SCL port is changed from 0V to 0.5V or more, SCL port pulls the current. It is same in SDA, XINT, and ROW[7:0] ports of 3V tolerant I/O. (VDDIO=0V in case of COL[11:0] ports)

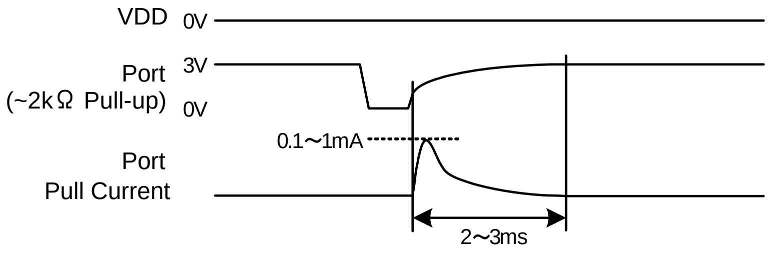


Fig.4 Port operating at VDD=0V

●**Package Specification**

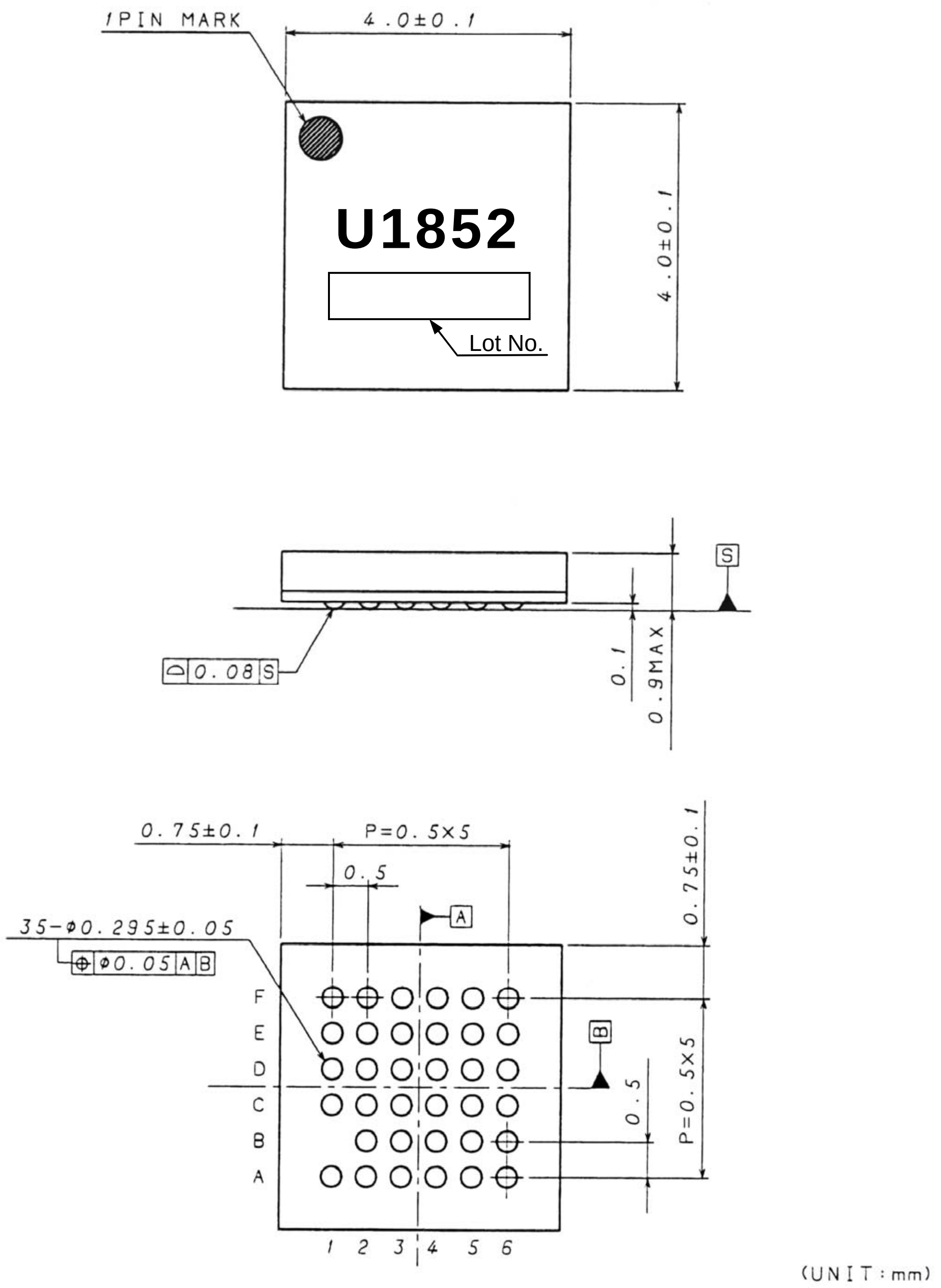


Fig.5 Package Specification (VBGA035W040)

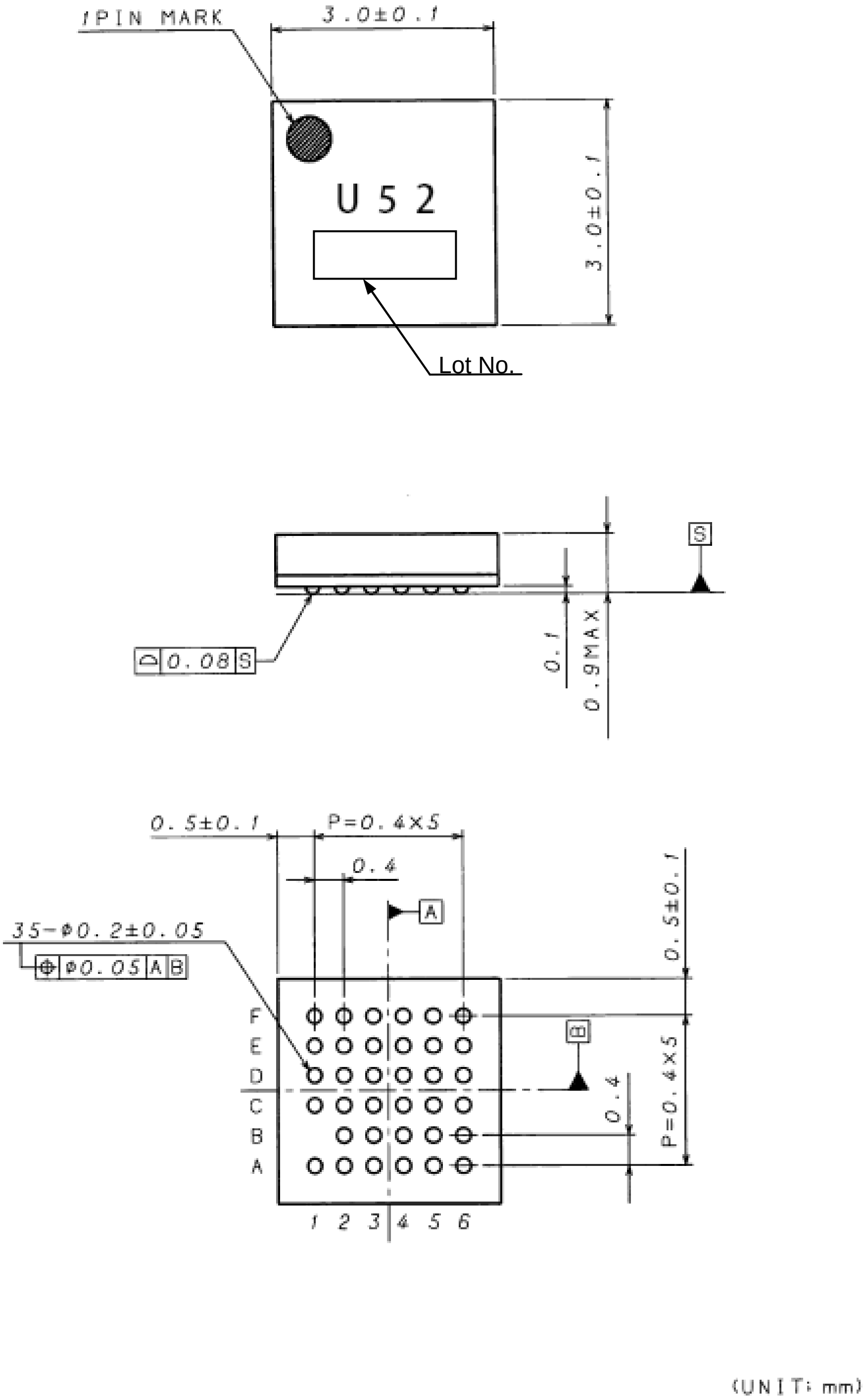


Fig.6 Package Specification (UBGA035W030)

●Pin Assignment

	1	2	3	4	5	6
A	TESTM0	XI	ROW0	ROW2	ROW4	TW
B		XRST	ROW1	ROW3	ROW6	ROW5
C	XINT	VDD	PORENB	VSS	ROW7	COL0
D	SDA	VDD	VDDIO	VSS	COL2	COL1
E	SCL	COL10	COL8	COL6	COL4	COL3
F	TESTM1	COL11	COL9	COL7	COL5	ADR

Fig.7 Pin Diagram (Top View)

●Block diagram

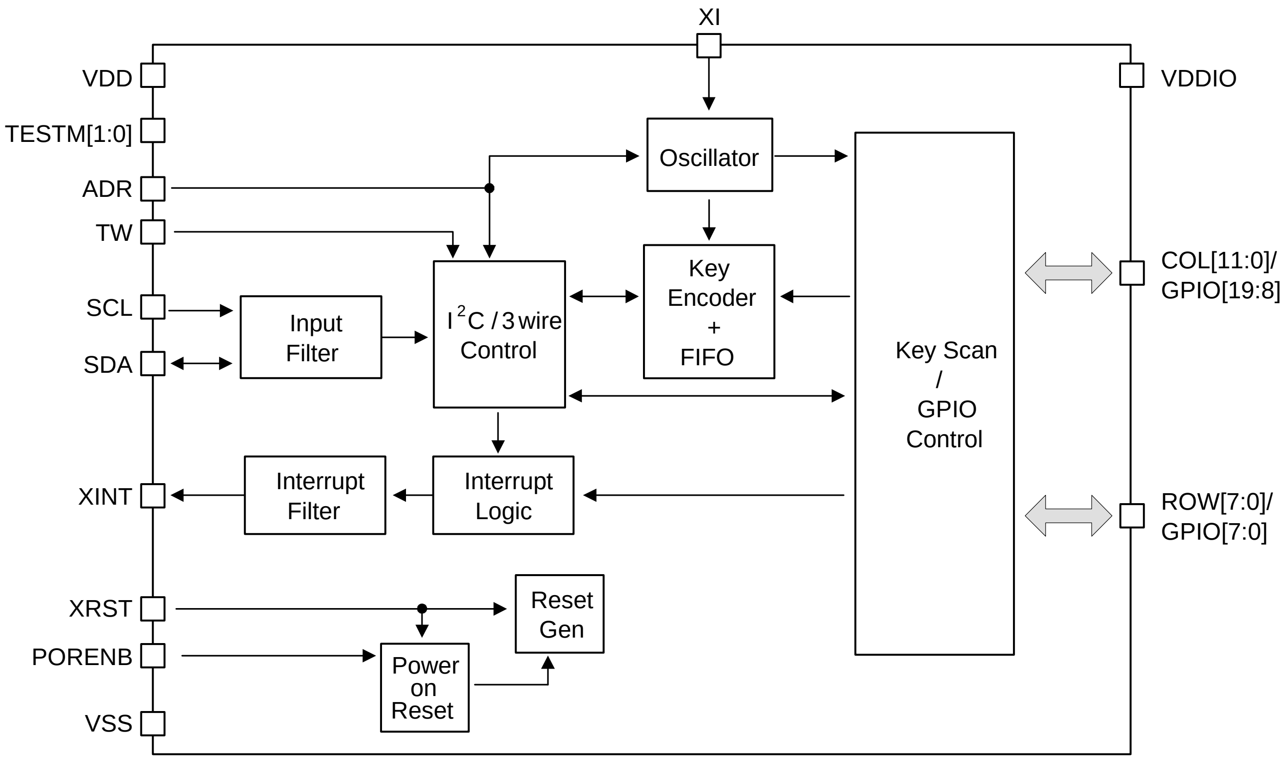


Fig.8 Functional Block Diagram

●**Pin Functional Descriptions**

PIN name	I/O	Function	Init	Cell Type
VDD	-	Power supply (Core, I/O except for COL[11:0], ADR)	-	-
VDDIO	-	Power supply (I/O for COL[11:0], ADR)	-	-
VSS	-	GND	-	-
XRST	I	Reset(Low Active)	I	A
XI	I	External clock input (32kHz)	I	I
TW	I	Select protocol H: original 3 wire L: I^2C	I	B
ADR	I	(TW=L) Select Device Address for I^2C (TW=H) H : Key scan rate 1/2 L : Key scan rate original	I	B
XINT	O	Key/GPIO Interrupt	H(TW=H) Hi-z(TW=L)	E
SCL	I	Clock for serial interface	I	D
SDA	I/O	Serial data inout for serial interface	I	F
ROW0	I/O	ROW0 / GPIO0	I [100kΩ Pull-up]	G
ROW1	I/O	ROW1 / GPIO1		
ROW2	I/O	ROW2 / GPIO2		
ROW3	I/O	ROW3 / GPIO3		
ROW4	I/O	ROW4 / GPIO4		
ROW5	I/O	ROW5 / GPIO5		
ROW6	I/O	ROW6 / GPIO6		
ROW7	I/O	ROW7 / GPIO7		
COL0	I/O	COL0 / GPIO8	L(TW=H) I [150kΩ Pull-down] (TW=L)	H
COL1	I/O	COL1 / GPIO9		
COL2	I/O	COL2 / GPIO10		
COL3	I/O	COL3 / GPIO11		
COL4	I/O	COL4 / GPIO12		
COL5	I/O	COL5 / GPIO13		
COL6	I/O	COL6 / GPIO14		
COL7	I/O	COL7 / GPIO15		
COL8	I/O	COL8 / GPIO16		
COL9	I/O	COL9 / GPIO17		
COL10	I/O	COL10 / GPIO18		
COL11	I/O	COL11 / GPIO19		
PORENB	I	Power on reset enable (Low Active)	I	B
TESTM0	I	Test Pins※1	I	C
TESTM1	I			

※1 Note: All these pins must be tied down to GND in normal operation.

●**I/O equivalence circuit**

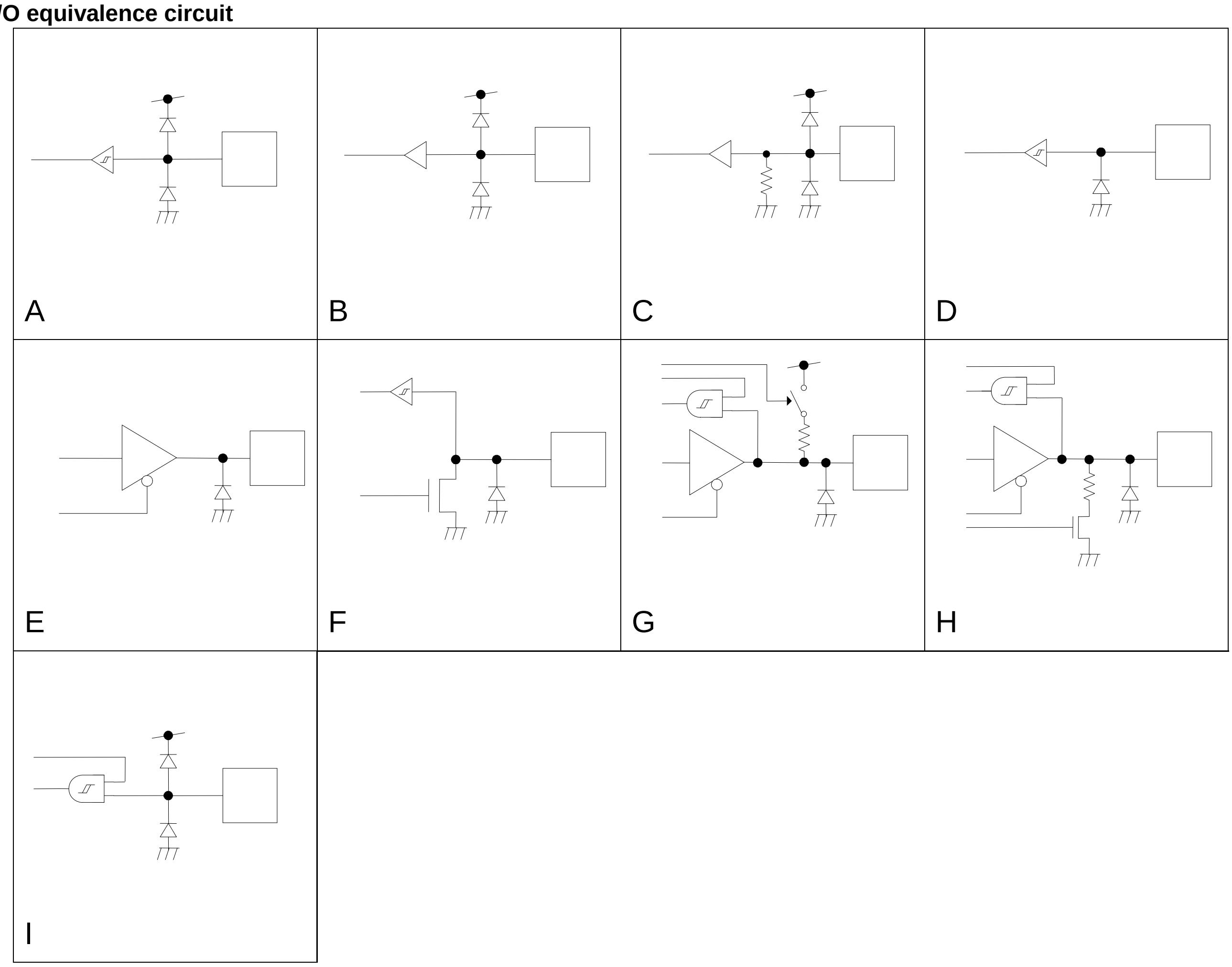


Fig.9 Equivalent I/O circuit diagram

●Functional Description

1. Power mode

The device enters the state of Power Down when XRST=”0”. When XRST becomes High after powered, the device enters the standby state.

Power On Reset

A Power On Reset logic is implemented in this device. Therefore, it will operate correctly even if the XRST port is not used. In this case, the XRST port must be connected to “1” (VDD), and the PORENB port must be connected to “0” (VSS). If you don’t want to use Power On reset, you must connect PORENB port to “1” (VDD).

Power Down State

The device enters Power Down state by XRST=”0”. An internal circuit is initialized, and key encoding and 3wire/I^2C interface are invalid. Power On Reset becomes inactive during this state.

Stand-by State

The device enters the stand-by state by setting XRST to "1". In this state, the device is waiting for keys pressed or I^2C communication (TW=”0”). When a key is pressed or I^2C start condition, the state will change to operation. Power On Reset is active in this state if PORENB = “0”.

Operating State

The device enters the operating state by pressing keys. The device will scan the key matrix and encode the key code, and then the 3wire/I^2C interface tries to start communication by driving XINT “0”. See next section for the details. After communicating with host device, when no keys are pressed, the device returns to the stand-by state. Power On Reset is active in this state if PORENB=”0”.

2. Protocol of serial interface

I^2C

When set to TW=”0”, SCL and SDA are used for I^2C communication. Any register shown in section 4 can be accessed through I^2C. Initially, all GPIO ports are set to GPI and pull-up/down ON. When the application requires GPO or key scan, proper register setting should be done through I^2C.

3 wire (Original)

When set to TW=”1”, SCL and SDA are used for original 3wire communication, which is not the standard interface. Any register shown in section 4 cannot be accessed through 3wire. With TW=”1”, only keyscan and key encoding are supposed to be performed. GPIO function is inactive. When the application needs kind of complex system (for instance, GPO+keyscan or GPIO+keyscan…), I2C mode is recommended.
See appendix for the details.

3. I^{2}C Bus Interface (TW="0")

Each function of GPIO is controlled by internal registers. The I^{2}C Slave interface is used to write or read those internal registers. The device supports 400kHz Fast-mode data transfer rate.

Slave address

Two device addresses (Slave address) can be selected by ADR port.

	A7	A6	A5	A4	A3	A2	A1	R/W
ADR=0	0	0	0	1	0	1	0	1/0
ADR=1	0	0	0	1	1	0	1	

Data transfer

One bit of data is transferred during SCL = "1". During the bit transfer SCL = "1" cycle, the signal SDA should keep the value. If SDA changes during SCL = "1", START condition or STOP condition occur and it is interpreted as a control signal.

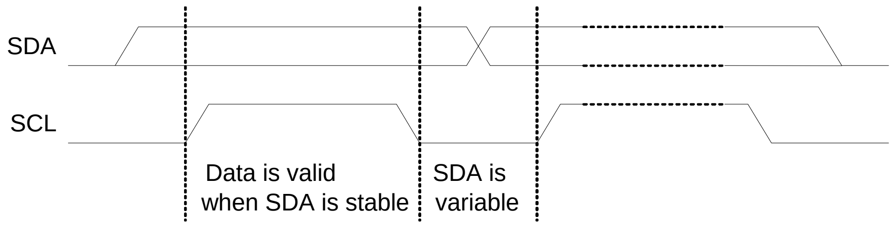


Fig.10 Data transfer

START・STOP・Repeated START conditions

When SDA and SCL are "1", the data isn't transferred on the I^{2}C bus. If SCL remains "1" and SDA transfers from "1" to "0", it means "Start condition" is occurred and access is started. If SCL remains "1" and SDA transfers from "0" to "1", it means "Stop condition" is occurred and access is stopped. It becomes repeated START condition (Sr) the START condition enters again although the STOP condition is not done.

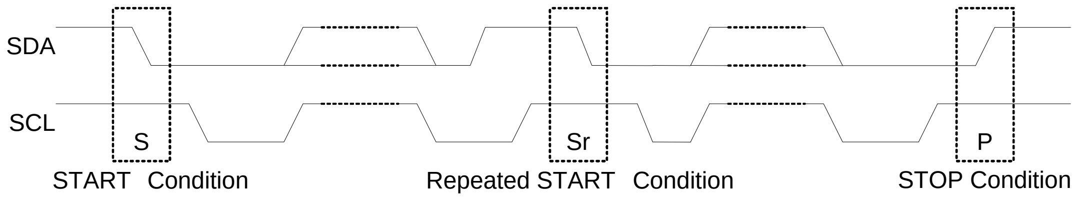


Fig.11 START・STOP・Repeated START conditions

Acknowledge

After start condition is occurred, 8 bits data will be transferred. SDA is latched by the rising edge of SCL. After 8 bits data transfer is finished by the “Master”, “Master” opens SDA to “1”. And then, “Slave” de-asserts SDA to “0” as “Acknowledge”.

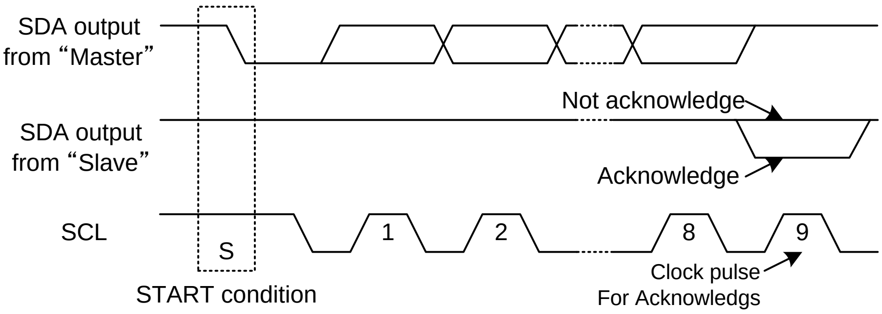


Fig.12 Acknowledge

Writing protocol

Register address is transferred after one byte of slave address with R/W bit. The 3rd byte data is written to internal register which defined by the 2nd byte. However, when the register address increased to the final address (18h), it will be reset to (00h) after the byte transfer.

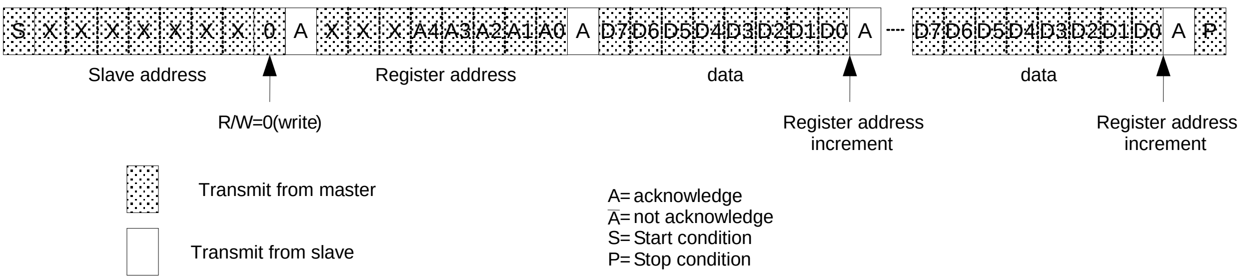


Fig.13 Writing protocol

Reading protocol

After Writing the slave address and Read command bit, the next byte is supposed to be read data. The reading register address is the next of the previous accessed address. Reading address is incremented one by one. When the incremented address reaches the last address, the following read address will be reset to (00h).

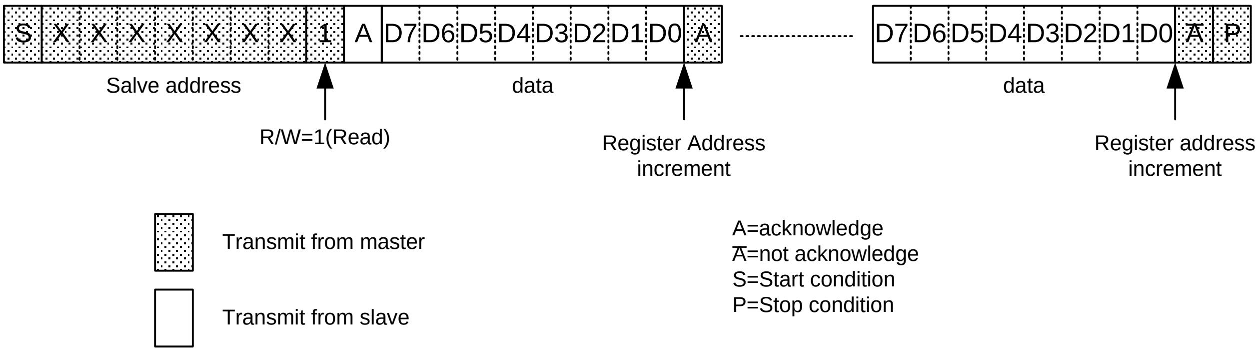


Fig.14 Readout protocol

Complex reading protocol

There is the complex reading protocol to read the specific address of registers that master wants to read.
After the specifying the internal register address as writing command, master occurs repeated START condition with read command. Then, the reading access of the specified registers is supposed to start. The register address increment is the same as normal reading protocol. If the address is increased to the last, it will be reset to (00h).

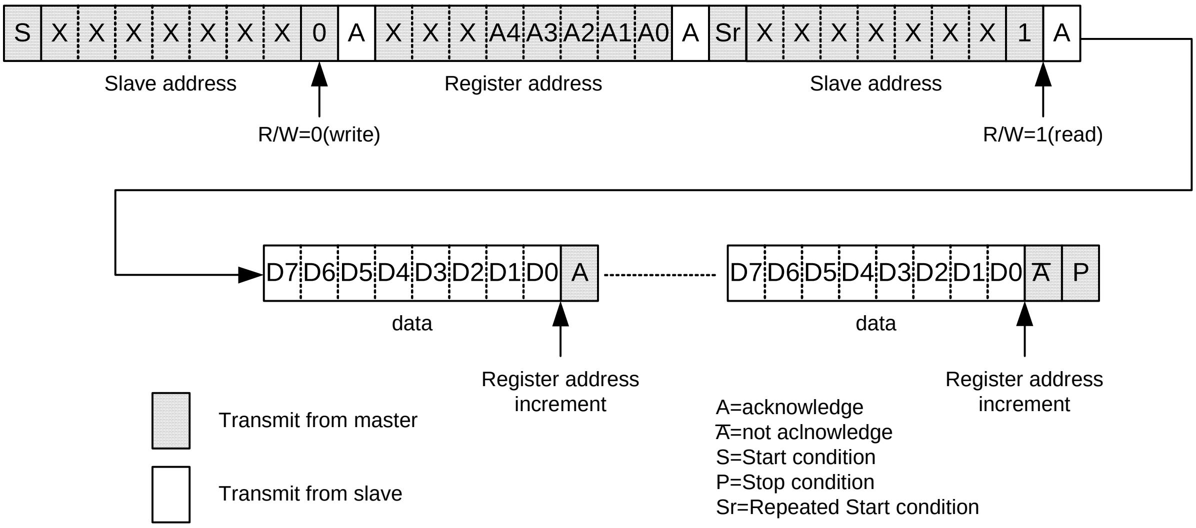


Fig.15 Complex reading protocol

Illegal access of I^2C

When illegal access happens, the data is annulled.
The illegal accesses are as follows.

- The START condition or the STOP condition is continuously generated.
- When the Slave address and the R/W bit are written, repeated START condition or the STOP condition are generated.
- Repeated START condition or the STOP condition is generated while writing data.

4. Register configuration

Table1 shows the register map and Table2 indicates each function in the corresponding bit. Only when TW is “0”, these registers can be accessed with I^2C. By making XRST “0”, the setting register value will be initialized shown in following register map.

Table1 Register map

Address	Init	Type	D7	D6	D5	D4	D3	D2	D1	D0
00h	00h	R/W	RESET	reserved	reserved	reserved	reserved	reserved	reserved	reserved
01h	00h	R/W	reserved	reserved	reserved	reserved	reserved	reserved	reserved	CLKSEL
02h	11h	R/W	reserved	KS_RATE *1						
03h	00h	R/W	reserved	reserved	reserved	reserved	KS_C11	KS_C10	KS_C9	KS_C8
04h	00h	R/W	KS_C7	KS_C6	KS_C5	KS_C4	KS_C3	KS_C2	KS_C1	KS_C0
05h	00h	R/W	KS_R7	KS_R6	KS_R5	KS_R4	KS_R3	KS_R2	KS_R1	KS_R0
06h	00h	R/W	reserved	reserved	reserved	reserved	IOD19	IOD18	IOD17	IOD16
07h	00h	R/W	IOD15	IOD14	IOD13	IOD12	IOD11	IOD10	IOD9	IOD8
08h	00h	R/W	IOD7	IOD6	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0
09h	00h	R/W	reserved	reserved	reserved	reserved	INTEN19	INTEN18	INTEN17	INTEN16
0Ah	00h	R/W	INTEN15	INTEN14	INTEN13	INTEN12	INTEN11	INTEN10	INTEN9	INTEN8
0Bh	00h	R/W	INTEN7	INTEN6	INTEN5	INTEN4	INTEN3	INTEN2	INTEN1	INTEN0
0Ch	00h	R/W	reserved	reserved	reserved	reserved	GPO19	GPO18	GPO17	GPO16
0Dh	00h	R/W	GPO15	GPO14	GPO13	GPO12	GPO11	GPO10	GPO9	GPO8
0Eh	00h	R/W	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0
0Fh	00h	R/W	reserved	reserved	reserved	reserved	XPD19	XPD18	XPD17	XPD16
10h	00h	R/W	XPD15	XPD14	XPD13	XPD12	XPD11	XPD10	XPD9	XPD8
11h	00h	R/W	XPU7	XPU6	XPU5	XPU4	XPU3	XPU2	XPU1	XPU0
12h	00h	R/W	reserved	reserved	reserved	reserved	reserved	reserved	reserved	INTFLT
13h	00h	-	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
14h	00h	R	keycode							
15h	00h	R	reserved	reserved	reserved	Reserved	reserved	reserved	fifo_ovf	fifo_ind
16h	00h	R	reserved	reserved	reserved	Reserved	GPI19	GPI18	GPI17	GPI16
17h	00h	R	GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8
18h	FFh	R	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0

*1 Do not write more than 0x7F in KS_RATE

※ Do not write “1” in the reserved resisters. The write commands to 13h-18h addresses’ registers are ignored.

Table2 Register function

Symbol	Address	Description
RESET	00h	Software reset. All registers are initialized by writing "1". This register value is returned to "0" automatically. Exceptionally, GPIn register is not initialized.
CLKSEL	01h	“1” : External clock from XI is used. “0” : Internal CR oscillator is used.
KS_RATE	02h	Key scan rate control
KS_Cx	03h-04h	When set to “1”, port is used as COLx for key scan. When set to “0”, it is used as GPIO port.
KS_Ry	05h	When set to “1”, port is used as ROWy for key scan. When set to “0”, it is used as GPIO port.
IODn	06h-08h	GPIOn’s IO direction. When set to “1”, GPIOn direction is output. When set to “0”, GPIOn direction is input.
INTENn	09h-0Bh	Interrupt of GPIOn port is enabled by "1". It is masked by "0".
GPOn	0Ch-0Eh	Output value of GPIOn port.
XPDn	0Fh-10h	Pull-down of GPIOn port is on by "0" and off by "1". GPIOn should be input.
XPUn	11h	Pull-up of GPIOn port is on by "0" and off by "1". GPIOn should be input.
INTFLT	12h	“1” : interrupt filter ON (1us pulse rejection) “0” : interrupt filter OFF (bypass)
keycode	14h	Keycode that Host can read currently
fifo_ind	15h	When there are keycode data in FIFO, fifo_ind is set to “1”. “0” means fifo empty.
fifo_ovf	15h	When FIFO overflow happens, fifo_ovf is set to “1”. Initially “0” is stored.
GPIn	16h-18h	Input value of GPIOn port. Write command is ignored. When interrupt happens, these registers must be read. Each bit is valid only when WRSELn=0(input). The bits at WRSELn=1(output) are fixed.

※"n" is the number of GPIO[19:0] ports. “x” is the number of COL[11:0]. “y” is the number of ROW[7:0].

5. GPIO function

GPIO configuration

When some ports of COL[11:0] and ROW[7:0] are needed to be used as GPIO, TW must be “0”. Then, set the proper value in the appropriate registers through I^2C. ROW[7:0] and COL[11:0] correspond to GPIO[7:0] and GPIO[19:8], respectively. By default, GPIO[19:0] ports are set to input(IODn=0) and Pull-up/down ON(XPUn/XPDn=0).
(n is the number of GPIO[19:0] ports.)

Refer to the following for the configuration of GPIO.

Table3 GPIO configuration

State of GPIO	Register		
	GPOn	IODn	XPDn/XPUn
Input, Pull-up/down ON	*	0	0
Input, Pull-up/down OFF	*	0	1
Output, H drive	1	1	*
Output, L drive	0	1	*
Output, Hi-Z※1	0	0	1

※1 It is required to pull-up to more than VDD potential.

How to deal with GPIO ports which are not using

When set to output, GPIO port must be open.
When set to input, don’t make GPIO port open. It must be forced by "0" or Pull-up/down on.

Interrupt configuration

The initial XINT output is Hi-Z, so it should be pull-up. When interrupt is generated, XINT port outputs L. By default, interrupt is masked with INTEN register "0". The bit to be used is made "1", and then the mask is released. In this case, IOD register should be "0"(input).

Write to GPIO port

After master sets the internal register address for write, the data is sent from MSB.
After Acknowledge is returned, the value of each GPIO port will be changed.
Write Configuration Pulse, which is trigger of changing registers, is generated at the timing of Acknowledge.

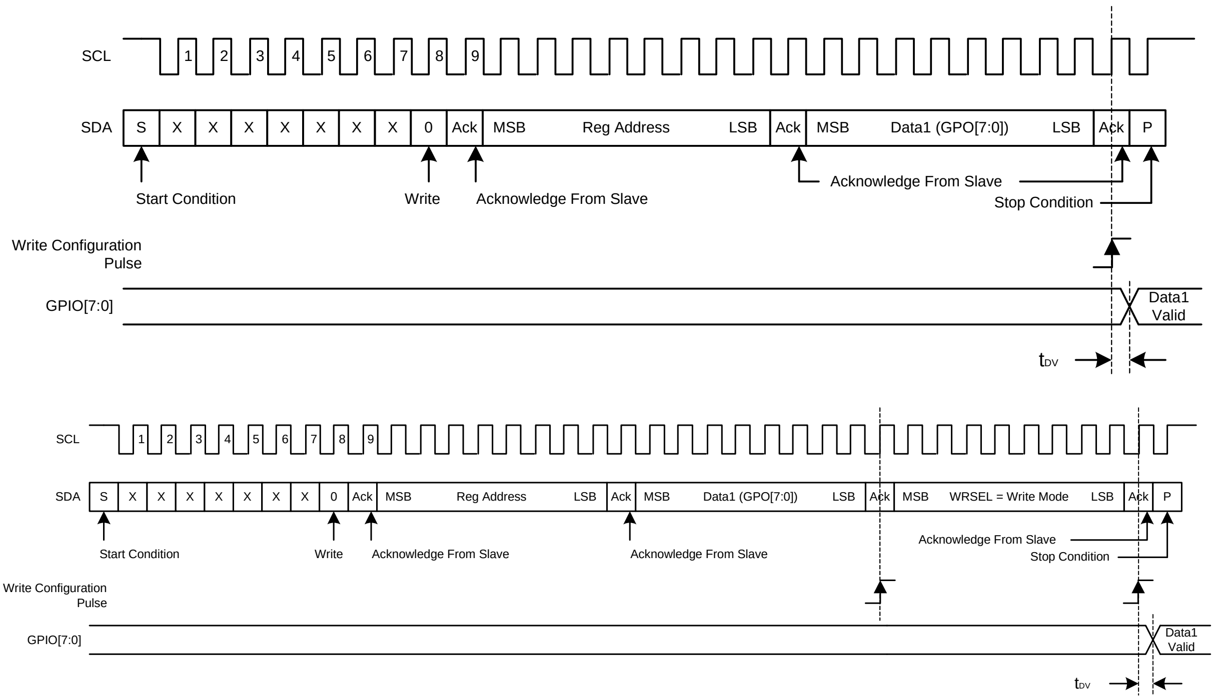


Fig.16 Write to GPIO port

Read from GPIO port

After writing of the Slave address and R/W bits by master, reading GPIO port procedure begins.
All ports' status that is set to the input by IOD registers are taken into the GPI register when ACK is sent.

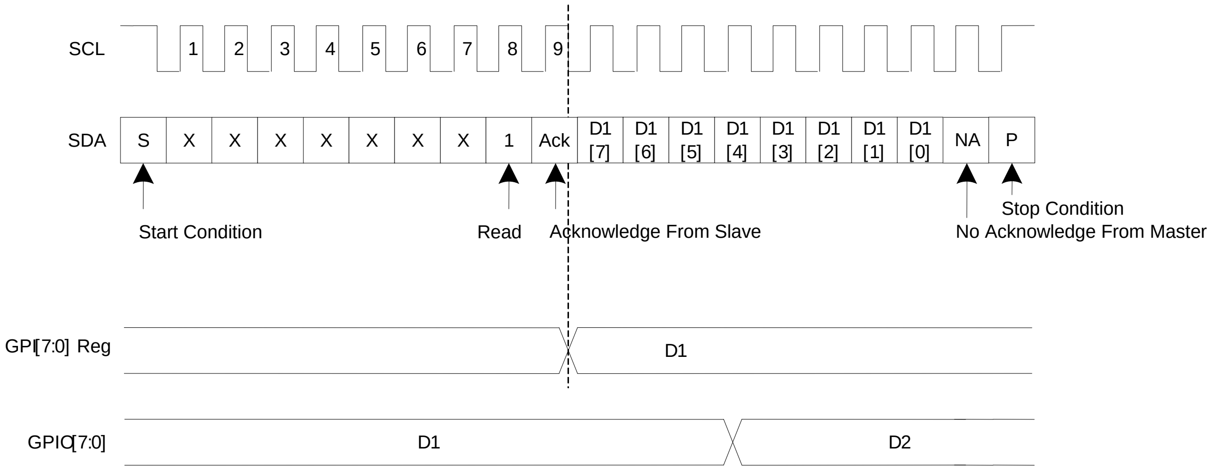


Fig.17 Read from GPIO port

Interrupt Valid/Reset

When the GPIO interrupt is used, some of INTEN registers are required to be written to "1".
When current GPIO port status becomes different from the value of the GPIn registers, XINT port is changed from "1" to "0". After reading GPI register, it will return to "1".

When Master detects interrupt, Master must read all GPI registers that is set to input(IODn=0), even if XINT is changed while reading. It is because BU1852 does not latch the XINT status. Fig.18 shows one of the example of using only ROW[7:0] as GPI. In this case, Master reads only 18h register immediate after detecting XINT.

XINT cannot distinguish whether just one port is different or multi ports are different from the previous value. Master is necessary to store the previous GPI register value and compare it with the current value after XINT is asserted.

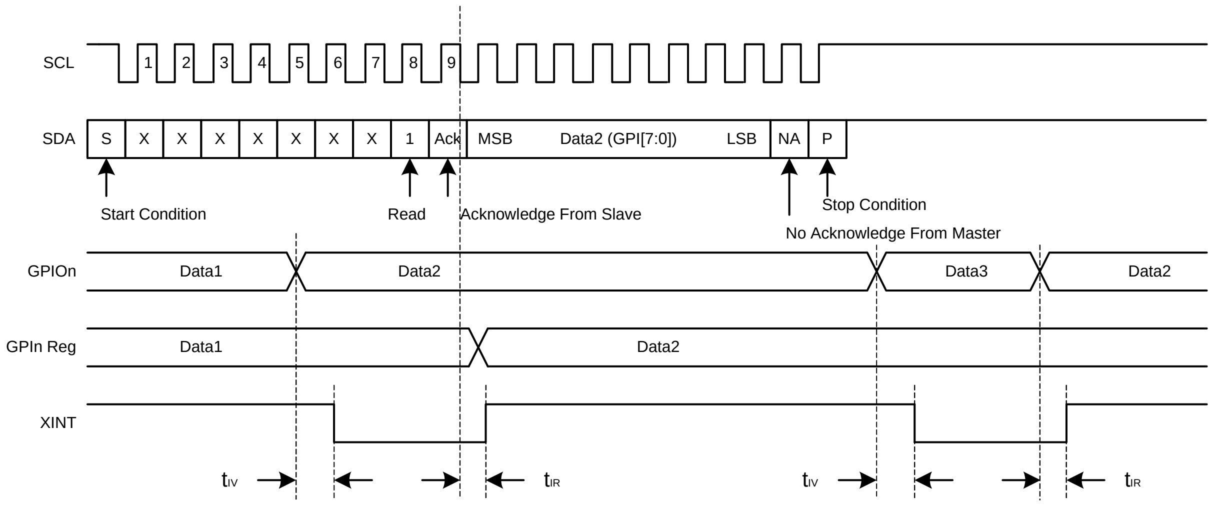


Fig.18 Interrupt Valid/Reset (Example : ROW[7:0] as GPI with interrupt)

6. Key code Assignment

Table 4 shows the key code assignment. These key codes are sent through 3wire or I^2C corresponding to the pushed or released keys.

Table4 Key codes

		ROW0	ROW1	ROW2	ROW3	ROW4	ROW5	ROW6	ROW7
COL0	M	0x01	0x11	0x21	0x31	0x41	0x51	0x61	0x71
	B	0x81	0x91	0xA1	0xB1	0xC1	0xD1	0xE1	0xF1
COL1	M	0x02	0x12	0x22	0x32	0x42	0x52	0x62	0x72
	B	0x82	0x92	0xA2	0xB2	0xC2	0xD2	0xE2	0xF2
COL2	M	0x03	0x13	0x23	0x33	0x43	0x53	0x63	0x73
	B	0x83	0x93	0xA3	0xB3	0xC3	0xD3	0xE3	0xF3
COL3	M	0x04	0x14	0x24	0x34	0x44	0x54	0x64	0x74
	B	0x84	0x94	0xA4	0xB4	0xC4	0xD4	0xE4	0xF4
COL4	M	0x05	0x15	0x25	0x35	0x45	0x55	0x65	0x75
	B	0x85	0x95	0xA5	0xB5	0xC5	0xD5	0xE5	0xF5
COL5	M	0x06	0x16	0x26	0x36	0x46	0x56	0x66	0x76
	B	0x86	0x96	0xA6	0xB6	0xC6	0xD6	0xE6	0xF6
COL6	M	0x07	0x17	0x27	0x37	0x47	0x57	0x67	0x77
	B	0x87	0x97	0xA7	0xB7	0xC7	0xD7	0xE7	0xF7
COL7	M	0x08	0x18	0x28	0x38	0x48	0x58	0x68	0x78
	B	0x88	0x98	0xA8	0xB8	0xC8	0xD8	0xE8	0xF8
COL8	M	0x09	0x19	0x29	0x39	0x49	0x59	0x69	0x79
	B	0x89	0x99	0xA9	0xB9	0xC9	0xD9	0xE9	0xF9
COL9	M	0x0A	0x1A	0x2A	0x3A	0x4A	0x5A	0x6A	0x7A
	B	0x8A	0x9A	0xAA	0xBA	0xCA	0xDA	0xEA	0xFA
COL10	M	0x0B	0x1B	0x2B	0x3B	0x4B	0x5B	0x6B	0x7B
	B	0x8B	0x9B	0xAB	0xBB	0xCB	0xDB	0xEB	0xFB
COL11	M	0x0C	0x1C	0x2C	0x3C	0x4C	0x5C	0x6C	0x7C
	B	0x8C	0x9C	0xAC	0xBC	0xCC	0xDC	0xEC	0xFC

M : Make Key (the code when the key is pressed)
B : Break Key (the code when the key is released)

7. Ghost Key Rejection

Ghost key is an inevitable phenomenon as long as key-switch matrices are used. When three switches located at the corners of a certain matrix rectangle are pressed simultaneously, the switch that is located at the last corner of the rectangle (the ghost key) also appears to be pressed, even though the last key is not pressed. This occurs because the ghost key switch is electrically shorted by the combination of the other three switches (Fig.19). Because the key appears to be pressed electrically, it is impossible to distinguish which key is the ghost key and which key is pressed. The BU1852 solves the ghost key problem to use the simple method. If BU1852 detects any three-key combination that generates a fourth ghost key, and BU1852 does not report anything, indicating the ghost keys are ignored. This means that many combinations of three keys are also ignored when pressed at the same time. Applications requiring three-key combinations (such as <Ctrl><Alt><Del>) must ensure that the three keys are not wired in positions that define the vertices of a rectangle (Fig. 20). There is no limit on the number of keys that can be pressed simultaneously as long as the keys do not generate ghost key events.

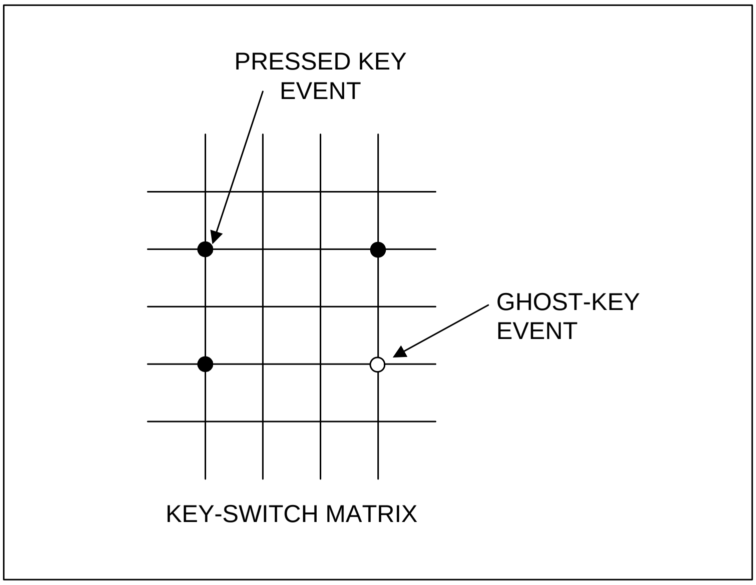


Fig.19 Ghost key phenomenon

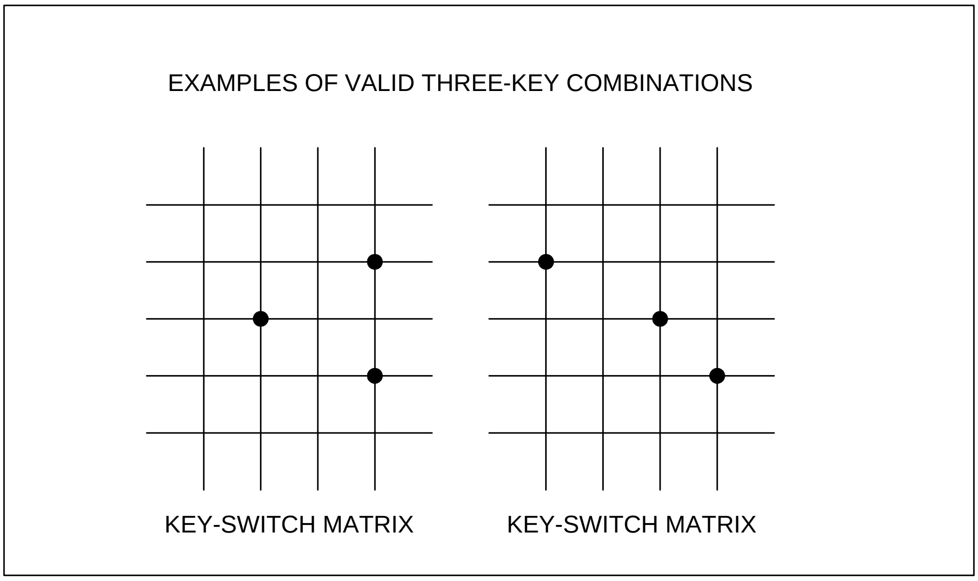


Fig.20 Valid three key combinations

8. Recommended flow

Fig.21 shows the recommended flow when TW=0(I^2C protocol is selected).

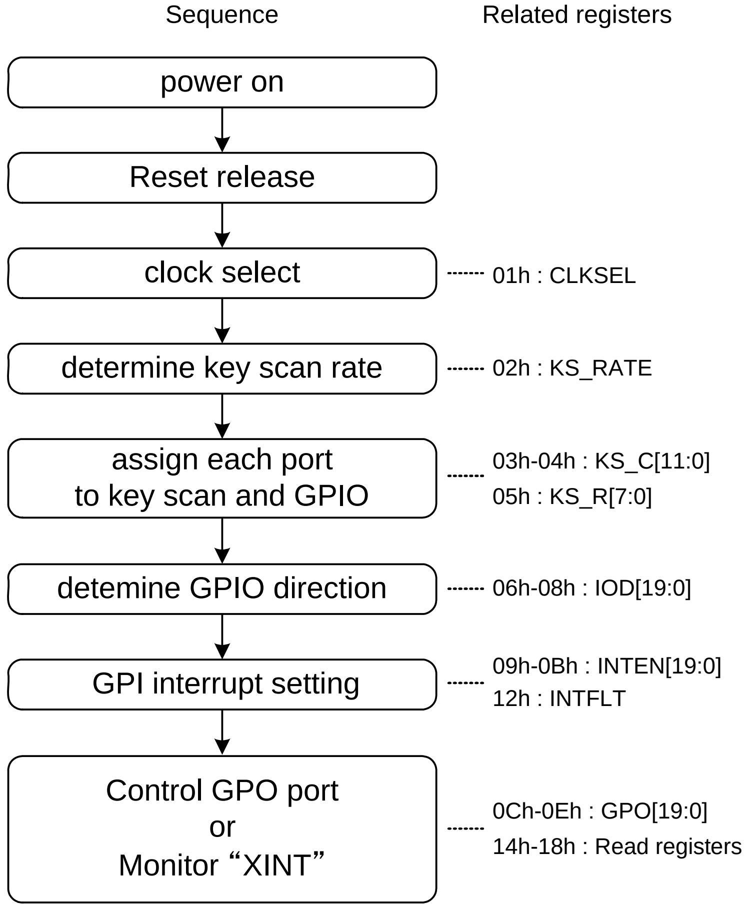


Fig.21 Recommended flow and related registers

Forbidden operation:

--- Dynamic change of TW (I^2C/3wire protocol should be fixed)
--- Dynamic assignment change of keyscan and GPIO (should be determined initially)
--- Dynamic change of keyscan rate (should be determined initially)
--- Dynamic change of CLKSEL (should be determined initially)

●**Application circuit example**

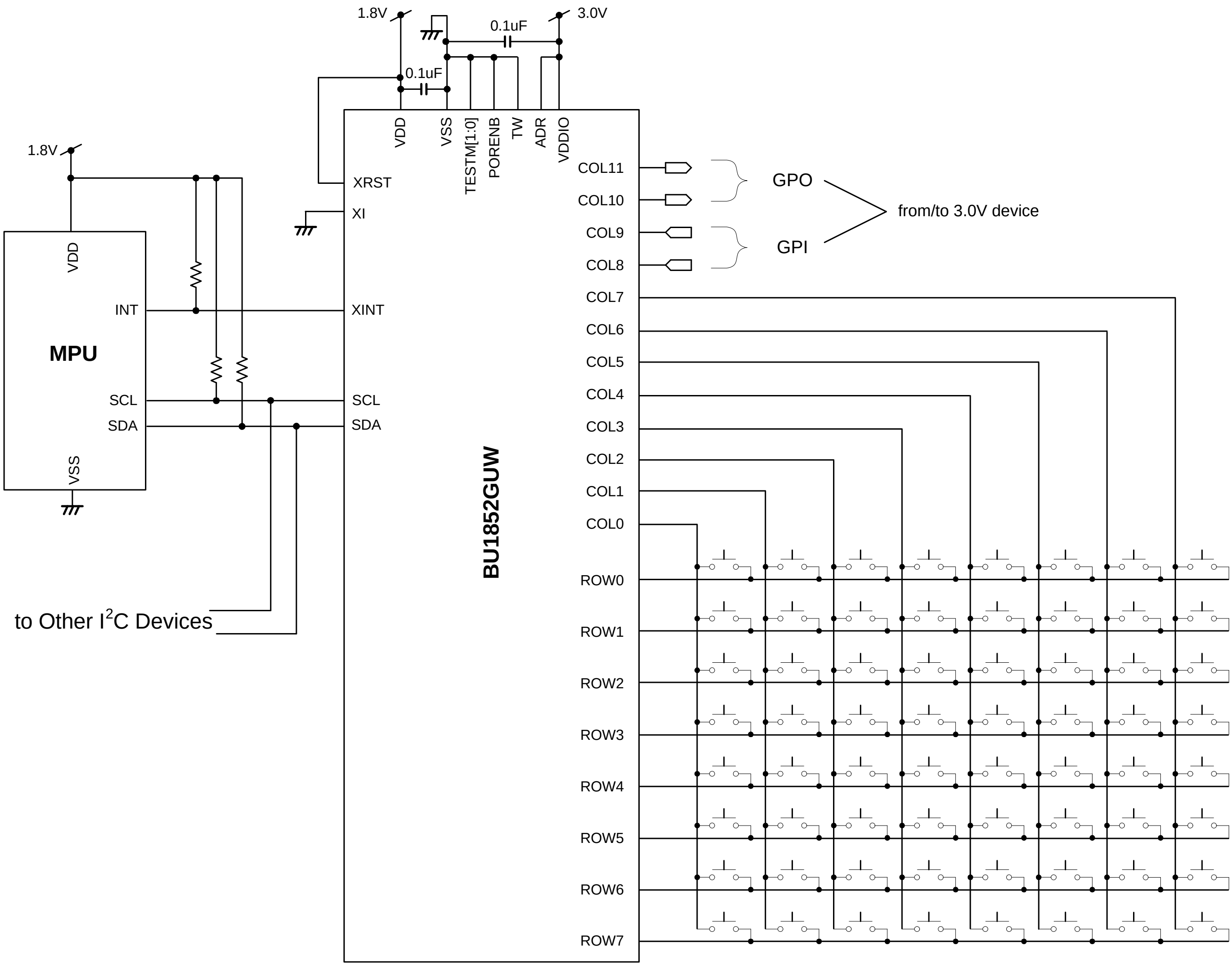


Fig.22 Application circuit example

●Appendix

1. 3wire Interface (TW=”1”)

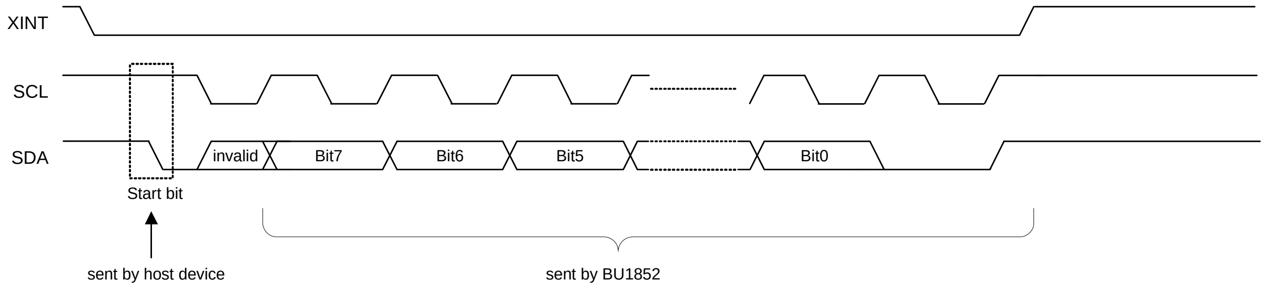


Fig.23 3wire protocol

Figure 23 shows the original 3wire protocol of BU1852. When this 3wire protocol is used, TW must be “1”. Note that this 3wire interface is completely different from I^2C and other standard bus interface.

<u>Procedure</u>

1. When BU1852 detects key events, XINT interrupt is generated to host with driving Low.
2. After the host detects XINT interrupt, the host is supposed to send start bit.
3. After BU1852 detects start bit, the 8bit data (key code) transmission on SDA will start synchronized with the rising edge of SCL clock signal, which is sent from the host.
4. 8 bit data are followed by “0” (9^{th} bit is always “0”), and then BU1852 drives High on XINT line.

See also section “3wire interface AC characteristics”.

2. 3wire Interface AC characteristics

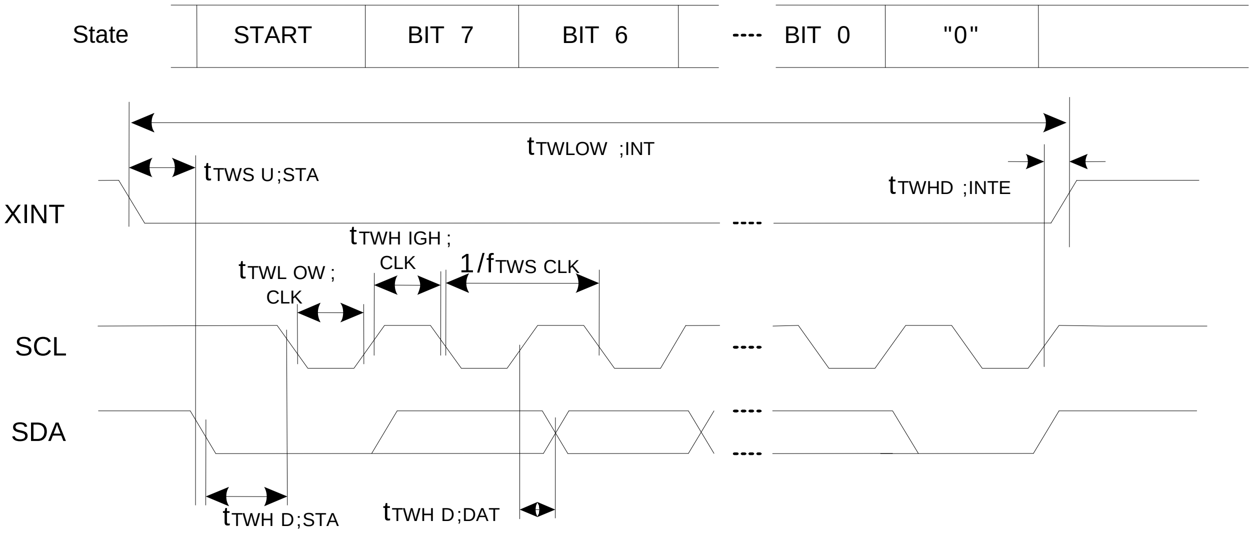


Fig.24 3wire interface AC timing

VDD=1.8V, VDDIO=1.8V,Topr=25℃,TW=VDD

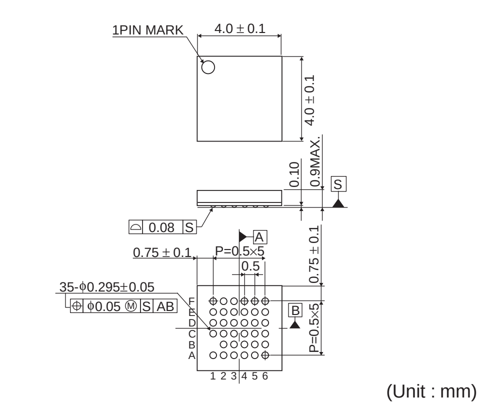
Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
SCL Clock Frequency	f_{TWSCLK}	-	-	21.5	kHz	
START Condition Setup Time	$t_{TWSU;STA}$	0.030	-	500	ms	
START Condition Hold Time	$t_{TWHD;STA}$	20	-	-	µs	
SCL Low Time	$t_{TWLOW;CLK}$	23	-	-	µs	
SCL High Time	$t_{TWHIGH;CLK}$	23	-	-	µs	
Data Hold Time	$t_{TWHD;DAT}$	0.1	-	1.0	µs	
XINT End Hold	$t_{TWHD;INTE}$	1.35	-	10.2	µs	
XINT Low Time	$t_{TWLOW;INT}$	500	800	1350	ms	

●Ordering part number

B	U		1	8	5	2		G	U	W	-	E	2

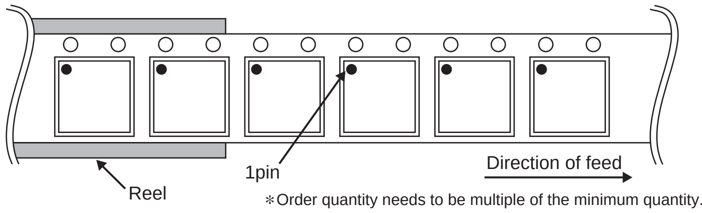
- BU — Part No.
- 1852 — Part No.
- GUW — Package
  GUW: VBGA035W040
  GXW: UBGA035W030
- E2 — Packaging and forming specification
  E2: Embossed tape and reel

VBGA035W040



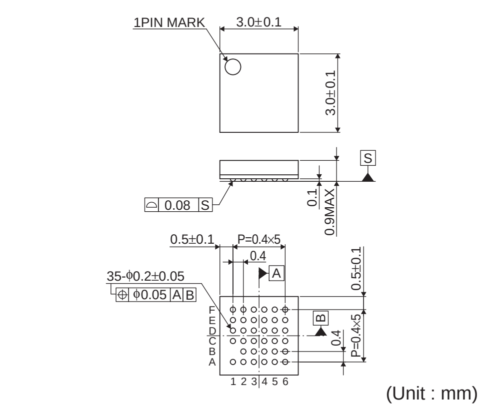
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



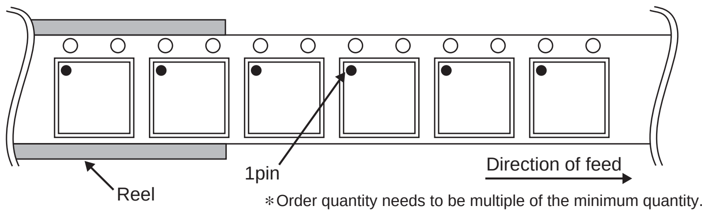
*Order quantity needs to be multiple of the minimum quantity.

UBGA035W030



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
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8. Confirm that operation temperature is within the specified range described in the product specification.

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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