



**THE DATASHEET OF  
BTA408X-1000C0TQ**



## 1. General description

Planar passivated high commutation three quadrant triac in a SOT186A "full pack" plastic package. This triac is intended for use in motor control circuits where very high blocking voltage, high static and dynamic  $dV/dt$  as well as high  $dI_{com}/dt$  can occur. This "series C0T" triac will commute the full RMS current at the maximum rated junction temperature ( $T_{j(max)} = 150\text{ °C}$ ) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

## 2. Features and benefits

- High minimum IGT for guaranteed immunity to gate noise
- Full cycle AC conduction
- High junction operating temperature capability ( $T_{j(max)} = 150\text{ °C}$ )
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Less sensitive gate for high noise immunity
- Triggering in three quadrants only
- Very high immunity to false turn-on by  $dV/dt$  and IEC 61000-4-4 fast transient
- Package meets UL94V0 flammability requirement
- Package is RoHS compliant
- Package meets UL1557 isolation test requirement rated at 2500V RMS

## 3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls e.g. vertical axis washing machines
- Applications subject to high temperature ( $T_{j(max)} = 150\text{ °C}$ )

## 4. Quick reference data

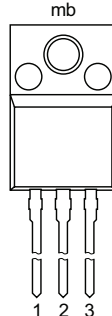
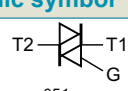
Table 1. Quick reference data

Symbol	Parameter	Conditions	Values	Unit
<b>Absolute maximum rating</b>				
$V_{DRM}$	repetitive peak off-state voltage		1000	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 105\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	8	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $t_p = 20\text{ ms}$ ; $T_{j(init)} = 25\text{ °C}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	100	A
		full sine wave; $t_p = 16.7\text{ ms}$ ; $T_{j(init)} = 25\text{ °C}$	110	A
$T_j$	junction temperature		150	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G+ T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	5	-	35	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G- T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	5	-	35	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G- T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	5	-	35	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a>	-	-	40	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	1.21	1.6	V
<b>Dynamic characteristics</b>						
dV <sub>D</sub> /dt	rate of rise of off-state voltage	V <sub>DM</sub> = 670 V; T <sub>j</sub> = 125 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit	1500	-	-	V/μs
		V <sub>DM</sub> = 670 V; T <sub>j</sub> = 150 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit	1000	-	-	V/μs
dI <sub>com</sub> /dt	rate of change of commutating current	V <sub>D</sub> = 400 V; T <sub>j</sub> = 150 °C; I <sub>T(RMS)</sub> = 8 A; dV <sub>com</sub> /dt = 20 V/μs; gate open circuit; snubberless condition	12	-	-	A/ms
		V <sub>D</sub> = 400 V; T <sub>j</sub> = 150 °C; I <sub>T(RMS)</sub> = 8 A; dV <sub>com</sub> /dt = 10 V/μs; gate open circuit	15	-	-	A/ms
		V <sub>D</sub> = 400 V; T <sub>j</sub> = 150 °C; I <sub>T(RMS)</sub> = 8 A; dV <sub>com</sub> /dt = 1 V/μs; gate open circuit	20	-	-	A/ms

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		 sym051
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BTA408X-1000C0T	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

## 7. Marking

Table 4. Marking codes

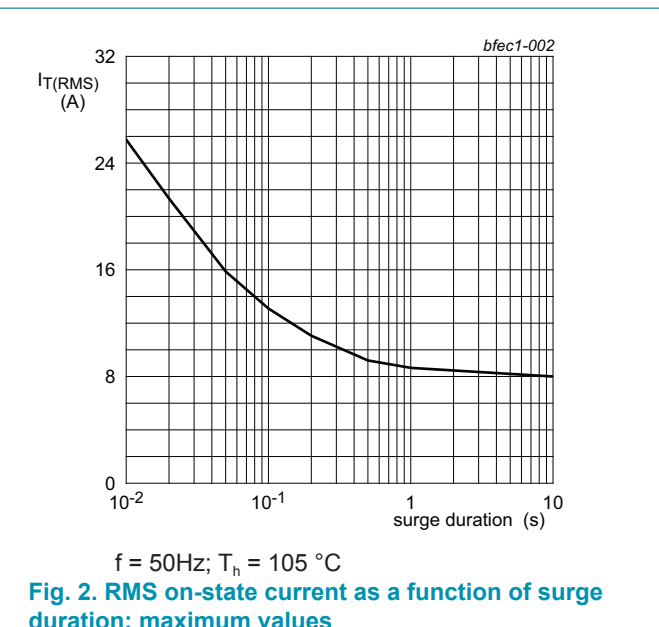
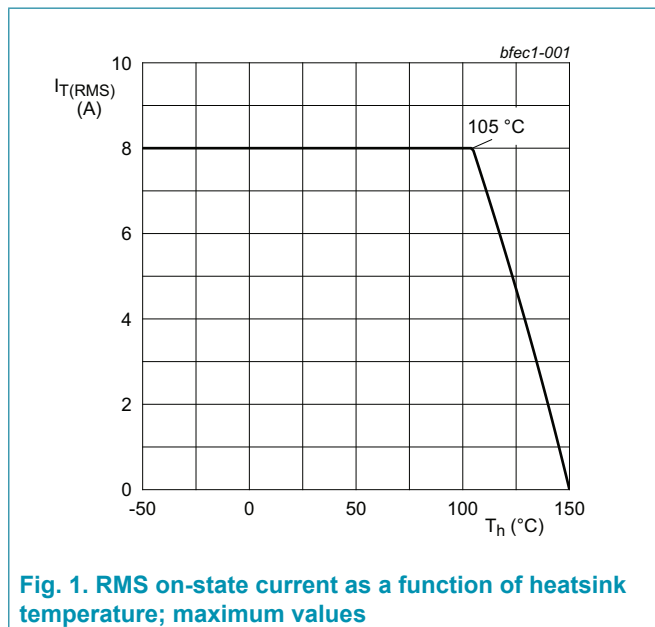
Type number	Marking codes
BTA408X-1000C0T	BTA408X-1000C0T

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
$V_{DRM}$	repetitive peak off-state voltage		1000	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 105^\circ\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	8	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $t_p = 20\text{ ms}$ ; $T_{j(\text{init})} = 25^\circ\text{C}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	100	A
		full sine wave; $t_p = 16.7\text{ ms}$ ; $T_{j(\text{init})} = 25^\circ\text{C}$	110	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ms}$ ; sine wave	50	$\text{A}^2\text{s}$
$dI_T/dt$	rate of rise of on-state current	$I_G = 70\text{mA}$	100	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current		2	A
$P_{GM}$	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
$T_{stg}$	storage temperature		-40 to 150	$^\circ\text{C}$
$T_j$	junction temperature		150	$^\circ\text{C}$
$V_{pp}$	peak pulse voltage	$T_j = 25^\circ\text{C}$ ; non-repetitive, off-state; ten pulses on each voltage polarity; 20s or more between successive pulses	2	kV



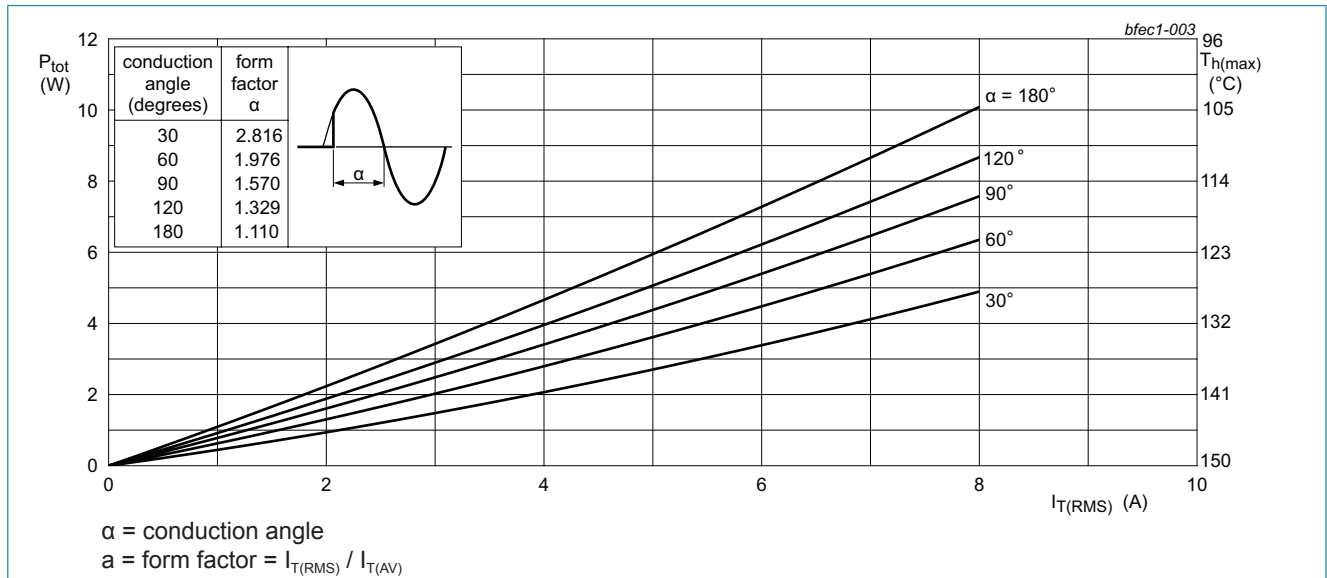


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

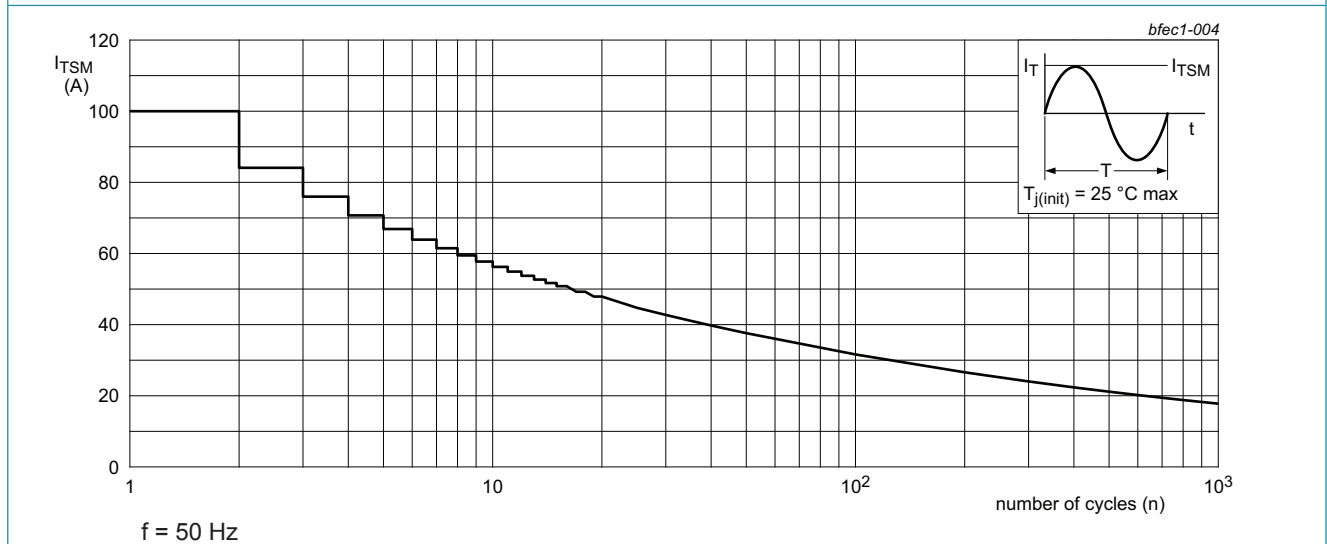


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

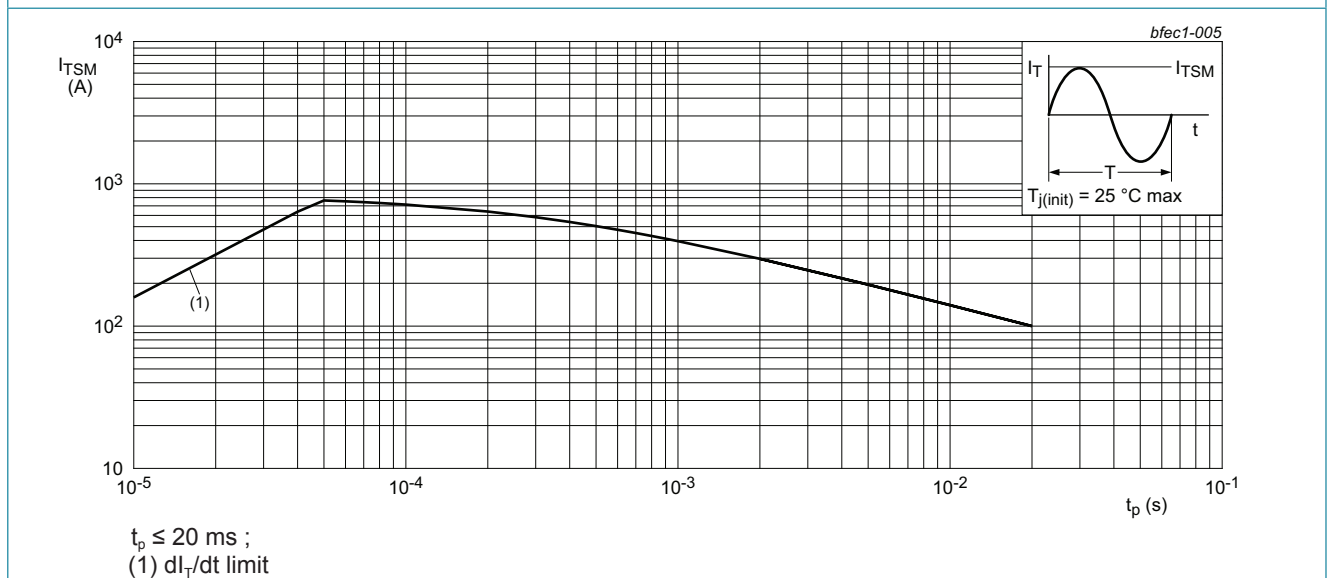


Fig. 5. Total power dissipation as a function of RMS on-state current; maximum values

## 9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; <a href="#">Fig. 6</a>	-	-	4.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W

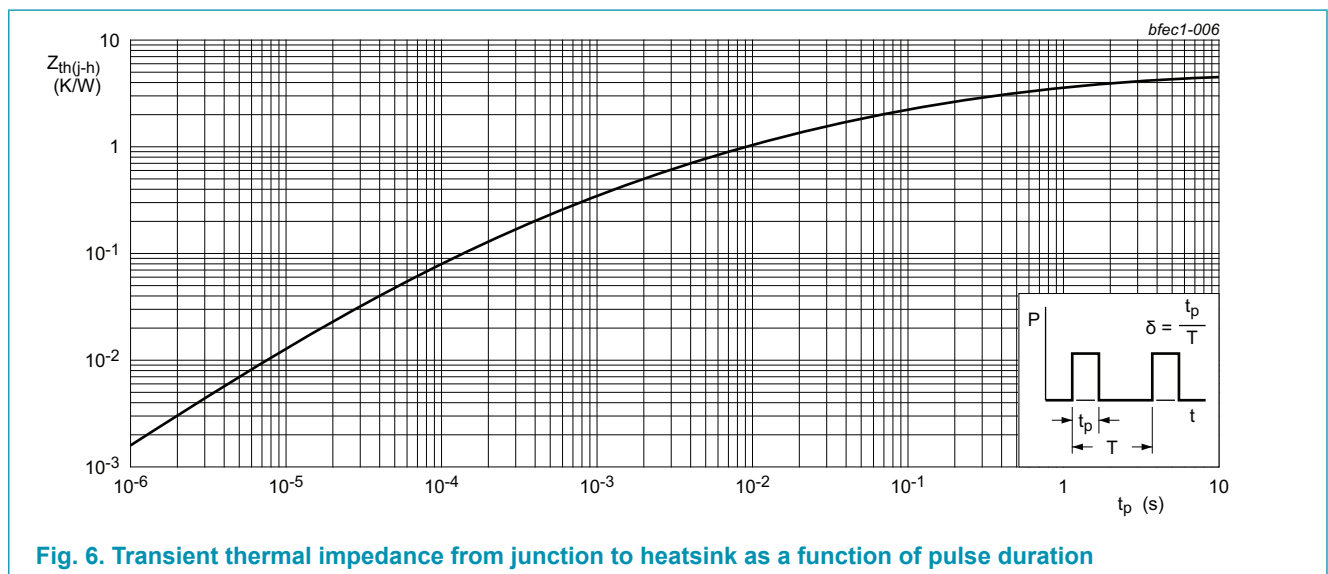


Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse duration

## 10. Isolation characteristics

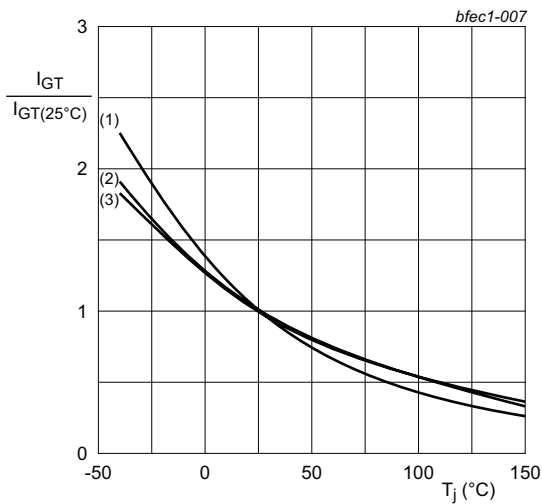
Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; from all pins to external heatsink; sinusoidal waveform; clean and dust free	-	-	2500	V
$C_{isol}$	isolation capacitance	from cathode to external heatsink	-	10	-	PF

## 11. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	5	-	35	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	5	-	35	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	5	-	35	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 8</a>	-	-	50	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 8</a>	-	-	70	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 8</a>	-	-	50	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	-	40	mA
$V_T$	on-state voltage	$I_T = 10\text{ A}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	1.21	1.6	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	0.7	1	V
		$V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_J = 150\text{ °C}$ ; <a href="#">Fig. 11</a>	0.25	0.4	-	V
$I_D$	off-state current	$V_D = 1000\text{ V}$ ; $T_J = 25\text{ °C}$	-	-	10	$\mu\text{A}$
		$V_D = 1000\text{ V}$ ; $T_J = 150\text{ °C}$	-	0.4	2	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 670\text{ V}$ ; $T_J = 125\text{ °C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	1500	-	-	V/ $\mu\text{s}$
		$V_{DM} = 670\text{ V}$ ; $T_J = 150\text{ °C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	1000	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}$ ; $T_J = 150\text{ °C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$ ; gate open circuit; snubberless condition	12	-	-	A/ms
		$V_D = 400\text{ V}$ ; $T_J = 150\text{ °C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit	15	-	-	A/ms
		$V_D = 400\text{ V}$ ; $T_J = 150\text{ °C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit	20	-	-	A/ms



- (1) T2- G-
- (2) T2+ G-
- (3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

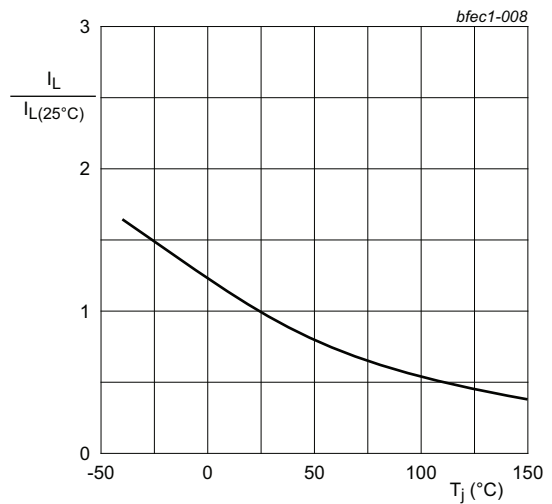


Fig. 8. Normalized latching current as a function of junction temperature

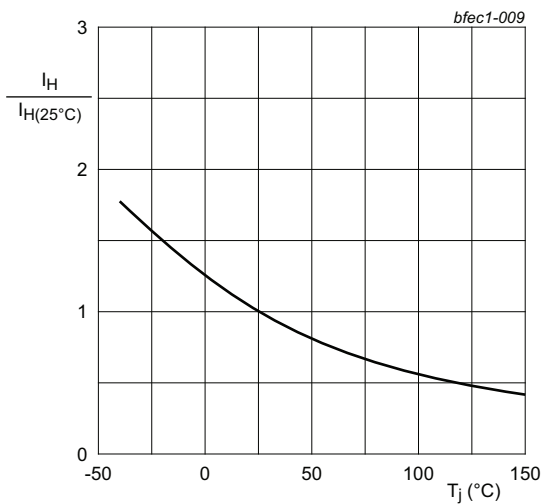
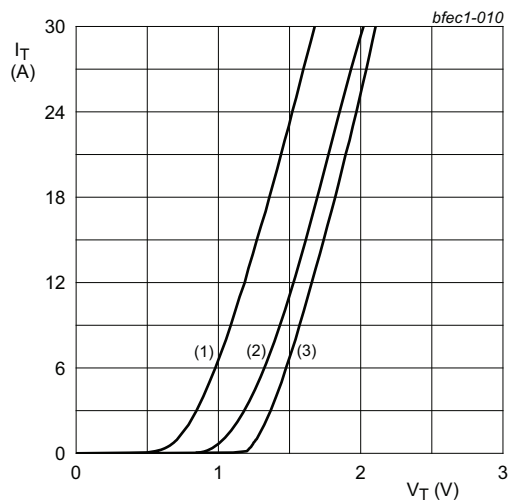


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.188 \text{ V}$ ;  $R_s = 0.0237 \ \Omega$

- (1)  $T_j = 150^\circ\text{C}$ ; typical values
- (2)  $T_j = 150^\circ\text{C}$ ; maximum values
- (3)  $T_j = 25^\circ\text{C}$ ; maximum values

Fig. 10. On-state current as a function of on-state voltage

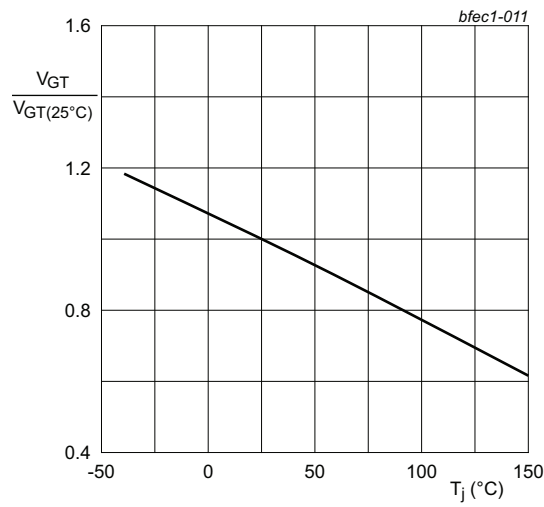
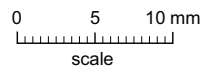
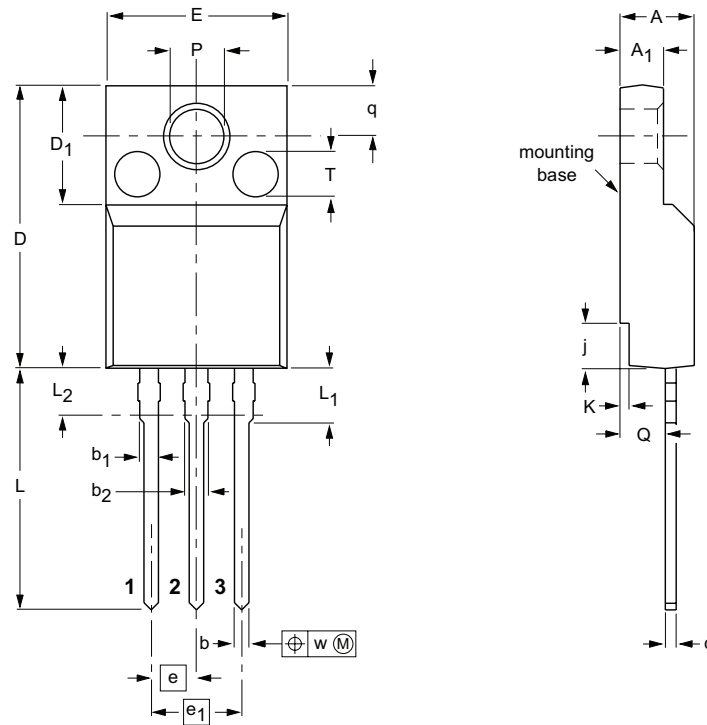


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

## 12. Package outline

Plastic single-ended package; isolated heatsink mounted;  
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	e <sub>1</sub>	j	K	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max.	P	Q	q	T <sup>(2)</sup>	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

**Notes**

- Terminal dimensions within this zone are uncontrolled.
- Both recesses are  $\square 2.5 \times 0.8$  max. depth

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT186A		3-lead TO-220F			02-04-09 06-02-14

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 12 July 2017

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