THE DATASHEET OF

BM81028AMWV-ZE2

Power Supply IC Series for TFT-LCD Panels

Multi-Channel System Power Supply IC

BM81028AMWV

●General Description

BM81028AMWV is a system power supply IC for TFT-LCD panels which are used in monitors, notebook type displays, and tablets.
This IC incorporates HAVDD, VCOM amplifier in addition to the power supply for panel driver (SOURCE, GATE, and LOGIC power supplies).
Moreover, this IC has a built-in EEPROM for sequence and output voltage setting retention.

●Applications

TFT-LCD Panels which are used in
Monitors, Note PCs and Tablets.

●Features

- Input voltage range: 2.7V to 5.5V
- Standby current: 1.4μA (Typ)
- Operating temperature range: -40℃ to +85℃
- Step-down DC/DC converter 2-channels (Synchronous rectification)
- Step-up DC/DC converter (Integrated load switch and Synchronous rectification)
- HAVDD amplifier (8bit Resolution)
- VCOM amplifier (8bit Resolution)
- Positive charge pump (Integrated diode)
- Negative charge pump
- I^2C Interface Output Voltage Setting Control Function (Integrated EEPROM)
- Switching frequency switching function (600kHz,1200kHz)
- Protection circuits
  - Under-Voltage Lockout
  - Thermal Shut Down
  - Over-Current Protection
  - Over-Voltage Protection
  - Short Circuit Protection (Timer Latch type)
- Input tolerant (SCL, SDA,EN)

●Package

	W(Typ)	D(Typ)	H(Max)
UQFN28V4040A	4.0mm	x 4.00mm	x 1.00m

●Typical Application Circuit

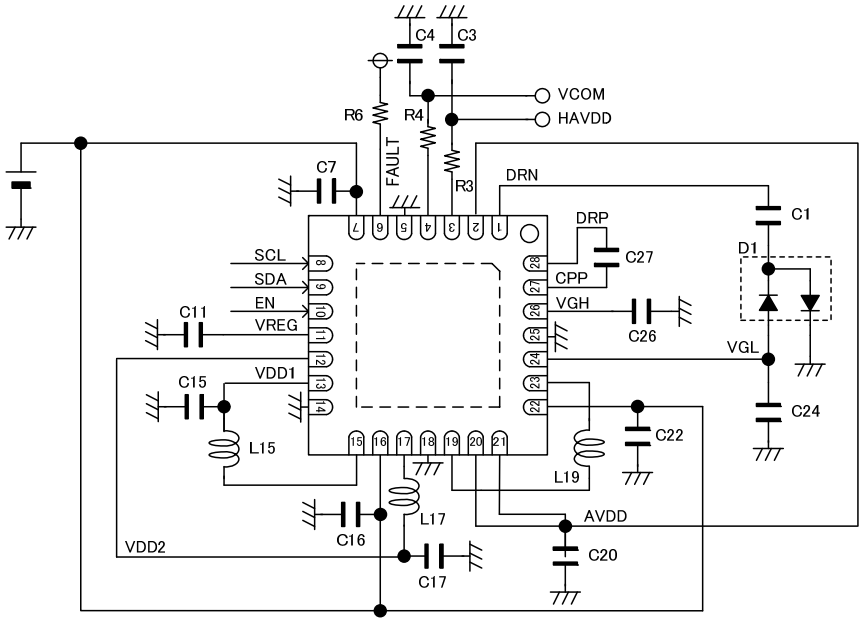


Fig.1. Typical Application Circuit

●Pin Configuration

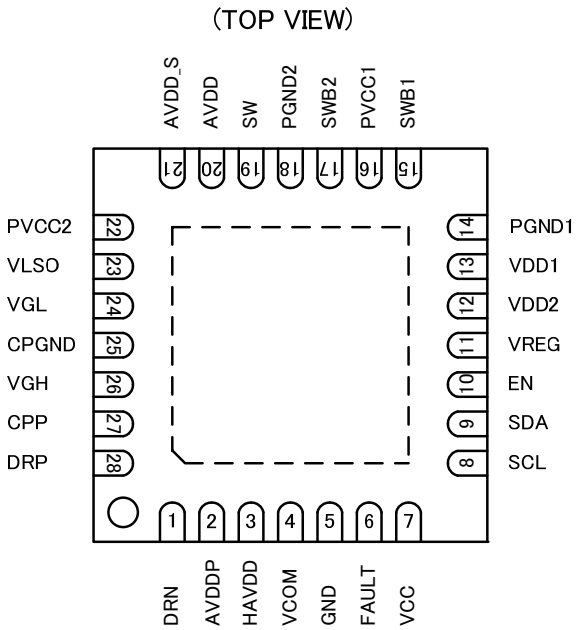


Fig.2 Pin Configuration

●Pin Descriptions

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	DRN	Negative charge pump driver pin	15	SWB1	Step-down DC/DC switching pin 1
2	AVDDP	AVDD input	16	PVCC1	Step-down DC/DC power supply input
3	HAVDD	HAVDD amplifier output	17	SWB2	Step-down DC/DC switching pin 2
4	VCOM	VCOM amplifier output	18	PGND2	Step-down/-up DC/DC ground
5	GND	Ground	19	SW	Step-up DC/DC switching pin
6	FAULT	FAULT signal output	20	AVDD	Step-up DC/DC output
7	VCC	Power supply input	21	AVDD_S	Step-up DC/DC output feedback
8	SCL	Serial clock input (I2C)	22	PVCC2	Step-up DC/DC load switch input
9	SDA	Serial clock data input (I2C)	23	VLSO	Step-up DC/DC load switch output
10	EN	Enable input	24	VGL	Negative charge pump feedback
11	VREG	Inner power supply output	25	CPGND	Charge pump ground
12	VDD2	Step-down DC/DC output feedback input 2	26	VGH	Positive charge pump feedback
13	VDD1	Step-down DC/DC output feedback input 1	27	CPP	Built-in Positive charge pump switching Di output
14	PGND1	Step-down DC/DC ground	28	DRP	Positive charge pump driver pin

●Block Diagram

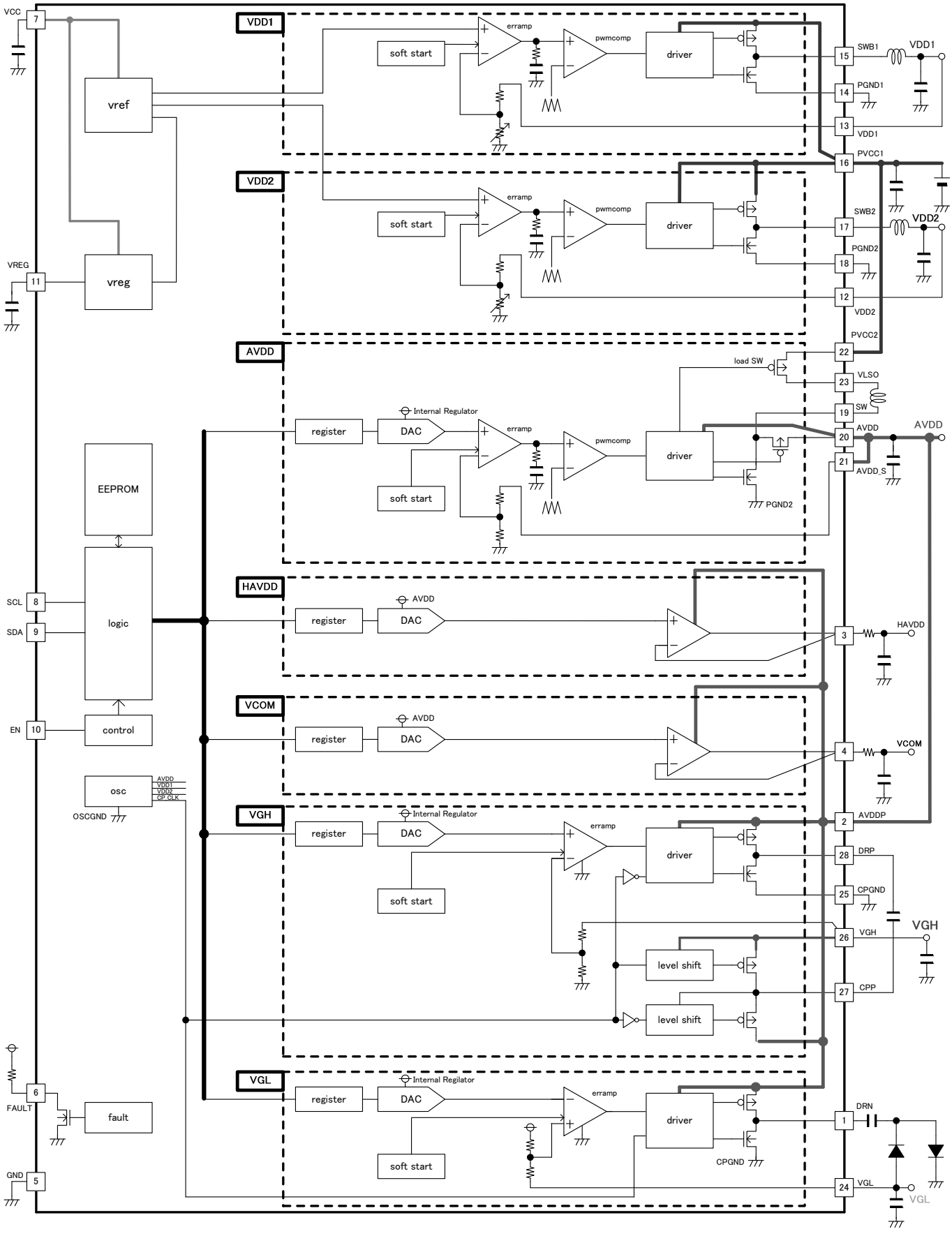


Fig.3 Block Diagram

●Function Description of Each Block

Enumerated below are the different blocks and the output voltages they generate. Also, discussed are the protection circuits that can shut down each block to prevent IC destruction.

All output voltages generated by each block, startup order, and delay time (DELAY1 and DELAY2) can be set through the EEPROM. Upon start-up, these settings are read from the EEPROM and copied to the registers.

① Buck Converter Block (VDD1, VDD2)
Generates the VDD1 and VDD2 voltages after VCC UVLO release at EN=High.
This block shuts down when SCP or OCP is detected.

② Boost Converter Block (AVDD)
Generates the AVDD voltage after the configured DELAY2 time.
This block shuts down when OVP, SCP, or OCP is detected.

③ HAVDD Amp Block (HAVDD)
Generates the HAVDD voltage based on the AVDD voltage.
Thus, the HAVDD voltage is produced after the AVDD voltage.

④ VCOM Amp Block (VCOM)
Generates the VCOM voltage based on the AVDD voltage.
Thus, the VCOM voltage is produced after the AVDD voltage.

⑤ Positive Charge Pump Block (VGH)
Generates the VGH voltage based on the AVDD voltage.
Thus, the VGH voltage is produced after the AVDD voltage.
This block shuts down when SCP is detected.

⑥ Negative Charge Pump Block (VGL)
Generates the VGL voltage based on the AVDD voltage.
It starts up after the configured DELAY2 time.
This block shuts down when SCP is detected.

●**Absolute Maximum Ratings**

PARAMETER	SYMBOL	LIMITS			Unit
		MIN	TYP	MAX	
Power Supply Voltage	VCC, PVCC1, PVCC2	-0.3	—	6.5	V
Output Pin	SWB1, SWB2	-0.3	—	PVCC1+0.3	V
	VDD1, VDD2	-0.3	—	6.5	V
	AVDD, AVDDP, SW	-0.3	—	19	V
	VLSO	-0.3	—	6.5	V
	HAVDD, VCOM	-0.3	—	AVDDP+0.3	V
	DRP, DRN	-0.3	—	AVDDP+0.3	V
	CPP	-0.3	—	30	V
	VGH,	-0.3	—	36	V
	VGL	-15	—	0.3	V
	VREG	-0.3	—	VCC+0.3	V
	FAULT	-0.3	—	6.5	V
Functional Pin Voltage	SCL, SDA, EN	-0.3	—	6.5	V
Maximum Junction temperature	Tjmax (1)	—	—	150	℃
Power Dissipation	Pd (2)	2.01			W
Operating Temperature Range	Topr	-40	—	85	℃
Storage Temperature Range	Tstg	-55	—	150	℃

(1) Junction temperature at storage time.
(2) JEDEC standard (4 layers)

●**Recommended Operating Ratings(T_A=-40℃ to +85℃)**

PARAMETER	SYMBOL	MIN	TYP	MAX	Unit
Power Supply Voltage 1 (DC/DC Block Protection Detection Voltage 1 setting)	VCC,PVCC1,PVCC2	2.7	—	5.5	V
Power Supply Voltage 2 (DC/DC Block Protection Detection Voltage 2 setting)		2.9	—	5.5	V
Power Supply Voltage 3 (DC/DC Block Protection Detection Voltage 3 setting)		3.1	—	5.5	V
Power Supply Voltage 4 (DC/DC Block Protection Detection Voltage 4 setting)		3.3	—	5.5	V
SWB1,SWB2 Current	ISW1	—	—	1.0	A
SW Current	ISW2	—	—	1.5	A
Functional Pin Voltage	EN	-0.1	—	5.5	V
2 Line Serial Pin Voltage	SDA, SCL	-0.1	—	5.5	V
2 Line Serial Frequency	FCLK	—	—	400	kHz

●**Electrical Characteristics (Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V)**

1. Buck DC/DC converter block 1 (VDD1)

PARAMETER	SYMBOL	LIMITS			Unit	Condition
		MIN	TYP	MAX		
Output Voltage Range	VDD1	1.7	–	1.9	V	50mV step
		2.4	–	2.6		
Output Voltage Accuracy	VDD1_R	1.782	1.8	1.818	V	VDD1=1.8V setting
		2.475	2.5	2.525	V	VDD1=2.5V setting
Soft Start time	VDD1_SS	0.5	1	2	msec	The time where 90% of set voltage is reached.
Timer Latch Starting Time	VDD1_SCP	–	VDD1×0.8	–	V	
SWB1 H Side ON Resistance	RON_H1	–	300	480	mΩ	
SWB1 L Side ON Resistance	RON_L1	–	300	480	mΩ	
SWB1 H Side Leak Current	IL_H1	–	0	10	μA	
SWB1 L Side Leak Current	IL_L1	–	0	10	μA	
Current Limit	ILMT_SWB1	1.0	1.5	–	A	
Discharge Resistance	DISR_VDD1	–	25	50	Ω	

2. Buck DC/DC converter block 2 (VDD2)

PARAMETER	SYMBOL	LIMITS			Unit	Condition
		MIN	TYP	MAX		
Output Voltage Range	VDD2	1.1	–	1.3	V	50mV step
Output Voltage Accuracy	VDD2_R	1.188	1.2	1.212	V	VDD2=1.2V setting
Soft Start Time	VDD2_SS	0.5	1	2	msec	The time where 90% of set voltage is reached.
Timer Latch Starting Time	VDD2_SCP	–	VDD2×0.8	–	V	
SWB2 H Side On Resistance	RON_H2	–	300	480	mΩ	
SWB2 L Side On Resistance	RON_L2	–	300	480	mΩ	
SWB2 H Side Leak Current	IL_H2	–	0	10	μA	
SWB2 L Side Leak Current	IL_L2	–	0	10	μA	
Current Limit	ILMT_SWB2	1.0	1.5	–	A	
Discharge Resistance	DISR_VDD2	–	25	50	Ω	

3. Boost DC/DC converter block (AVDD)

PARAMETER	SYMBOL	LIMITS			Unit	Condition
		MIN	TYP	MAX		
Output Voltage Range	AVDD	8.0	–	14.5	V	0.1V step
Output Voltage Accuracy1	AVDD_R1	10.395	10.5	10.605	V	AVDD=10.5V setting
Output Voltage Accuracy2	AVDD_R2	-1.0	0	+1.0	%	AVDD=9.7 to 11.2V setting
Output Voltage Accuracy3	AVDD_R3	-1.7	0	+1.7	%	AVDD=8.0 to 9.6V, 11.3 to 12.8V setting
Output Voltage Accuracy4	AVDD_R4	-2.0	0	+2.0	%	AVDD=12.9 to 14.5V setting
Load Switch Soft Start time	LS_SS	1	2	4	msec	
Soft Start Time	AVDD_SS	3.5	5	6.5	msec	AVDD=10.5V setting
Timer Latch Starting Time	AVDD_SCP	–	AVDD×0.8	–	V	
Over-Voltage Protection voltage	AVDD_OVP	–	16	–	V	
SW H Side On Resistance	RON_H3	–	350	560	mΩ	
SW L Side On Resistance	RON_L3	–	350	560	mΩ	
SW H Side Leak Current	IL_H3	–	0	10	μA	
SW L Side Leak Current	IL_L3	–	0	10	μA	
Current Limit	ILMT_SW	1.5	2.0	–	A	
Load Switch ON Resistor	RON_LS	–	250	400	mΩ	
Maximum Duty	DMAX	80	90	–	%	
Discharge Resistance	DISR_AVDD	–	25	50	Ω	

●**Electrical Characteristics (Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V)**

4. HAVDD amplifier block (HAVDD)

PARAMETER	SYMBOL	LIMITS			Unit	Condition
		MIN	TYP	MAX		
Output Voltage Range	HAVDD	0.6×AVDD-3.1875	—	0.6×AVDD	V	12.5mV step
Resolution	RES1	—	8	—	Bit	
Integral Non-Linearity Error (INL)	INL1	-1	—	+1	LSB	Input code: 02h to FDh
Differential Non-Linearity Error (DNL)	DNL1	-1	—	+1	LSB	Input code: 02h to FDh
Output Current Ability (Source)	ISOURCE1	—	200	—	mA	
Output Current Ability (Sink)	ISINK1	—	200	—	mA	
Load Stability	ΔVO1	—	10	70	mV	Io=-15mA to +15mA
Slew Rate	SR1	—	20	—	V/μsec	

5. VCOM amplifier block (VCOM)

PARAMETER	SYMBOL	LIMITS			Unit	Condition
		MIN	TYP	MAX		
Output Voltage Range	VCOM	0.45×AVDD-3.1875	—	0.45×AVDD	V	12.5mV step
Resolution	RES2	—	8	—	Bit	
Integral Non-Linearity Error (INL)	INL2	-1	—	+1	LSB	Input code: 02h to FDh
Differential Non-Linearity Error (DNL)	DNL2	-1	—	+1	LSB	Input code: 02h to FDh
Output Current Ability (Source)	VOL2	—	200	—	mA	
Output Current Ability (Sink)	ISOURCE2	—	200	—	mA	
Load Stability	ISINK2	—	10	70	mV	Io=-15mA to +15mA
Slew Rate	SR2	—	20	—	V/μsec	
Discharge Resistor	DISR_VCOM	—	50	100	Ω	

6. Positive charge pump block (VGH)

PARAMETER	SYMBOL	LIMITS			Unit	Condition
		MIN	TYP	MAX		
Output Voltage Range	VGH	13	—	26	V	0.2V step
Output Voltage Accuracy	VGH_R	17.1	18	18.9	V	VGH=18V setting
Soft Start time	VGH_SS	3.5	5	6.5	msec	VGH=18V setting
Timer Latch Starting Time	VGH_SCP	—	VGH×0.8	—	V	
DRP H Side On Resistance	RON_H4	—	5	—	Ω	
DRP L Side On Resistance	RON_L4	—	10	—	Ω	
CPP H Side On Resistance	RON_H4	—	10	—	Ω	
CPP L Side On Resistance	RON_L4	—	10	—	Ω	
Discharge Resistance	DISR_VGH	—	150	300	Ω	

7. Negative charge pump block (VGL)

PARAMETER	SYMBOL	LIMITS			Unit	Condition
		MIN	TYP	MAX		
Output Voltage Range	VGL	-9.5	—	-4	V	0.1V step
Output Voltage Accuracy	VGL_R	-6.3	-6	-5.7	V	VGH=-6.0V setting
Soft Start time	VGL_SS	3.5	5	6.5	msec	
Timer Latch Starting Time	VGL_SCP	—	VGL×0.8	—	V	
DRN H Side On Resistance	RON_H5	—	5	—	Ω	
DRN L Side On Resistance	RON_L5	—	10	—	Ω	
Discharge Resistance	DISR_VGL	—	250	500	Ω	

●**Electrical Characteristics (Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V)**

8. Overall (Entire device)

PARAMETER	SYMBOL	LIMITS			Unit	Condition
		MIN	TYP	MAX		
【Inside Regulator Voltage】						
VREG Output Voltage	VREG	2.15	2.3	2.45	V	
Load Stability	⊿V	—	20	100	mV	IVREG=20mA
【Oscillator Block】						
DC/DC Block Oscillating Frequency 1	FOSC1	480	600	720	KHz	
DC/DC Block Oscillating Frequency 2	FOSC2	960	1200	1440	KHz	
Charge Pump block Oscillating Frequency 1	FOSC1_CP	240	300	360	KHz	
Charge Pump block Oscillating Frequency 2	FOSC2_CP	480	600	720	KHz	
【Under Voltage Lock Out (UVLO) Circuit】						
UVLO return voltage	VUVLO	2.2	2.4	2.6	V	
UVLO detection voltage	VDET	1.9	2.1	2.3	V	
Hysteresis	VHYS	-	0.3	-	V	
【DC/DC Block Under-Voltage Lockout Circuit Block】						
DC/DC Block Protection Detection Voltage 1	DC_DET1	2.35	2.5	2.65	V	UVLO is released when VCC exceeds 2.8V.
DC/DC Block Protection Detection Voltage 2	DC_DET2	2.55	2.7	2.85	V	UVLO is released when VCC exceeds 3.0V.
DC/DC Block Protection Detection Voltage 3	DC_DET3	2.75	2.9	3.05	V	UVLO is released when VCC exceeds 3.2V.
DC/DC Block Protection Detection Voltage 4	DC_DET4	2.95	3.1	3.25	V	UVLO is released when VCC exceeds 3.4V.
DC/DC Block Protection Return Voltage 1	DC_REL1	2.55	2.7	2.85	V	
DC/DC Block Protection Return Voltage 2	DC_REL2	2.75	2.9	3.05	V	
DC/DC Block Protection Return Voltage 3	DC_REL3	2.95	3.1	3.25	V	
DC/DC Block Protection Return Voltage 4	DC_REL4	3.15	3.3	3.45	V	
【FAULT Signal Output Block】						
Output Off Leak Current	IFL	—	0	10	uA	
Output On Resistance	RON_F	—	1	2	kΩ	
【Control Signal Block1 SDA, SCL】						
Minimum Output Voltage	VSDA	—	—	0.4	V	ISDA=3mA
H Level Input Voltage	VIH1	1.7	—	—	V	VCC=2.5～5.5V Ta=-40～+85℃
L Level Input Voltage	VIL1	—	—	0.6	V	VCC=2.5～5.5V Ta=-40～+85℃
【Control Signal Block2 EN】						
Pull-Down Resistance Value	RCTL2	280	400	520	kΩ	
H Level Input Voltage	VIH2	1.7	—	—	V	VCC=2.5～5.5V Ta=-40～+85℃
L Level Input Voltage	VIL2	—	—	0.6	V	VCC=2.5～5.5V Ta=-40～+85℃
【Overall】						
Standby Consumption Current	ICC1	0.8	1.4	2.0	μA	EN=L
Consumption Current	ICC2	1.7	3.2	4.7	mA	EN=H, No switching

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

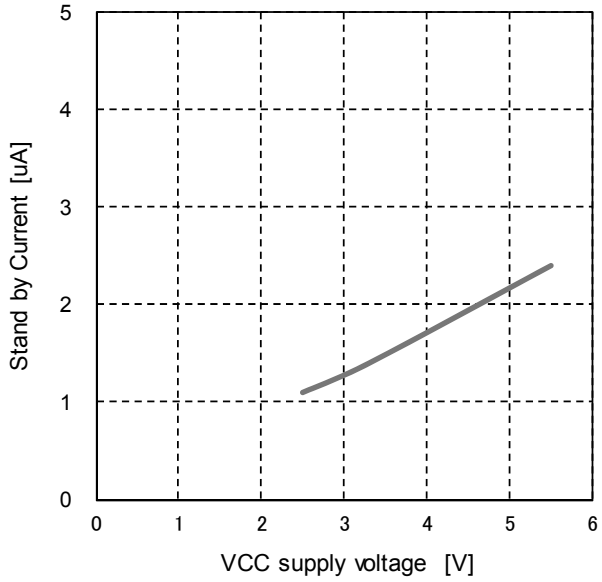


Fig.4 Standby Current

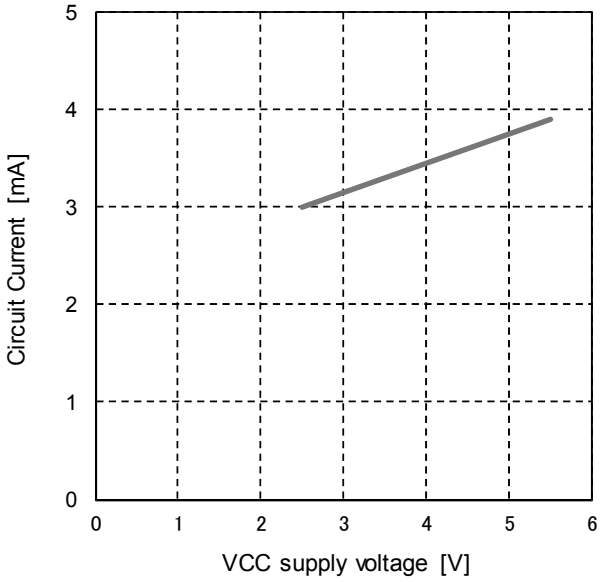


Fig.5 Circuit Current (No switching)

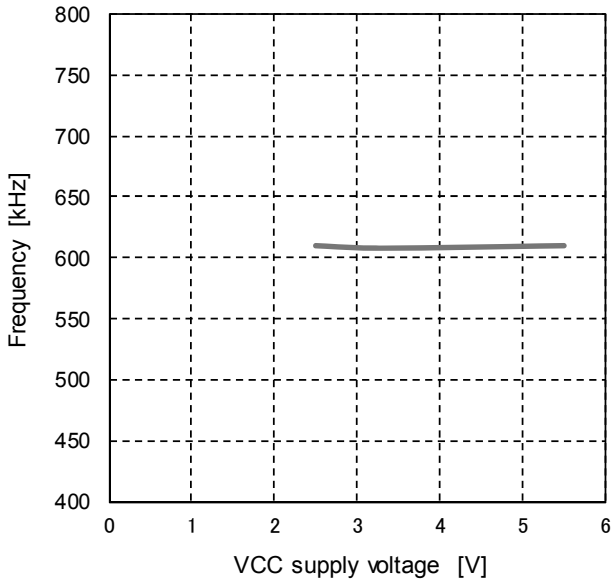


Fig.6 Switching Frequency (600kHz)

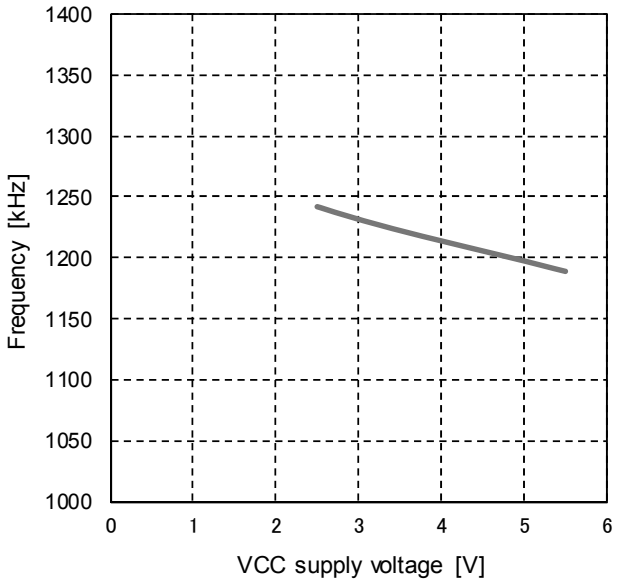


Fig.7 Switching Frequency (1200kHz)

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

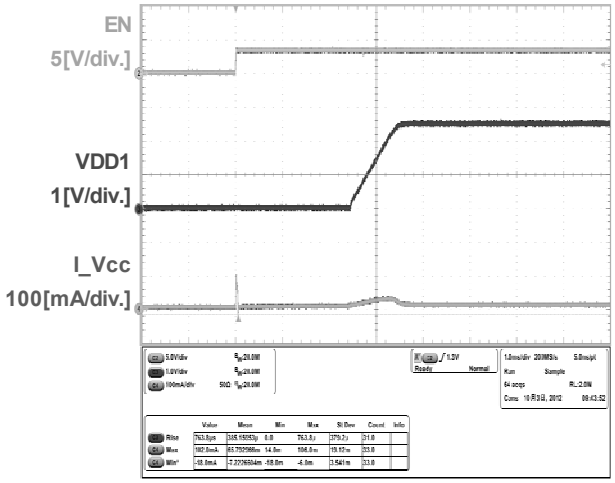


Fig.8 VDD1Start-up Sequence

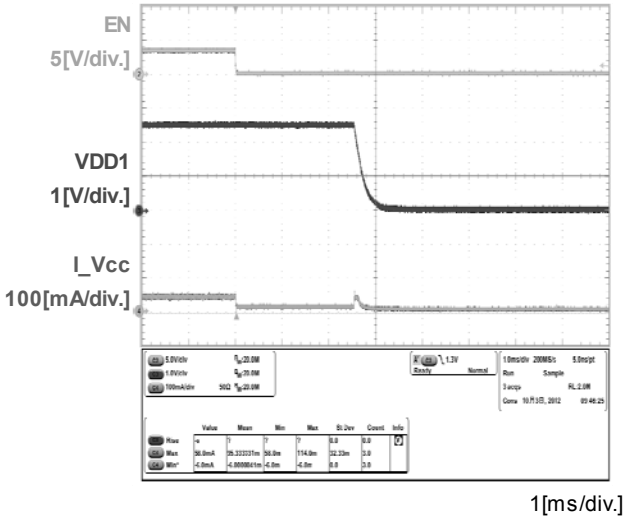


Fig.9 VDD1 Off Sequence

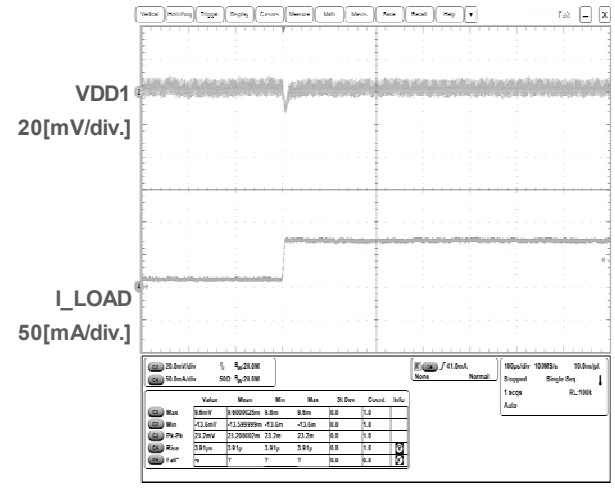


Fig.10 VDD1Load Transient
(25mA→75mA,tr=4us)

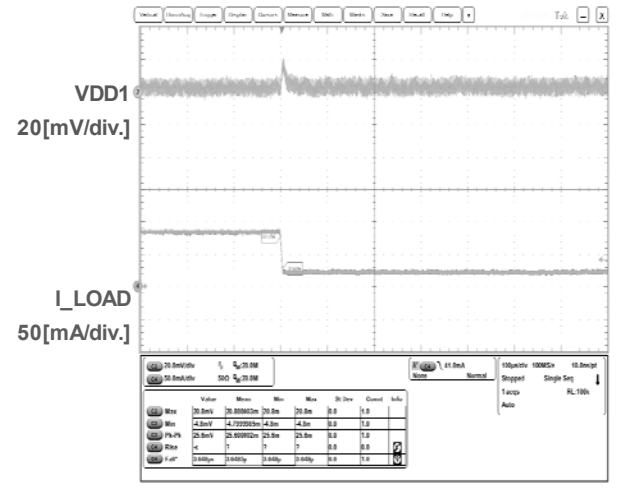


Fig.11 VDD1Load Transeint
(75mA→25mA,tf=4us)

●**Reference**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

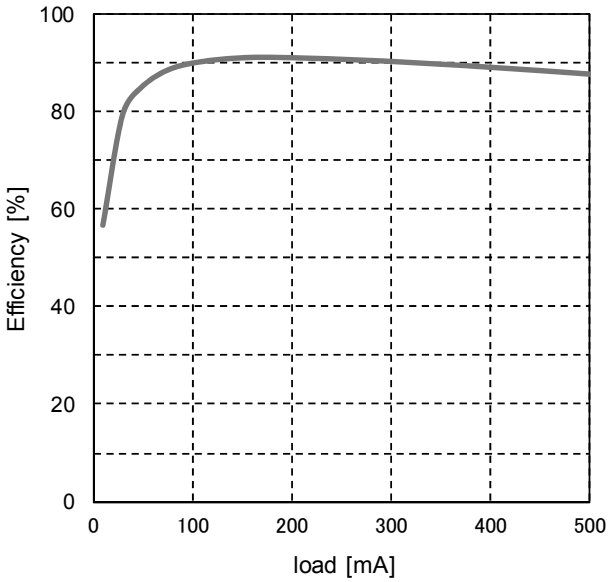


Fig.12 VDD1 Efficiency

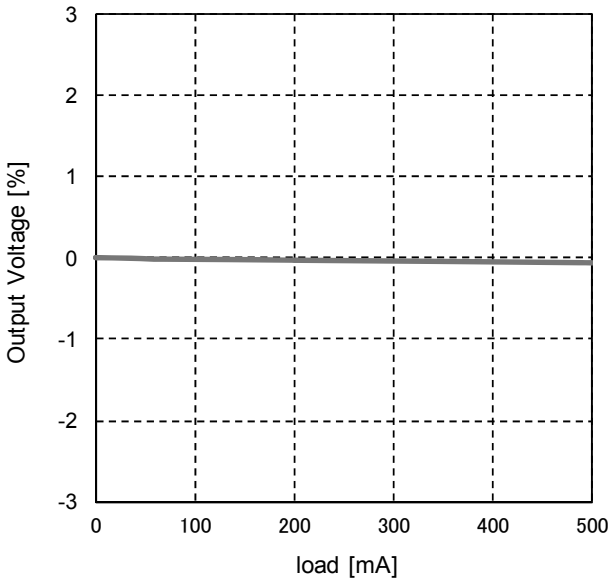


Fig.13 VDD1Load Regulation

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

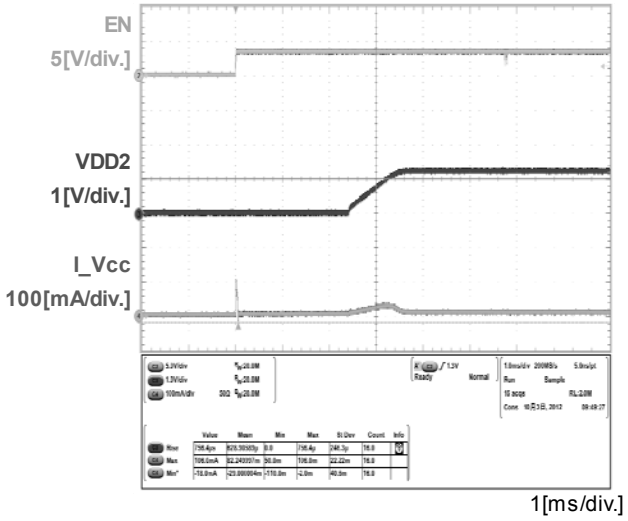


Fig.14 VDD2 Start-up Sequence

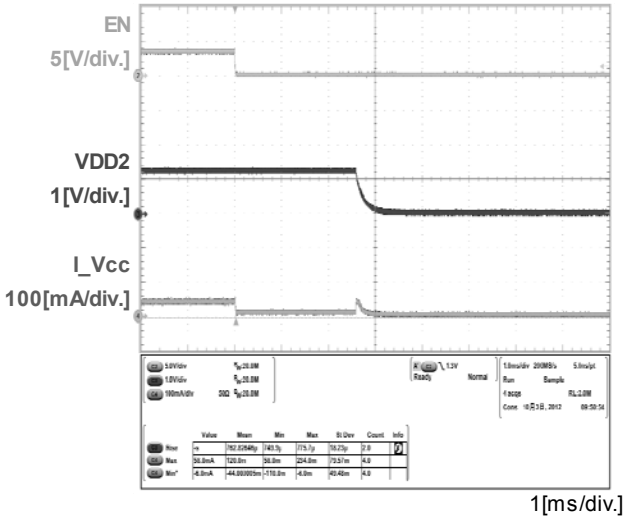


Fig.15 VDD2 Off Sequence

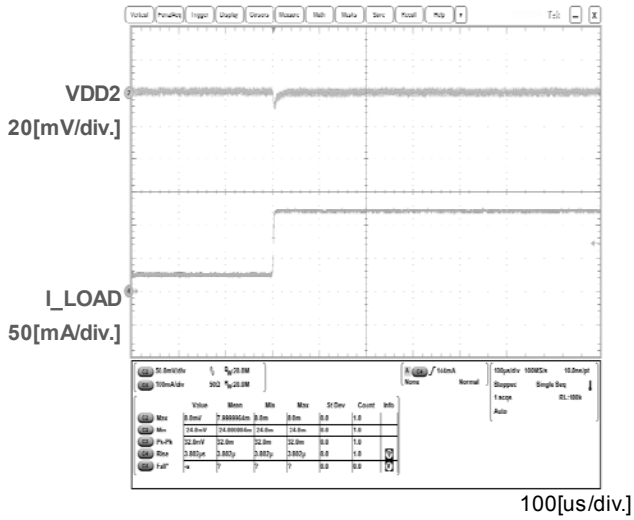


Fig.16 VDD2 Load Transient
(50mA→250mA,tr=4us)

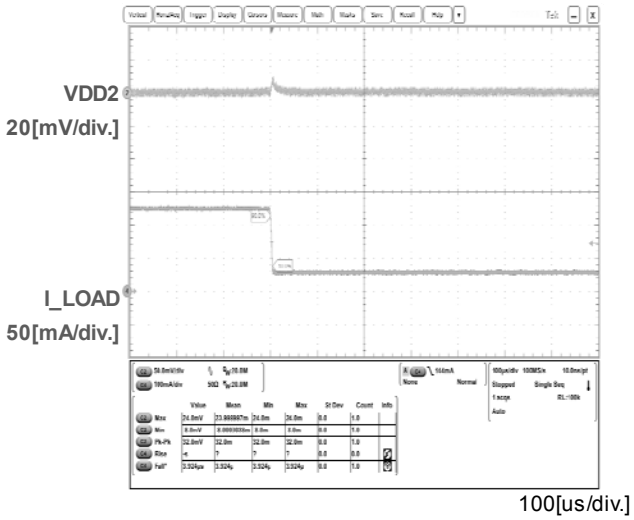


Fig.17 VDD2 Load Transient
(250mA→50mA,tf=4us)

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

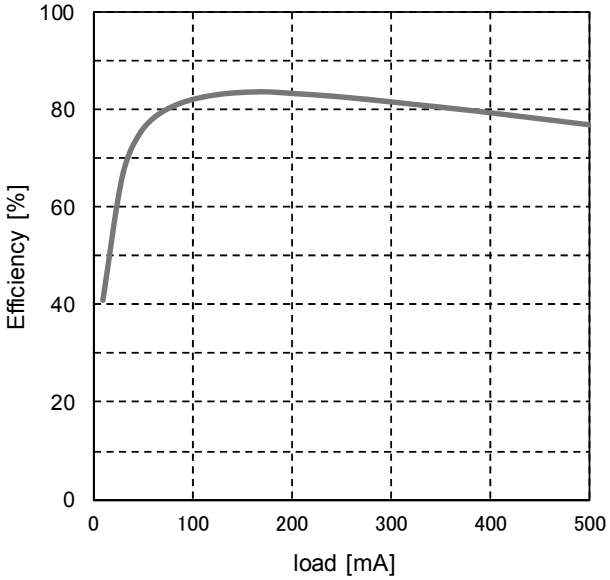


Fig.18 VDD2 Efficiency

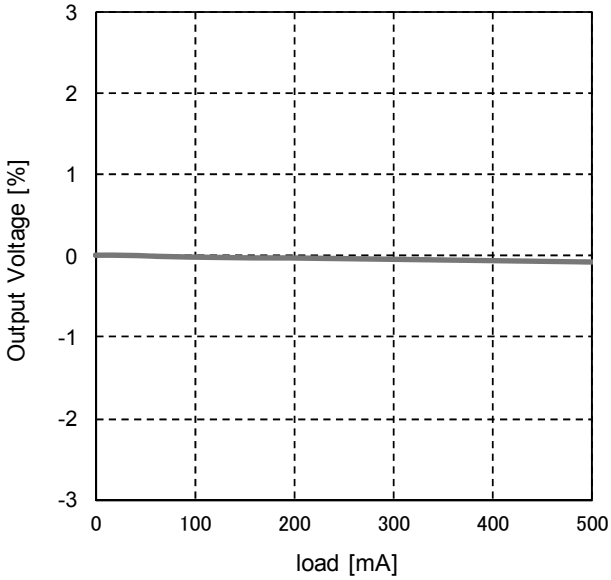


Fig.19 VDD2 Load Regulation

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

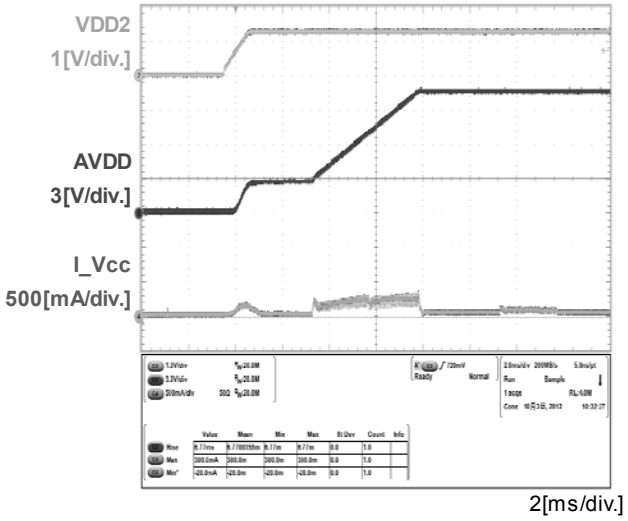


Fig.20 AVDD Start-up Sequence

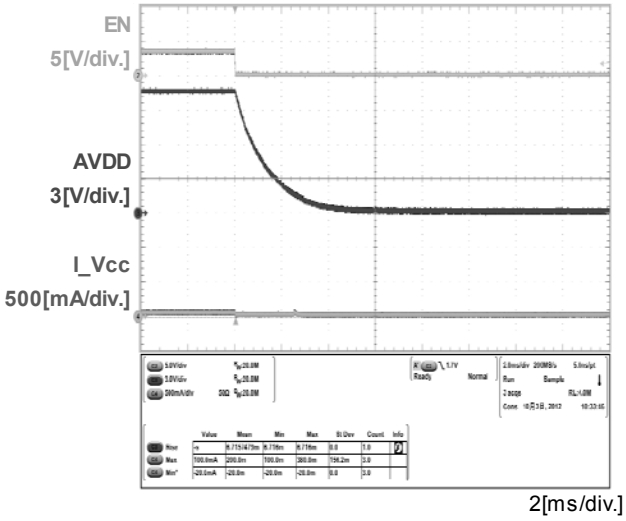


Fig.21 AVDD Off Sequence

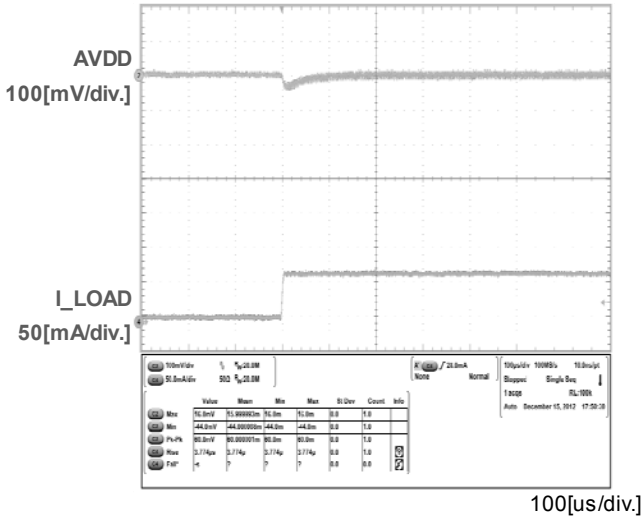


Fig.22 AVDD Load Transient
(10mA→70mA,tr=4us)

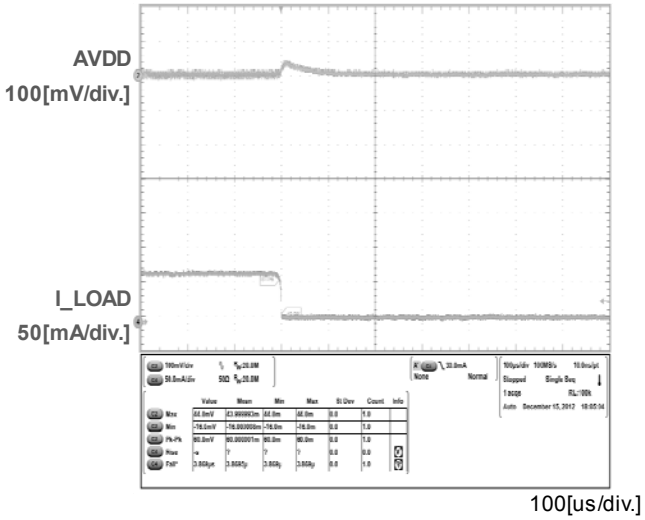


Fig.23 AVDD Load Transient
(70mA→10mA,tf=4us)

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

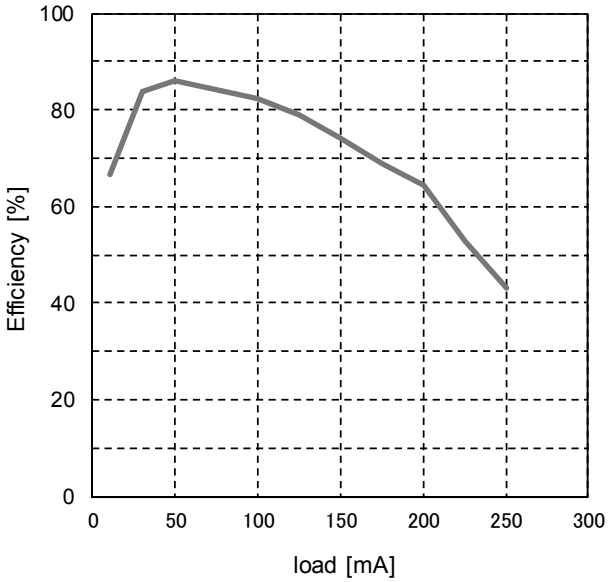


Fig.24 AVDD Efficiency

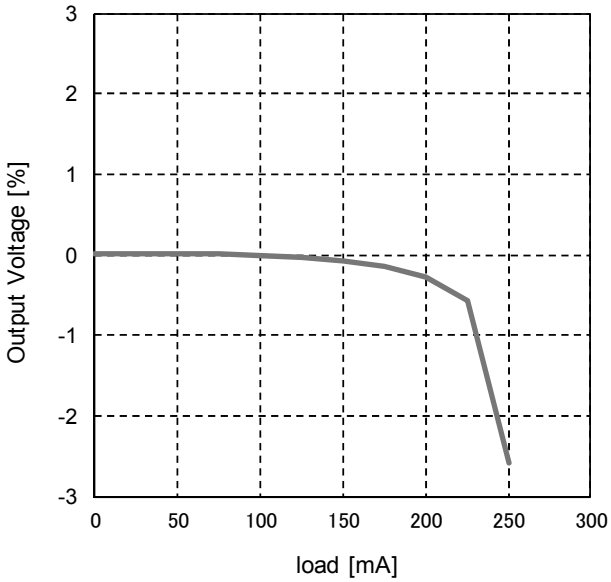


Fig.25 AVDD Load Regulation

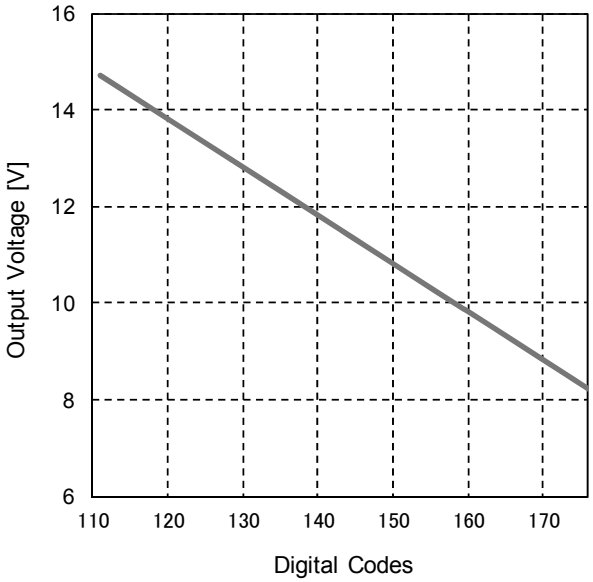


Fig.26 AVDD Linearity

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

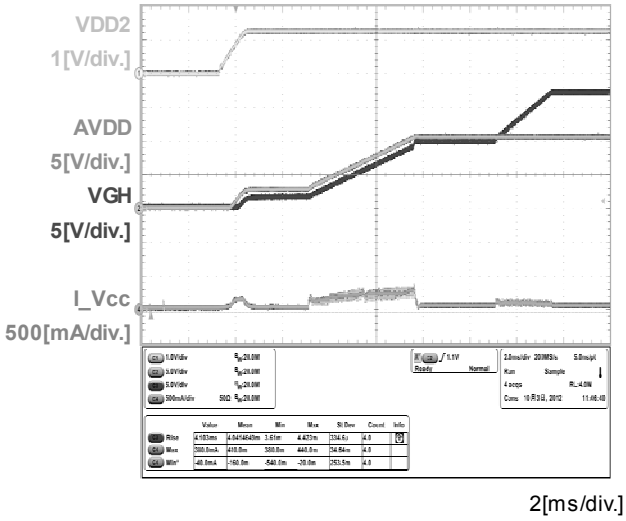


Fig.27 VGH Start-up Sequence

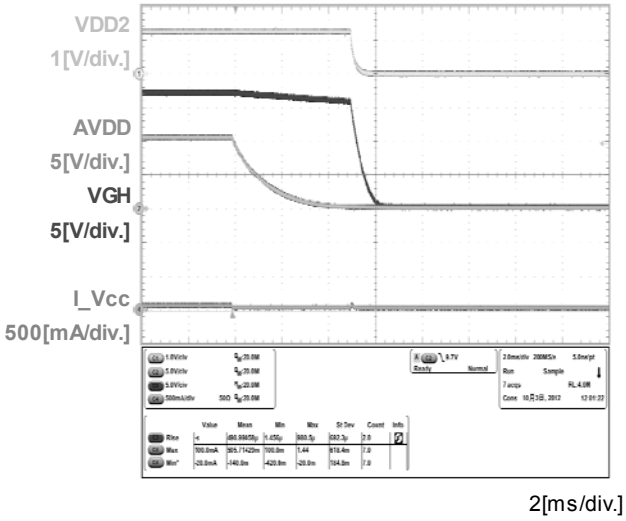


Fig.28 VGH Off Sequence

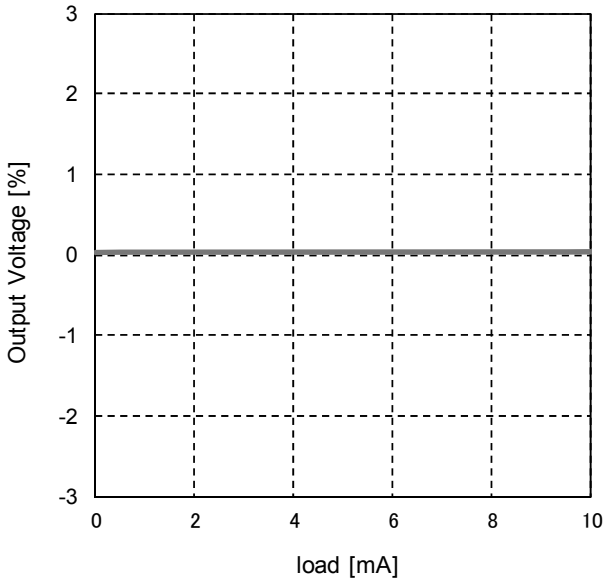


Fig.29 VGH Load Regulation

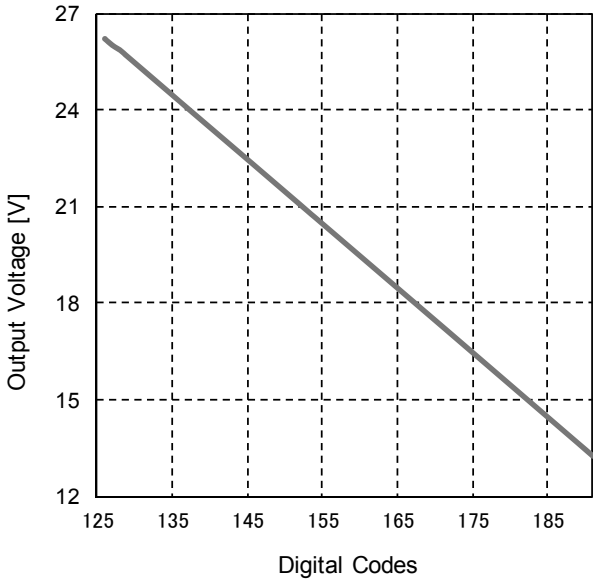


Fig.30 VGH Linearity

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

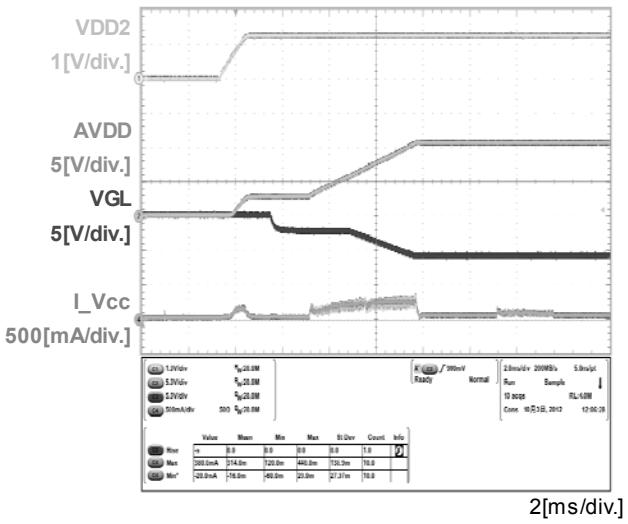


Fig.31 VGL Start-up Sequence

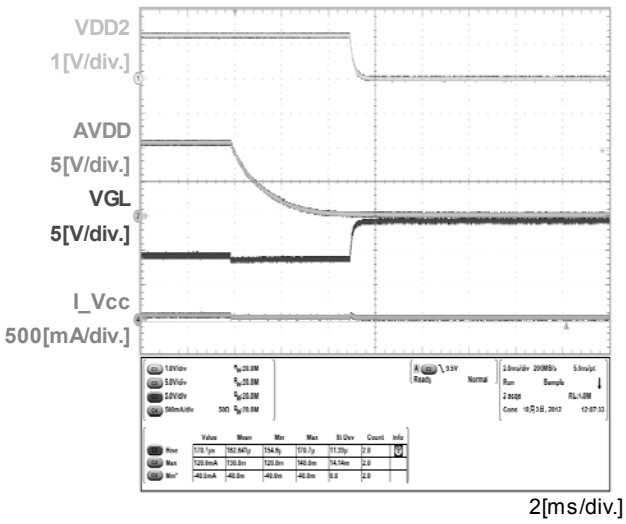


Fig.32 VGL Off Sequence

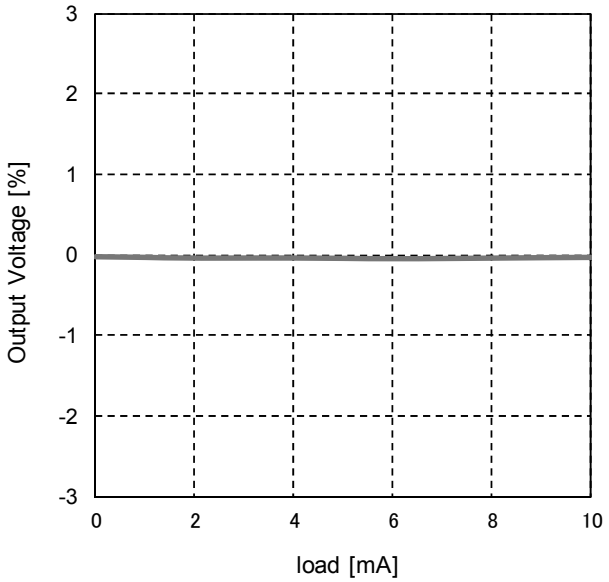


Fig.33 VGL Load Regulation

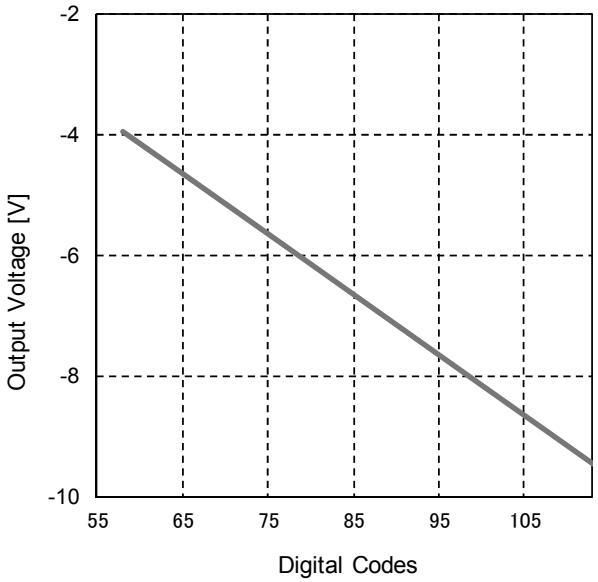


Fig.34 VGL Linearity

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

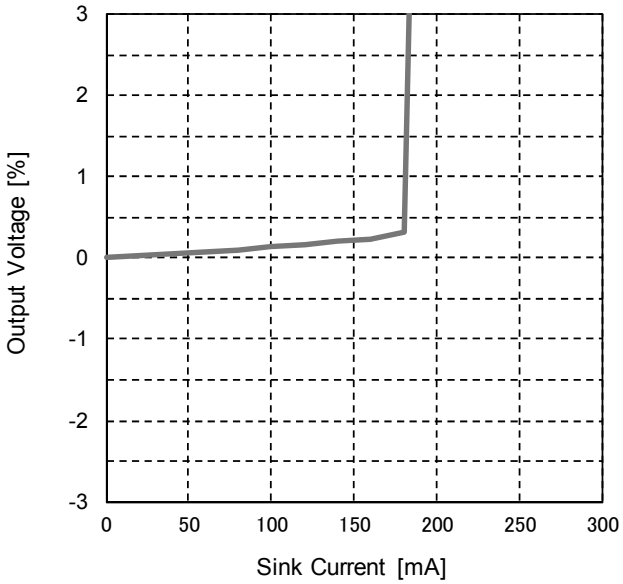


Fig.35 HAVDD Sink Current

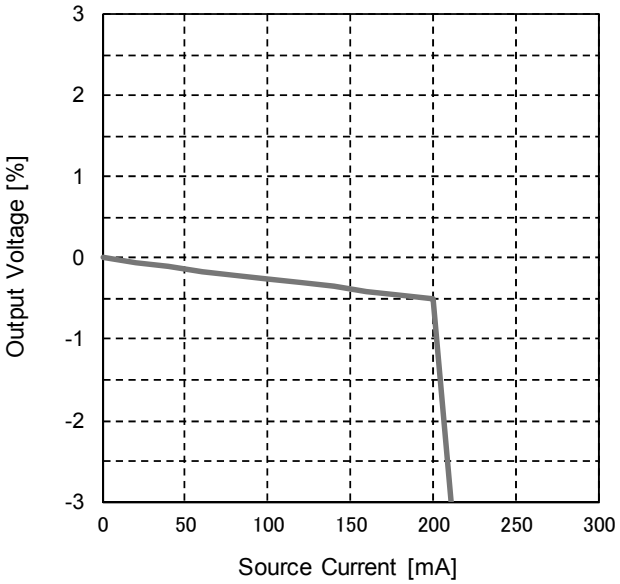


Fig.36 HAVDD Source Current

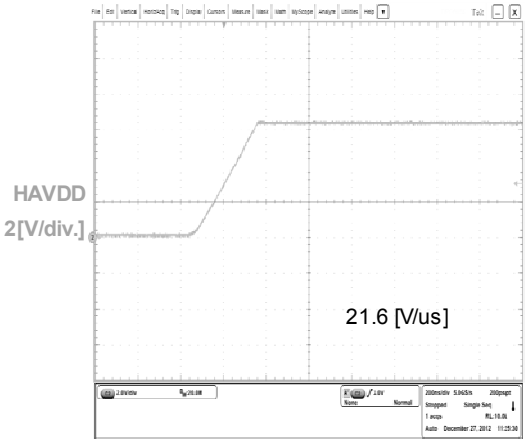


Fig.37 HAVDD Slew Rate （Rise）

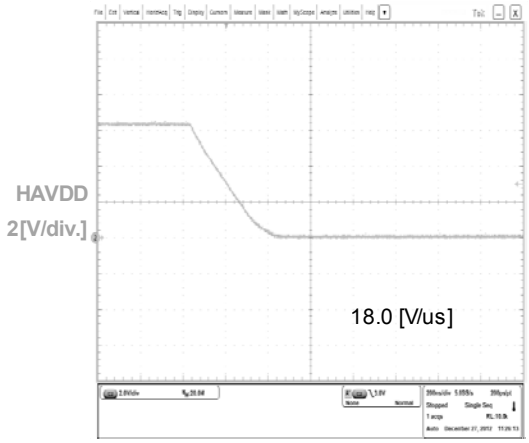


Fig.38 HAVDD Slew Rate （Fall）

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

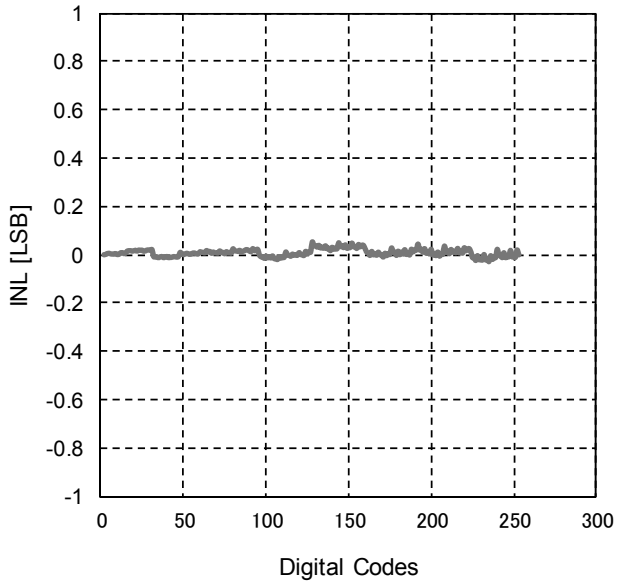


Fig.39 HAVDD INL

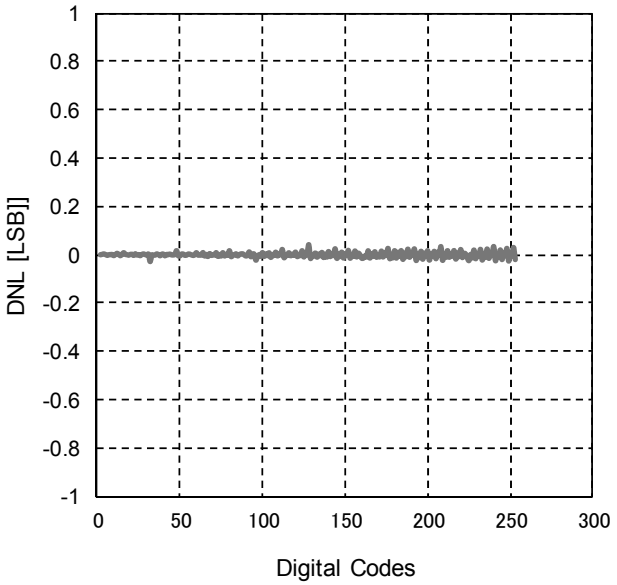


Fig.40 HAVDD DNL

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

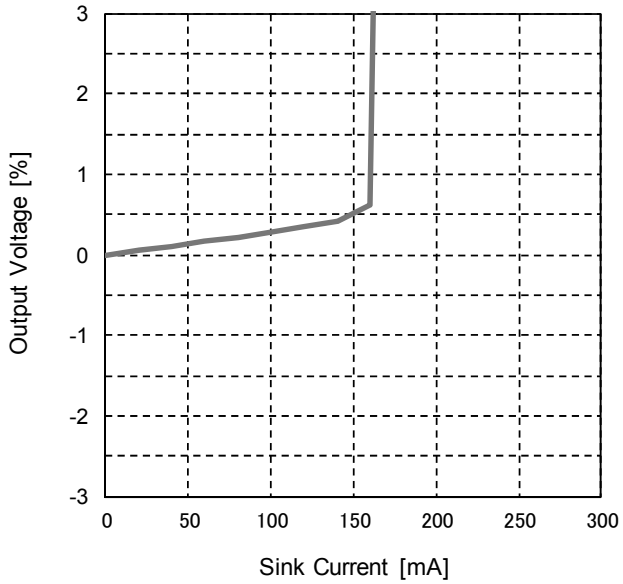


Fig.41 VCOM Sink Current

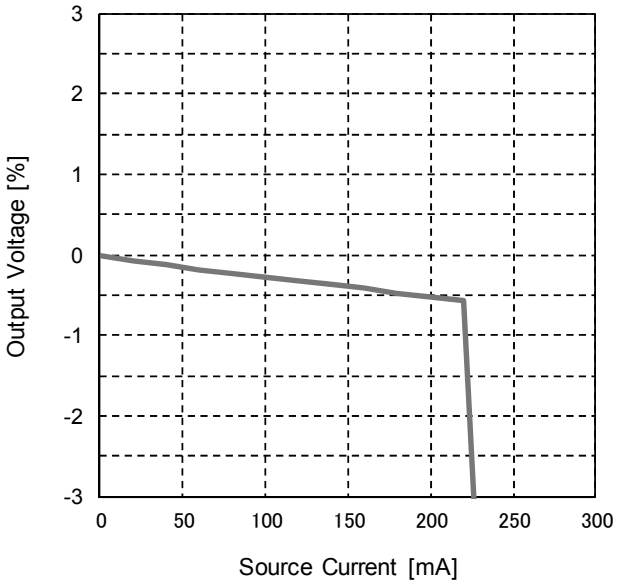


Fig.42 VCOM Source Current

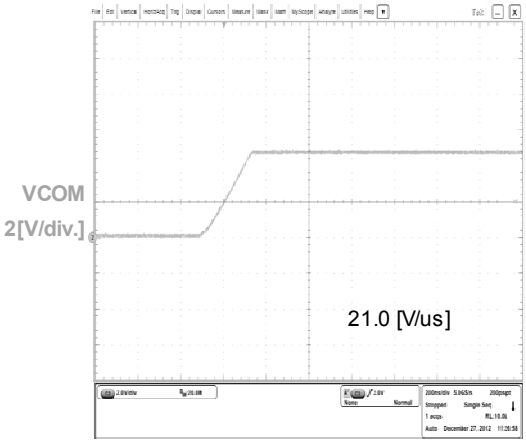


Fig.43 VCOM Slew Rate（Rise）

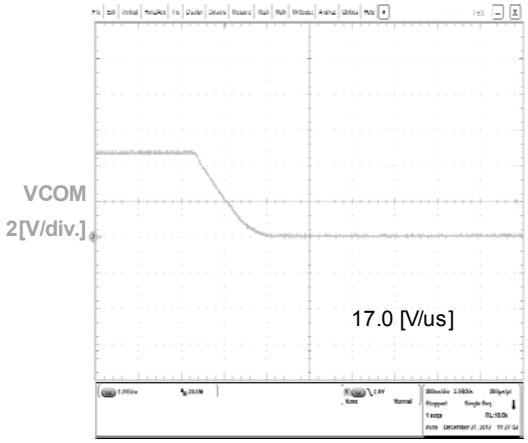


Fig.44 VCOM Slew Rate（Fall）

●**Reference Data**

(Unless otherwise specified, Ta=25℃, VCC, PVCC1, PVCC2=3.3V, VDD1=2.5V, VDD2=1.2V, AVDD=10.5V, VGH=18V, VGL=-6V, HAVDD=5.25V, VCOM=3.25V, no load)

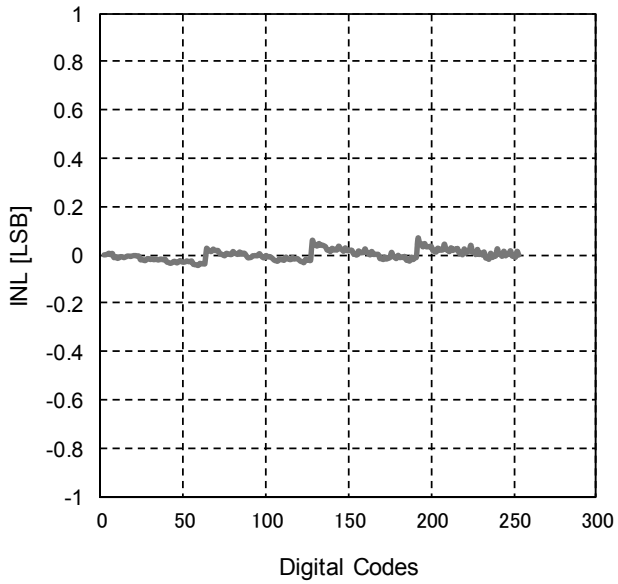


Fig.45 VCOM INL

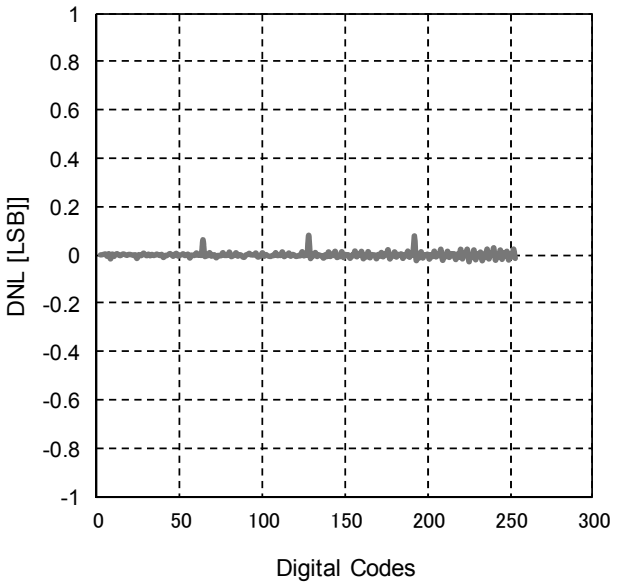


Fig.46 VCOM DNL

●**Timing Chart1**

●**Start-up Sequence (when operated by EN control)**

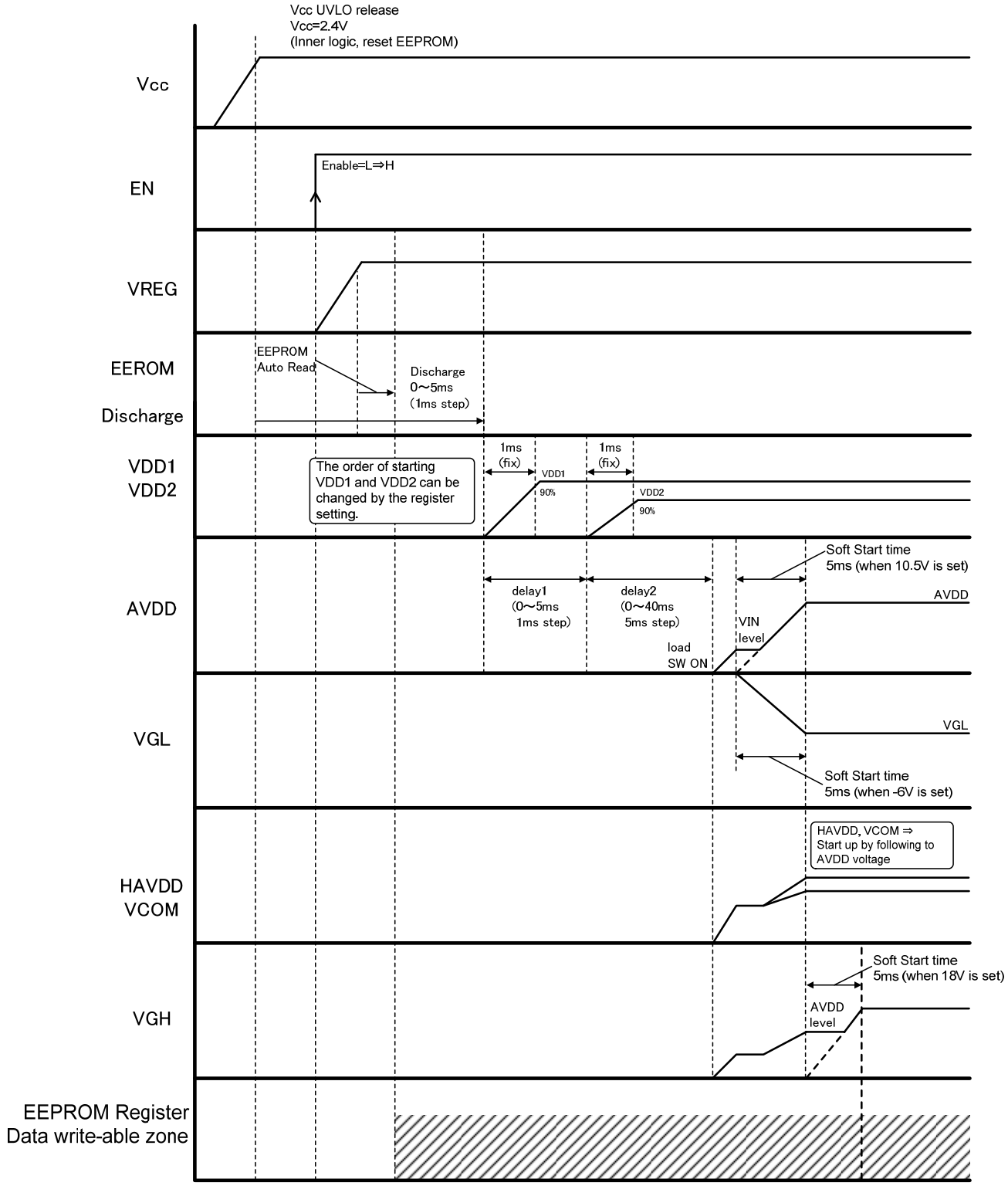


Fig.47 Start-Up Sequence Diagram (when operated by EN control)

●**Timing Chart1**

●**OFF Sequence (when operated by EN control)**

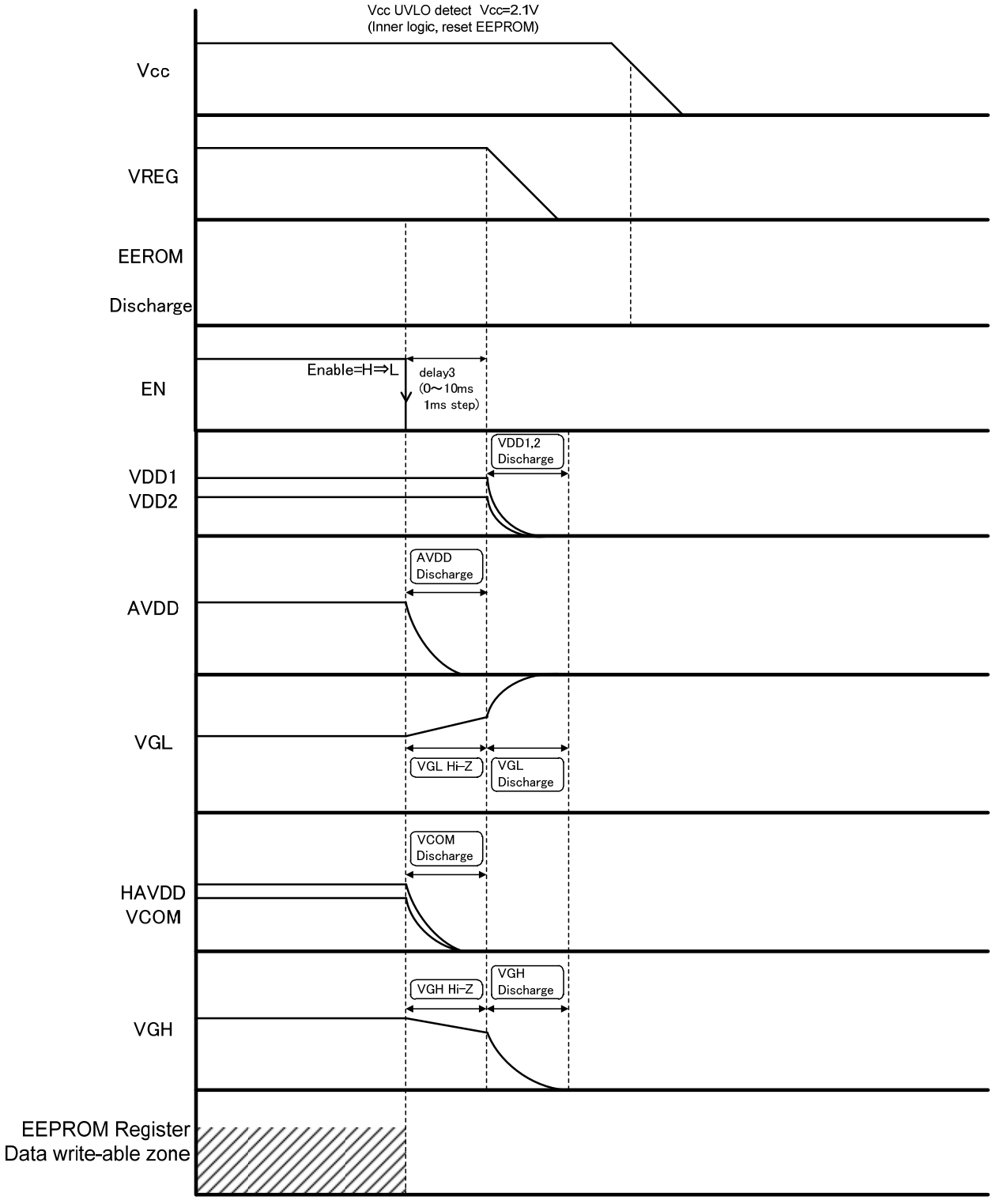


Fig.48 OFF Sequence Block (when operated by EN control)

●Timing Chart2

●Start-up Sequence (when operated with EN= VCC condition)

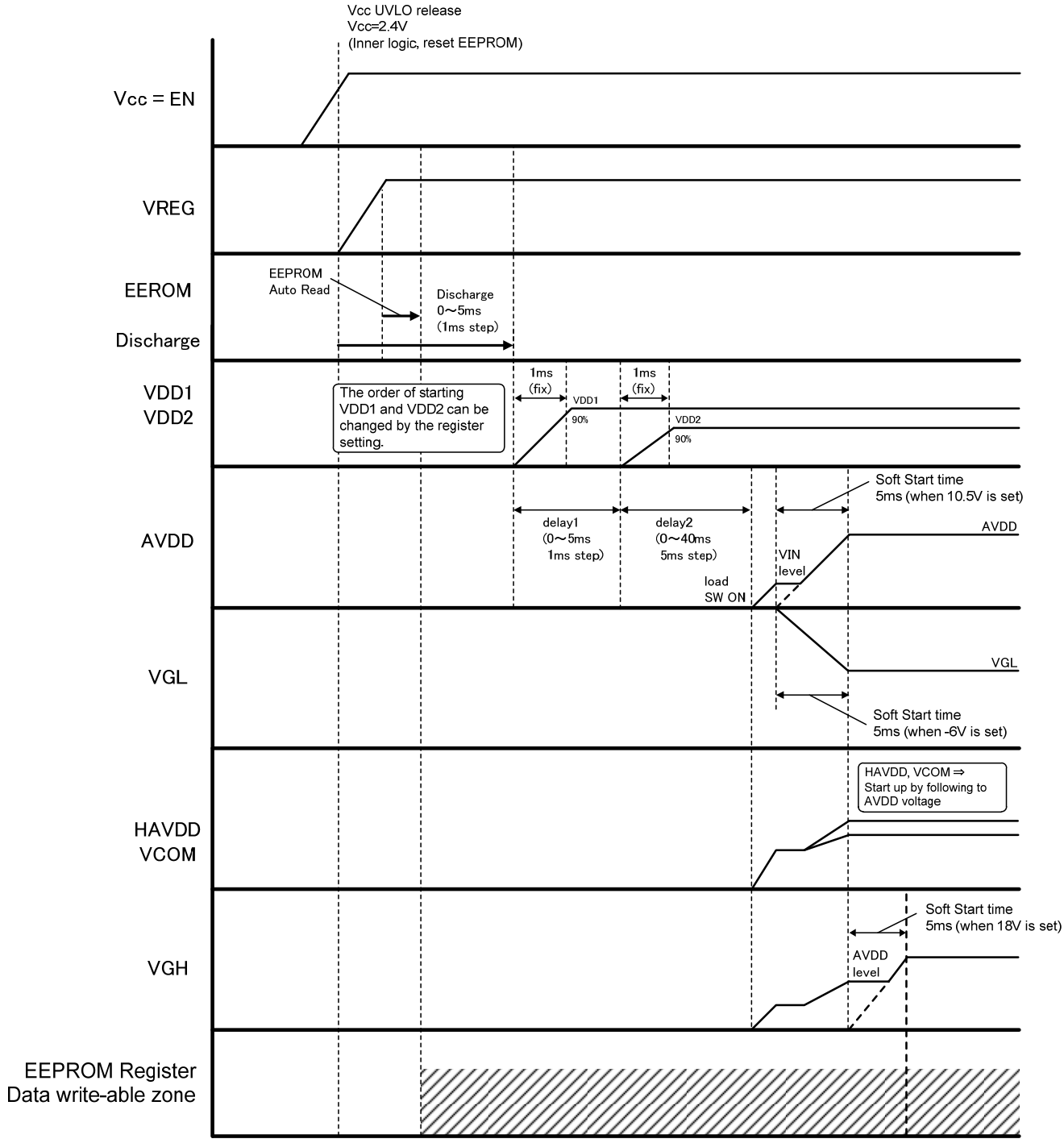


Fig.49 Start-Up Sequence Diagram (when operated with EN= VCC condition)

●**Timing Chart2**

●**OFF Sequence (when operated with EN= VCC condition)**

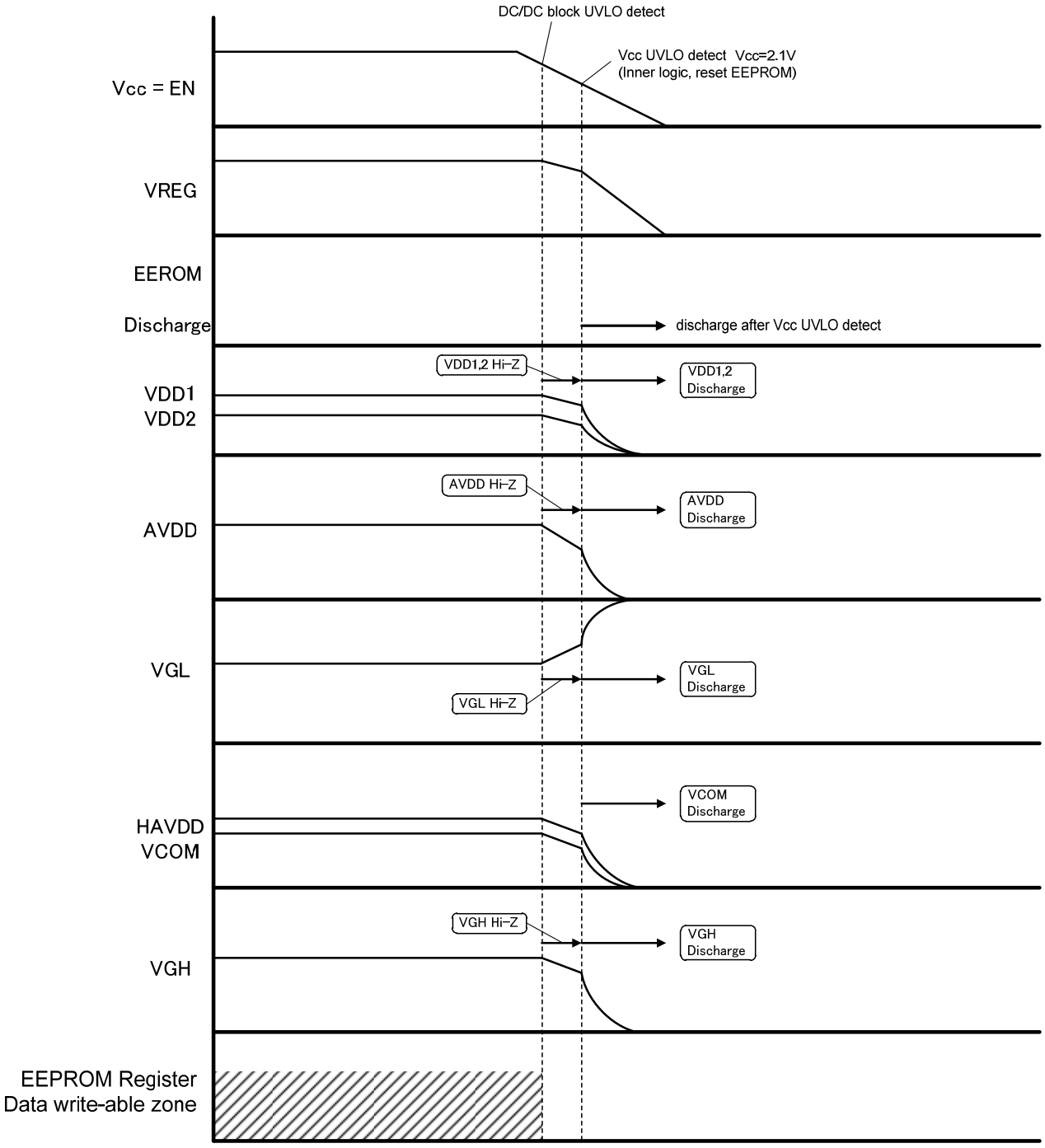


Fig.50 OFF Sequence Diagram (when operated with EN= VCC condition)

●Application Example

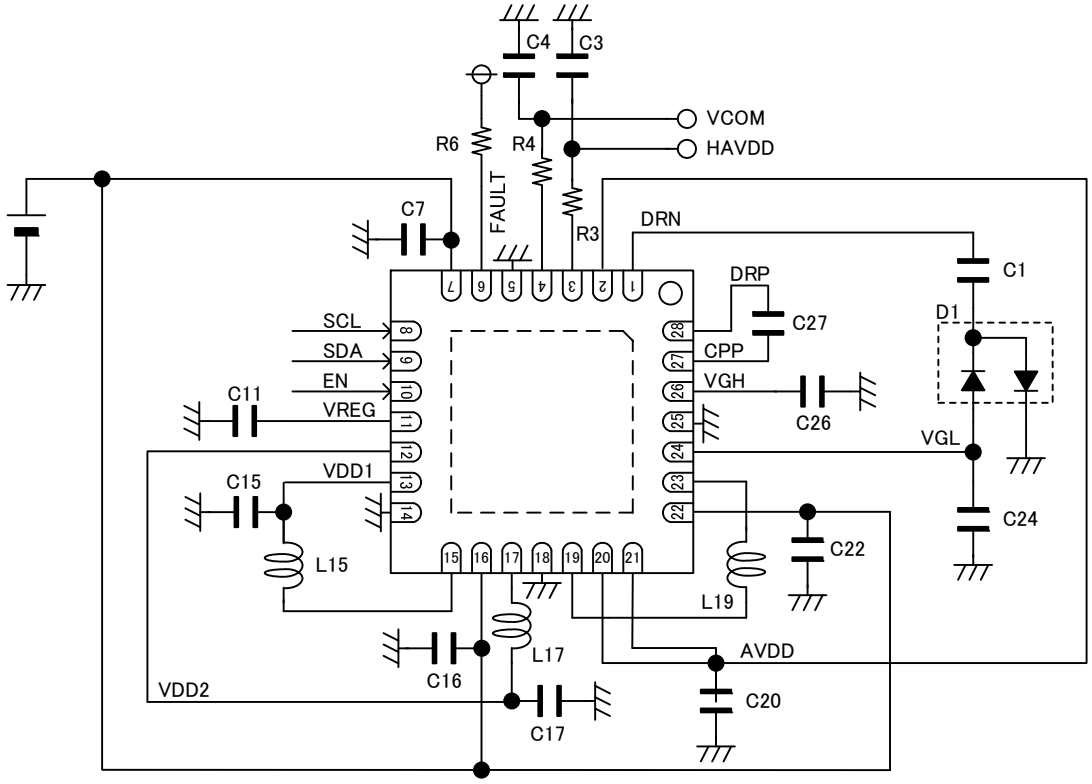


Fig.51 Application Example

Parts name	Value	Company	Parts Number	Parts name	Value	Company	Parts Number
C1	0.1 [μF]	MURATA	GRM155R61H104KE14D	C24	1[μF]	MURATA	GRM188B31C105KA92D
C3	22[μF]	TAIYO YUDEN	EMK316ABJ226KD-T	C26	1[μF]	MURATA	GRM219B31H105KA73
C4	22[μF]	TAIYO YUDEN	EMK316ABJ226KD-T	C27	0.1[μF]	MURATA	GRM155R61H104KE14D
C7	4.7[μF]	TAIYO YUDEN	LMK107BJ475KA-T	R3	10[Ω]	ROHM	MCR03EZPD
C11	1[μF]	MURATA	GRM188B31C105KA92D	R4	10[Ω]	ROHM	MCR03EZPD
C15	10[μF]	TAIYO YUDEN	JMK107BJ106MA-T	R6	100[kΩ]	ROHM	MCR03EZPD
C16	4.7[μF]	TAIYO YUDEN	LMK107BJ475KA-T	D1	-	ROHM	RB558W
C17	10[μF]	TAIYO YUDEN	JMK107BJ106MA-T	L15	4.7[μH]	TOKO	1269AS-H-4R7M
C20	10[μF]×2	TAIYO YUDEN	TMK316ABJ106KD-T	L17	4.7[μH]	TOKO	1269AS-H-4R7M
C22	4.7[μF]	TAIYO YUDEN	LMK107BJ475KA-T	L19	4.7[μH]	TOKO	1276AS-H-4R7M

●**Selecting Application Components**

・Selecting the Output LC Constant (Buck Converter : VDD1, VDD2)

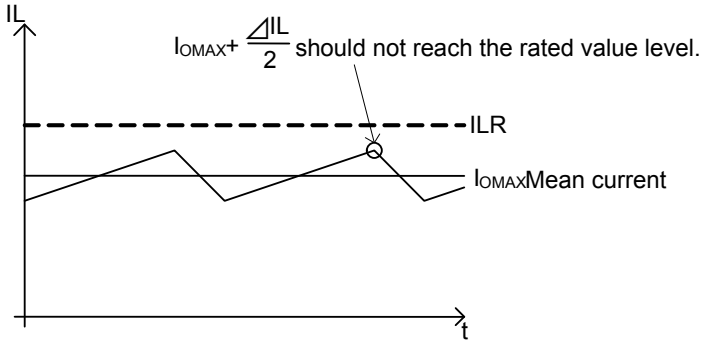


Fig.52 Inductor Current Waveform (Buck Converter : VDD)

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input current (I_{OMAX}) of the inductance.
Adjust so that $I_{OMAX} + \Delta I_L / 2$ does not reach the rated current value.

ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (VIN - VO) \times \frac{VO}{VIN} \times \frac{1}{f} \text{ [A]}$$

where f is the switching frequency

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the coil current exceeds the rated current (I_{LR}), the IC may be damaged.

The output capacitor (C_O) smoothens the ripple voltage at the output. Select a capacitor that will regulate the output ripple voltage within the specifications.

Output ripple voltage can be obtained by the following equation.

$$\Delta VPP = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2\,Co} \times \frac{VO}{VIN} \times \frac{1}{f}$$

However, since the aforementioned conditions are based on a lot of factors, verify the results using the actual product.

・Selecting the Output LC Constant (Boost Converter : AVDD)

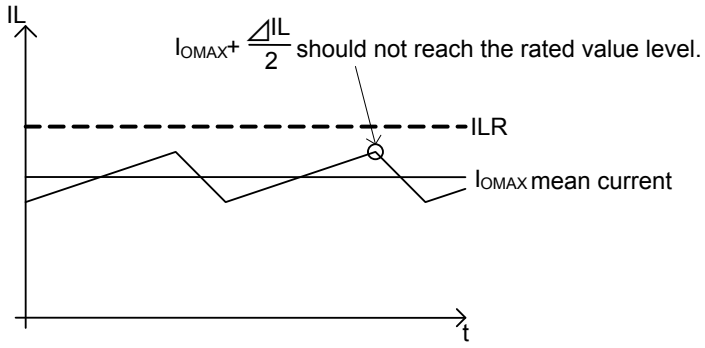


Fig.53 Inductor Current Waveform (Boost Converter : AVDD)

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input current (I_{INMAX}) of the inductance.
Adjust so that $I_{INMAX} + \Delta I_L / 2$ does not reach the rated current value.

ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} VIN \times \frac{VO - VIN}{VO} \times \frac{1}{f} [A]$$

where f is the switching frequency

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the coil current exceeds the rated current (I_{LR}), the IC may be damaged.

The output capacitor (C_O) smoothens the ripple voltage at the output. Select a capacitor that will regulate the output ripple voltage within the specifications.

Output ripple voltage can be obtained by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{f \times CO} \times \frac{VIN}{VO} \times \left(I_{LMAX} - \frac{\Delta I_L}{2} \right)$$

However, since the aforementioned conditions are based on a lot of factors, verify the results using the actual product.

●Serial Transmission

BD81028AMWV uses the I^2C bus in communicating with host addresses.
The device/slave address is always followed by the 1 byte register/select address as shown in the I^2C bus format below.

	MSB						LSB			MSB							LSB		MSB							LSB		
Start	Device address							R/W	ACK	Register address								ACK	Data								ACK	STOP
	A6	A5	A4	A3	A2	A1	A0			R7	R6	R5	R4	R3	R2	R1	R0		D7	D6	D5	D4	D3	D2	D1	D0		

Start : Start bit
Device Address : Consists of 8 bits in total (A6 to A0 and the R/W bit) (MSB fast).
If the R/W bit is H, this means read mode.
If the R/W bit is L, this means write mode.
ACK : Acknowledge bit.
When sending and receiving data, there should be an acknowledge bit after each byte.
If data is sent and received properly, 'L' is replied to the sender.
If data is not received properly, 'H' is replied to the sender.
Register Address : 1 byte select address.
Data : Data byte. Sending and Receiving data (MSB Fast)
STOP : Stop bit

There are two writing modes from I^2C bus to the registers, single mode and multi mode.
In single mode, communication is sent to a single register.
In multi mode, communication is sent to multiple registers by entering multiple data before the stop bit.

●Device address

Slave address specific to the IC is 1000000 (A6 to A0).

●Register address

R7 is for TEST MODE. Normally, this should be set to 0.
R6 and R5 are don't care bits.
R4 to R0 are the register address bits.

●Command interface

Transmission format for data sent and received to the EEPROM is shown below.

Write operation

・PM I^2C Write format (Register Address: 01h to 08h)

Start	Device address							R/W	ACK	Register address	ACK	N-bytes Data	ACK	STOP
	1	0	0	0	0	0	0	0	0	01h～08h	0		0	

Write data in multi mode by entering data continuously after the register address.
Data entry should be 8 bits.

・VCOM I^2C Write format (Register Address: 09h)

Start	Device address							R/W	ACK	Register address	ACK	DATA								ACK	STOP
	1	0	0	0	0	0	0	0	0	09h	0	D7	D6	D5	D4	D3	D2	D1	D0	0	

Write data in single mode (VCOM), designate a register address of 09h.

Read operation

・I^2C Read format

Start	Device address							R/W	ACK	Register address	ACK	Repeated Start	Device address							R/W	ACK	N-bytes Data	ACK	STOP
	1	0	0	0	0	0	0	0	0	01h～09h	0		1	0	0	0	0	0	0	1	0		1	

Read data in the PMIC register through the read command.

●I^2C Timing

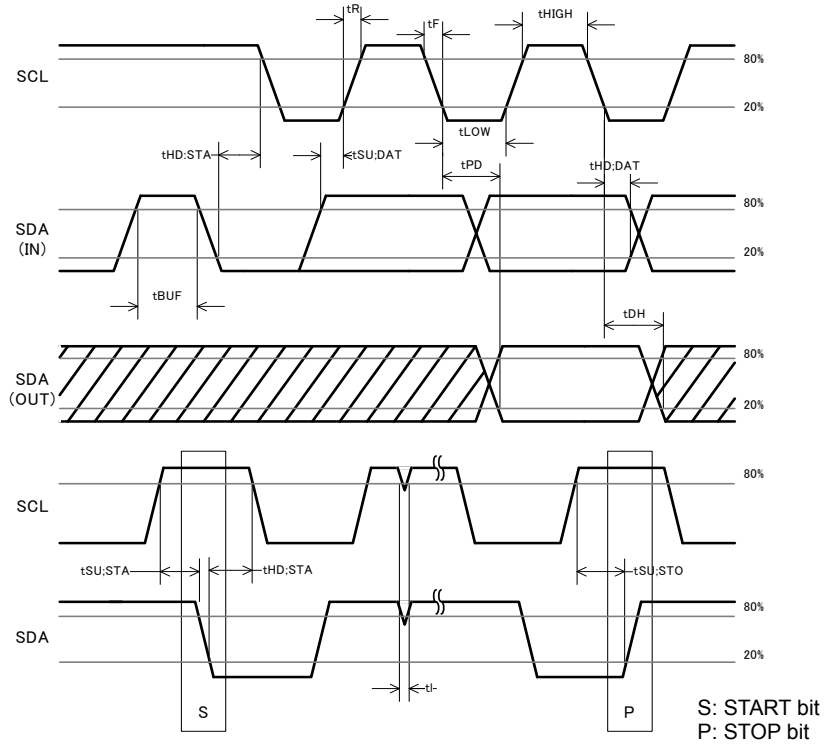


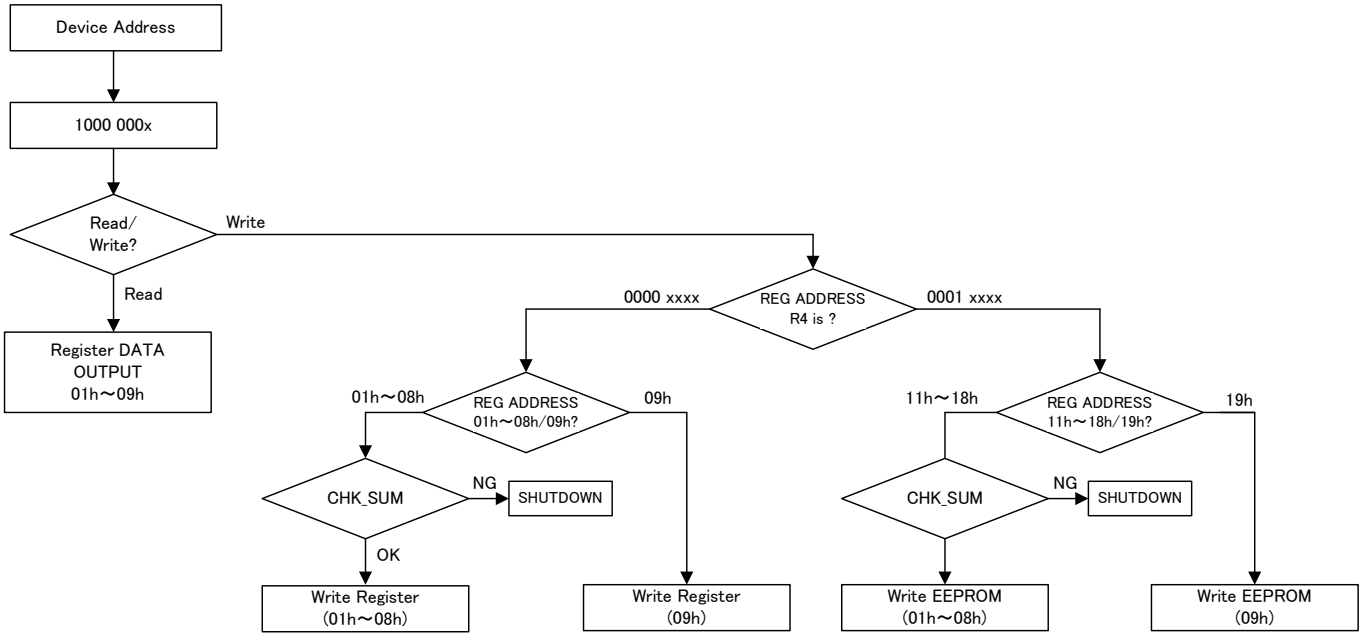
Fig.54. I^2C Timing

・Timing Specification

PARAMETER	SYMBOL	NORMAL mode			FAST mode			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SCL frequency	f_{SCL}	-	-	100	-	-	400	kHz
SCL"H" time	t_{HIGH}	4.0	-	-	0.6	-	-	μs
SCL"L" time	t_{LOW}	4.7	-	-	1.2	-	-	μs
Rising time	t_R	-	-	1.0	-	-	0.3	μs
Falling time	t_F	-	-	0.3	-	-	0.3	μs
Start bit holding time	$t_{HD\ ;\ STA}$	4.0	-	-	0.6	-	-	μs
Start bit setup time	$t_{SU\ ;\ STA}$	4.7	-	-	0.6	-	-	μs
SDA holding time	$t_{HD\ ;\ DAT}$	200	-	-	100	-	-	ns
SDA setup time	$t_{SU\ ;\ DAT}$	200	-	-	100	-	-	ns
Acknowledge delay time	t_{PD}	-	-	0.9	-	-	0.9	μs
Acknowledge hold time	t_{DH}	-	0.1	-	-	0.1	-	μs
Stop bit setup time	$t_{SU\ ;\ STO}$	4.7	-	-	0.6	-	-	μs
BUS open time	t_{BUF}	4.7	-	-	1.2	-	-	μs
Noise spike width	t_I	-	0.1	-	-	0.1	-	μs

●Writing Data to the Register/EEPROM

After power up and when EN is high, data can be written to the registers or the EEPROM.
The logic of the register address R4 will determine where the data will be written.
Check-sum is installed before writing data to prevent malfunctions caused by data error.
The flowchart of the writing process to the register and EEPROM is shown below.



・Writing Data to the Register

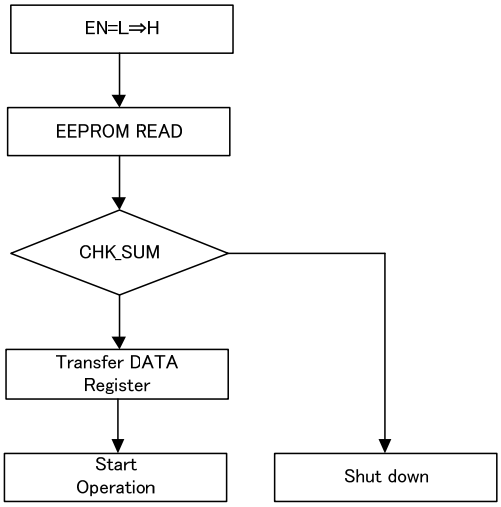
Data is written to the registers when register address R4 is “0”.
AVDD, VGH, VGL, HAVDD, and VCOM (register address: 01h to 04h) output voltage can be changed by writing data to the registers.

・Writing Data to the EEPROM

Data is written to the EEPROM when register address R4 is “1”.
Upon start-up and EN is high, data which is stored in the EEPROM is copied to the registers.
Therefore, by writing to the EEPROM, the start-up settings will be changed.

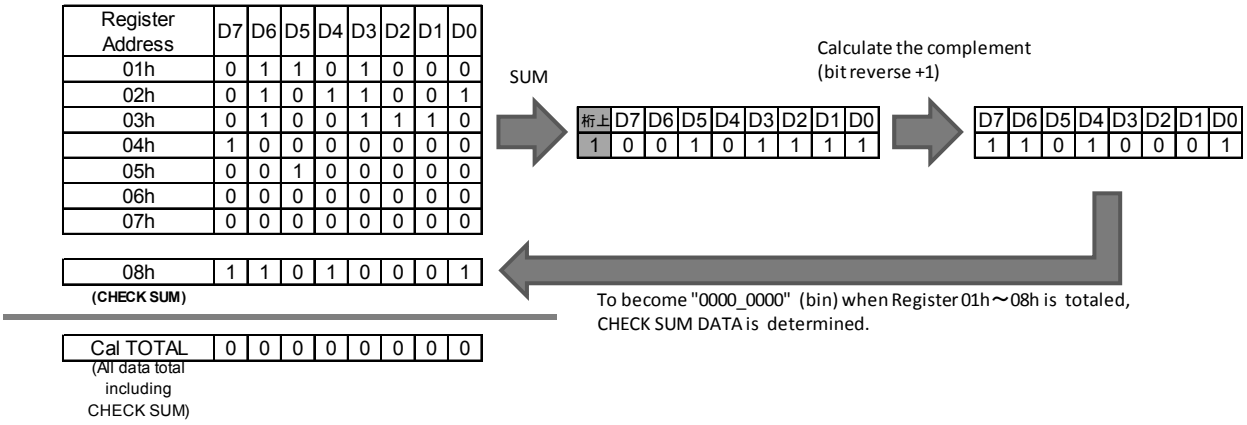
●Automatic EEPROM Read Function at Start-up

Upon BD81028AMWV start-up, a reset signal is generated and each register is initialized.
After that, when EN is changed from low to high, data which is stored in the EEPROM is copied to the registers.
Furthermore, the check-sum function is installed to prevent malfunctions caused by data error.
The automatic EEPROM read function at start-up is further explained by the flow chart below.



●Check-Sum Data

If data is written to the Register and EEPROM, it is necessary to set check-sum data to prevent malfunctions caused by data error. Check-sum data is the complement of the sum of all data. When check-sum data is added to the sum of all data, the result should be zero.



●Return to Normal Operation after Shutdown at Check-Sum Error

A check-sum of zero indicates a data error and this causes the PMIC to latch in shutdown. There are two ways to reactivate the PMIC. First, write to the EEPROM the correct data while the power supply is turned on and EN=L; then toggle EN to H. Lastly, reset the power supply and enter the correct data while EN=H.

●**EEPROM Parameter Setting**

Register Address	Bits	Function	Default	Resolution
01h	8	AVDD Output voltage setting	9.8V	0.1V [8V to 14.5V]
02h	8	VGH Output voltage setting	18V	0.2V [13V to 26V]
03h	8	VGL Output voltage setting	-6.0V	0.1V [-9.5V to -4.0]
04h	8	HAVDD Output voltage setting	4.23V	12.5mV
05h	8	VDD1 Output voltage setting [3:0] VDD2 Output voltage setting [6:4] VDD startup order setting [7]	1.8V 1.2V 0	0.05V [1.7 to 1.9, 2.4 to 2.6V] 0.05V [1.1V to 1.3V] 0：VDD1→2,　1：VDD2→1
06h	7	Discharge time setting [2:0] DELAY1 time setting [5:3] DC/DC UVLO detect/release voltage [7:6]	0msec 0msec 2.5/2.7V	1msec [0 to 5msec] 1msec [0 to 5msec] 0.2V step
07h	7	DELAY2 time setting [2:0] DELAY3 time setting [6:3] Frequency setting [7]	30msec 0msec 1200kHz	5msec [0 to 40msec] 2msec [0 to 10msec] 0：600kHz , 1：1200kHz
08h	8	8 bit Check-sum	42h	―
09h	8	VCOM Output voltage setting	2.1225V	12.5mV

●**Register map**

Resister Address	D7	D6	D5	D4	D3	D2	D1	D0
01h	AVDD [7:0]							
02h	VGH [7:0]							
03h	VGL [7:0]							
04h	HAVDD [7:0]							
05h	SEQ[0]	VDD2 [2:0]			VDD1 [3:0]			
06h	UVLO[1:0]		DELAY1[2:0]			DISCHG[2:0]		
07h	FREQ[0]	DELAY3 [2:0]			DELAY2 [3:0]			
08h	CHECK SUM[7:0]							
09h	VCOM [7:0]							

●Command Table 1

DATA		Register													
		01h	02h	03h	04h	05h			06h			07h			09h
		AVDD Voltage Setting	VGH Voltage Setting	VGL Voltage Setting	HAVDD Voltage Setting	VDD ON Sequence	VDD2 Voltage Setting	VDD1 Voltage Setting	DC/DC UVLO Detect/Release Voltage	DELAY1 Time Setting	Discharge Time Setting	Frequency Setting	DELAY3 Time Setting	DELAY2 Time Setting	VCOM Voltage Setting
DEC.	HEX.	[V]	[V]	[V]	[V]		[V]	[V]	[V]	[msec]	[msec]	[kHz]	[msec]	[msec]	[V]
0	00	14.5	26.0	−4.0	0.6×AVDD	VDD1→VDD2	1.10	1.70	2.5 / 2.7	0	0	600	0	0	0.45×AVDD
1	01	14.5	26.0	−4.0	0.6×AVDD−0.0125	VDD1→VDD2	1.10	1.75	2.5 / 2.7	0	1	600	0	5	0.45×AVDD−0.0125
2	02	14.5	26.0	−4.0	0.6×AVDD−0.0250	VDD1→VDD2	1.10	1.80	2.5 / 2.7	0	2	600	0	10	0.45×AVDD−0.0250
3	03	14.5	26.0	−4.0	0.6×AVDD−0.0375	VDD1→VDD2	1.10	1.85	2.5 / 2.7	0	3	600	0	15	0.45×AVDD−0.0375
4	04	14.5	26.0	−4.0	0.6×AVDD−0.0500	VDD1→VDD2	1.10	1.90	2.5 / 2.7	0	4	600	0	20	0.45×AVDD−0.0500
5	05	14.5	26.0	−4.0	0.6×AVDD−0.0625	VDD1→VDD2	1.10	2.40	2.5 / 2.7	0	5	600	0	25	0.45×AVDD−0.0625
6	06	14.5	26.0	−4.0	0.6×AVDD−0.0750	VDD1→VDD2	1.10	2.45	2.5 / 2.7	0	0	600	0	30	0.45×AVDD−0.0750
7	07	14.5	26.0	−4.0	0.6×AVDD−0.0875	VDD1→VDD2	1.10	2.50	2.5 / 2.7	0	0	600	0	35	0.45×AVDD−0.0875
8	08	14.5	26.0	−4.0	0.6×AVDD−0.1000	VDD1→VDD2	1.10	2.55	2.5 / 2.7	1	0	600	0	40	0.45×AVDD−0.1000
9	09	14.5	26.0	−4.0	0.6×AVDD−0.1125	VDD1→VDD2	1.10	2.60	2.5 / 2.7	1	1	600	0	0	0.45×AVDD−0.1125
10	0A	14.5	26.0	−4.0	0.6×AVDD−0.1250	VDD1→VDD2	1.10	2.60	2.5 / 2.7	1	2	600	0	0	0.45×AVDD−0.1250
11	0B	14.5	26.0	−4.0	0.6×AVDD−0.1375	VDD1→VDD2	1.10	2.60	2.5 / 2.7	1	3	600	0	0	0.45×AVDD−0.1375
12	0C	14.5	26.0	−4.0	0.6×AVDD−0.1500	VDD1→VDD2	1.10	2.60	2.5 / 2.7	1	4	600	0	0	0.45×AVDD−0.1500
13	0D	14.5	26.0	−4.0	0.6×AVDD−0.1625	VDD1→VDD2	1.10	2.60	2.5 / 2.7	1	5	600	0	0	0.45×AVDD−0.1625
14	0E	14.5	26.0	−4.0	0.6×AVDD−0.1750	VDD1→VDD2	1.10	2.60	2.5 / 2.7	1	0	600	0	0	0.45×AVDD−0.1750
15	0F	14.5	26.0	−4.0	0.6×AVDD−0.1875	VDD1→VDD2	1.10	2.60	2.5 / 2.7	1	0	600	0	0	0.45×AVDD−0.1875
16	10	14.5	26.0	−4.0	0.6×AVDD−0.2000	VDD1→VDD2	1.15	1.70	2.5 / 2.7	2	0	600	2	0	0.45×AVDD−0.2000
17	11	14.5	26.0	−4.0	0.6×AVDD−0.2125	VDD1→VDD2	1.15	1.75	2.5 / 2.7	2	1	600	2	5	0.45×AVDD−0.2125
18	12	14.5	26.0	−4.0	0.6×AVDD−0.2250	VDD1→VDD2	1.15	1.80	2.5 / 2.7	2	2	600	2	10	0.45×AVDD−0.2250
19	13	14.5	26.0	−4.0	0.6×AVDD−0.2375	VDD1→VDD2	1.15	1.85	2.5 / 2.7	2	3	600	2	15	0.45×AVDD−0.2375
20	14	14.5	26.0	−4.0	0.6×AVDD−0.2500	VDD1→VDD2	1.15	1.90	2.5 / 2.7	2	4	600	2	20	0.45×AVDD−0.2500
21	15	14.5	26.0	−4.0	0.6×AVDD−0.2625	VDD1→VDD2	1.15	2.40	2.5 / 2.7	2	5	600	2	25	0.45×AVDD−0.2625
22	16	14.5	26.0	−4.0	0.6×AVDD−0.2750	VDD1→VDD2	1.15	2.45	2.5 / 2.7	2	0	600	2	30	0.45×AVDD−0.2750
23	17	14.5	26.0	−4.0	0.6×AVDD−0.2875	VDD1→VDD2	1.15	2.50	2.5 / 2.7	2	0	600	2	35	0.45×AVDD−0.2875
24	18	14.5	26.0	−4.0	0.6×AVDD−0.3000	VDD1→VDD2	1.15	2.55	2.5 / 2.7	3	0	600	2	40	0.45×AVDD−0.3000
25	19	14.5	26.0	−4.0	0.6×AVDD−0.3125	VDD1→VDD2	1.15	2.60	2.5 / 2.7	3	1	600	2	0	0.45×AVDD−0.3125
26	1A	14.5	26.0	−4.0	0.6×AVDD−0.3250	VDD1→VDD2	1.15	2.60	2.5 / 2.7	3	2	600	2	0	0.45×AVDD−0.3250
27	1B	14.5	26.0	−4.0	0.6×AVDD−0.3375	VDD1→VDD2	1.15	2.60	2.5 / 2.7	3	3	600	2	0	0.45×AVDD−0.3375
28	1C	14.5	26.0	−4.0	0.6×AVDD−0.3500	VDD1→VDD2	1.15	2.60	2.5 / 2.7	3	4	600	2	0	0.45×AVDD−0.3500
29	1D	14.5	26.0	−4.0	0.6×AVDD−0.3625	VDD1→VDD2	1.15	2.60	2.5 / 2.7	3	5	600	2	0	0.45×AVDD−0.3625
30	1E	14.5	26.0	−4.0	0.6×AVDD−0.3750	VDD1→VDD2	1.15	2.60	2.5 / 2.7	3	0	600	2	0	0.45×AVDD−0.3750
31	1F	14.5	26.0	−4.0	0.6×AVDD−0.3875	VDD1→VDD2	1.15	2.60	2.5 / 2.7	3	0	600	2	0	0.45×AVDD−0.3875
32	20	14.5	26.0	−4.0	0.6×AVDD−0.4000	VDD1→VDD2	1.20	1.70	2.5 / 2.7	4	0	600	4	0	0.45×AVDD−0.4000
33	21	14.5	26.0	−4.0	0.6×AVDD−0.4125	VDD1→VDD2	1.20	1.75	2.5 / 2.7	4	1	600	4	5	0.45×AVDD−0.4125
34	22	14.5	26.0	−4.0	0.6×AVDD−0.4250	VDD1→VDD2	1.20	1.80	2.5 / 2.7	4	2	600	4	10	0.45×AVDD−0.4250
35	23	14.5	26.0	−4.0	0.6×AVDD−0.4375	VDD1→VDD2	1.20	1.85	2.5 / 2.7	4	3	600	4	15	0.45×AVDD−0.4375
36	24	14.5	26.0	−4.0	0.6×AVDD−0.4500	VDD1→VDD2	1.20	1.90	2.5 / 2.7	4	4	600	4	20	0.45×AVDD−0.4500
37	25	14.5	26.0	−4.0	0.6×AVDD−0.4625	VDD1→VDD2	1.20	2.40	2.5 / 2.7	4	5	600	4	25	0.45×AVDD−0.4625
38	26	14.5	26.0	−4.0	0.6×AVDD−0.4750	VDD1→VDD2	1.20	2.45	2.5 / 2.7	4	0	600	4	30	0.45×AVDD−0.4750
39	27	14.5	26.0	−4.0	0.6×AVDD−0.4875	VDD1→VDD2	1.20	2.50	2.5 / 2.7	4	0	600	4	35	0.45×AVDD−0.4875
40	28	14.5	26.0	−4.0	0.6×AVDD−0.5000	VDD1→VDD2	1.20	2.55	2.5 / 2.7	5	0	600	4	40	0.45×AVDD−0.5000
41	29	14.5	26.0	−4.0	0.6×AVDD−0.5125	VDD1→VDD2	1.20	2.60	2.5 / 2.7	5	1	600	4	0	0.45×AVDD−0.5125
42	2A	14.5	26.0	−4.0	0.6×AVDD−0.5250	VDD1→VDD2	1.20	2.60	2.5 / 2.7	5	2	600	4	0	0.45×AVDD−0.5250
43	2B	14.5	26.0	−4.0	0.6×AVDD−0.5375	VDD1→VDD2	1.20	2.60	2.5 / 2.7	5	3	600	4	0	0.45×AVDD−0.5375
44	2C	14.5	26.0	−4.0	0.6×AVDD−0.5500	VDD1→VDD2	1.20	2.60	2.5 / 2.7	5	4	600	4	0	0.45×AVDD−0.5500
45	2D	14.5	26.0	−4.0	0.6×AVDD−0.5625	VDD1→VDD2	1.20	2.60	2.5 / 2.7	5	5	600	4	0	0.45×AVDD−0.5625
46	2E	14.5	26.0	−4.0	0.6×AVDD−0.5750	VDD1→VDD2	1.20	2.60	2.5 / 2.7	5	0	600	4	0	0.45×AVDD−0.5750
47	2F	14.5	26.0	−4.0	0.6×AVDD−0.5875	VDD1→VDD2	1.20	2.60	2.5 / 2.7	5	0	600	4	0	0.45×AVDD−0.5875
48	30	14.5	26.0	−4.0	0.6×AVDD−0.6000	VDD1→VDD2	1.25	1.70	2.5 / 2.7	0	0	600	6	0	0.45×AVDD−0.6000
49	31	14.5	26.0	−4.0	0.6×AVDD−0.6125	VDD1→VDD2	1.25	1.75	2.5 / 2.7	0	1	600	6	5	0.45×AVDD−0.6125
50	32	14.5	26.0	−4.0	0.6×AVDD−0.6250	VDD1→VDD2	1.25	1.80	2.5 / 2.7	0	2	600	6	10	0.45×AVDD−0.6250
51	33	14.5	26.0	−4.0	0.6×AVDD−0.6375	VDD1→VDD2	1.25	1.85	2.5 / 2.7	0	3	600	6	15	0.45×AVDD−0.6375
52	34	14.5	26.0	−4.0	0.6×AVDD−0.6500	VDD1→VDD2	1.25	1.90	2.5 / 2.7	0	4	600	6	20	0.45×AVDD−0.6500
53	35	14.5	26.0	−4.0	0.6×AVDD−0.6625	VDD1→VDD2	1.25	2.40	2.5 / 2.7	0	5	600	6	25	0.45×AVDD−0.6625
54	36	14.5	26.0	−4.0	0.6×AVDD−0.6750	VDD1→VDD2	1.25	2.45	2.5 / 2.7	0	0	600	6	30	0.45×AVDD−0.6750
55	37	14.5	26.0	−4.0	0.6×AVDD−0.6875	VDD1→VDD2	1.25	2.50	2.5 / 2.7	0	0	600	6	35	0.45×AVDD−0.6875
56	38	14.5	26.0	−4.0	0.6×AVDD−0.7000	VDD1→VDD2	1.25	2.55	2.5 / 2.7	0	0	600	6	40	0.45×AVDD−0.7000
57	39	14.5	26.0	−4.0	0.6×AVDD−0.7125	VDD1→VDD2	1.25	2.60	2.5 / 2.7	0	1	600	6	0	0.45×AVDD−0.7125
58	3A	14.5	26.0	−4.0	0.6×AVDD−0.7250	VDD1→VDD2	1.25	2.60	2.5 / 2.7	0	2	600	6	0	0.45×AVDD−0.7250
59	3B	14.5	26.0	−4.1	0.6×AVDD−0.7375	VDD1→VDD2	1.25	2.60	2.5 / 2.7	0	3	600	6	0	0.45×AVDD−0.7375
60	3C	14.5	26.0	−4.2	0.6×AVDD−0.7500	VDD1→VDD2	1.25	2.60	2.5 / 2.7	0	4	600	6	0	0.45×AVDD−0.7500
61	3D	14.5	26.0	−4.3	0.6×AVDD−0.7625	VDD1→VDD2	1.25	2.60	2.5 / 2.7	0	5	600	6	0	0.45×AVDD−0.7625
62	3E	14.5	26.0	−4.4	0.6×AVDD−0.7750	VDD1→VDD2	1.25	2.60	2.5 / 2.7	0	0	600	6	0	0.45×AVDD−0.7750
63	3F	14.5	26.0	−4.5	0.6×AVDD−0.7875	VDD1→VDD2	1.25	2.60	2.5 / 2.7	0	0	600	6	0	0.45×AVDD−0.7875

●Command Table 2

		Register													
DATA		01h	02h	03h	04h	05h			06h			07h			09h
		AVDD Voltage Setting	VGH Voltage Setting	VGL Voltage Setting	HAVDD Voltage Setting	VDD ON Sequence	VDD2 Voltage Setting	VDD1 Voltage Setting	DC/DC UVLO Detect/Release Voltage	DELAY1 Time Setting	Discharge Time Setting	Frequency Setting	DELAY3 Time Setting	DELAY2 Time Setting	VCOM Voltage Setting
DEC.	HEX.	[V]	[V]	[V]	[V]		[V]	[V]	[V]	[msec]	[msec]	[kHz]	[msec]	[msec]	[V]
64	40	14.5	26.0	−4.6	0.6×AVDD−0.8000	VDD1→VDD2	1.30	1.70	2.7 / 2.9	0	0	600	8	0	0.45×AVDD−0.8000
65	41	14.5	26.0	−4.7	0.6×AVDD−0.8125	VDD1→VDD2	1.30	1.75	2.7 / 2.9	0	1	600	8	5	0.45×AVDD−0.8125
66	42	14.5	26.0	−4.8	0.6×AVDD−0.8250	VDD1→VDD2	1.30	1.80	2.7 / 2.9	0	2	600	8	10	0.45×AVDD−0.8250
67	43	14.5	26.0	−4.9	0.6×AVDD−0.8375	VDD1→VDD2	1.30	1.85	2.7 / 2.9	0	3	600	8	15	0.45×AVDD−0.8375
68	44	14.5	26.0	−5.0	0.6×AVDD−0.8500	VDD1→VDD2	1.30	1.90	2.7 / 2.9	0	4	600	8	20	0.45×AVDD−0.8500
69	45	14.5	26.0	−5.1	0.6×AVDD−0.8625	VDD1→VDD2	1.30	2.40	2.7 / 2.9	0	5	600	8	25	0.45×AVDD−0.8625
70	46	14.5	26.0	−5.2	0.6×AVDD−0.8750	VDD1→VDD2	1.30	2.45	2.7 / 2.9	0	0	600	8	30	0.45×AVDD−0.8750
71	47	14.5	26.0	−5.3	0.6×AVDD−0.8875	VDD1→VDD2	1.30	2.50	2.7 / 2.9	0	0	600	8	35	0.45×AVDD−0.8875
72	48	14.5	26.0	−5.4	0.6×AVDD−0.9000	VDD1→VDD2	1.30	2.55	2.7 / 2.9	1	0	600	8	40	0.45×AVDD−0.9000
73	49	14.5	26.0	−5.5	0.6×AVDD−0.9125	VDD1→VDD2	1.30	2.60	2.7 / 2.9	1	1	600	8	0	0.45×AVDD−0.9125
74	4A	14.5	26.0	−5.6	0.6×AVDD−0.9250	VDD1→VDD2	1.30	2.60	2.7 / 2.9	1	2	600	8	0	0.45×AVDD−0.9250
75	4B	14.5	26.0	−5.7	0.6×AVDD−0.9375	VDD1→VDD2	1.30	2.60	2.7 / 2.9	1	3	600	8	0	0.45×AVDD−0.9375
76	4C	14.5	26.0	−5.8	0.6×AVDD−0.9500	VDD1→VDD2	1.30	2.60	2.7 / 2.9	1	4	600	8	0	0.45×AVDD−0.9500
77	4D	14.5	26.0	−5.9	0.6×AVDD−0.9625	VDD1→VDD2	1.30	2.60	2.7 / 2.9	1	5	600	8	0	0.45×AVDD−0.9625
78	4E	14.5	26.0	−6.0	0.6×AVDD−0.9750	VDD1→VDD2	1.30	2.60	2.7 / 2.9	1	0	600	8	0	0.45×AVDD−0.9750
79	4F	14.5	26.0	−6.1	0.6×AVDD−0.9875	VDD1→VDD2	1.30	2.60	2.7 / 2.9	1	0	600	8	0	0.45×AVDD−0.9875
80	50	14.5	26.0	−6.2	0.6×AVDD−1.0000	VDD1→VDD2	1.30	1.70	2.7 / 2.9	2	0	600	10	0	0.45×AVDD−1.0000
81	51	14.5	26.0	−6.3	0.6×AVDD−1.0125	VDD1→VDD2	1.30	1.75	2.7 / 2.9	2	1	600	10	5	0.45×AVDD−1.0125
82	52	14.5	26.0	−6.4	0.6×AVDD−1.0250	VDD1→VDD2	1.30	1.80	2.7 / 2.9	2	2	600	10	10	0.45×AVDD−1.0250
83	53	14.5	26.0	−6.5	0.6×AVDD−1.0375	VDD1→VDD2	1.30	1.85	2.7 / 2.9	2	3	600	10	15	0.45×AVDD−1.0375
84	54	14.5	26.0	−6.6	0.6×AVDD−1.0500	VDD1→VDD2	1.30	1.90	2.7 / 2.9	2	4	600	10	20	0.45×AVDD−1.0500
85	55	14.5	26.0	−6.7	0.6×AVDD−1.0625	VDD1→VDD2	1.30	2.40	2.7 / 2.9	2	5	600	10	25	0.45×AVDD−1.0625
86	56	14.5	26.0	−6.8	0.6×AVDD−1.0750	VDD1→VDD2	1.30	2.45	2.7 / 2.9	2	0	600	10	30	0.45×AVDD−1.0750
87	57	14.5	26.0	−6.9	0.6×AVDD−1.0875	VDD1→VDD2	1.30	2.50	2.7 / 2.9	2	0	600	10	35	0.45×AVDD−1.0875
88	58	14.5	26.0	−7.0	0.6×AVDD−1.1000	VDD1→VDD2	1.30	2.55	2.7 / 2.9	3	0	600	10	40	0.45×AVDD−1.1000
89	59	14.5	26.0	−7.1	0.6×AVDD−1.1125	VDD1→VDD2	1.30	2.60	2.7 / 2.9	3	1	600	10	0	0.45×AVDD−1.1125
90	5A	14.5	26.0	−7.2	0.6×AVDD−1.1250	VDD1→VDD2	1.30	2.60	2.7 / 2.9	3	2	600	10	0	0.45×AVDD−1.1250
91	5B	14.5	26.0	−7.3	0.6×AVDD−1.1375	VDD1→VDD2	1.30	2.60	2.7 / 2.9	3	3	600	10	0	0.45×AVDD−1.1375
92	5C	14.5	26.0	−7.4	0.6×AVDD−1.1500	VDD1→VDD2	1.30	2.60	2.7 / 2.9	3	4	600	10	0	0.45×AVDD−1.1500
93	5D	14.5	26.0	−7.5	0.6×AVDD−1.1625	VDD1→VDD2	1.30	2.60	2.7 / 2.9	3	5	600	10	0	0.45×AVDD−1.1625
94	5E	14.5	26.0	−7.6	0.6×AVDD−1.1750	VDD1→VDD2	1.30	2.60	2.7 / 2.9	3	0	600	10	0	0.45×AVDD−1.1750
95	5F	14.5	26.0	−7.7	0.6×AVDD−1.1875	VDD1→VDD2	1.30	2.60	2.7 / 2.9	3	0	600	10	0	0.45×AVDD−1.1875
96	60	14.5	26.0	−7.8	0.6×AVDD−1.2000	VDD1→VDD2	1.30	1.70	2.7 / 2.9	4	0	600	0	0	0.45×AVDD−1.2000
97	61	14.5	26.0	−7.9	0.6×AVDD−1.2125	VDD1→VDD2	1.30	1.75	2.7 / 2.9	4	1	600	0	5	0.45×AVDD−1.2125
98	62	14.5	26.0	−8.0	0.6×AVDD−1.2250	VDD1→VDD2	1.30	1.80	2.7 / 2.9	4	2	600	0	10	0.45×AVDD−1.2250
99	63	14.5	26.0	−8.1	0.6×AVDD−1.2375	VDD1→VDD2	1.30	1.85	2.7 / 2.9	4	3	600	0	15	0.45×AVDD−1.2375
100	64	14.5	26.0	−8.2	0.6×AVDD−1.2500	VDD1→VDD2	1.30	1.90	2.7 / 2.9	4	4	600	0	20	0.45×AVDD−1.2500
101	65	14.5	26.0	−8.3	0.6×AVDD−1.2625	VDD1→VDD2	1.30	2.40	2.7 / 2.9	4	5	600	0	25	0.45×AVDD−1.2625
102	66	14.5	26.0	−8.4	0.6×AVDD−1.2750	VDD1→VDD2	1.30	2.45	2.7 / 2.9	4	0	600	0	30	0.45×AVDD−1.2750
103	67	14.5	26.0	−8.5	0.6×AVDD−1.2875	VDD1→VDD2	1.30	2.50	2.7 / 2.9	4	0	600	0	35	0.45×AVDD−1.2875
104	68	14.5	26.0	−8.6	0.6×AVDD−1.3000	VDD1→VDD2	1.30	2.55	2.7 / 2.9	5	0	600	0	40	0.45×AVDD−1.3000
105	69	14.5	26.0	−8.7	0.6×AVDD−1.3125	VDD1→VDD2	1.30	2.60	2.7 / 2.9	5	1	600	0	0	0.45×AVDD−1.3125
106	6A	14.5	26.0	−8.8	0.6×AVDD−1.3250	VDD1→VDD2	1.30	2.60	2.7 / 2.9	5	2	600	0	0	0.45×AVDD−1.3250
107	6B	14.5	26.0	−8.9	0.6×AVDD−1.3375	VDD1→VDD2	1.30	2.60	2.7 / 2.9	5	3	600	0	0	0.45×AVDD−1.3375
108	6C	14.5	26.0	−9.0	0.6×AVDD−1.3500	VDD1→VDD2	1.30	2.60	2.7 / 2.9	5	4	600	0	0	0.45×AVDD−1.3500
109	6D	14.5	26.0	−9.1	0.6×AVDD−1.3625	VDD1→VDD2	1.30	2.60	2.7 / 2.9	5	5	600	0	0	0.45×AVDD−1.3625
110	6E	14.5	26.0	−9.2	0.6×AVDD−1.3750	VDD1→VDD2	1.30	2.60	2.7 / 2.9	5	0	600	0	0	0.45×AVDD−1.3750
111	6F	14.5	26.0	−9.3	0.6×AVDD−1.3875	VDD1→VDD2	1.30	2.60	2.7 / 2.9	5	0	600	0	0	0.45×AVDD−1.3875
112	70	14.4	26.0	−9.4	0.6×AVDD−1.4000	VDD1→VDD2	1.30	1.70	2.7 / 2.9	0	0	600	0	0	0.45×AVDD−1.4000
113	71	14.3	26.0	−9.5	0.6×AVDD−1.4125	VDD1→VDD2	1.30	1.75	2.7 / 2.9	0	1	600	0	5	0.45×AVDD−1.4125
114	72	14.2	26.0	−9.5	0.6×AVDD−1.4250	VDD1→VDD2	1.30	1.80	2.7 / 2.9	0	2	600	0	10	0.45×AVDD−1.4250
115	73	14.1	26.0	−9.5	0.6×AVDD−1.4375	VDD1→VDD2	1.30	1.85	2.7 / 2.9	0	3	600	0	15	0.45×AVDD−1.4375
116	74	14.0	26.0	−9.5	0.6×AVDD−1.4500	VDD1→VDD2	1.30	1.90	2.7 / 2.9	0	4	600	0	20	0.45×AVDD−1.4500
117	75	13.9	26.0	−9.5	0.6×AVDD−1.4625	VDD1→VDD2	1.30	2.40	2.7 / 2.9	0	5	600	0	25	0.45×AVDD−1.4625
118	76	13.8	26.0	−9.5	0.6×AVDD−1.4750	VDD1→VDD2	1.30	2.45	2.7 / 2.9	0	0	600	0	30	0.45×AVDD−1.4750
119	77	13.7	26.0	−9.5	0.6×AVDD−1.4875	VDD1→VDD2	1.30	2.50	2.7 / 2.9	0	0	600	0	35	0.45×AVDD−1.4875
120	78	13.6	26.0	−9.5	0.6×AVDD−1.5000	VDD1→VDD2	1.30	2.55	2.7 / 2.9	0	0	600	0	40	0.45×AVDD−1.5000
121	79	13.5	26.0	−9.5	0.6×AVDD−1.5125	VDD1→VDD2	1.30	2.60	2.7 / 2.9	0	1	600	0	0	0.45×AVDD−1.5125
122	7A	13.4	26.0	−9.5	0.6×AVDD−1.5250	VDD1→VDD2	1.30	2.60	2.7 / 2.9	0	2	600	0	0	0.45×AVDD−1.5250
123	7B	13.3	26.0	−9.5	0.6×AVDD−1.5375	VDD1→VDD2	1.30	2.60	2.7 / 2.9	0	3	600	0	0	0.45×AVDD−1.5375
124	7C	13.2	26.0	−9.5	0.6×AVDD−1.5500	VDD1→VDD2	1.30	2.60	2.7 / 2.9	0	4	600	0	0	0.45×AVDD−1.5500
125	7D	13.1	26.0	−9.5	0.6×AVDD−1.5625	VDD1→VDD2	1.30	2.60	2.7 / 2.9	0	5	600	0	0	0.45×AVDD−1.5625
126	7E	13.0	26.0	−9.5	0.6×AVDD−1.5750	VDD1→VDD2	1.30	2.60	2.7 / 2.9	0	0	600	0	0	0.45×AVDD−1.5750
127	7F	12.9	25.8	−9.5	0.6×AVDD−1.5875	VDD1→VDD2	1.30	2.60	2.7 / 2.9	0	0	600	0	0	0.45×AVDD−1.5875

●Command Table 3

		Register													
DATA		01h	02h	03h	04h	05h			06h			07h			09h
		AVDD Voltage Setting	VGH Voltage Setting	VGL Voltage Setting	HAVDD Voltage Setting	VDD ON Sequence	VDD2 Voltage Setting	VDD1 Voltage Setting	DC/DC UVLO Detect/Release Voltage	DELAY1 Time Setting	Discharge Time Setting	Frequency Setting	DELAY3 Time Setting	DELAY2 Time Setting	VCOM Voltage Setting
DEC.	HEX.	[V]	[V]	[V]	[V]		[V]	[V]	[V]	[msec]	[msec]	[kHz]	[msec]	[msec]	[V]
128	80	12.8	25.6	−9.5	0.6×AVDD−1.6000	VDD2→VDD1	1.10	1.70	2.9 / 3.1	0	0	1200	0	0	0.45×AVDD−1.6000
129	81	12.7	25.4	−9.5	0.6×AVDD−1.6125	VDD2→VDD1	1.10	1.75	2.9 / 3.1	0	1	1200	0	5	0.45×AVDD−1.6125
130	82	12.6	25.2	−9.5	0.6×AVDD−1.6250	VDD2→VDD1	1.10	1.80	2.9 / 3.1	0	2	1200	0	10	0.45×AVDD−1.6250
131	83	12.5	25.0	−9.5	0.6×AVDD−1.6375	VDD2→VDD1	1.10	1.85	2.9 / 3.1	0	3	1200	0	15	0.45×AVDD−1.6375
132	84	12.4	24.8	−9.5	0.6×AVDD−1.6500	VDD2→VDD1	1.10	1.90	2.9 / 3.1	0	4	1200	0	20	0.45×AVDD−1.6500
133	85	12.3	24.6	−9.5	0.6×AVDD−1.6625	VDD2→VDD1	1.10	2.40	2.9 / 3.1	0	5	1200	0	25	0.45×AVDD−1.6625
134	86	12.2	24.4	−9.5	0.6×AVDD−1.6750	VDD2→VDD1	1.10	2.45	2.9 / 3.1	0	0	1200	0	30	0.45×AVDD−1.6750
135	87	12.1	24.2	−9.5	0.6×AVDD−1.6875	VDD2→VDD1	1.10	2.50	2.9 / 3.1	0	0	1200	0	35	0.45×AVDD−1.6875
136	88	12.0	24.0	−9.5	0.6×AVDD−1.7000	VDD2→VDD1	1.10	2.55	2.9 / 3.1	1	0	1200	0	40	0.45×AVDD−1.7000
137	89	11.9	23.8	−9.5	0.6×AVDD−1.7125	VDD2→VDD1	1.10	2.60	2.9 / 3.1	1	1	1200	0	0	0.45×AVDD−1.7125
138	8A	11.8	23.6	−9.5	0.6×AVDD−1.7250	VDD2→VDD1	1.10	2.60	2.9 / 3.1	1	2	1200	0	0	0.45×AVDD−1.7250
139	8B	11.7	23.4	−9.5	0.6×AVDD−1.7375	VDD2→VDD1	1.10	2.60	2.9 / 3.1	1	3	1200	0	0	0.45×AVDD−1.7375
140	8C	11.6	23.2	−9.5	0.6×AVDD−1.7500	VDD2→VDD1	1.10	2.60	2.9 / 3.1	1	4	1200	0	0	0.45×AVDD−1.7500
141	8D	11.5	23.0	−9.5	0.6×AVDD−1.7625	VDD2→VDD1	1.10	2.60	2.9 / 3.1	1	5	1200	0	0	0.45×AVDD−1.7625
142	8E	11.4	22.8	−9.5	0.6×AVDD−1.7750	VDD2→VDD1	1.10	2.60	2.9 / 3.1	1	0	1200	0	0	0.45×AVDD−1.7750
143	8F	11.3	22.6	−9.5	0.6×AVDD−1.7875	VDD2→VDD1	1.10	2.60	2.9 / 3.1	1	0	1200	0	0	0.45×AVDD−1.7875
144	90	11.2	22.4	−9.5	0.6×AVDD−1.8000	VDD2→VDD1	1.15	1.70	2.9 / 3.1	2	0	1200	2	0	0.45×AVDD−1.8000
145	91	11.1	22.2	−9.5	0.6×AVDD−1.8125	VDD2→VDD1	1.15	1.75	2.9 / 3.1	2	1	1200	2	5	0.45×AVDD−1.8125
146	92	11.0	22.0	−9.5	0.6×AVDD−1.8250	VDD2→VDD1	1.15	1.80	2.9 / 3.1	2	2	1200	2	10	0.45×AVDD−1.8250
147	93	10.9	21.8	−9.5	0.6×AVDD−1.8375	VDD2→VDD1	1.15	1.85	2.9 / 3.1	2	3	1200	2	15	0.45×AVDD−1.8375
148	94	10.8	21.6	−9.5	0.6×AVDD−1.8500	VDD2→VDD1	1.15	1.90	2.9 / 3.1	2	4	1200	2	20	0.45×AVDD−1.8500
149	95	10.7	21.4	−9.5	0.6×AVDD−1.8625	VDD2→VDD1	1.15	2.40	2.9 / 3.1	2	5	1200	2	25	0.45×AVDD−1.8625
150	96	10.6	21.2	−9.5	0.6×AVDD−1.8750	VDD2→VDD1	1.15	2.45	2.9 / 3.1	2	0	1200	2	30	0.45×AVDD−1.8750
151	97	10.5	21.0	−9.5	0.6×AVDD−1.8875	VDD2→VDD1	1.15	2.50	2.9 / 3.1	2	0	1200	2	35	0.45×AVDD−1.8875
152	98	10.4	20.8	−9.5	0.6×AVDD−1.9000	VDD2→VDD1	1.15	2.55	2.9 / 3.1	3	0	1200	2	40	0.45×AVDD−1.9000
153	99	10.3	20.6	−9.5	0.6×AVDD−1.9125	VDD2→VDD1	1.15	2.60	2.9 / 3.1	3	1	1200	2	0	0.45×AVDD−1.9125
154	9A	10.2	20.4	−9.5	0.6×AVDD−1.9250	VDD2→VDD1	1.15	2.60	2.9 / 3.1	3	2	1200	2	0	0.45×AVDD−1.9250
155	9B	10.1	20.2	−9.5	0.6×AVDD−1.9375	VDD2→VDD1	1.15	2.60	2.9 / 3.1	3	3	1200	2	0	0.45×AVDD−1.9375
156	9C	10.0	20.0	−9.5	0.6×AVDD−1.9500	VDD2→VDD1	1.15	2.60	2.9 / 3.1	3	4	1200	2	0	0.45×AVDD−1.9500
157	9D	9.9	19.8	−9.5	0.6×AVDD−1.9625	VDD2→VDD1	1.15	2.60	2.9 / 3.1	3	5	1200	2	0	0.45×AVDD−1.9625
158	9E	9.8	19.6	−9.5	0.6×AVDD−1.9750	VDD2→VDD1	1.15	2.60	2.9 / 3.1	3	0	1200	2	0	0.45×AVDD−1.9750
159	9F	9.7	19.4	−9.5	0.6×AVDD−1.9875	VDD2→VDD1	1.15	2.60	2.9 / 3.1	3	0	1200	2	0	0.45×AVDD−1.9875
160	A0	9.6	19.2	−9.5	0.6×AVDD−2.0000	VDD2→VDD1	1.20	1.70	2.9 / 3.1	4	0	1200	4	0	0.45×AVDD−2.0000
161	A1	9.5	19.0	−9.5	0.6×AVDD−2.0125	VDD2→VDD1	1.20	1.75	2.9 / 3.1	4	1	1200	4	5	0.45×AVDD−2.0125
162	A2	9.4	18.8	−9.5	0.6×AVDD−2.0250	VDD2→VDD1	1.20	1.80	2.9 / 3.1	4	2	1200	4	10	0.45×AVDD−2.0250
163	A3	9.3	18.6	−9.5	0.6×AVDD−2.0375	VDD2→VDD1	1.20	1.85	2.9 / 3.1	4	3	1200	4	15	0.45×AVDD−2.0375
164	A4	9.2	18.4	−9.5	0.6×AVDD−2.0500	VDD2→VDD1	1.20	1.90	2.9 / 3.1	4	4	1200	4	20	0.45×AVDD−2.0500
165	A5	9.1	18.2	−9.5	0.6×AVDD−2.0625	VDD2→VDD1	1.20	2.40	2.9 / 3.1	4	5	1200	4	25	0.45×AVDD−2.0625
166	A6	9.0	18.0	−9.5	0.6×AVDD−2.0750	VDD2→VDD1	1.20	2.45	2.9 / 3.1	4	0	1200	4	30	0.45×AVDD−2.0750
167	A7	8.9	17.8	−9.5	0.6×AVDD−2.0875	VDD2→VDD1	1.20	2.50	2.9 / 3.1	4	0	1200	4	35	0.45×AVDD−2.0875
168	A8	8.8	17.6	−9.5	0.6×AVDD−2.1000	VDD2→VDD1	1.20	2.55	2.9 / 3.1	5	0	1200	4	40	0.45×AVDD−2.1000
169	A9	8.7	17.4	−9.5	0.6×AVDD−2.1125	VDD2→VDD1	1.20	2.60	2.9 / 3.1	5	1	1200	4	0	0.45×AVDD−2.1125
170	AA	8.6	17.2	−9.5	0.6×AVDD−2.1250	VDD2→VDD1	1.20	2.60	2.9 / 3.1	5	2	1200	4	0	0.45×AVDD−2.1250
171	AB	8.5	17.0	−9.5	0.6×AVDD−2.1375	VDD2→VDD1	1.20	2.60	2.9 / 3.1	5	3	1200	4	0	0.45×AVDD−2.1375
172	AC	8.4	16.8	−9.5	0.6×AVDD−2.1500	VDD2→VDD1	1.20	2.60	2.9 / 3.1	5	4	1200	4	0	0.45×AVDD−2.1500
173	AD	8.3	16.6	−9.5	0.6×AVDD−2.1625	VDD2→VDD1	1.20	2.60	2.9 / 3.1	5	5	1200	4	0	0.45×AVDD−2.1625
174	AE	8.2	16.4	−9.5	0.6×AVDD−2.1750	VDD2→VDD1	1.20	2.60	2.9 / 3.1	5	0	1200	4	0	0.45×AVDD−2.1750
175	AF	8.1	16.2	−9.5	0.6×AVDD−2.1875	VDD2→VDD1	1.20	2.60	2.9 / 3.1	5	0	1200	4	0	0.45×AVDD−2.1875
176	B0	8.0	16.0	−9.5	0.6×AVDD−2.2000	VDD2→VDD1	1.25	1.70	2.9 / 3.1	0	0	1200	6	0	0.45×AVDD−2.2000
177	B1	8.0	15.8	−9.5	0.6×AVDD−2.2125	VDD2→VDD1	1.25	1.75	2.9 / 3.1	0	1	1200	6	5	0.45×AVDD−2.2125
178	B2	8.0	15.6	−9.5	0.6×AVDD−2.2250	VDD2→VDD1	1.25	1.80	2.9 / 3.1	0	2	1200	6	10	0.45×AVDD−2.2250
179	B3	8.0	15.4	−9.5	0.6×AVDD−2.2375	VDD2→VDD1	1.25	1.85	2.9 / 3.1	0	3	1200	6	15	0.45×AVDD−2.2375
180	B4	8.0	15.2	−9.5	0.6×AVDD−2.2500	VDD2→VDD1	1.25	1.90	2.9 / 3.1	0	4	1200	6	20	0.45×AVDD−2.2500
181	B5	8.0	15.0	−9.5	0.6×AVDD−2.2625	VDD2→VDD1	1.25	2.40	2.9 / 3.1	0	5	1200	6	25	0.45×AVDD−2.2625
182	B6	8.0	14.8	−9.5	0.6×AVDD−2.2750	VDD2→VDD1	1.25	2.45	2.9 / 3.1	0	0	1200	6	30	0.45×AVDD−2.2750
183	B7	8.0	14.6	−9.5	0.6×AVDD−2.2875	VDD2→VDD1	1.25	2.50	2.9 / 3.1	0	0	1200	6	35	0.45×AVDD−2.2875
184	B8	8.0	14.4	−9.5	0.6×AVDD−2.3000	VDD2→VDD1	1.25	2.55	2.9 / 3.1	0	0	1200	6	40	0.45×AVDD−2.3000
185	B9	8.0	14.2	−9.5	0.6×AVDD−2.3125	VDD2→VDD1	1.25	2.60	2.9 / 3.1	0	1	1200	6	0	0.45×AVDD−2.3125
186	BA	8.0	14.0	−9.5	0.6×AVDD−2.3250	VDD2→VDD1	1.25	2.60	2.9 / 3.1	0	2	1200	6	0	0.45×AVDD−2.3250
187	BB	8.0	13.8	−9.5	0.6×AVDD−2.3375	VDD2→VDD1	1.25	2.60	2.9 / 3.1	0	3	1200	6	0	0.45×AVDD−2.3375
188	BC	8.0	13.6	−9.5	0.6×AVDD−2.3500	VDD2→VDD1	1.25	2.60	2.9 / 3.1	0	4	1200	6	0	0.45×AVDD−2.3500
189	BD	8.0	13.4	−9.5	0.6×AVDD−2.3625	VDD2→VDD1	1.25	2.60	2.9 / 3.1	0	5	1200	6	0	0.45×AVDD−2.3625
190	BE	8.0	13.2	−9.5	0.6×AVDD−2.3750	VDD2→VDD1	1.25	2.60	2.9 / 3.1	0	0	1200	6	0	0.45×AVDD−2.3750
191	BF	8.0	13.0	−9.5	0.6×AVDD−2.3875	VDD2→VDD1	1.25	2.60	2.9 / 3.1	0	0	1200	6	0	0.45×AVDD−2.3875

●Command Table 4

		Register													
DATA		01h	02h	03h	04h	05h			06h			07h			09h
		AVDD Voltage Setting	VGH Voltage Setting	VGL Voltage Setting	HAVDD Voltage Setting	VDD ON Sequence	VDD2 Voltage Setting	VDD1 Voltage Setting	DC/DC UVLO Detect/Release Voltage	DELAY1 Time Setting	Discharge Time Setting	Frequency Setting	DELAY3 Time Setting	DELAY2 Time Setting	VCOM Voltage Setting
DEC.	HEX.	[V]	[V]	[V]	[V]		[V]	[V]	[V]	[msec]	[msec]	[kHz]	[msec]	[msec]	[V]
192	C0	8.0	13.0	−9.5	0.6×AVDD−2.4000	VDD2→VDD1	1.30	1.70	3.1 / 3.3	0	0	1200	8	0	0.45×AVDD−2.4000
193	C1	8.0	13.0	−9.5	0.6×AVDD−2.4125	VDD2→VDD1	1.30	1.75	3.1 / 3.3	0	1	1200	8	5	0.45×AVDD−2.4125
194	C2	8.0	13.0	−9.5	0.6×AVDD−2.4250	VDD2→VDD1	1.30	1.80	3.1 / 3.3	0	2	1200	8	10	0.45×AVDD−2.4250
195	C3	8.0	13.0	−9.5	0.6×AVDD−2.4375	VDD2→VDD1	1.30	1.85	3.1 / 3.3	0	3	1200	8	15	0.45×AVDD−2.4375
196	C4	8.0	13.0	−9.5	0.6×AVDD−2.4500	VDD2→VDD1	1.30	1.90	3.1 / 3.3	0	4	1200	8	20	0.45×AVDD−2.4500
197	C5	8.0	13.0	−9.5	0.6×AVDD−2.4625	VDD2→VDD1	1.30	2.40	3.1 / 3.3	0	5	1200	8	25	0.45×AVDD−2.4625
198	C6	8.0	13.0	−9.5	0.6×AVDD−2.4750	VDD2→VDD1	1.30	2.45	3.1 / 3.3	0	0	1200	8	30	0.45×AVDD−2.4750
199	C7	8.0	13.0	−9.5	0.6×AVDD−2.4875	VDD2→VDD1	1.30	2.50	3.1 / 3.3	0	0	1200	8	35	0.45×AVDD−2.4875
200	C8	8.0	13.0	−9.5	0.6×AVDD−2.5000	VDD2→VDD1	1.30	2.55	3.1 / 3.3	1	0	1200	8	40	0.45×AVDD−2.5000
201	C9	8.0	13.0	−9.5	0.6×AVDD−2.5125	VDD2→VDD1	1.30	2.60	3.1 / 3.3	1	1	1200	8	0	0.45×AVDD−2.5125
202	CA	8.0	13.0	−9.5	0.6×AVDD−2.5250	VDD2→VDD1	1.30	2.60	3.1 / 3.3	1	2	1200	8	0	0.45×AVDD−2.5250
203	CB	8.0	13.0	−9.5	0.6×AVDD−2.5375	VDD2→VDD1	1.30	2.60	3.1 / 3.3	1	3	1200	8	0	0.45×AVDD−2.5375
204	CC	8.0	13.0	−9.5	0.6×AVDD−2.5500	VDD2→VDD1	1.30	2.60	3.1 / 3.3	1	4	1200	8	0	0.45×AVDD−2.5500
205	CD	8.0	13.0	−9.5	0.6×AVDD−2.5625	VDD2→VDD1	1.30	2.60	3.1 / 3.3	1	5	1200	8	0	0.45×AVDD−2.5625
206	CE	8.0	13.0	−9.5	0.6×AVDD−2.5750	VDD2→VDD1	1.30	2.60	3.1 / 3.3	1	0	1200	8	0	0.45×AVDD−2.5750
207	CF	8.0	13.0	−9.5	0.6×AVDD−2.5875	VDD2→VDD1	1.30	2.60	3.1 / 3.3	1	0	1200	8	0	0.45×AVDD−2.5875
208	D0	8.0	13.0	−9.5	0.6×AVDD−2.6000	VDD2→VDD1	1.30	1.70	3.1 / 3.3	2	0	1200	10	0	0.45×AVDD−2.6000
209	D1	8.0	13.0	−9.5	0.6×AVDD−2.6125	VDD2→VDD1	1.30	1.75	3.1 / 3.3	2	1	1200	10	5	0.45×AVDD−2.6125
210	D2	8.0	13.0	−9.5	0.6×AVDD−2.6250	VDD2→VDD1	1.30	1.80	3.1 / 3.3	2	2	1200	10	10	0.45×AVDD−2.6250
211	D3	8.0	13.0	−9.5	0.6×AVDD−2.6375	VDD2→VDD1	1.30	1.85	3.1 / 3.3	2	3	1200	10	15	0.45×AVDD−2.6375
212	D4	8.0	13.0	−9.5	0.6×AVDD−2.6500	VDD2→VDD1	1.30	1.90	3.1 / 3.3	2	4	1200	10	20	0.45×AVDD−2.6500
213	D5	8.0	13.0	−9.5	0.6×AVDD−2.6625	VDD2→VDD1	1.30	2.40	3.1 / 3.3	2	5	1200	10	25	0.45×AVDD−2.6625
214	D6	8.0	13.0	−9.5	0.6×AVDD−2.6750	VDD2→VDD1	1.30	2.45	3.1 / 3.3	2	0	1200	10	30	0.45×AVDD−2.6750
215	D7	8.0	13.0	−9.5	0.6×AVDD−2.6875	VDD2→VDD1	1.30	2.50	3.1 / 3.3	2	0	1200	10	35	0.45×AVDD−2.6875
216	D8	8.0	13.0	−9.5	0.6×AVDD−2.7000	VDD2→VDD1	1.30	2.55	3.1 / 3.3	3	0	1200	10	40	0.45×AVDD−2.7000
217	D9	8.0	13.0	−9.5	0.6×AVDD−2.7125	VDD2→VDD1	1.30	2.60	3.1 / 3.3	3	1	1200	10	0	0.45×AVDD−2.7125
218	DA	8.0	13.0	−9.5	0.6×AVDD−2.7250	VDD2→VDD1	1.30	2.60	3.1 / 3.3	3	2	1200	10	0	0.45×AVDD−2.7250
219	DB	8.0	13.0	−9.5	0.6×AVDD−2.7375	VDD2→VDD1	1.30	2.60	3.1 / 3.3	3	3	1200	10	0	0.45×AVDD−2.7375
220	DC	8.0	13.0	−9.5	0.6×AVDD−2.7500	VDD2→VDD1	1.30	2.60	3.1 / 3.3	3	4	1200	10	0	0.45×AVDD−2.7500
221	DD	8.0	13.0	−9.5	0.6×AVDD−2.7625	VDD2→VDD1	1.30	2.60	3.1 / 3.3	3	5	1200	10	0	0.45×AVDD−2.7625
222	DE	8.0	13.0	−9.5	0.6×AVDD−2.7750	VDD2→VDD1	1.30	2.60	3.1 / 3.3	3	0	1200	10	0	0.45×AVDD−2.7750
223	DF	8.0	13.0	−9.5	0.6×AVDD−2.7875	VDD2→VDD1	1.30	2.60	3.1 / 3.3	3	0	1200	10	0	0.45×AVDD−2.7875
224	E0	8.0	13.0	−9.5	0.6×AVDD−2.8000	VDD2→VDD1	1.30	1.70	3.1 / 3.3	4	0	1200	0	0	0.45×AVDD−2.8000
225	E1	8.0	13.0	−9.5	0.6×AVDD−2.8125	VDD2→VDD1	1.30	1.75	3.1 / 3.3	4	1	1200	0	5	0.45×AVDD−2.8125
226	E2	8.0	13.0	−9.5	0.6×AVDD−2.8250	VDD2→VDD1	1.30	1.80	3.1 / 3.3	4	2	1200	0	10	0.45×AVDD−2.8250
227	E3	8.0	13.0	−9.5	0.6×AVDD−2.8375	VDD2→VDD1	1.30	1.85	3.1 / 3.3	4	3	1200	0	15	0.45×AVDD−2.8375
228	E4	8.0	13.0	−9.5	0.6×AVDD−2.8500	VDD2→VDD1	1.30	1.90	3.1 / 3.3	4	4	1200	0	20	0.45×AVDD−2.8500
229	E5	8.0	13.0	−9.5	0.6×AVDD−2.8625	VDD2→VDD1	1.30	2.40	3.1 / 3.3	4	5	1200	0	25	0.45×AVDD−2.8625
230	E6	8.0	13.0	−9.5	0.6×AVDD−2.8750	VDD2→VDD1	1.30	2.45	3.1 / 3.3	4	0	1200	0	30	0.45×AVDD−2.8750
231	E7	8.0	13.0	−9.5	0.6×AVDD−2.8875	VDD2→VDD1	1.30	2.50	3.1 / 3.3	4	0	1200	0	35	0.45×AVDD−2.8875
232	E8	8.0	13.0	−9.5	0.6×AVDD−2.9000	VDD2→VDD1	1.30	2.55	3.1 / 3.3	5	0	1200	0	40	0.45×AVDD−2.9000
233	E9	8.0	13.0	−9.5	0.6×AVDD−2.9125	VDD2→VDD1	1.30	2.60	3.1 / 3.3	5	1	1200	0	0	0.45×AVDD−2.9125
234	EA	8.0	13.0	−9.5	0.6×AVDD−2.9250	VDD2→VDD1	1.30	2.60	3.1 / 3.3	5	2	1200	0	0	0.45×AVDD−2.9250
235	EB	8.0	13.0	−9.5	0.6×AVDD−2.9375	VDD2→VDD1	1.30	2.60	3.1 / 3.3	5	3	1200	0	0	0.45×AVDD−2.9375
236	EC	8.0	13.0	−9.5	0.6×AVDD−2.9500	VDD2→VDD1	1.30	2.60	3.1 / 3.3	5	4	1200	0	0	0.45×AVDD−2.9500
237	ED	8.0	13.0	−9.5	0.6×AVDD−2.9625	VDD2→VDD1	1.30	2.60	3.1 / 3.3	5	5	1200	0	0	0.45×AVDD−2.9625
238	EE	8.0	13.0	−9.5	0.6×AVDD−2.9750	VDD2→VDD1	1.30	2.60	3.1 / 3.3	5	0	1200	0	0	0.45×AVDD−2.9750
239	EF	8.0	13.0	−9.5	0.6×AVDD−2.9875	VDD2→VDD1	1.30	2.60	3.1 / 3.3	5	0	1200	0	0	0.45×AVDD−2.9875
240	F0	8.0	13.0	−9.5	0.6×AVDD−3.0000	VDD2→VDD1	1.30	1.70	3.1 / 3.3	0	0	1200	0	0	0.45×AVDD−3.0000
241	F1	8.0	13.0	−9.5	0.6×AVDD−3.0125	VDD2→VDD1	1.30	1.75	3.1 / 3.3	0	1	1200	0	5	0.45×AVDD−3.0125
242	F2	8.0	13.0	−9.5	0.6×AVDD−3.0250	VDD2→VDD1	1.30	1.80	3.1 / 3.3	0	2	1200	0	10	0.45×AVDD−3.0250
243	F3	8.0	13.0	−9.5	0.6×AVDD−3.0375	VDD2→VDD1	1.30	1.85	3.1 / 3.3	0	3	1200	0	15	0.45×AVDD−3.0375
244	F4	8.0	13.0	−9.5	0.6×AVDD−3.0500	VDD2→VDD1	1.30	1.90	3.1 / 3.3	0	4	1200	0	20	0.45×AVDD−3.0500
245	F5	8.0	13.0	−9.5	0.6×AVDD−3.0625	VDD2→VDD1	1.30	2.40	3.1 / 3.3	0	5	1200	0	25	0.45×AVDD−3.0625
246	F6	8.0	13.0	−9.5	0.6×AVDD−3.0750	VDD2→VDD1	1.30	2.45	3.1 / 3.3	0	0	1200	0	30	0.45×AVDD−3.0750
247	F7	8.0	13.0	−9.5	0.6×AVDD−3.0875	VDD2→VDD1	1.30	2.50	3.1 / 3.3	0	0	1200	0	35	0.45×AVDD−3.0875
248	F8	8.0	13.0	−9.5	0.6×AVDD−3.1000	VDD2→VDD1	1.30	2.55	3.1 / 3.3	0	0	1200	0	40	0.45×AVDD−3.1000
249	F9	8.0	13.0	−9.5	0.6×AVDD−3.1125	VDD2→VDD1	1.30	2.60	3.1 / 3.3	0	1	1200	0	0	0.45×AVDD−3.1125
250	FA	8.0	13.0	−9.5	0.6×AVDD−3.1250	VDD2→VDD1	1.30	2.60	3.1 / 3.3	0	2	1200	0	0	0.45×AVDD−3.1250
251	FB	8.0	13.0	−9.5	0.6×AVDD−3.1375	VDD2→VDD1	1.30	2.60	3.1 / 3.3	0	3	1200	0	0	0.45×AVDD−3.1375
252	FC	8.0	13.0	−9.5	0.6×AVDD−3.1500	VDD2→VDD1	1.30	2.60	3.1 / 3.3	0	4	1200	0	0	0.45×AVDD−3.1500
253	FD	8.0	13.0	−9.5	0.6×AVDD−3.1625	VDD2→VDD1	1.30	2.60	3.1 / 3.3	0	5	1200	0	0	0.45×AVDD−3.1625
254	FE	8.0	13.0	−9.5	0.6×AVDD−3.1750	VDD2→VDD1	1.30	2.60	3.1 / 3.3	0	0	1200	0	0	0.45×AVDD−3.1750
255	FF	8.0	13.0	−9.5	0.6×AVDD−3.1875	VDD2→VDD1	1.30	2.60	3.1 / 3.3	0	0	1200	0	0	0.45×AVDD−3.1875

●Protection functions

・Over-Voltage Protection

	AVDD
Threshold (Typ)	16V
Operation	When OVP is detected, switching turns OFF to control the rising output voltage. When the output voltage decreases to a lower value, the switching will turn back ON.

・Short Circuit Protection

	VDD1	VDD2	AVDD	VGH	VGL
Threshold (Typ)	VDD1×0.8	VDD2×0.8	AVDD×0.8	VGH×0.8	VGL×0.8
Operation	When a channel detects SCP, a timer is activated. 10msec after that, all channels will be latched to shutdown state. To return to normal operation, reset the power supply.				

・Over-Current Protect

	VDD1	VDD2	AVDD
Threshold (Min)	1.0A	1.0A	1.5A
Operation	When OCP is detected, switching turns OFF to limit the FET from generating current. When the FET current decreases to a lower value, the switching will turn back ON.		

・Thermal Shutdown

	VDD1	VDD2	AVDD	HAVDD	VCOM	VGH	VGL
Threshold (Typ)	175℃						
Operation	When device temperature goes above 175℃ (Typ), all channels are shut down.						

・VCC UVLO

	VDD1	VDD2	AVDD	HAVDD	VCOM	VGH	VGL
Falling (Typ)	2.4V						
Rising (Typ)	2.1V						
Operation	Circuit malfunction is prevented by making sure the IC is turned off when VCC is below the UVLO threshold. There is a hysteresis between the rising and falling threshold to avoid triggering UVLO by power supply noise.						

・DC/DC converter UVLO

	VDD1	VDD2	AVDD	HAVDD	VCOM	VGH	VGL
Falling (Typ)	2.5 / 2.7 / 2.9 / 3.1V						
Rising (Typ)	2.7 / 2.9 / 3.1 / 3.3 V						
Watch start (Typ)	2.8 / 3.0 / 3.2 / 3.4 V						
Operation	DC/DC converter output error is prevented by making sure all channels are turned off when a DC/DC converter output is below the UVLO threshold.						

●FAULT Output

The FAULT output indicates the status of the protection circuits of this IC.
Because FAULT is an open-drain output, place a pull-up resistor externally.
When the FAULT output will not be used, connect to GND.

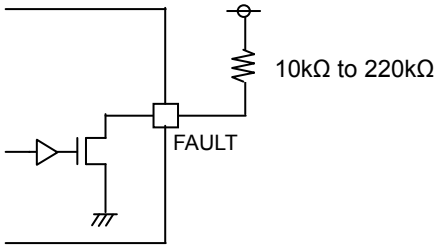


Fig. 55 FAULT Output

FAULT=H

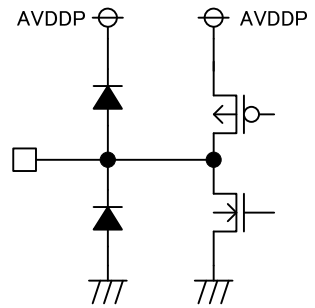
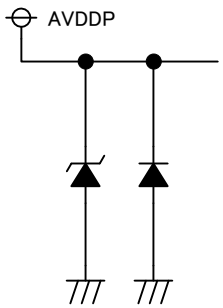
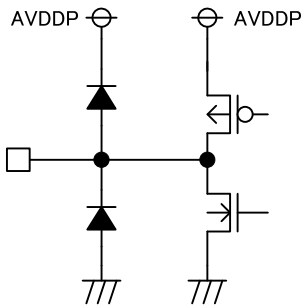
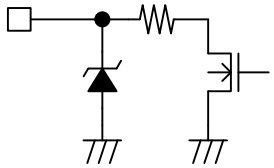
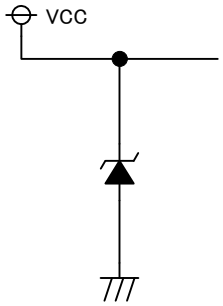
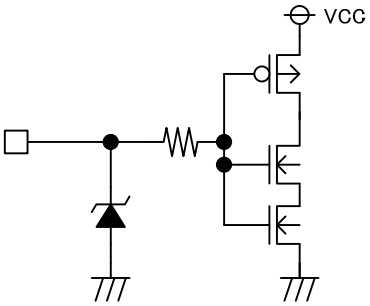
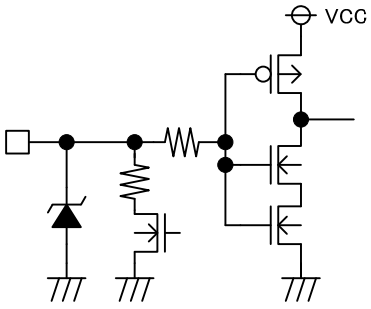
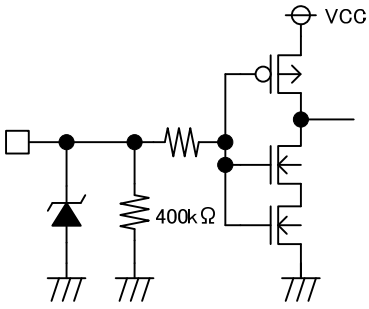
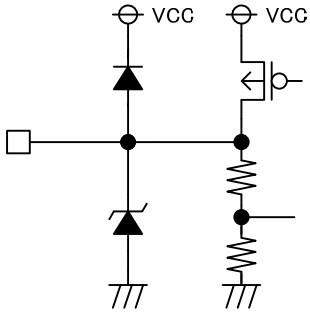
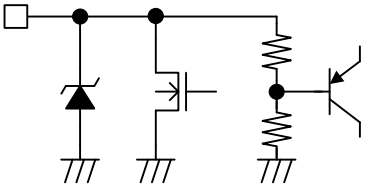
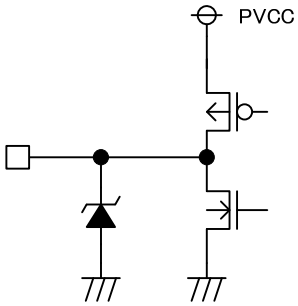
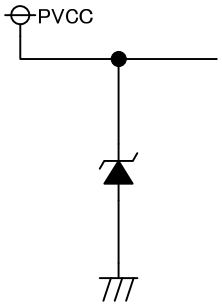
During stable operation when none of the protection circuits are in effect.
This is due to the external pull-up resistance.

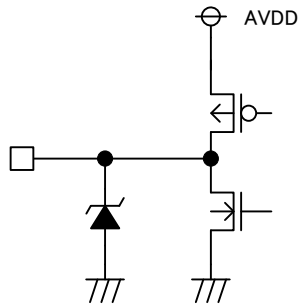
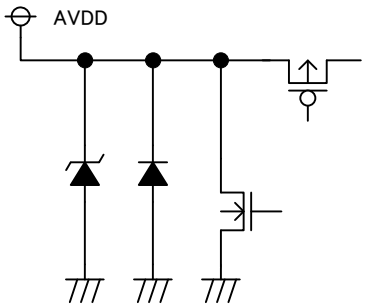
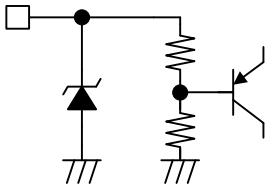
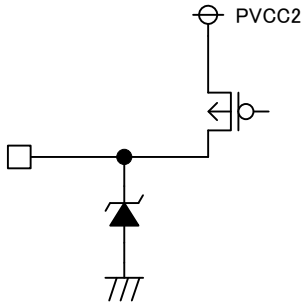
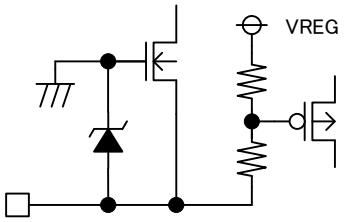
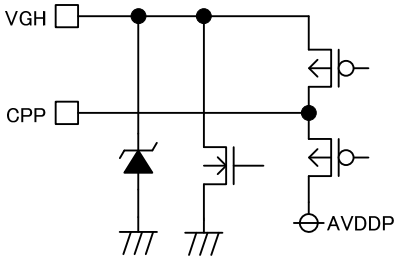
FAULT=L

When any of the protection circuits (UVLO, OCP, OVP, TSD, and SCP) are triggered.
This indicates a circuit error.

The recommended external pull-up resistance for the FAULT output is 10kΩ to 220kΩ. An external resistance of under 10kΩ can generate an offset voltage during FAULT=L caused by the voltage drop across the internal on resistance. On the other hand, an external resistance of more than 220kΩ can interfere with the output during FAULT=H because of leak current.

●I/O Equivalent Circuits

1.DRN, 28. DRP	2.AVDDP	3.HAVDD, 4.VCOM
		
6.FAULT	7.VCC	8.SCL
		
9.SDA	10.EN	11.VREG
		
12.VDD2, 13.VDD1	15.SWB1, 17.SWB2	16.PVCC1, 22.PVCC2
		

19.SW	20.AVDD	21.AVDD_S
		
23.VLSO	24.VGL	26.VGH, 27CPP
		

● Operational Notes

1) Absolute maximum ratings
Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

2) Ground potential
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

3) Thermal consideration
Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.

4) Short between pins and mounting errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

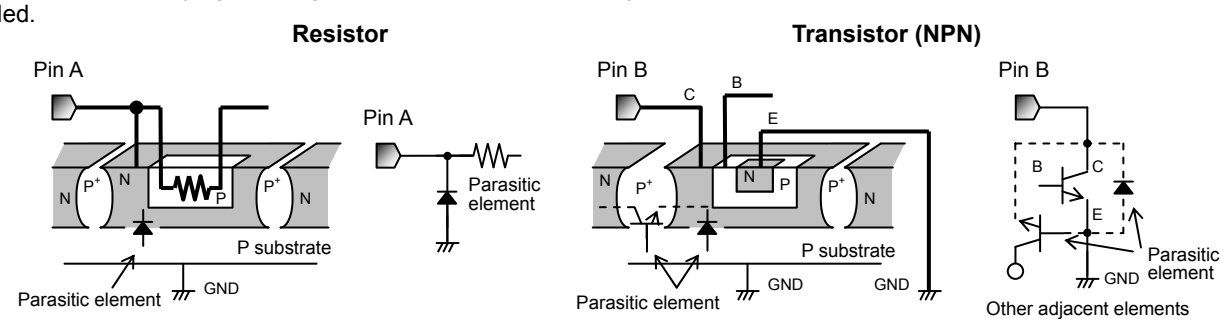
5) Operation under strong electromagnetic field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

7) Regarding input pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of a Simple Monolithic IC Structure

8) Over-current protection circuit (OCP)
The IC incorporates an over-current protection circuit that operates in accordance with the rated output capacity. This circuit protects the IC from damage when the load becomes shorted. It is also designed to limit the output current (without latching) in the event of a large transient current flow, such as from a large capacitor or other component connected to the output pin. This protection circuit is effective in preventing damage to the IC in cases of sudden and unexpected current surges. The IC should not be used in applications where the over current protection circuit will be activated continuously.

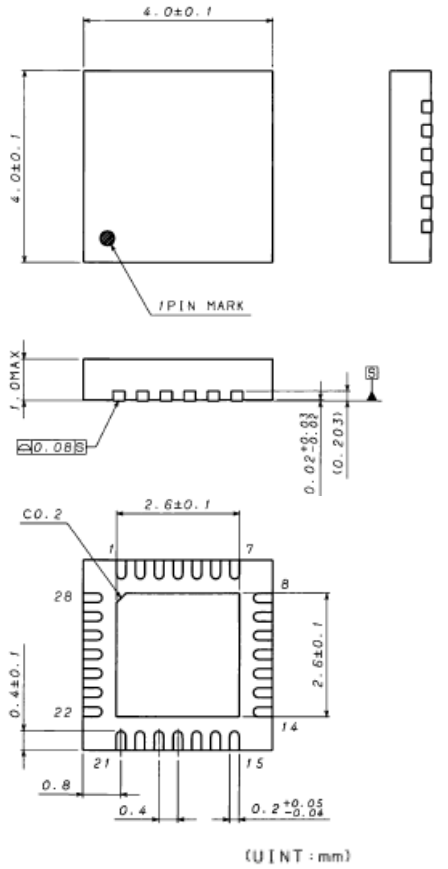
9) Thermal shutdown circuit (TSD)
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

10) DC/DC switching line wiring pattern
DC/DC converter switching line (wiring from the switching pin to inductor, Nch MOS) must be as short and thick as possible to reduce line impedance. If the wiring is long, ringing caused by switching would increase and this may exceed the absolute maximum voltage ratings. If the parts are located far apart, consider inserting a snubber circuit.

●Ordering Information

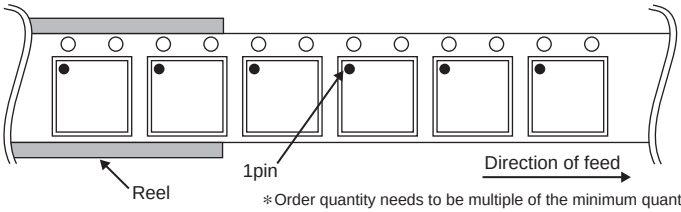
B M 8 1 0 2 8 A M W V	ZE2
Part Number	Package MWV: UQFN28V4040A
	Packaging and forming specification ZE2: Embossed tape and reel

●Physical Dimension Tape and Reel Information



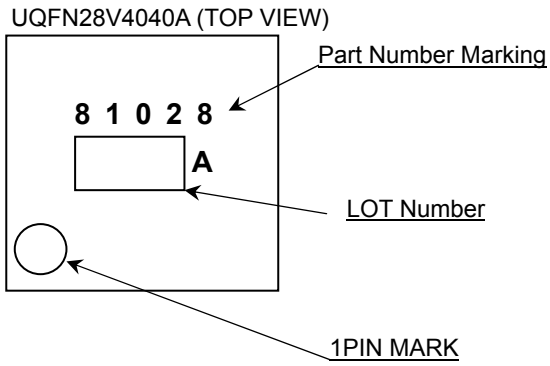
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	**ZE2** (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram (TOP VIEW)



●MODIFICATION RECORD

Rev.001	-	Original
Rev.002	P.1	Change input voltage range, Add Input tolerant
	P.5	Change Recommended Operating Ratings (Power Supply Voltage, SWB1,SWB2 Current, SW Current)
Rev.003	P.1, P.43	Change package name
	P.26	Clerical error correction (D1)

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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