



**THE DATASHEET OF  
BLC10G18XS-301AVTZ**



# BLC10G18XS-301AVT

Power LDMOS transistor

Rev. 1 — 23 May 2019

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

300 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1805 MHz to 1880 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty demo circuit.  $V_{DS} = 30\text{ V}$ ;  $I_{DQ} = 300\text{ mA}$  (main);  $V_{GS(amp)peak} = 1.15\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1805 to 1880	30	47	16	52	-30 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1880 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G18XS-301AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+9	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C
$T_{case}$	case temperature	operating <a href="#">[1]</a>	-40	+150	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 30\text{ V}; I_{Dq} = 300\text{ mA (main)};$ $V_{GS(amp)peak} = 1.15\text{ V}; T_{case} = 80\text{ °C}$		
		$P_L = 50\text{ W}$	0.27	k/W
		$P_L = 80\text{ W}$	0.22	k/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.8\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 180\text{ mA}$	1.6	2.0	2.4	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 30\text{ V}; I_D = 300\text{ mA}$	-	2.2	-	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 30\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 2.37\text{ V}; V_{DS} = 10\text{ V}$	-	17.5	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 9\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 4.5\text{ A}$	-	8.85	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 2.37\text{ V}; I_D = 3.15\text{ A}$	-	146	210	$\text{m}\Omega$
<b>Peak device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 3.8\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 380\text{ mA}$	1.6	2.0	2.4	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 30\text{ V}; I_D = 1900\text{ mA}$	-	2.2	-	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 30\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 2.37\text{ V}; V_{DS} = 10\text{ V}$	-	35	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 9\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 9.5\text{ A}$	-	18.17	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 2.37\text{ V}; I_D = 6.65\text{ A}$	-	70	135	$\text{m}\Omega$

**Table 7. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH;  $f_1 = 1807.5\text{ MHz}$ ;  $f_2 = 1877.5\text{ MHz}$ ; RF performance at  $V_{DS} = 30\text{ V}$ ;  $I_{Dq} = 300\text{ mA}$  (main);  $V_{GS(amp)peak} = 1.15\text{ V}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 50\text{ W}$	14.5	15.6	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 50\text{ W}$	-	-11	-7	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 50\text{ W}$	45	49	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 50\text{ W}$	-	-30	-27	dBc

**Table 8. RF characteristics**

Pulsed CW signal at a frequency of 1880 MHz;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ;  $V_{DS} = 30\text{ V}$ ;  $I_{Dq} = 300\text{ mA}$  (main);  $V_{GS(amp)peak} = 1.2\text{ V}$ ;  $T_{case} = 25\text{ °C}$ ; in a Doherty production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(M)}$	peak output power	$P_{L(AV)} = 115\text{ W}$	280	300	-	W

## 7. Test information

### 7.1 Ruggedness in Doherty operation

The BLC10G18XS-301AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 30\text{ V}$ ;  $I_{Dq} = 300\text{ mA}$ ;  $V_{GS(amp)peak} = 1.15\text{ V}$ ;  $f = 1805\text{ MHz}$ ;  $P_L = 200\text{ W (CW)}$ .

### 7.2 Impedance information

**Table 9. Typical impedance of main device**

Measured load-pull data of main device;  $I_{Dq} = 300\text{ mA (main)}$ ;  $V_{DS} = 28\text{ V}$ ; pulsed CW ( $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
<b>Maximum power load</b>					
1810	4.4 – j10.3	2.7 – j4.4	129	57.6	14.9
1845	5.3 – j11.3	3.4 – j3.6	127	65.6	16.2
1880	7.1 – j12.2	2.8 – j4.8	129	57.9	15.5
<b>Maximum drain efficiency load</b>					
1810	4.5 – j10.6	5.1 – j1.8	93	70.7	17.2
1845	5.7 – j11.6	4.8 – j0.8	80	71.6	17.8
1880	7.4 – j12.7	5.4 – j2.3	88	70.2	17.7

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.

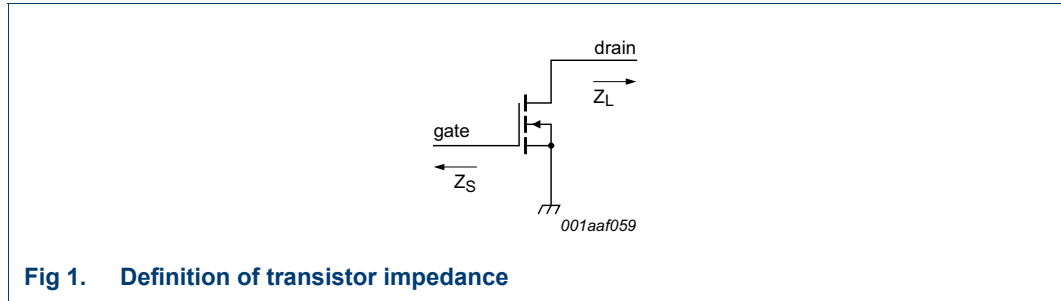
**Table 10. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{Dq} = 1900\text{ mA (peak)}$ ;  $V_{DS} = 32\text{ V}$ ; pulsed CW ( $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ).

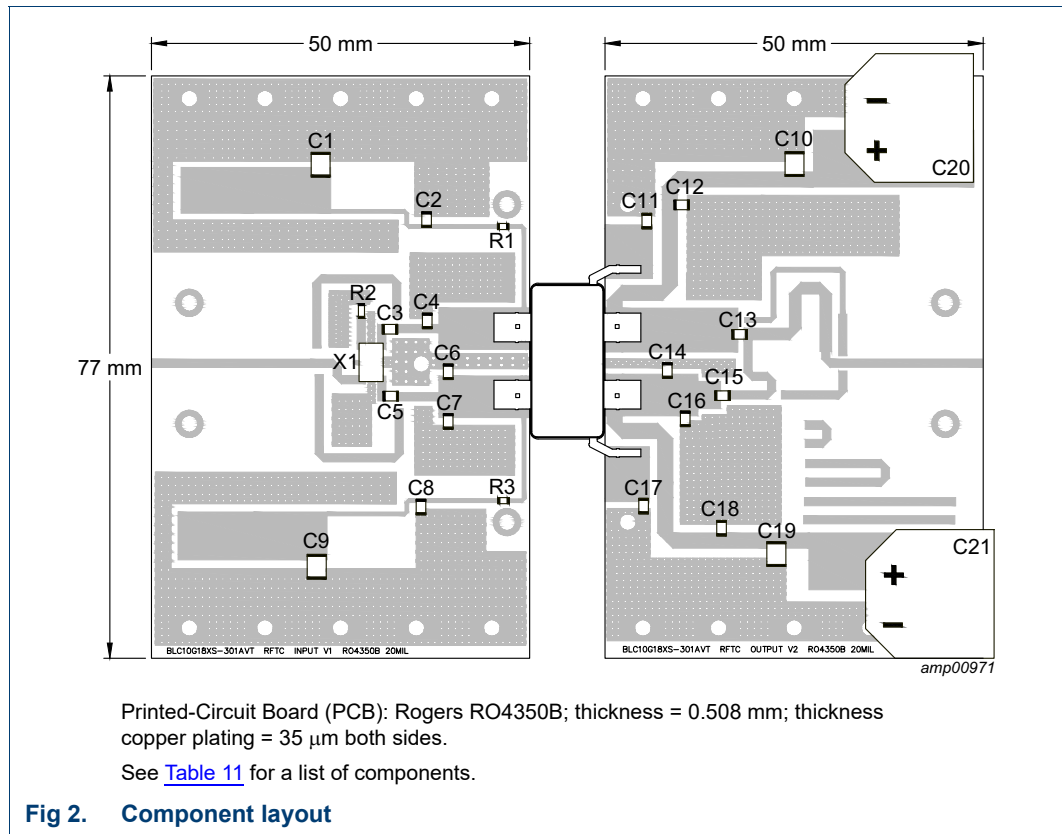
f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
<b>Maximum power load</b>					
1810	3.3 – j10.0	2.7 – j4.4	265	60	13.5
1845	3.9 – j10.9	2.3 – j4.3	260	58	13.7
1880	5.0 – j12.0	2.8 – j4.8	262	58	13.9
<b>Maximum drain efficiency load</b>					
1810	2.8 – j10.0	3.1 – j1.2	160	69.9	15.6
1845	3.3 – j10.9	2.6 – j1.4	152	70.2	16.1
1880	4.5 – j12.0	2.6 – j2.5	159	69.5	15.6

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.



7.3 Test circuit



**Table 11. List of components**

See [Figure 2](#) for component layout.

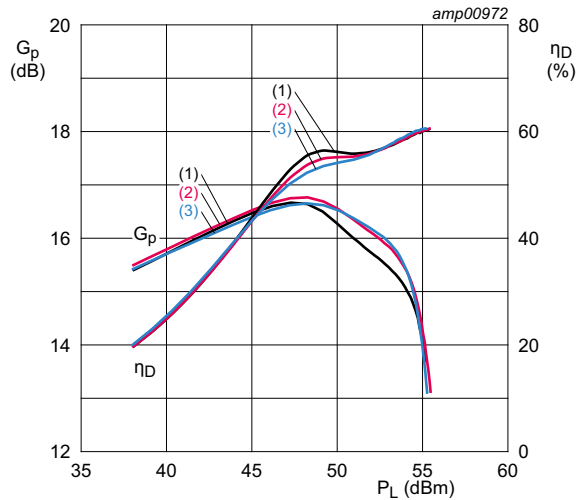
Component	Description	Value	Remarks
C1, C9, C10, C19	multilayer ceramic chip capacitor	10 μF, 50 V	[1]
C2, C3, C5, C8, C12, C15, C18	multilayer ceramic chip capacitor	18 pF	[2]
C4, C6	multilayer ceramic chip capacitor	0.5 pF	[2]
C7	multilayer ceramic chip capacitor	0.8 pF	[2]
C11, C17	multilayer ceramic chip capacitor	1 μF, 50 V	[2]
C13	multilayer ceramic chip capacitor	9.1 pF	[2]
C14, C16	multilayer ceramic chip capacitor	1 pF	[2]
C20, C21	electrolytic capacitor	1000 μF, 100 V	
R1, R3	resistor	5.6 Ω	SMD 0805
R2	resistor	50 Ω	SMD 0805
X1	hybrid coupler		X3C20F1-02S

[1] Murata or capacitor of same quality.

[2] American Technical Ceramics type 600F or capacitor of same quality.

7.4 Graphical data

7.4.1 Pulsed CW



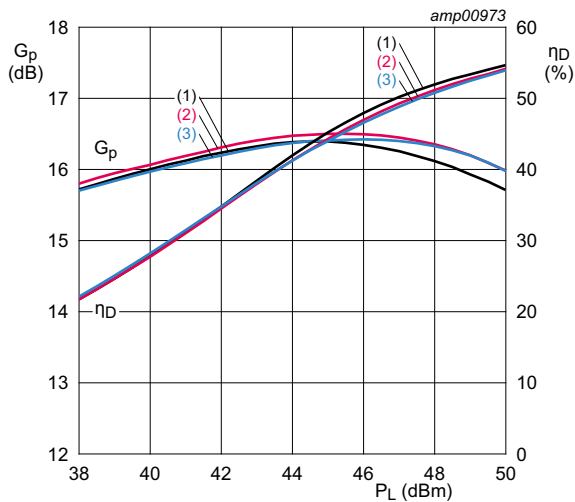
$V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 750\text{ mA}$ ;  $V_{GS(amp)peak} = 1.18\text{ V}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

- (1)  $f = 1805\text{ MHz}$
- (2)  $f = 1842.5\text{ MHz}$
- (3)  $f = 1880\text{ MHz}$

Fig 3. Power gain and drain efficiency as function of output power; typical values

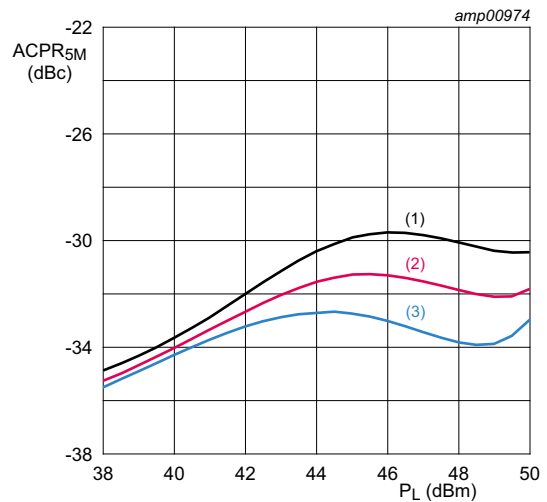
7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.



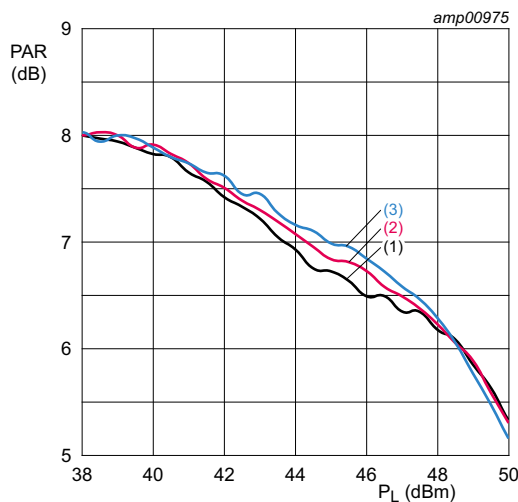
$V_{DS} = 32\text{ V}; I_{Dq} = 750\text{ mA}; V_{GS(amp)peak} = 1.18\text{ V}.$   
 (1)  $f = 1805\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1880\text{ MHz}$

**Fig 4. Power gain and drain efficiency as function of output power; typical values**



$V_{DS} = 32\text{ V}; I_{Dq} = 750\text{ mA}; V_{GS(amp)peak} = 1.18\text{ V}.$   
 (1)  $f = 1805\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1880\text{ MHz}$

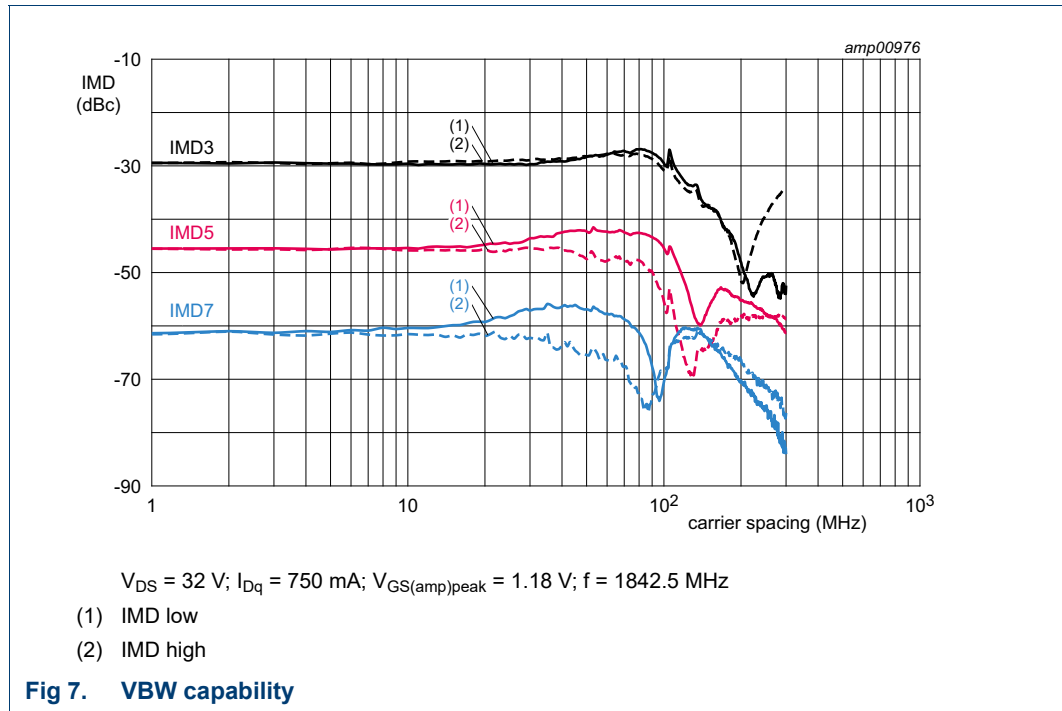
**Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values**



$V_{DS} = 32\text{ V}; I_{Dq} = 750\text{ mA}; V_{GS(amp)peak} = 1.18\text{ V}.$   
 (1)  $f = 1805\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1880\text{ MHz}$

**Fig 6. Peak-to-average power ratio as a function of output power; typical values**

7.4.3 2-Tone VBW





## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 12. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

**Table 13. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 14. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G18XS-301AVT v.1	20190523	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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