



**THE DATASHEET OF
BGA824N6E6329XTSA1**

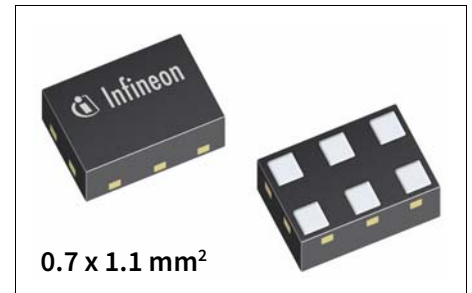


BGA824N6

Silicon Germanium Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

Features

- Operating frequencies: 1164 - 1615 MHz
- Insertion power gain: 17.0 dB
- Input 1 dB compression point: -6 dBm
- Low noise figure: 0.55 dB
- Low current consumption: 3.8 mA
- Digital on/off switch
- Ultra small TSNP-6-2 and TSNP-6-10 leadless package
- RF output internally matched to 50 Ohm
- Low external component count



Application

Ideal for all Global Navigation Satellite Systems (GNSS) like GPS, GLONASS, Beidou, Galileo and others.

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Block diagram

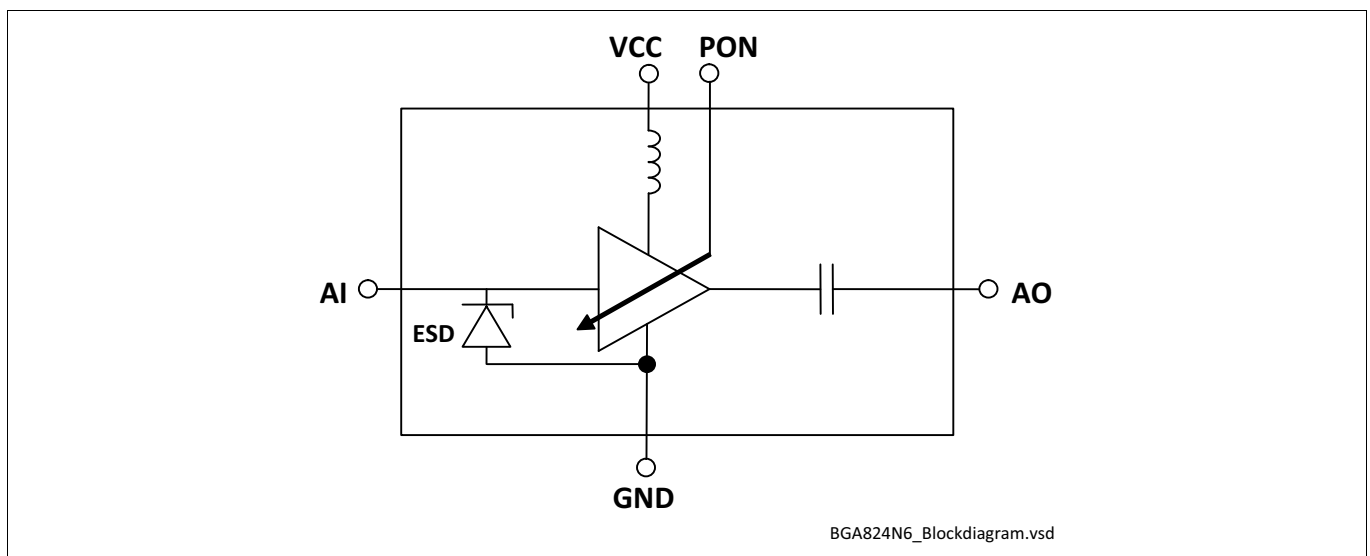




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Features

1 Features

- Insertion power gain: 17.0 dB
- Out-of-band input 3rd order intercept point: +7 dBm
- Input 1 dB compression point: -6 dBm
- Low noise figure: 0.55 dB
- Low current consumption: 3.8 mA
- Operating frequencies: 1164 - 1615 MHz
- Digital on/off switch
- Supply voltage: 1.5 V to 3.6 V
- Ultra small TSNP-6-2 and TSNP-6-10 leadless package (footprint: 0.7 x 1.1 mm²)
- B7HF Silicon Germanium technology
- RF output internally matched to 50 Ohm
- Low external component count
- 2kV HBM ESD protection (including AI-pin)
- Pb-free (RoHS compliant) package

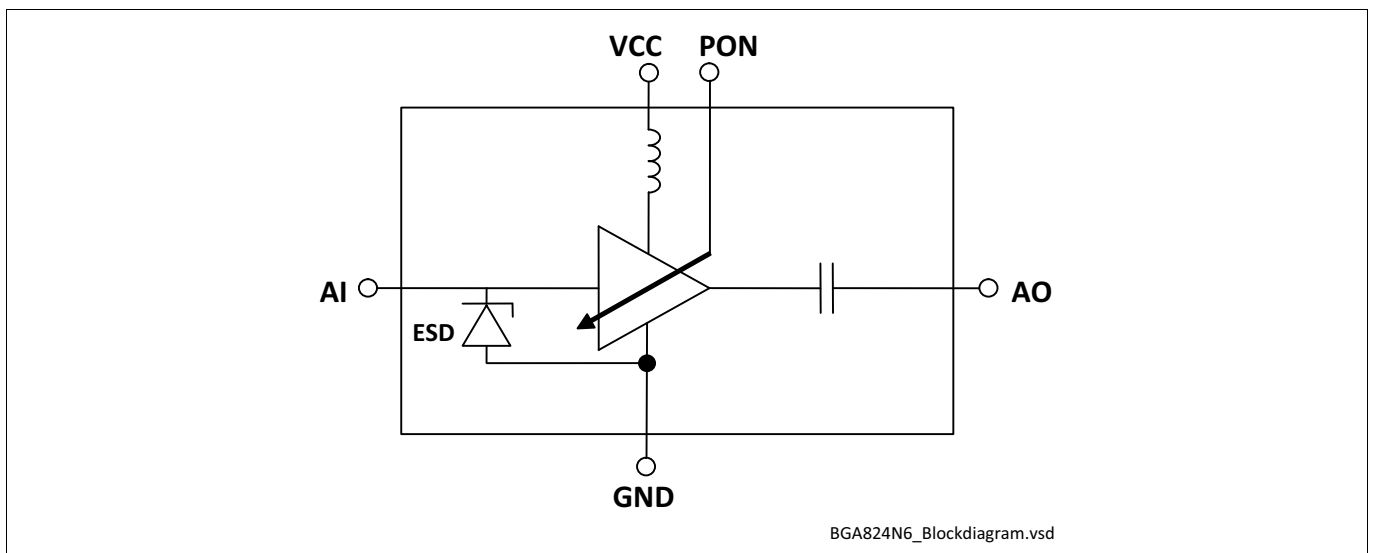


Figure 1 Block Diagram

Product Name	Marking	Package
BGA824N6	F	TSNP-6-2/TSNP-6-10

Features**Description**

The BGA824N6 is a front-end low noise amplifier for Global Navigation Satellite Systems (GNSS) from 1164 MHz to 1615 MHz like GPS, GLONASS, Beidou, Galileo and others. The LNA provides 17.0 dB gain and 0.55 dB noise figure at a current consumption of 3.8 mA in the application configuration described in [Chapter 4](#). The BGA824N6 is based upon Infineon Technologies' B7HF Silicon Germanium technology. It operates from 1.5 V to 3.6 V supply voltage.

Pin Definition and Function**Table 1 Pin Definition and Function**

Pin No.	Name	Function
1	GND	Ground
2	VCC	DC supply
3	AO	LNA output
4	GND	Ground
5	AI	LNA input
6	PON	Power on control

Maximum Ratings

2 Maximum Ratings

Table 2 Maximum Ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Voltage at pin VCC	V_{CC}	-0.3	–	3.6	V	1)
Voltage at pin AI	V_{AI}	-0.3	–	0.9	V	–
Voltage at pin AO	V_{AO}	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin PON	V_{PON}	-0.3	–	$V_{CC} + 0.3$	V	–
Voltage at pin GNDRF	V_{GNDRF}	-0.3	–	0.3	V	–
Current into pin VCC	I_{CC}	–	–	23	mA	–
RF input power	P_{IN}	–	–	25	dBm	–
Total power dissipation, $T_S < 148\text{ °C}^2)$	P_{tot}	–	–	60	mW	–
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-40	–	85	°C	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
ESD capability all pins	V_{ESD_HBM}	-2000	–	+2000	V	according to JS-001

1) All voltages refer to GND-Node unless otherwise noted

2) T_S is measured on the ground lead at the soldering point

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

Thermal Resistance

Table 3 Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}	25	K/W

1) For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics

3 Electrical Characteristics

Table 4 Electrical Characteristics $f = 1550 - 1615$ MHz, $V_{CC} = 1.8V^{1)}$ $T_A = 25$ °C, $V_{CC} = 1.8$ V, $V_{PON,ON} = 1.8$ V, $V_{PON,OFF} = 0$ V, $f = 1550 - 1615$ MHz

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	1.8	3.6	V	–
Supply current	I_{CC}	–	3.8	4.8	mA	ON-mode
		–	0.2	3	μA	OFF-mode
Power On voltage	V_{PON}	0.8	–	V_{CC}	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{PON}	–	5	10	μA	ON-mode
		–	–	1	μA	OFF-mode
Insertion power gain $f = 1575$ MHz	$ S_{21} ^2$	16.0	17.0	18.0	dB	–
Noise figure ²⁾ $f = 1575$ MHz	NF	–	0.55	1.1	dB	–
Input return loss ³⁾ $f = 1575$ MHz	RL_{IN}	10	14	–	dB	–
Output return loss ³⁾ $f = 1575$ MHz	RL_{OUT}	10	17	–	dB	–
Reverse isolation ³⁾ $f = 1575$ MHz	$1/ S_{12} ^2$	19	23	–	dB	–
Power gain settling time ⁴⁾⁵⁾	t_s	–	5	8	μs	OFF- to ON-mode
		–	5	8	μs	ON- to OFF-mode
		–	1.2	3	μs	OFF- to ON-mode ⁶⁾
		–	0.9	3	μs	ON- to OFF-mode ⁶⁾
Inband input 1dB-compression point ³⁾ $f = 1575$ MHz	IP_{1dB}	-13	-9	–	dBm	–
Inband input 3 rd -order intercept point ³⁾⁷⁾	IIP_3	-3	+2	–	dBm	$f_1 = 1575$ MHz $f_2 = f_1 \pm 1$ MHz
Out-of-band input 3 rd -order intercept point ⁵⁾⁸⁾	IIP_{3OOB}	+2	+7	–	dBm	$f_1 = 1712.7$ MHz $f_2 = 1850$ MHz
Stability ⁵⁾	k	> 1	–	–		$f = 20$ MHz ... 10 GHz

1) Based on the application described in Figure 2 in [Chapter 4](#)

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain OFF- to ON-mode; to be within 3 dB of the final gain ON- to OFF-mode

5) Guaranteed by device design; not tested in production

6) 120 pF DC block capacitor at RF input

7) Input power = -30 dBm for each tone

8) Input power = -20 dBm for each tone

Electrical Characteristics

Table 5 Electrical Characteristics $f = 1550 - 1615$ MHz, $V_{CC} = 2.8V$ ¹⁾ $T_A = 25$ °C, $V_{CC} = 2.8$ V, $V_{PON,ON} = 2.8$ V, $V_{PON,OFF} = 0$ V, $f = 1550 - 1615$ MHz

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	2.8	3.6	V	–
Supply current	I_{CC}	–	3.9	4.9	mA	ON-mode
		–	0.2	3	μA	OFF-mode
Power On voltage	V_{PON}	0.8	–	V_{CC}	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{PON}	–	10	15	μA	ON-mode
		–	–	1	μA	OFF-mode
Insertion power gain $f = 1575$ MHz	$ S_{21} ^2$	16.1	17.1	18.1	dB	–
Noise figure ²⁾ $f = 1575$ MHz	NF	–	0.55	1.1	dB	–
Input return loss ³⁾ $f = 1575$ MHz	RL_{IN}	10	15	–	dB	–
Output return loss ³⁾ $f = 1575$ MHz	RL_{OUT}	10	18	–	dB	–
Reverse isolation ³⁾ $f = 1575$ MHz	$1/ S_{12} ^2$	19	23	–	dB	–
Power gain settling time ⁴⁾⁵⁾	t_s	–	5	8	μs	OFF- to ON-mode
		–	5	8	μs	ON- to OFF-mode
		–	1.2	3	μs	OFF- to ON-mode ⁶⁾
		–	0.9	3	μs	ON- to OFF-mode ⁶⁾
Inband input 1dB-compression point ³⁾ $f = 1575$ MHz	IP_{1dB}	-10	-6	–	dBm	–
Inband input 3 rd -order intercept point ³⁾⁷⁾	IIP_3	-2	+3	–	dBm	$f_1 = 1575$ MHz $f_2 = f_1 \pm 1$ MHz
Out-of-band input 3 rd -order intercept point ⁵⁾⁸⁾	IIP_{3OoB}	+2	+7	–	dBm	$f_1 = 1712.7$ MHz $f_2 = 1850$ MHz
Stability ⁵⁾	k	> 1	–	–		$f = 20$ MHz ... 10 GHz

1) Based on the application described in Figure 2 in [Chapter 4](#)

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain OFF- to ON-mode; to be within 3 dB of the final gain ON- to OFF-mode

5) Guaranteed by device design; not tested in production

6) 120 pF DC block capacitor at RF input

7) Input power = -30 dBm for each tone

8) Input power = -20 dBm for each tone

Electrical Characteristics

Table 6 Electrical Characteristics $f = 1164 - 1300$ MHz, $V_{CC} = 1.8$ V¹⁾ $T_A = 25$ °C, $V_{CC} = 1.8$ V, $V_{PON,ON} = 1.8$ V, $V_{PON,OFF} = 0$ V, $f = 1164 - 1300$ MHz

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	1.8	3.6	V	–
Supply current	I_{CC}	–	3.8	4.8	mA	ON-mode
		–	0.2	3	μA	OFF-mode
Power On voltage	V_{PON}	0.8	–	V_{CC}	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{PON}	–	5	10	μA	ON-mode
		–	–	1	μA	OFF-mode
Insertion power gain $f = 1214$ MHz	$ S_{21} ^2$	16.4	17.9	19.4	dB	–
Noise figure ²⁾ $f = 1214$ MHz	NF	–	0.70	1.25	dB	–
Input return loss ³⁾ $f = 1214$ MHz	RL_{IN}	10	15	–	dB	–
Output return loss ³⁾ $f = 1214$ MHz	RL_{OUT}	10	18	–	dB	–
Reverse isolation ³⁾ $f = 1214$ MHz	$1/ S_{12} ^2$	19	25	–	dB	–
Power gain settling time ⁴⁾⁵⁾	t_s	–	5	8	μs	OFF- to ON-mode
		–	5	8	μs	ON- to OFF-mode
		–	1.2	3	μs	OFF- to ON-mode ⁶⁾
		–	0.9	3	μs	ON- to OFF-mode ⁶⁾
Inband input 1dB-compression point ³⁾ $f = 1214$ MHz	IP_{1dB}	-16	-12	–	dBm	–
Inband input 3 rd -order intercept point ³⁾⁷⁾	IIP_3	-11	-6	–	dBm	$f_1 = 1214$ MHz $f_2 = f_1 \pm 1$ MHz
Out-of-band input 3 rd -order intercept point ⁵⁾⁸⁾	IIP_{3OoB}	-3	+1.3	–	dBm	$f_1 = 1850$ MHz $f_2 = 2500$ MHz
Stability ⁵⁾	k	> 1	–	–		$f = 20$ MHz ... 10 GHz

1) Based on the application described in Figure 3 in [Chapter 4](#)

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain OFF- to ON-mode; to be within 3 dB of the final gain ON- to OFF-mode

5) Guaranteed by device design; not tested in production

6) 120 pF DC block capacitor at RF input

7) Input power = -30 dBm for each tone

8) Input power = -25 dBm for each tone

Electrical Characteristics

Table 7 Electrical Characteristics $f = 1164 - 1300$ MHz, $V_{CC} = 2.8V$ ¹⁾ $T_A = 25$ °C, $V_{CC} = 2.8$ V, $V_{PON,ON} = 2.8$ V, $V_{PON,OFF} = 0$ V, $f = 1164 - 1300$ MHz

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.5	2.8	3.6	V	–
Supply current	I_{CC}	–	3.9	4.8	mA	ON-mode
		–	0.2	3	μA	OFF-mode
Power On voltage	V_{PON}	0.8	–	V_{CC}	V	ON-mode
		0	–	0.4	V	OFF-mode
Power On current	I_{PON}	–	10	15	μA	ON-mode
		–	–	1	μA	OFF-mode
Insertion power gain $f = 1214$ MHz	$ S_{21} ^2$	16.5	18.0	19.5	dB	–
Noise figure ²⁾ $f = 1214$ MHz	NF	–	0.70	1.25	dB	–
Input return loss ³⁾ $f = 1214$ MHz	RL_{IN}	10	16	–	dB	–
Output return loss ³⁾ $f = 1214$ MHz	RL_{OUT}	10	18	–	dB	–
Reverse isolation ³⁾ $f = 1214$ MHz	$1/ S_{12} ^2$	19	26	–	dB	–
Power gain settling time ⁴⁾⁵⁾	t_s	–	5	8	μs	OFF- to ON-mode
		–	5	8	μs	ON- to OFF-mode
		–	1.2	3	μs	OFF- to ON-mode ⁶⁾
		–	0.9	3	μs	ON- to OFF-mode ⁶⁾
Inband input 1dB-compression point ³⁾ $f = 1214$ MHz	IP_{1dB}	-13	-9	–	dBm	–
Inband input 3 rd -order intercept point ³⁾⁷⁾	IIP_3	-10	-5	–	dBm	$f_1 = 1214$ MHz $f_2 = f_1 \pm 1$ MHz
Out-of-band input 3 rd -order intercept point ⁵⁾⁸⁾	IIP_{300B}	-3	+1.3	–	dBm	$f_1 = 1850$ MHz $f_2 = 2500$ MHz
Stability ⁵⁾	k	> 1	–	–		$f = 20$ MHz ... 10 GHz

1) Based on the application described in Figure 3 in [Chapter 4](#)

2) PCB losses are subtracted

3) Verification based on AQL; not 100% tested in production

4) To be within 1 dB of the final gain OFF- to ON-mode; to be within 3 dB of the final gain ON- to OFF-mode

5) Guaranteed by device design; not tested in production

6) 120 pF DC block capacitor at RF input

7) Input power = -30 dBm for each tone

8) Input power = -25 dBm for each tone

4 Application Information

Application Board Configuration f = 1550 - 1615 MHz

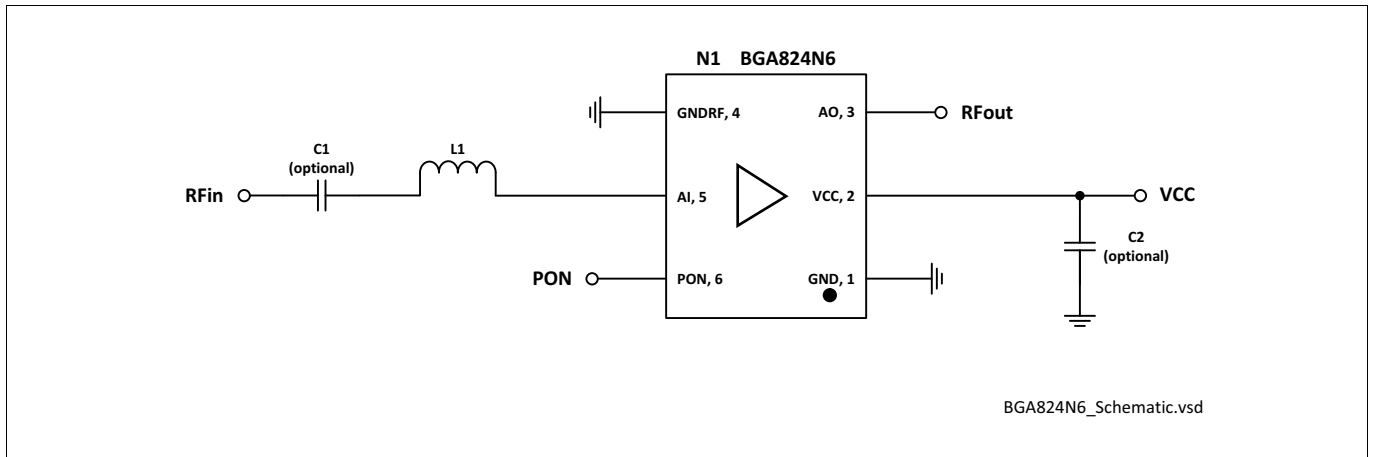


Figure 2 Application Schematic BGA824N6 f = 1550 - 1615 MHz

Table 8 Bill of Materials

Name	Value	Package	Manufacturer	Function
C1 (optional)	1nF	0402	Various	DC block ¹⁾
C2 (optional)	≥ 10nF ²⁾	0402	Various	RF bypass ³⁾
L1	6.8nH	0402	Murata LQW type	Input matching
N1	BGA824N6	TSNP-6-2 and TSNP-6-10	Infineon	SiGe LNA

1) DC block might be realized with pre-filter in GNSS application

2) For data sheet characteristics 1μF used

3) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at <http://www.infineon.com/gpslna.appnotes>

Application Information

Application Board Configuration f = 1164 - 1300 MHz

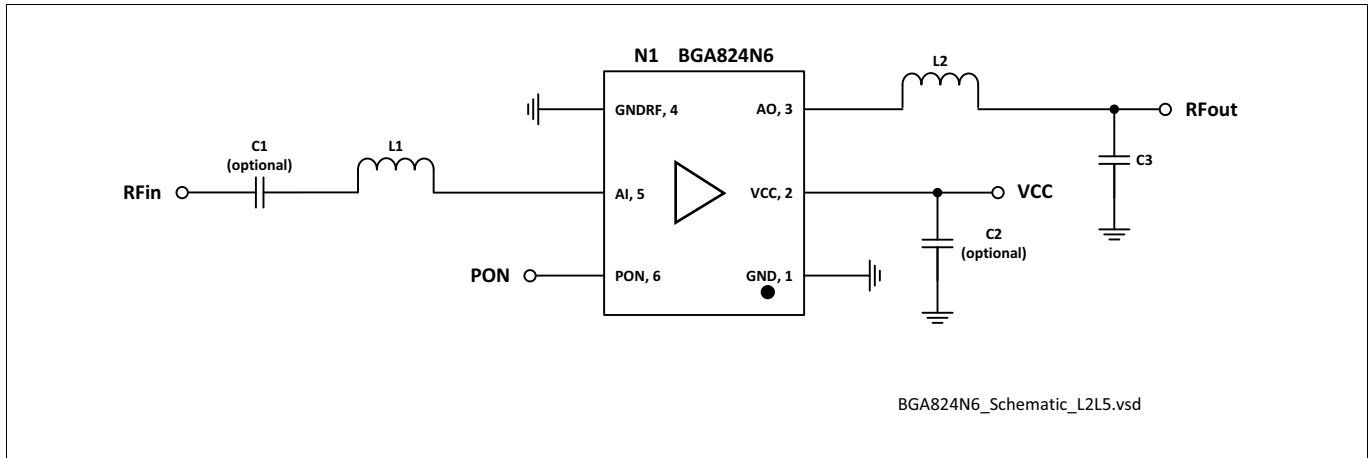


Figure 3 Application Schematic BGA824N6 f = 1164 - 1300 MHz

Table 9 Bill of Materials

Name	Value	Package	Manufacturer	Function
C1 (optional)	1nF	0402	Various	DC block ¹⁾
C2 (optional)	≥ 10nF ²⁾	0402	Various	RF bypass ³⁾
C3	3.9pF	0402	Various	Output matching
L1	12nH	0402	Murata LQW type	Input matching
L2	3.9nH	0402	Murata LQW type	Output matching
N1	BGA824N6	TSNP-6-2 and TSNP-6-10	Infineon	SiGe LNA

1) DC block might be realized with pre-filter in GNSS application

2) For data sheet characteristics 1μF used

3) RF bypass recommended to mitigate power supply noise

A list of all application notes is available at <http://www.infineon.com/gpslna.appnotes>

Application Information

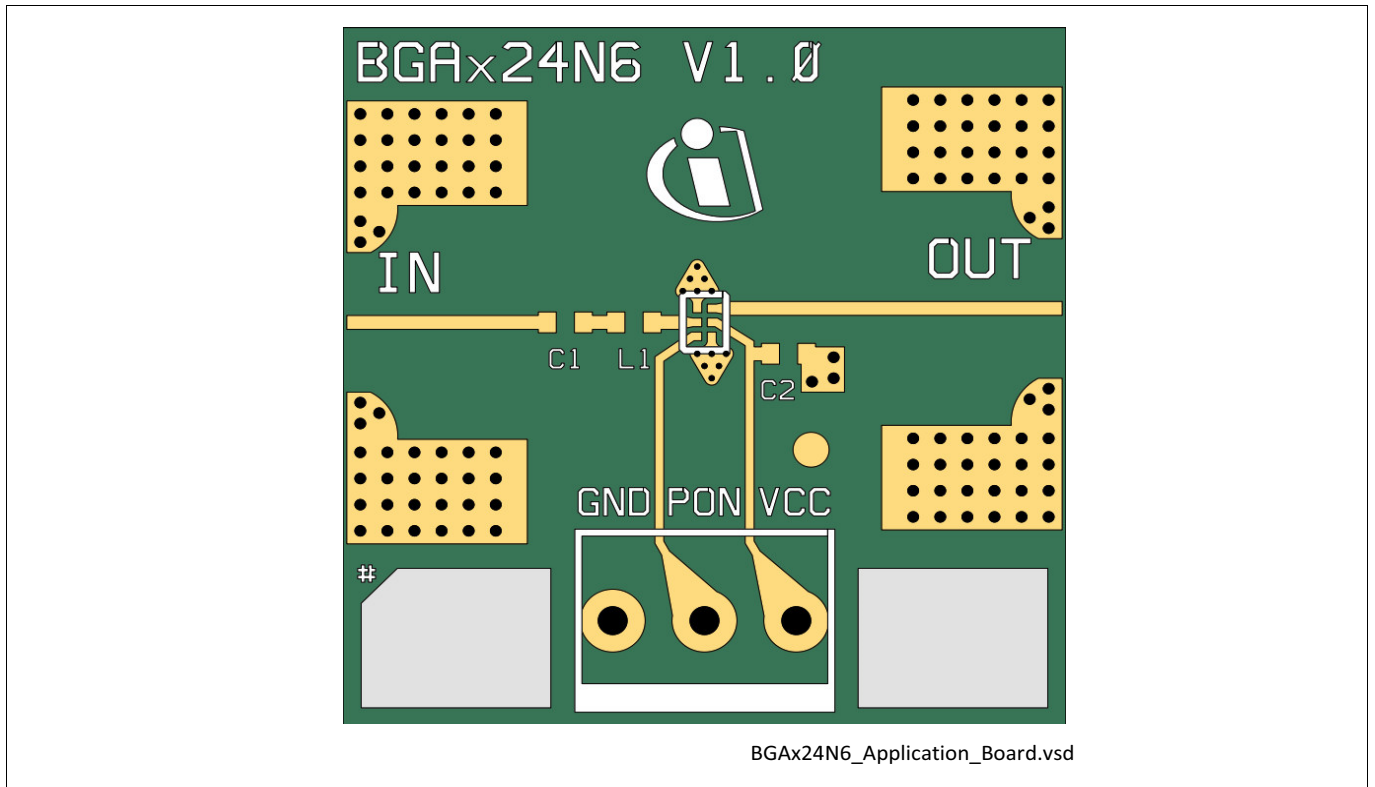


Figure 4 Drawing of Application Board

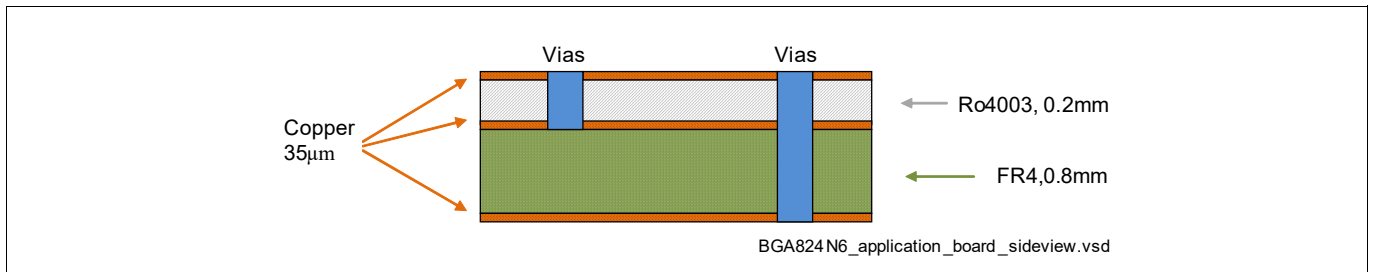


Figure 5 Application Board Cross-Section

Package Information

5 Package Information

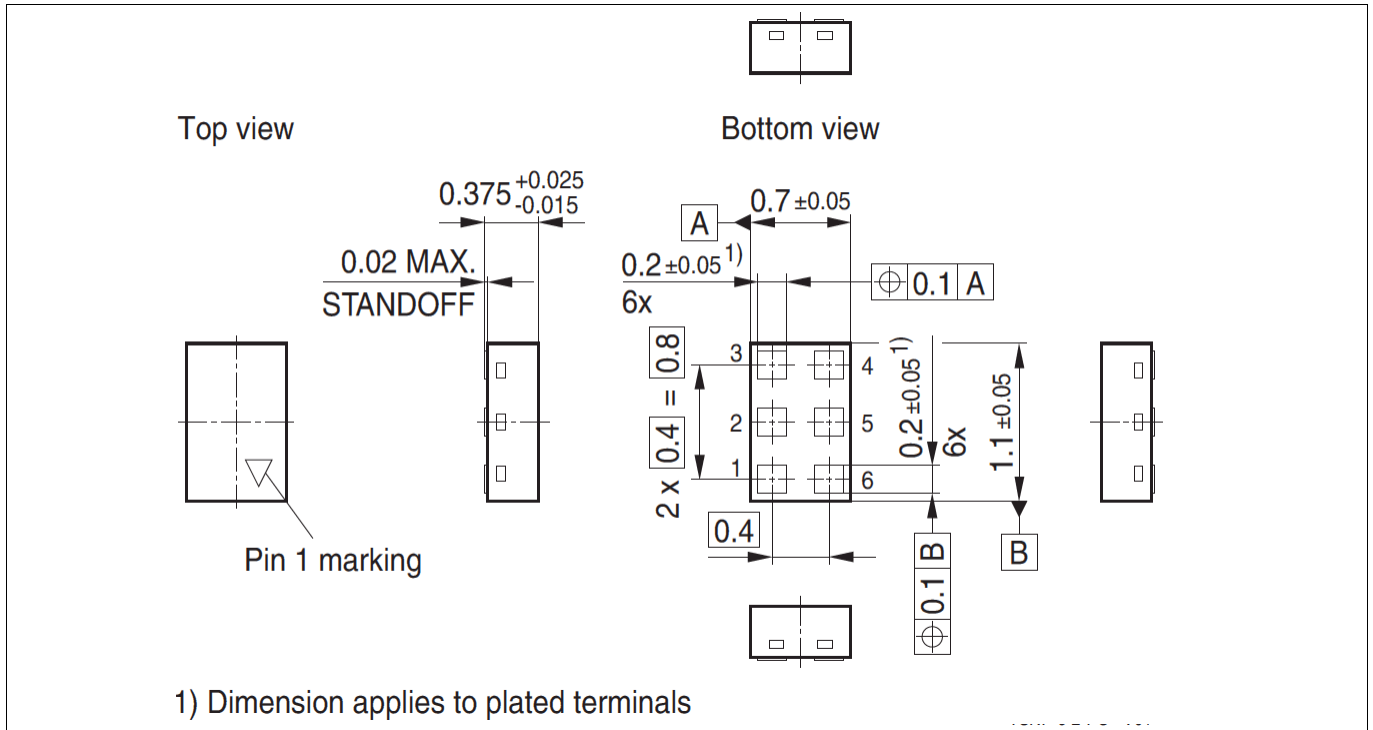


Figure 6 TSNP-6-2 Package Outline (top, side and bottom views)

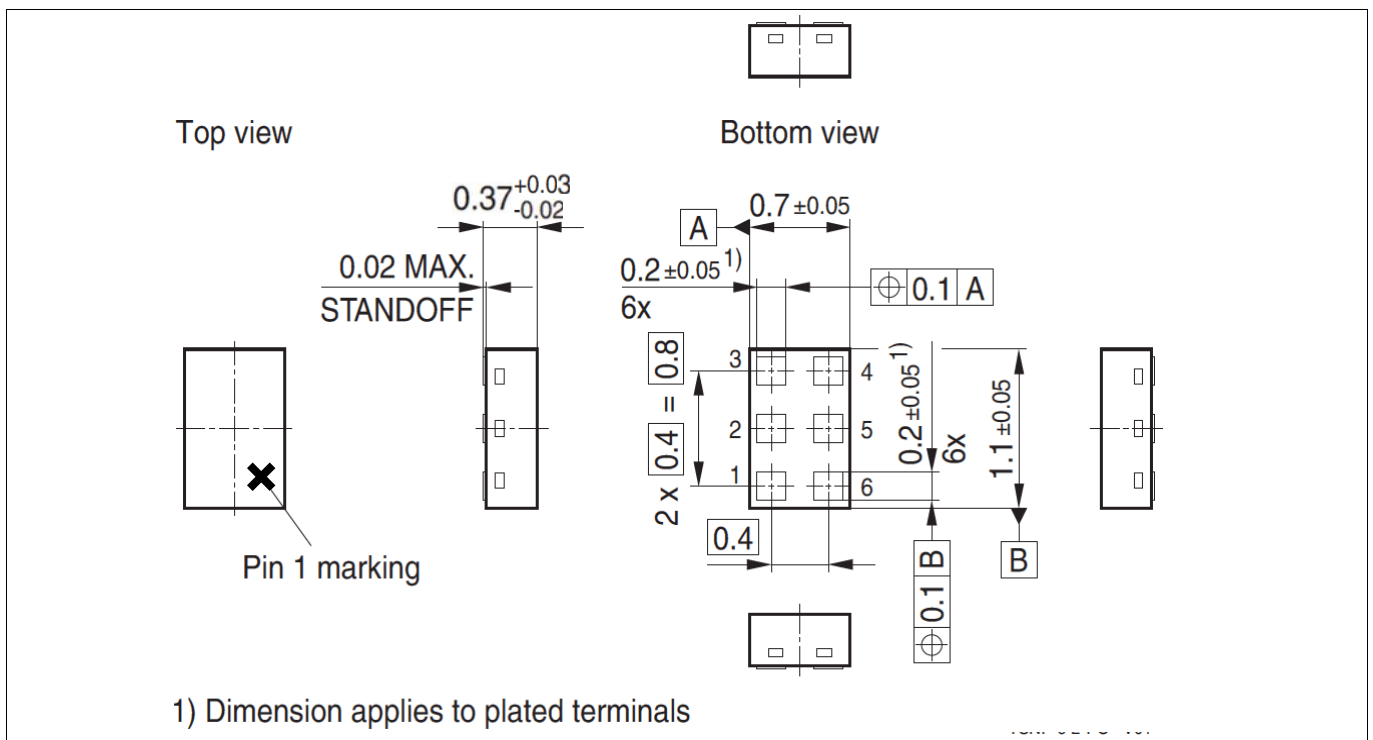


Figure 7 TSNP-6-10 Package Outline (top, side and bottom views)

Package Information

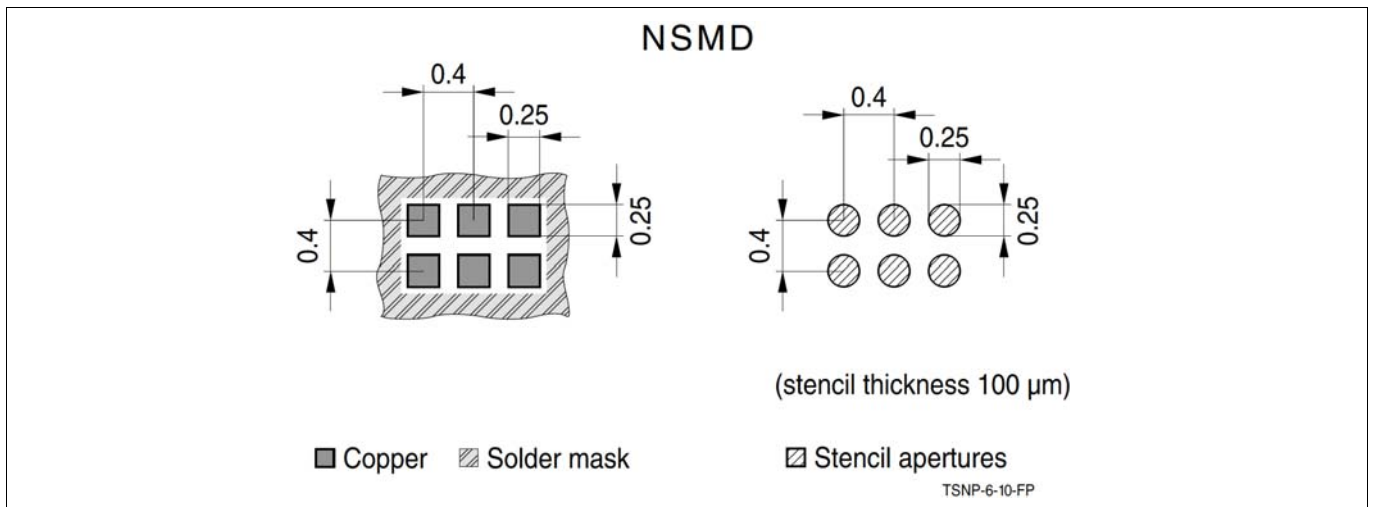


Figure 8 Footprint Recommendation TSNP-6-2 and TSNP-6-10

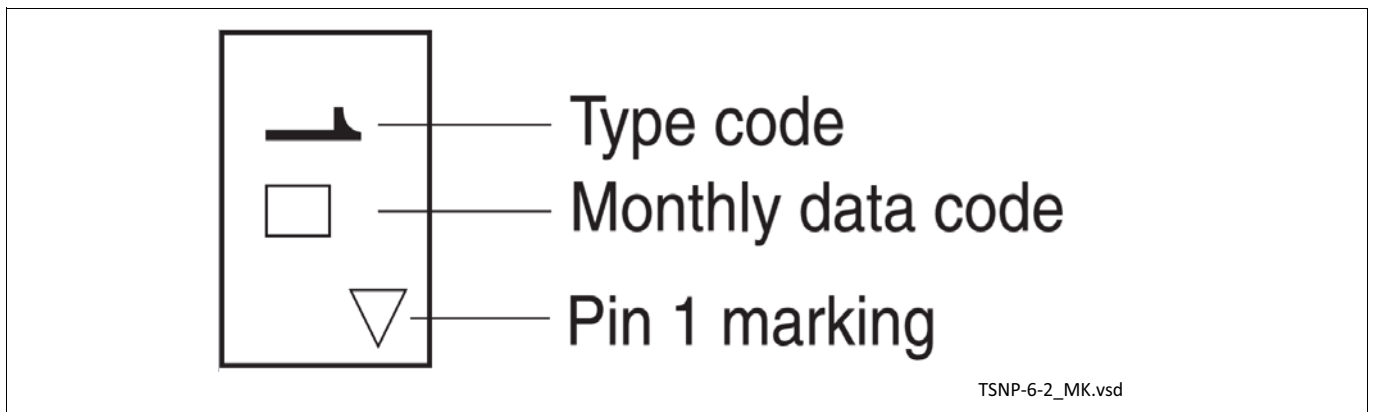


Figure 9 Marking Layout TSNP-6-2 (top view)

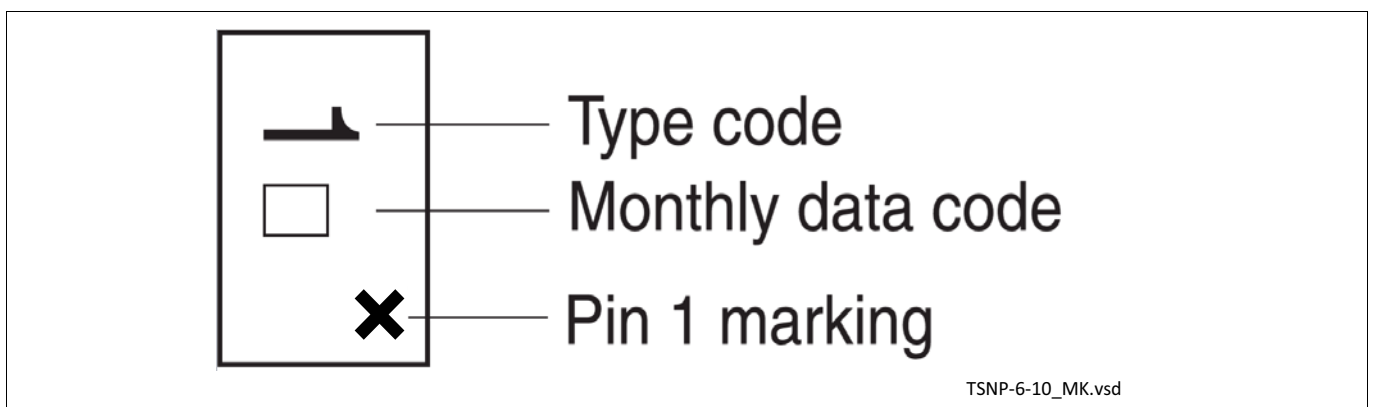


Figure 10 Marking Layout TSNP-6-10 (top view)

Package Information

Month	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

Figure 11 Date Code Marking TSNP-6-2 and TSNP-6-10

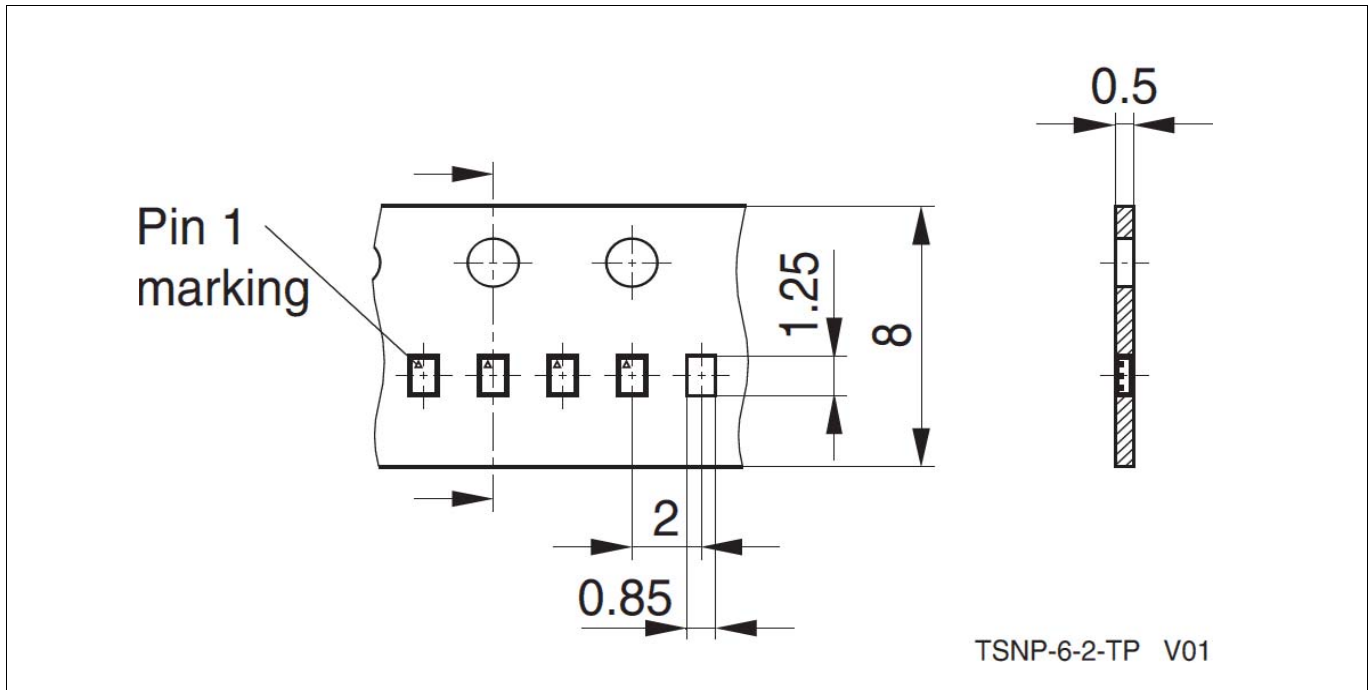


Figure 12 Tape & Reel Dimensions TSNP-6-2 (reel diameter 180 mm, pieces/reel 15000)

Package Information

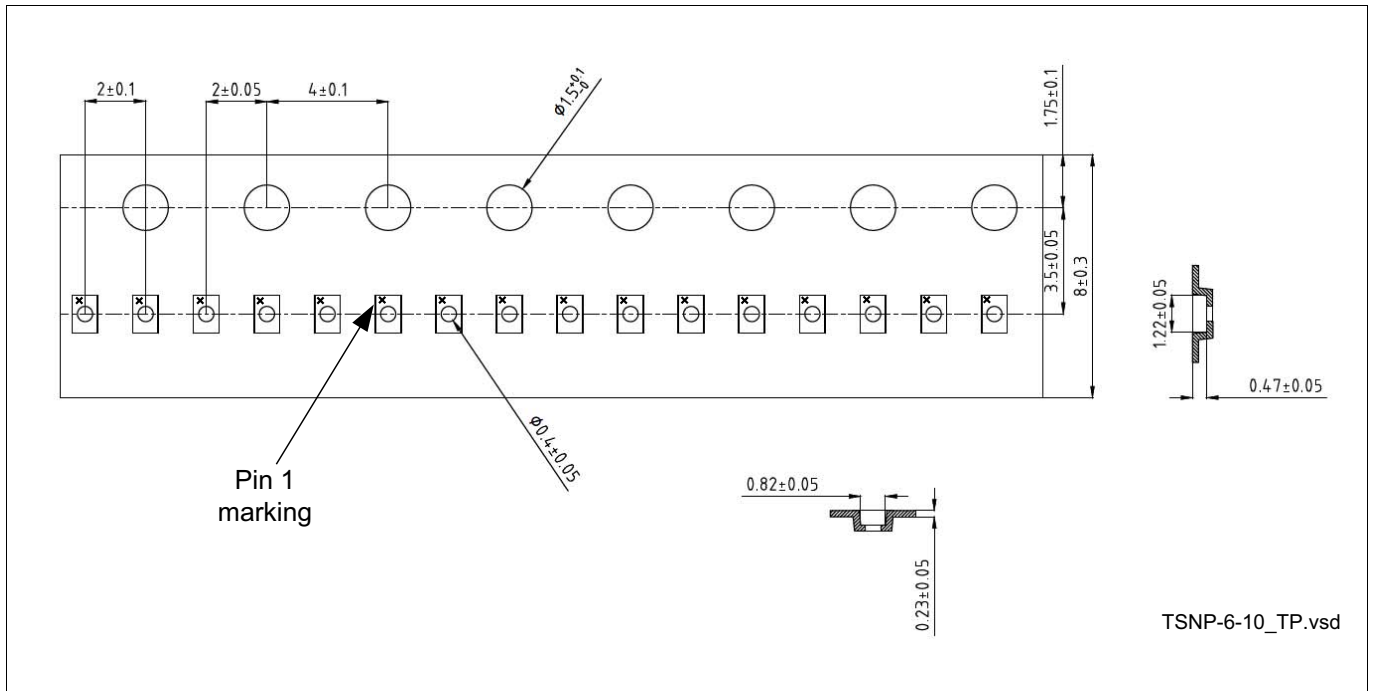


Figure 13 Tape & Reel Dimensions TSNP-6-10 (reel diameter 180 mm, pieces/reel 12000)



Revision History

Page or Item	Subjects (major changes since previous revision)
Revision 3.5, 2023-01-12	
6-9	Update Power On Voltage in On-Mode

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