



**THE DATASHEET OF
BD63800MUF-CE2**



40 V Max Stepping Motor Driver for Automotive

BD63800MUF-C

General Description

BD63800MUF-C is a bipolar low-consumption driver that is driven by PWM current. Rated power supply voltage of the device is 40 V, and rated output current is 1.35 A. BD63800MUF-C has two input interface as driving mode: CLK-IN and SPI-IN, and six excitation modes: Full step, 1/2, 1/4, 1/8, 1/16 and 1/32 step. Mix Decay Mode: the seamless adjustment function of slow/fast decay ratio, and Auto Decay Mode: Automatic switching function of slow/fast decay, can realize the optimized control status for all kinds of motor. In addition, BD63800MUF-C operates with single power supply which can simplify the set design.

Features

- AEC-Q100 Qualified (Note 1)
- Low ON Resistance DMOS Output
- CLK-IN Drive Mode
- PWM Constant Current Control (Separately Excited)
- Built-in Spike Noise Cancel Function (No external noise filter is required)
- Supported Modes: Full step, 1/2, 1/4, 1/8, 1/16 and 1/32 step
- Excitation Mode Switching Timing Free
- Current Decay Mode Switch Function
 - Mix Decay: Linear Adjustment of Slow Decay / Fast Decay Ratio
 - Auto Decay: Automatic Switch of Slow Decay / Fast Decay
- Selectable Rotation Direction: Clockwise/Counter Clockwise
- Power Save Function
- Built-in Pull-down Resistors for Logic Input
- Power-on Reset Function
- Malfunction prevention function w/o power supply (Ghost Supply Prevention Function)
- Thermal Shutdown Function (TSD)
- Thermal Warning Function (TW)
- Over Current Protection Function (OCP)
- Over Voltage Lock-out Function (OVLO)
- Under Voltage Lock-out Function (UVLO)
- Under Voltage Motor Hold Function
- Open Detection Function
- Stall Detection Function
- Adjacent Pin Short Protection

(Note 1) Grade 1

Applications

- Head-up Display
- LED Headlight
- etc.

Key Specifications

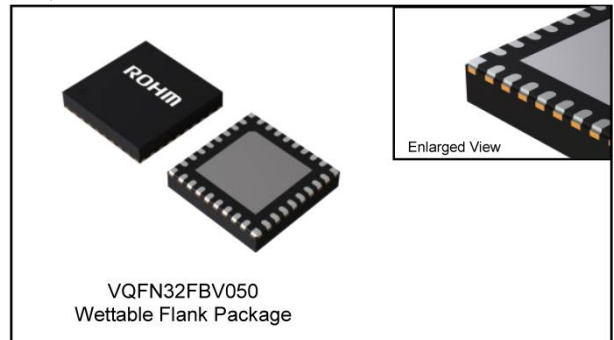
- Supply Voltage Range: 6.0 V to 28.0 V
- Output Current Rating (peak): 1.35 A
- Output Current Rating (DC): 1.21 A
- Output On Resistance (up and down): 0.75 Ω
- Operating Temperature Range: -40 °C to +125 °C

Package

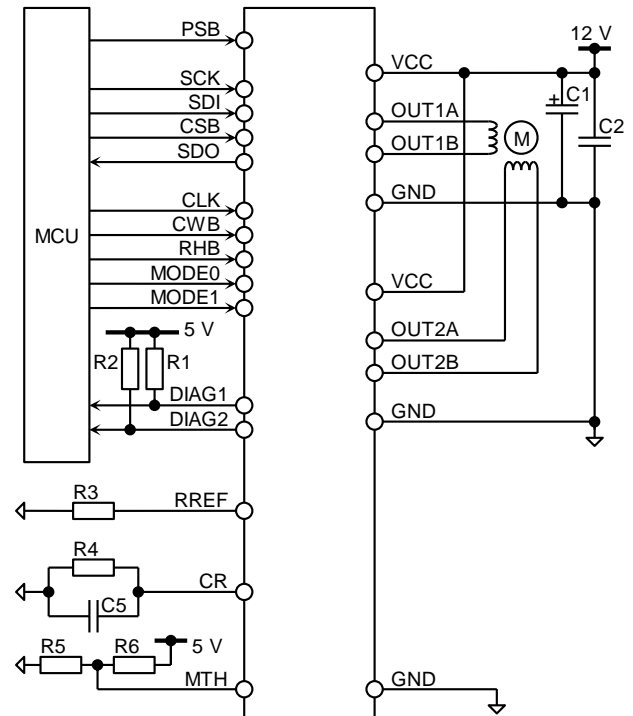
W (Typ) x D (Typ) x H (Max)

VQFN32FBV050

5.0 mm x 5.0 mm x 1.0 mm



Typical Application Circuits

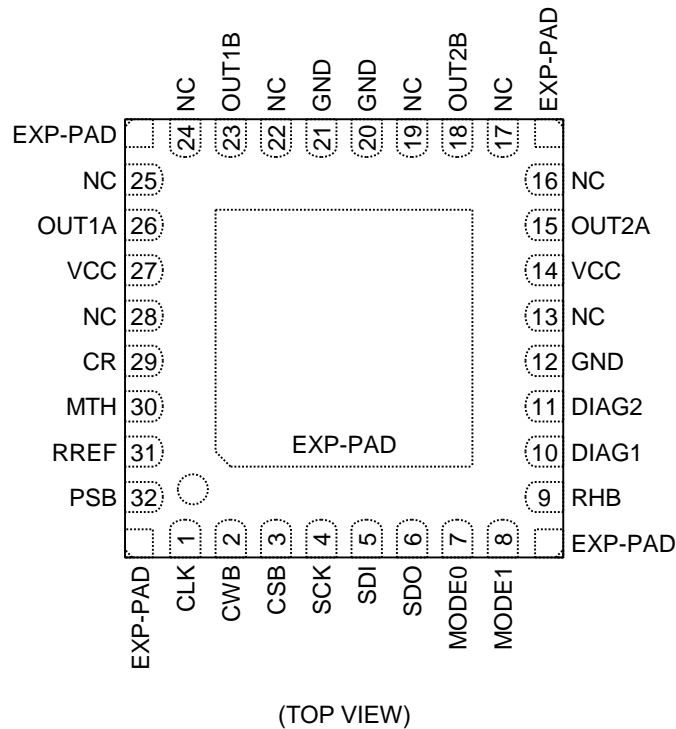


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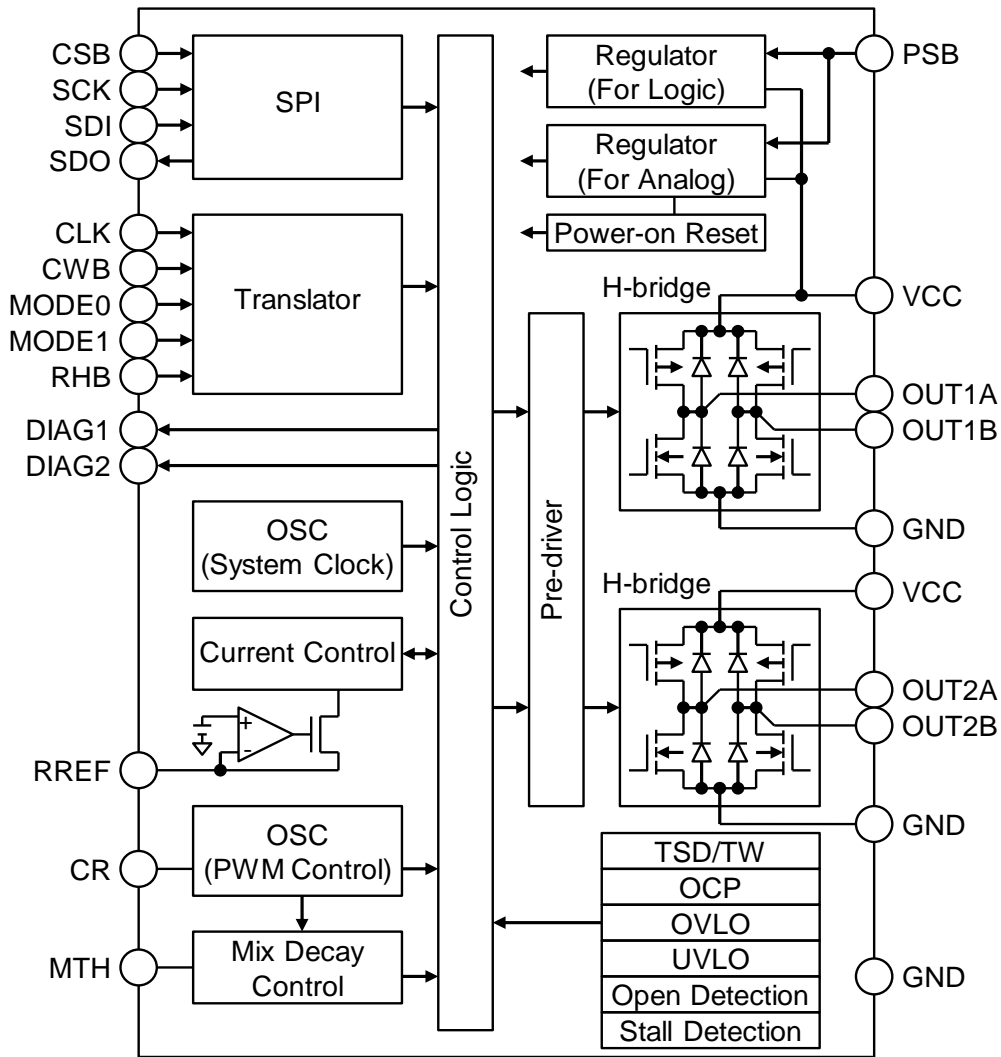
Pin Configuration



Pin Description

| Pin No. | Pin Name | P/G/I/O | Function |
|------------------------|----------|---------|--|
| 1 | CLK | Input | Micro step clock input pin |
| 2 | CWB | Input | Motor rotation direction selection pin |
| 3 | CSB | Input | Serial interface chip select pin |
| 4 | SCK | Input | Serial interface clock pin |
| 5 | SDI | Input | Serial interface data input pin |
| 6 | SDO | Output | Serial interface data output pin |
| 7 | MODE0 | Input | Motor excitation mode selection pin |
| 8 | MODE1 | Input | Motor excitation mode selection pin |
| 9 | RHB | Input | Motor drive / hold mode selection pin |
| 10 | DIAG1 | Output | Protection / detection output pin |
| 11 | DIAG2 | Output | Protection / detection output pin |
| 15 | OUT2A | Output | H-bridge output pin |
| 18 | OUT2B | Output | H-bridge output pin |
| 23 | OUT1B | Output | H-bridge output pin |
| 26 | OUT1A | Output | H-bridge output pin |
| 29 | CR | Output | Chopping frequency setting pin |
| 30 | MTH | Input | Current decay mode setting pin |
| 31 | RREF | Input | Output current level setting pin |
| 32 | PSB | Input | Power save pin |
| 14, 27 | VCC | Power | Input power supply pin |
| 12, 20, 21 | GND | Ground | Ground pin |
| 13, 28 | NC | - | No-Connection (Keep this pin open to avoid damage when it shorts with the VCC pin) |
| 16, 17, 19, 22, 24, 25 | NC | - | No-Connection |
| - | EXP-PAD | Ground | Connect central EXP-PAD to GND The central EXP-PAD and the corner EXP-PADs are shorted inside the package |

Block Diagram



Function Description

Detailed Description for Pin Function

CLK (Clock Input Pin for Micro Step)

The electrical angle changes by one step for each rising edge of input clock pulse.

The effect is also the same when '1' is written to CLKP in the Control Register.

Noise introduced to the CLK pin can cause missteps in motor. Design the PCB layout so that noise will not affect the CLK input easily.

MODE0, MODE1 (Motor Excitation Mode Selection Pin)

These pins set the motor excitation mode. The motor excitation mode can also be set through SM[2:0] in the Control Register.

The setting change of excitation mode is forcibly reflected regardless of the clock pulse input to the CLK pin. Refer to [P17 Switching of Motor Excitation Mode](#).

In case SM[2:0] is not used (SM[2:0] = '000'):

| MODE1 | MODE0 | Excitation Mode |
|-------|-------|-----------------|
| L | L | Full step |
| L | H | 1/2 step |
| H | L | 1/8 step |
| H | H | 1/16 step |

In case the MODE1 and MODE0 pins are not used (MODE1 = L and MODE0 = L):

| SM2 | SM1 | SM0 | Excitation Mode |
|-----|-----|-----|-----------------|
| 0 | 0 | 0 | Full step |
| 0 | 0 | 1 | 1/2 step |
| 0 | 1 | 0 | 1/8 step |
| 0 | 1 | 1 | 1/16 step |
| 1 | 0 | 0 | Full step |
| 1 | 0 | 1 | 1/2 step |
| 1 | 1 | 0 | 1/4 step |
| 1 | 1 | 1 | 1/32 step |

In case both SM[2:0] and the MODE1, MODE0 pins are used:

| SM2 | MODE1 xor SM1 | MODE0 xor SM0 | Excitation Mode |
|-----|---------------|---------------|-----------------|
| 0 | 0 | 0 | Full step |
| 0 | 0 | 1 | 1/2 step |
| 0 | 1 | 0 | 1/8 step |
| 0 | 1 | 1 | 1/16 step |
| 1 | 0 | 0 | Full step |
| 1 | 0 | 1 | 1/2 step |
| 1 | 1 | 0 | 1/4 step |
| 1 | 1 | 1 | 1/32 step |

Detailed description for Pin function – continued

CWB (Motor Rotation Direction Selection Pin)

This pin sets the direction of the motor rotation. Changes in the CWB pin settings are reflected at the rising edge of the following clock pulse input to the CLK pin(Refer to [P16 Switching of CWB](#)).

The effect of the CWB pin is inverted when CWBP is '1' in the Control Register.

| CWBP | CWB | Rotation Direction |
|------|-----|--|
| 0 | L | Clockwise The phase of CH1 current output is advanced by 90° from the phase of CH2 current output. |
| 0 | H | Counter Clockwise The phase of CH1 current output is delayed by 90° from the phase of CH2 current output. |
| 1 | L | Counter Clockwise The phase of CH1 current output is delayed by 90° from the phase of CH2 current output. |
| 1 | H | Clockwise The phase of CH1 current output is advanced by 90° from the phase of CH2 current output. |

RHB (Drive/Hold Mode Selection Pin)

This pin selects modes from a drive mode where the IC drives output / a hold mode where the IC holds an electrical angle. In the hold mode, the input clock pulse to the CLK pin is ignored and the micro stepping behavior in the internal translator circuit is stopped. The logic of the RHB pin is inverted when RHBP register is '1'. Refer to a table below for each setting.

If MCU changes the motor excitation mode setting (the level of the MODE0 pin and the MODE1 pin and the value of SM[2:0] register) during the hold mode, the actual excitation mode switches after changing from the hold mode to the drive mode.

| RHBP | RHB | Mode |
|------|-----|------------|
| 0 | L | Hold mode |
| 0 | H | Drive mode |
| 1 | L | Drive mode |
| 1 | H | Hold mode |

PSB (Power Save Pin)

This pin puts the IC in standby state and sets the motor output to open state. In standby state, the translator circuit is RESET and the electrical angle is initialized.

When PSB = L→H, there is a delay of up to 40 μs before returning from standby state to normal state, so be sure to switch each input at least 40 μs after switching PSB. Refer to [P15 Reset Operation](#).

| PSB | Motor Output State |
|-----|-----------------------|
| L | Standby State (RESET) |
| H | ACTIVE |

The initial electrical angle of each excitation mode after RESET is as follows. (Refer to [P18 Step Sequence](#))

| Excitation mode | Initial electrical angle |
|-----------------|--------------------------|
| Full step | 45° |
| 1/2 step | 45° |
| 1/4 step | 45° |
| 1/8 step | 45° |
| 1/16 step | 45° |
| 1/32 step | 45° |

Detailed description for Pin function – continued**VCC (Power Supply Pin)**

Since the motor driving current flows into the VCC pin, design the PCB layout with low impedance by making the trace for the VCC pin thick and short. VCC voltage has large fluctuations due to back electromotive force of the motor, PWM switching noise etc. In order to stabilize VCC voltage level, place the bypass capacitors (ranged from 100 μF to 470 μF) as close as possible to the VCC pin.

Larger capacitors are necessary especially when the application needs larger current or when the motor has large back electromotive force. In addition, we recommend placing multilayer ceramic capacitors (ranged from 0.01 μF to 0.1 μF) in parallel to the bypass capacitor. The purpose is to decrease the impedance of the power supply in a wide frequency bandwidth.

Higher VCC voltage level than the rating is prohibited even for a moment.

Make sure to short all VCC pins on the PCB layout though they are shorted inside IC. When these are not shorted, malfunction or destruction may occur because of current flow concentration.

Each power supply pin has a built-in clamper for preventing electrostatic damage. When a steep pulse signal or voltage, such as a surge exceeding the absolute maximum rating is applied to power supply pins, the clammers are actuated and destroyed. Therefore, do not exceed the absolute maximum rating. It is also recommended to attach a Zener diode that matches the absolute maximum rating.

Between the VCC pins and the GND pins, diodes are inserted for preventing electrostatic damage. Note that the IC will be destroyed if reversed voltage is applied between them.

GND (Ground Pin)

In order to reduce the noise caused by switching current and to stabilize the internal reference voltage of IC, design the PCB layout to make the wiring impedance from these pins as low as possible to achieve the lowest electrical potential in any operating conditions. Design the PCB layout so that it does not have common impedance with other GND patterns.

OUT1A, OUT1B, OUT2A, OUT2B (H-Bridge Output Pin)

Since the motor driving current flows into these pins, design the PCB layout with low impedance by making the trace for the output pin thick and short. It is recommended to add Schottky diodes in case that the output voltage swings largely between positive and negative side in an application with large current, and in case that the back electromotive voltage level is large. Each output pin has a built-in clamper for preventing electrostatic damage. When a steep pulse signal or voltage, such as a surge exceeding the absolute maximum rating is applied to the power supply pins, the clammers are actuated and destroyed. Therefore, do not exceed the absolute maximum rating.

RREF (Output Current Level Setting Pin)

This pin is used to set output current level. The maximum output current value can be set by current-setting resistor (RREF resistor).

$$I_{OUT} = 5.87 \times (R_{RREF})^{-0.919} \quad [A]$$

Where:

I_{OUT} is the Maximum Output Current

R_{RREF} is the RREF Resistor [kΩ]. 6.2 kΩ to 43 kΩ.

If the RREF pin is open, the output current is set to 700 mA. The minimum current that can be controlled by the RREF resistor, will depend on L/R value of the motor coil and the minimum ON time of PWM Drive.

Detailed description for Pin function – continued

CR (Chopping Frequency Setting Pin)

This pin is to set the output chopping frequency. Connect an external capacitance (470 pF to 3,300 pF) and resistor (6.8 kΩ to 200 kΩ) to GND.

Refer to 3) CR Timer in [P10 PWM Constant Current control](#) for setting method of the chopping frequency.

In PCB, ensure that GND line from the external components has no common impedance with other GND patterns. Also ensure that it is far from wires with steep pulses like square waves, etc. to prevent noise.

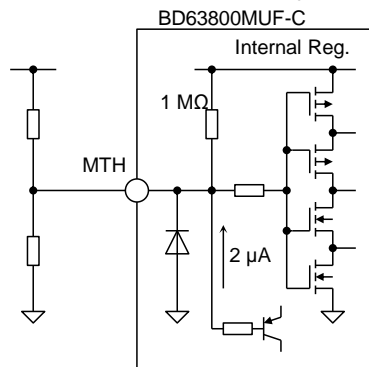
Both of capacitance and resistance must be attached when PWM constant current control is used. The control doesn't work correctly if the external voltage is applied to the CR pin.

MTH (Current Damping Method Setting Pin)

This pin is for setting the current decay method. It can be selected by changing the input voltage level.

| Input voltage in the MTH pin | Current Decay Method |
|------------------------------|----------------------|
| 0.0 V to 0.3 V | Slow Decay |
| 0.4 V to 1.0 V | Mix Decay |
| 1.5 V to 2.0 V | Fast Decay |
| 2.5 V or more, or open | Auto Decay |

In case of using slow decay mode, connect MTH to GND. If MTH voltage is generated by a voltage divider composed of resistors, select the resistance value in taking the outflow current (Max 2 μA) and the internal pull-up resistor (1 MΩ) into consideration. Refer to [P13 Current Decay Mode](#) for each current decay method.

**NC Pins**

These are no connection pins. They are not connected electrically to the internal circuit of IC.

IC Backside Metal

VQFN32FBV050 package has a metal for heat dissipation on the back of the IC. Since the heat is supposed to be dissipated through this metal, the metal must be connected to GND plane on substrate with soldering and GND pattern as large as possible must be used for the sufficient heat dissipation area.

In addition, the backside metal is shorted to the back of the IC chip. So the backside metal is at GND potential. If it is shorted to a potential other than GND potential, malfunction and destruction will occur. Don't route signals other than GND potential at the back-side of the IC

Function Description – continued

PWM Constant Current control

1) Current Control Operation

The output current increases when the output transistor is turned on. When the current reaches the level set by RREF resistor and DAC in IC, the current limit comparator operates, then the IC enters current decay mode. After a wait period set by CR timer, the output transistor turns on again. This sequence repeats continuously.

2) Noise Canceling Function

To avoid misdetection of current-sense comparator caused by spike noise generated when the output turns ON, the IC has a minimum ON time t_{ONMIN} (Blank time). The current detection is invalid for the minimum ON time after the output transistor is turned on.

3) CR Timer

The CR pin is repeatedly charged and discharged between the VCRH and VCRL levels through the external capacitor and resistor.

The detection of the current-sense comparator is disabled while charging from VCRL level to VCRH level.

This charging period is the minimum ON Time: t_{ONMIN} .

After CR level reaches VCRH, CR starts discharging. During this discharge period, IC enters current decay mode when the output current reaches the target current level.

When CR is discharged to VCRL level, IC recovers to output ON mode from current decay mode. At the same time, IC starts charging again.

CR charging time: the minimum ON Time t_{ONMIN} and CR discharge time $t_{DISCHARGE}$ are determined by the following formula (Typ) with external capacitor (C) and resistor (R). The sum of two parameters is the chopping cycle time t_{CHOP} .

$$t_{ONMIN} \approx C \times \frac{R \times R'}{R + R'} \times \ln \left(\frac{VCR - 0.4}{VCR - 1.0} \right) \quad [s]$$

$$t_{DISCHARGE} \approx C \times R \times \ln \left(\frac{1 + \alpha}{0.4} \right) \quad [s]$$

$$t_{CHOP} \approx t_{ONMIN} + t_{DISCHARGE} \quad [s]$$

Where:

- R is the external resistor in the CR pin
- C is the external capacitor in the CR pin
- V is the internal regulator output voltage. 5 V (Typ)
- R' is the internal impedance in the CR pin. 5 kΩ (Typ)
- α is referred to the chart to the right

$$VCR = \frac{R}{R + R'} \times V$$

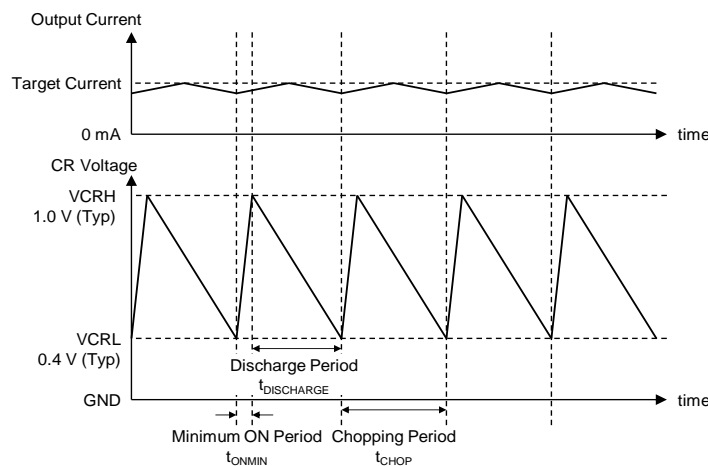
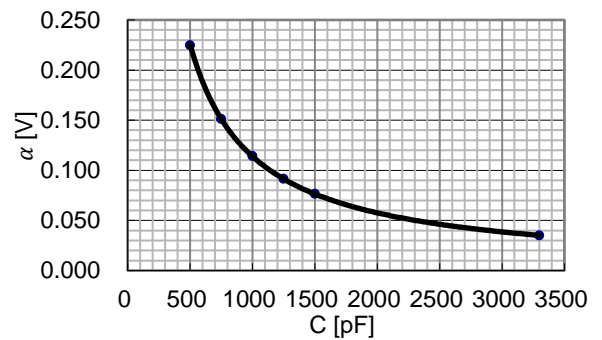


Figure 1. Timing Chart of CR Voltage and Output Current

Use 6.8 kΩ or more for the resistor in the CR pin since CR level doesn't reach VCRH level(1.0V(Typ)) with lower resistor values. (6.8 kΩ to 200 kΩ is recommended).

For the capacitor in the CR pin, the minimum ON time: t_{ONMIN} will become long by the capacitance value of over several thousand pF. So note that output current may exceed the target current level depending on L and R values of the motor coils (470 pF to 3,300 pF is recommended as the capacitance value).

Note that a very long chopping cycle time: t_{CHOP} causes larger ripple in output current, smaller average output current and lower rotation efficiency. Select the optimum value of the resistor and the capacitor for the CR pin to minimize motor sound and distortion of output current waveform.

If the minimum ON time t_{ONMIN} is shortened (slew rate is slowed down), chopping may occur at a current value lower than the set current value due to interference between motor output transistors. To deal with this, either insert a Schottky diode between OUT and GND, or refer to the graph below to determine the minimum on time (set the minimum on time longer than the curve in the graph). When calculating C and R, which determine the minimum ON time t_{ONMIN} , use the internal regulator voltage V of 5 V (Typ) and the CR pin internal impedance R' of 5 k Ω (Typ). The likelihood of the above phenomenon occurring differs depending on the motor, so please be sure to check the actual motor.

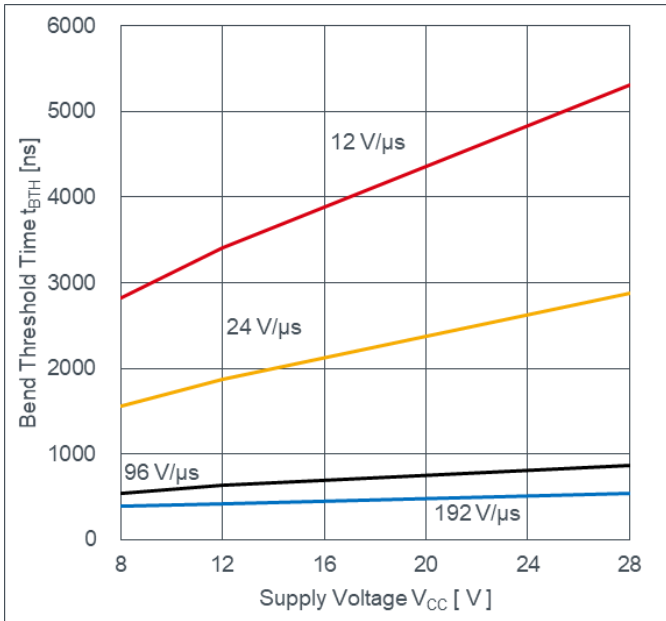


Figure 2. Supply voltage, Bend threshold time (-40 °C)

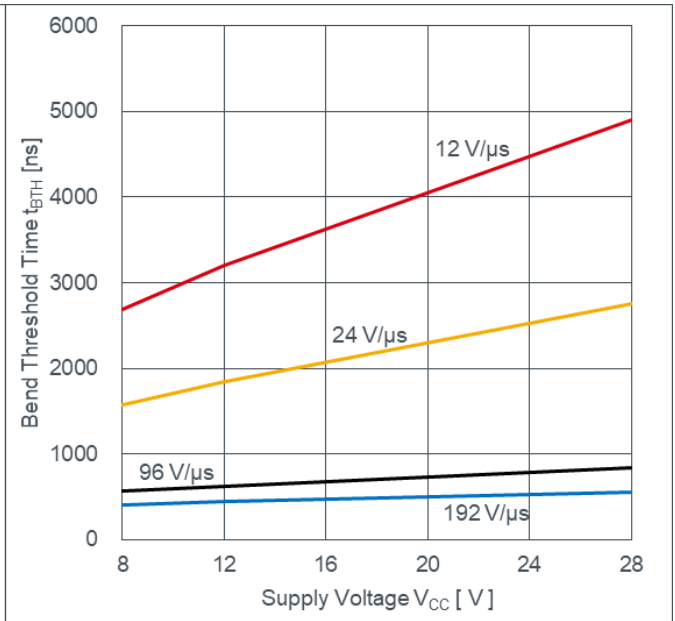


Figure 3. Supply voltage, Bend threshold time (25 °C)

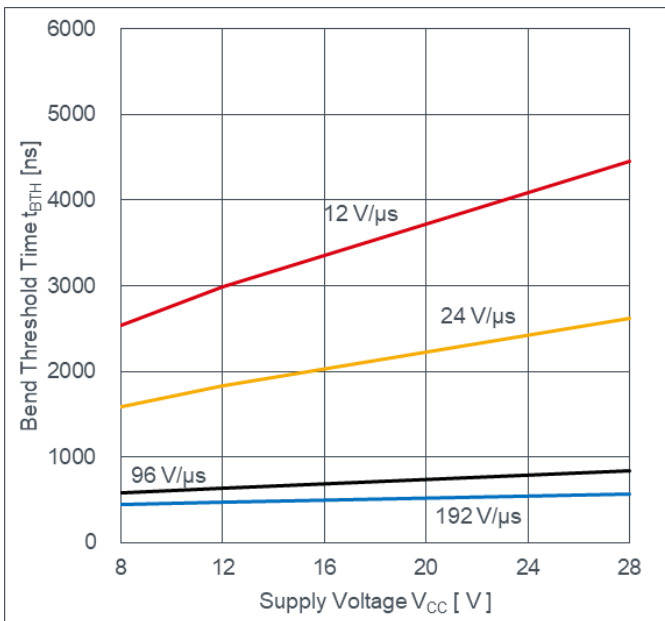


Figure 4. Supply voltage, Bend threshold time (125 °C)

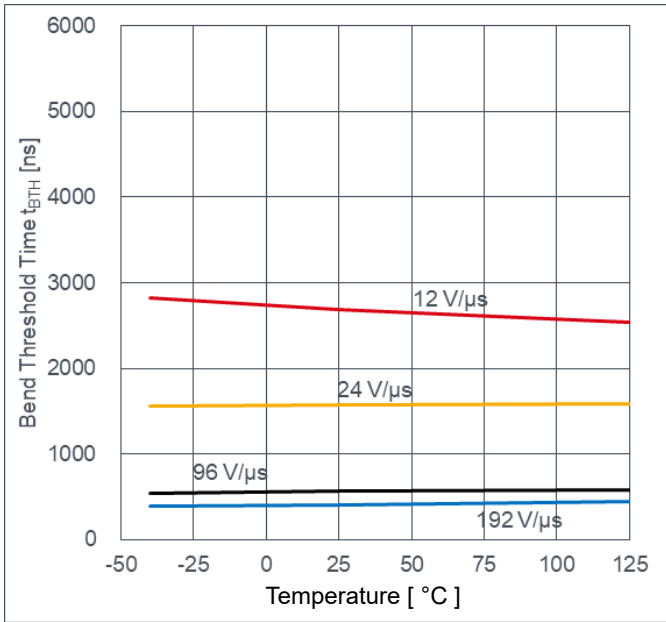


Figure 5. Temperature, Bend threshold time (V_{CC}: 8 V)

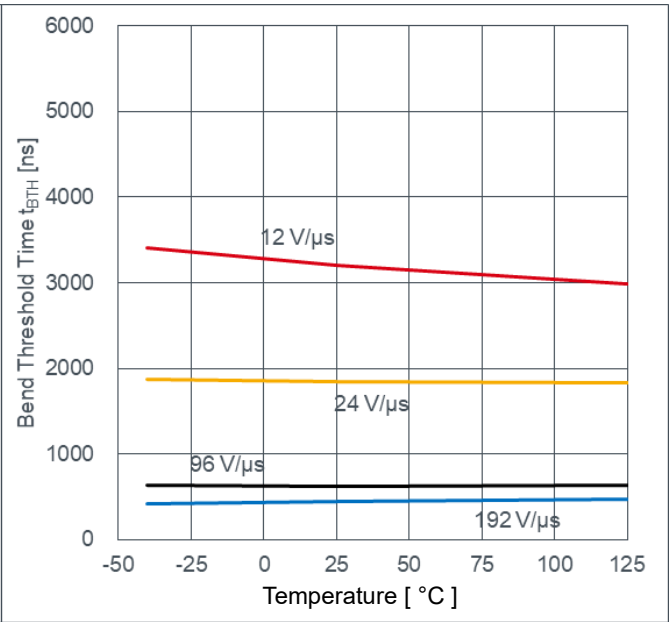


Figure 6. Temperature, Bend threshold time (V_{CC}: 12 V)

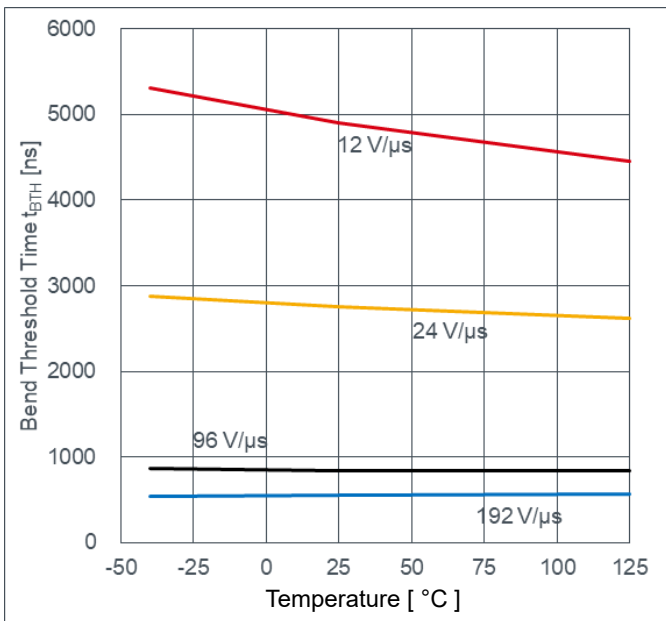


Figure 7. Temperature, Bend threshold time (V_{CC}: 28 V)

PWM Constant Current control - continued

Current Decay Mode

BD63800MUF-C PWM realizes a PWM Constant Current Control with two kinds of decay state (Fast Decay/Slow Decay). The following diagrams show the states of output transistors and paths of the motor regenerative current during current decay period in each decay mode.

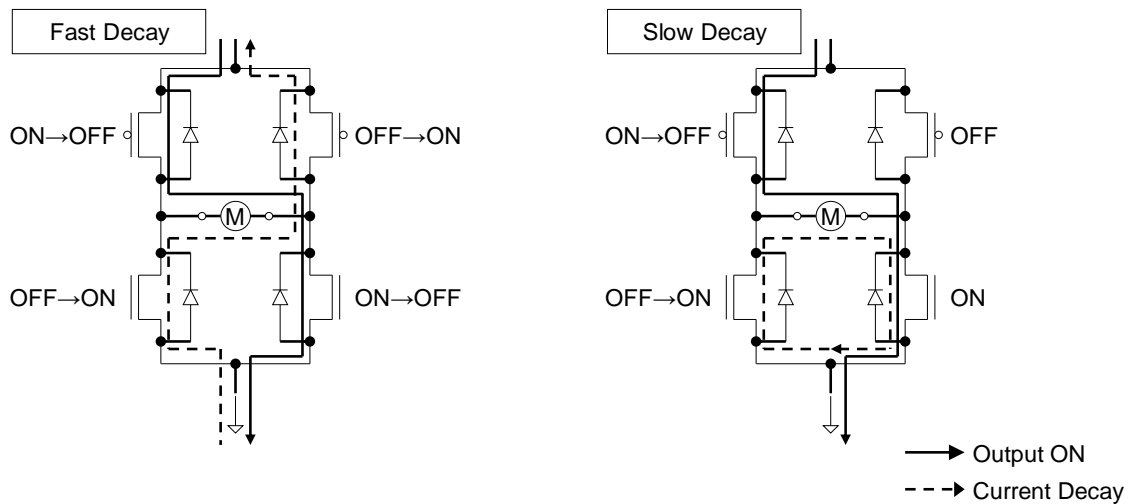


Figure 8. Paths of Regenerated Current during Current Decay

BD63800MUF-C implements 4 decay mode of combination of these decay states in order to realize optimized operation for motor characteristics, excitation mode and pulse rate.

The features of each decay mode are as follows:

Slow Decay Mode

During current decay period, regenerative current decreases slowly because of smaller voltage between both ends of a motor coil. It makes ripple on output current smaller and torque of motor higher.

However, (1) in the lower operating current condition, the output current increases because of lower controllability of current. And (2) in using 1/2 step to 1/32 step with high-pulse-rate driving, the current waveform cannot follow the change of the current target due to the influence of motor back electromotive voltage. As the result, the distortion and motor vibration are increased.

Thus, this decay mode is suitable for Full step mode or low-pulse-rate driven 1/2 step to 1/32 step modes.

Fast Decay Mode

The regeneration current is decreased quickly, so distortion of the output current waveform is reduced even in the high-pulse-rate driving condition.

However, the average current is reduced by large ripple of output current. It causes (1) Motor torque reduction (This issue can be solved by larger current limit setting though the rated output current must be satisfied) and (2) Heat Generation caused by motor power loss.

If these points can be allowed, fast decay is stable for high-pulse rate 1/2 step to 1/32 step modes.

PWM Constant Current control - continued

Mix Decay Mode

The mix decay mode can improve issues caused in both of slow and fast decay mode. It can improve current controllability without increasing the current ripple by switching slow and fast decay states during current decay period. In addition, the time ratio of slow decay and fast decay can be adjusted by the voltage applied to the MTH pin. So it can provide the optimal control state for any kind of motors. In decay state, period from t1 to t2 of the discharge section of the CR pin in the chopping cycle t_{CHOP} is the slow decay, and the remaining interval from t2 to t3 is the fast decay. If the current doesn't reach the target value during the period from t1 to t2, the slow decay is skipped and only fast decay is applied.

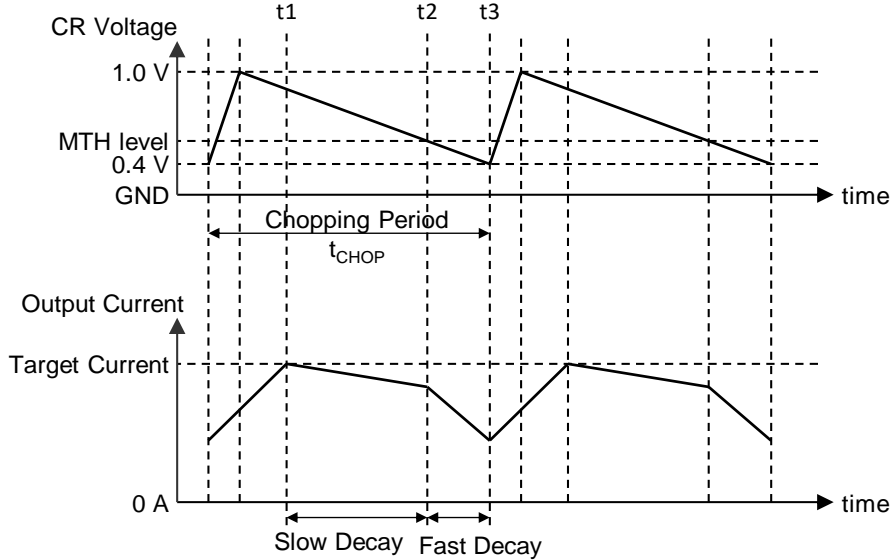


Figure 9. CR Pin Voltage and Output Current during Mix Decay

Auto Decay Mode

In the auto decay mode automatically select fast decay and slow decay during decay state according to the difference between the target current and the output current. It causes small current ripple and quick following for the change of target current. For example, when target current drops and the output current is excess the target current, Fast decay is selected as current decay mode.

Current waveform in Auto decay is shown below.

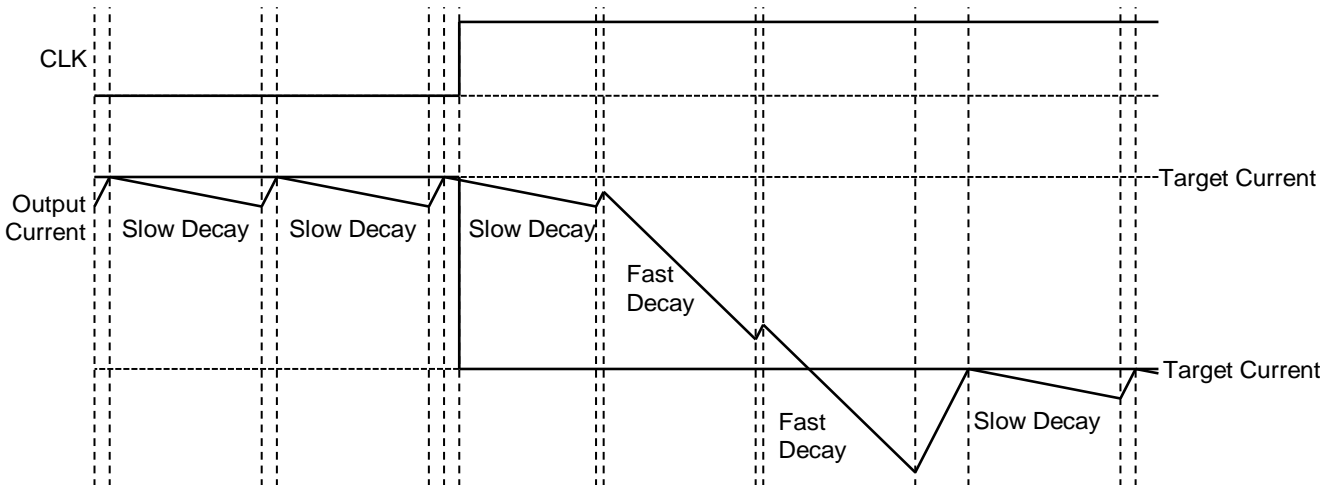


Figure 10. Current Decay by Auto Decay in Reducing Target Current

Function Description – continued

Translator Circuit Operation

This IC has a built-in translator circuit and can drive stepping motors by CLK-IN mode and SPI command. The operation of the translator circuit in CLK-IN drive mode is described below.

Reset Operation

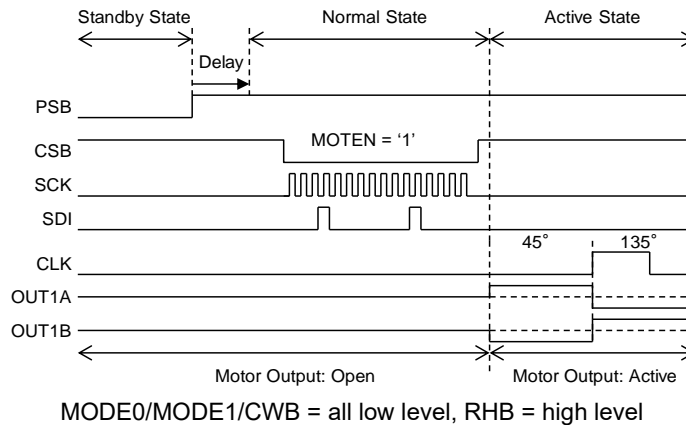
The translator circuit is initialized by power ON reset function and the PSB pin.

Initializing sequence when power supply is turned on

(1) Power-on in PSB = L (Recommended)

When power supply is turned on, the internal power-on reset function initializes IC. During PSB = L, IC is in standby state and the motor output keeps open state. After PSB = Low to High, IC enters normal state and it can accept SPI command. In this state, by setting '1' to MOTEN in the control register CR1 by SPI, IC enters active state and the motor output becomes active and the excitation starts in the initial electrical angle.

When PSB = L→H, there is a delay of up to 40 μs before returning from standby state to normal state, so be sure to switch each input at least 40 μs after switching PSB.

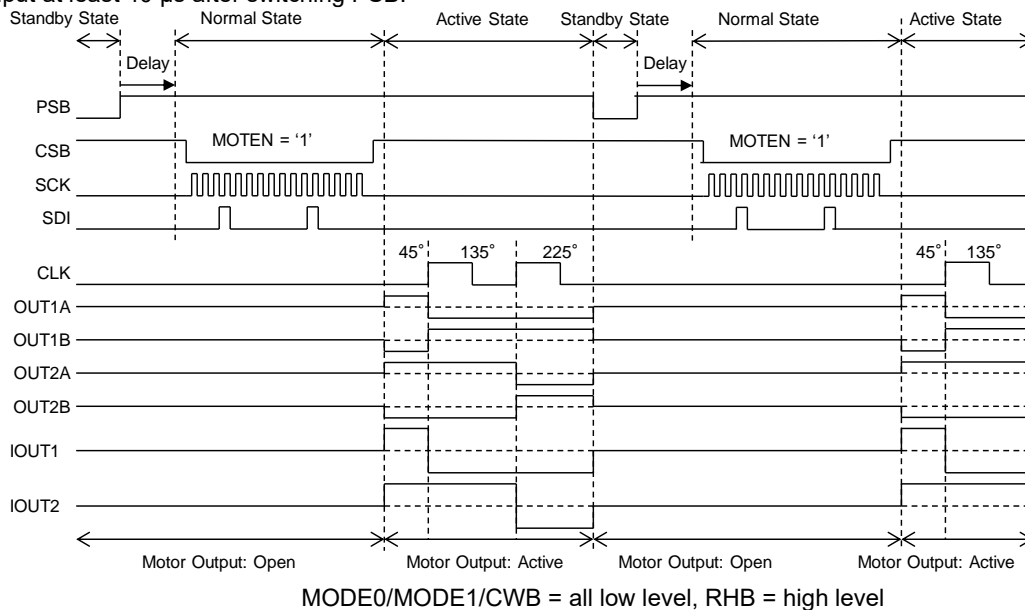


(2) Power-on in PSB = H

When power supply is turned on, the Power-on reset function in IC operates and the IC is initialized. Then, by setting '1' to MOTEN in the control register CR1 by SPI, IC enters active state and the motor output becomes active and the excitation starts in the initial electrical angle. However, there is a possibility that IC is not initialized normally if VCC rises up rapidly because of no Power-on reset operation. In that case, set PSB level to ground level once after VCC rises up. (Refer to [P40 Power-on Sequence](#) and [P16 Control Input Timing](#))

Initialization sequence during motor operation

Input a reset signal to the PSB pin to initialize translator circuit during motor operation. IC is reset only by the PSB pin regardless of the other input signals. After reset, IC internal circuit enters the normal state and makes the motor output open. When PSB = L→H, there is a delay of up to 40 μs before returning from standby state to normal state, so be sure to switch each input at least 40 μs after switching PSB.



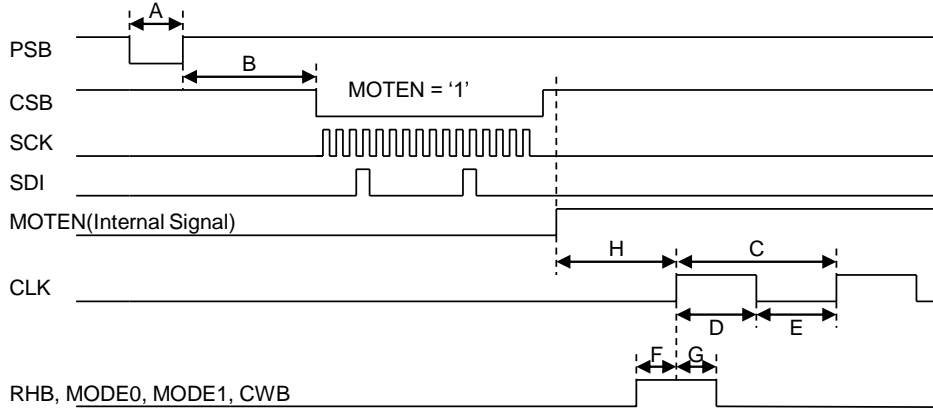
Translator Circuit Operation - continued

Control Input Timing

The translator circuit operates at the rising edge of the CLK signal. The input timing shown below must be satisfied.

Note that there is a risk that the translator circuit will not operate as expected if input timing is violated.

Also, when PSB = L→H, there is a delay of up to 40 μs (section B) before returning from standby state to normal state, so input the SPI command at least 40 μs after switching the PSB.

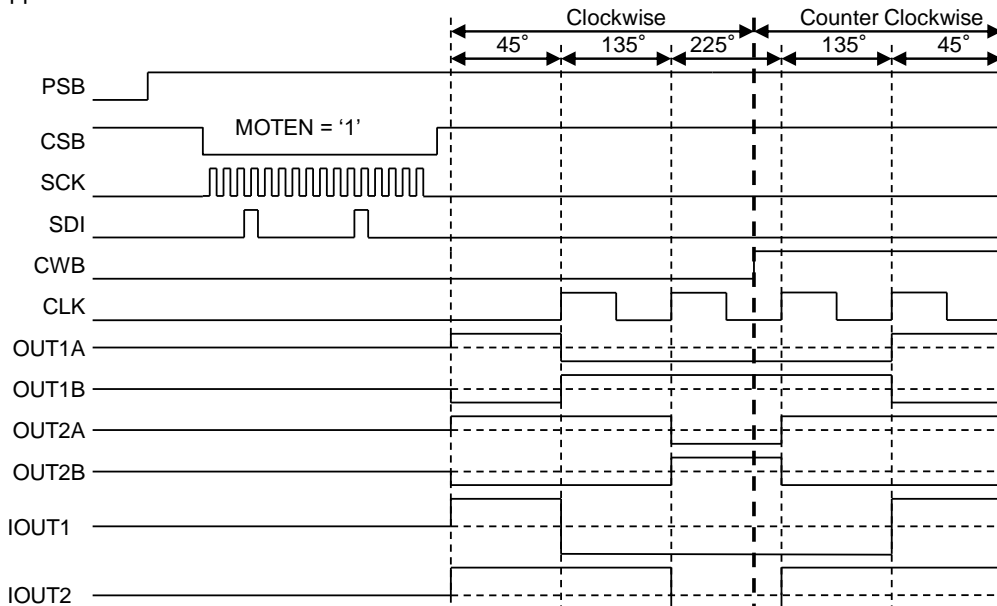


| Symbol | Item | Required Time |
|--------|---|---------------|
| A | Low pulse width of PSB | 20 μs (Min) |
| B | Period from PSB rising edge to SPI command input start time | 40 μs (Max) |
| C | Cycle time of CLK | 4 μs (Min) |
| D | High pulse width of CLK | 2 μs (Min) |
| E | Low pulse width of CLK | 2 μs (Min) |
| F | Set-up time of RHB, MODE0, MODE1, CWB for CLK | 1 μs (Min) |
| G | Hold time of RHB, MODE0, MODE1, CWB for CLK | 1 μs (Min) |
| H | Setup time of MOTEN for CLK | 1 μs (Min) |

Switching of CWB

The switch in CWB is reflected at the next rising edge of CLK after CWB is changed.

However, depending on the motor status at CWB switching, there are possibilities of step-out or misstep in motor when the motor cannot follow the input even if the control input for driver IC is valid. Therefore, the transition sequence must be evaluated with application condition well.



MODE0/MODE1 = all low level, RHB = high level

Translator Circuit Operation - continued

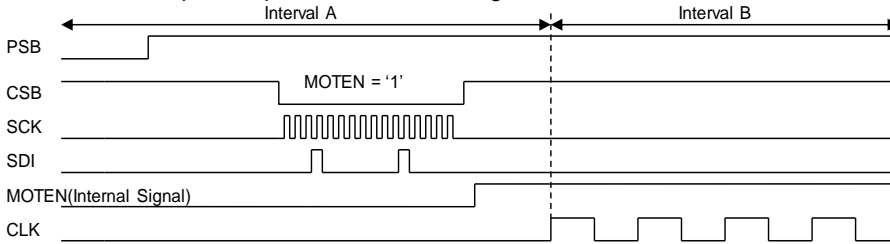
Switching of Motor Excitation Mode

The excitation mode is switched at the timing of changing MODE0, MODE1 level regardless of CLK signal.

This product has a function which can prevent motor out-of-step caused by discrepancies of torque vector between transition excitations. However, depending on the motor status at MODE0 and MODE1 switching, there are possibilities of step-out or misstep in motor when the motor cannot follow the input even if the control input for driver IC is valid. Therefore, evaluate the switching sequence of excitation mode fully.

Cautions on Simultaneous Switching of CWB and Excitation Mode (MODE0, MODE1)

Interval A is defined as the period from reset (PSB = L to H) to the 1st CLK pulse input and Interval B is defined as the period after the 1st CLK pulse input as shown in the figure below.



| | |
|------------|--|
| Interval A | There is no constraint in switching CWB and the excitation mode. |
| Interval B | During one CLK cycle or MOTEN = L, simultaneous switching of CWB and excitation mode should be avoided. If this is violated, it is possible to have misstep of motor (extra one more step) and out-of-step in motor. |

Therefore, when switching CWB and excitation mode simultaneously, reset first the IC by setting PSB = L → H. Then set CWB and excitation mode during interval A.

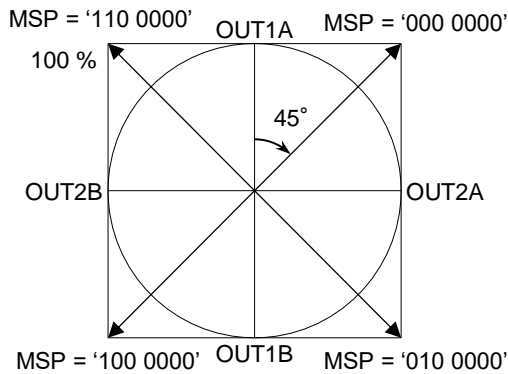
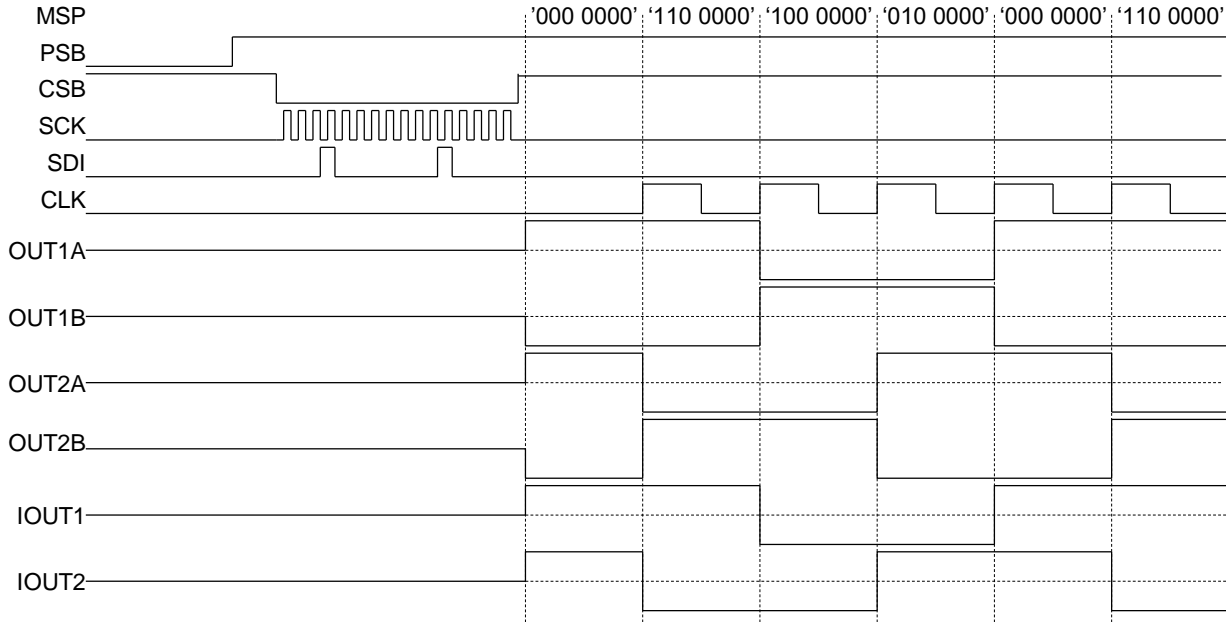
Translator Circuit Operation – continued

Step Sequence

In motor stepping, Micro-step Position (MSP), IOUT current ratio and electric angle of each step are decided depending on the excitation mode. The initial excited position is 45° in all excitation modes. It is not possible to change the excitation position (MSP[6:0]) inside the IC without moving the motor (without flowing output current).

Step Sequence in Full Step Mode

Timing chart, MSP, IOUT current ratio and the electric angle for Full step mode are shown in the figure below.
 ({SM2, MODE1 xor SM1, MODE0 xor SM0} = '100' or '000', CWB = High)



Step Sequence - continued

Step Sequence in 1/2, 1/4, 1/8, 1/16 and 1/32 Step Modes

MSP, IOUT current ratio and the electric angle for 1/2, 1/4, 1/8, 1/16 and 1/32 step of each excitation mode are shown in the figure below. (CWB = L)

| MSP[6:0] | Step Mode {SM2, MODE1 xor SM1, MODE0 xor SM0} | | | | | % of I _{max} | | Step angle [°] |
|----------|--|------|-----|-----|-----------|-----------------------|--------|-------------------|
| | 111 | 011 | 010 | 110 | 101 / 001 | Coil 1 | Coil 2 | |
| | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | | | |
| 111 0000 | 112 | 56 | 28 | 14 | 7 | 100.0 | 0.0 | 0.0 |
| 111 0001 | 113 | | | | | 99.9 | 4.9 | 2.8 |
| 111 0010 | 114 | 57 | | | | 99.5 | 9.8 | 5.6 |
| 111 0011 | 115 | | | | | 98.9 | 14.7 | 8.5 |
| 111 0100 | 116 | 58 | 29 | | | 98.1 | 19.5 | 11.2 |
| 111 0101 | 117 | | | | | 97.0 | 24.3 | 14.1 |
| 111 0110 | 118 | 59 | | | | 95.7 | 29.0 | 16.9 |
| 111 0111 | 119 | | | | | 94.2 | 33.7 | 19.7 |
| 111 1000 | 120 | 60 | 30 | 15 | | 92.4 | 38.3 | 22.5 |
| 111 1001 | 121 | | | | | 90.4 | 42.8 | 25.3 |
| 111 1010 | 122 | 61 | | | | 88.2 | 47.1 | 28.1 |
| 111 1011 | 123 | | | | | 85.8 | 51.4 | 30.9 |
| 111 1100 | 124 | 62 | 31 | | | 83.1 | 55.6 | 33.8 |
| 111 1101 | 125 | | | | | 80.3 | 59.6 | 36.6 |
| 111 1110 | 126 | 63 | | | | 77.3 | 63.4 | 39.4 |
| 111 1111 | 127 | | | | | 74.1 | 67.2 | 42.2 |
| 000 0000 | 0 | 0 | 0 | 0 | 0 | 70.7 | 70.7 | 45.0 |
| 000 0001 | 1 | | | | | 67.2 | 74.1 | 47.8 |
| 000 0010 | 2 | 1 | | | | 63.4 | 77.3 | 50.6 |
| 000 0011 | 3 | | | | | 59.6 | 80.3 | 53.4 |
| 000 0100 | 4 | 2 | 1 | | | 55.6 | 83.1 | 56.2 |
| 000 0101 | 5 | | | | | 51.4 | 85.8 | 59.1 |
| 000 0110 | 6 | 3 | | | | 47.1 | 88.2 | 61.9 |
| 000 0111 | 7 | | | | | 42.8 | 90.4 | 64.7 |
| 000 1000 | 8 | 4 | 2 | 1 | | 38.3 | 92.4 | 67.5 |
| 000 1001 | 9 | | | | | 33.7 | 94.2 | 70.3 |
| 000 1010 | 10 | 5 | | | | 29.0 | 95.7 | 73.1 |
| 000 1011 | 11 | | | | | 24.3 | 97.0 | 75.9 |
| 000 1100 | 12 | 6 | 3 | | | 19.5 | 98.1 | 78.8 |
| 000 1101 | 13 | | | | | 14.7 | 98.9 | 81.5 |
| 000 1110 | 14 | 7 | | | | 9.8 | 99.5 | 84.4 |
| 000 1111 | 15 | | | | | 4.9 | 99.9 | 87.2 |

Step Sequence in 1/2, 1/4, 1/8, 1/16 and 1/32 Step Modes – continued

| MSP[6:0] | Step Mode {SM2, MODE1 xor SM1, MODE0 xor SM0} | | | | | % of I _{max} | | Step angle [°] |
|----------|--|------|-----|-----|-----------|-----------------------|--------|-------------------|
| | 111 | 011 | 010 | 110 | 101 / 001 | Coil 1 | Coil 2 | |
| | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | | | |
| 001 0000 | 16 | 8 | 4 | 2 | 1 | 0.0 | 100.0 | 90.0 |
| 001 0001 | 17 | | | | | -4.9 | 99.9 | 92.8 |
| 001 0010 | 18 | 9 | | | | -9.8 | 99.5 | 95.6 |
| 001 0011 | 19 | | | | | -14.7 | 98.9 | 98.5 |
| 001 0100 | 20 | 10 | 5 | | | -19.5 | 98.1 | 101.2 |
| 001 0101 | 21 | | | | | -24.3 | 97.0 | 104.1 |
| 001 0110 | 22 | 11 | | | | -29.0 | 95.7 | 106.9 |
| 001 0111 | 23 | | | | | -33.7 | 94.2 | 109.7 |
| 001 1000 | 24 | 12 | 6 | 3 | | -38.3 | 92.4 | 112.5 |
| 001 1001 | 25 | | | | | -42.8 | 90.4 | 115.3 |
| 001 1010 | 26 | 13 | | | | -47.1 | 88.2 | 118.1 |
| 001 1011 | 27 | | | | | -51.4 | 85.8 | 120.9 |
| 001 1100 | 28 | 14 | 7 | | | -55.6 | 83.1 | 123.8 |
| 001 1101 | 29 | | | | | -59.6 | 80.3 | 126.6 |
| 001 1110 | 30 | 15 | | | | -63.4 | 77.3 | 129.4 |
| 001 1111 | 31 | | | | | -67.2 | 74.1 | 132.2 |
| 010 0000 | 32 | 16 | 8 | 4 | 2 | -70.7 | 70.7 | 135.0 |
| 010 0001 | 33 | | | | | -74.1 | 67.2 | 137.8 |
| 010 0010 | 34 | 17 | | | | -77.3 | 63.4 | 140.6 |
| 010 0011 | 35 | | | | | -80.3 | 59.6 | 143.4 |
| 010 0100 | 36 | 18 | 9 | | | -83.1 | 55.6 | 146.2 |
| 010 0101 | 37 | | | | | -85.8 | 51.4 | 149.1 |
| 010 0110 | 38 | 19 | | | | -88.2 | 47.1 | 151.9 |
| 010 0111 | 39 | | | | | -90.4 | 42.8 | 154.7 |
| 010 1000 | 40 | 20 | 10 | 5 | | -92.4 | 38.3 | 157.5 |
| 010 1001 | 41 | | | | | -94.2 | 33.7 | 160.3 |
| 010 1010 | 42 | 21 | | | | -95.7 | 29.0 | 163.1 |
| 010 1011 | 43 | | | | | -97.0 | 24.3 | 165.9 |
| 010 1100 | 44 | 22 | 11 | | | -98.1 | 19.5 | 168.8 |
| 010 1101 | 45 | | | | | -98.9 | 14.7 | 171.5 |
| 010 1110 | 46 | 23 | | | | -99.5 | 9.8 | 174.4 |
| 010 1111 | 47 | | | | | -99.9 | 4.9 | 177.2 |

Step Sequence in 1/2, 1/4, 1/8, 1/16 and 1/32 step Modes – continued

| MSP[6:0] | Step Mode {SM2, MODE1 xor SM1, MODE0 xor SM0} | | | | | % of I _{max} | | Step angle [°] |
|----------|--|------|-----|-----|-----------|-----------------------|--------|-------------------|
| | 111 | 011 | 010 | 110 | 101 / 001 | Coil 1 | Coil 2 | |
| | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | | | |
| 011 0000 | 48 | 24 | 12 | 6 | 3 | -100.0 | 0.0 | 180.0 |
| 011 0001 | 49 | | | | | -99.9 | -4.9 | 182.8 |
| 011 0010 | 50 | 25 | | | | -99.5 | -9.8 | 185.6 |
| 011 0011 | 51 | | | | | -98.9 | -14.7 | 188.5 |
| 011 0100 | 52 | 26 | 13 | | | -98.1 | -19.5 | 191.2 |
| 011 0101 | 53 | | | | | -97.0 | -24.3 | 194.1 |
| 011 0110 | 54 | 27 | | | | -95.7 | -29.0 | 196.9 |
| 011 0111 | 55 | | | | | -94.2 | -33.7 | 199.7 |
| 011 1000 | 56 | 28 | 14 | 7 | | -92.4 | -38.3 | 202.5 |
| 011 1001 | 57 | | | | | -90.4 | -42.8 | 205.3 |
| 011 1010 | 58 | 29 | | | | -88.2 | -47.1 | 208.1 |
| 011 1011 | 59 | | | | | -85.8 | -51.4 | 210.9 |
| 011 1100 | 60 | 30 | 15 | | | -83.1 | -55.6 | 213.8 |
| 011 1101 | 61 | | | | | -80.3 | -59.6 | 216.6 |
| 011 1110 | 62 | 31 | | | | -77.3 | -63.4 | 219.4 |
| 011 1111 | 63 | | | | | -74.1 | -67.2 | 222.2 |
| 100 0000 | 64 | 32 | 16 | 8 | 4 | -70.7 | -70.7 | 225.0 |
| 100 0001 | 65 | | | | | -67.2 | -74.1 | 227.8 |
| 100 0010 | 66 | 33 | | | | -63.4 | -77.3 | 230.6 |
| 100 0011 | 67 | | | | | -59.6 | -80.3 | 233.4 |
| 100 0100 | 68 | 34 | 17 | | | -55.6 | -83.1 | 236.2 |
| 100 0101 | 69 | | | | | -51.4 | -85.8 | 239.1 |
| 100 0110 | 70 | 35 | | | | -47.1 | -88.2 | 241.9 |
| 100 0111 | 71 | | | | | -42.8 | -90.4 | 244.7 |
| 100 1000 | 72 | 36 | 18 | 9 | | -38.3 | -92.4 | 247.5 |
| 100 1001 | 73 | | | | | -33.7 | -94.2 | 250.3 |
| 100 1010 | 74 | 37 | | | | -29.0 | -95.7 | 253.1 |
| 100 1011 | 75 | | | | | -24.3 | -97.0 | 255.9 |
| 100 1100 | 76 | 38 | 19 | | | -19.5 | -98.1 | 258.8 |
| 100 1101 | 77 | | | | | -14.7 | -98.9 | 261.5 |
| 100 1110 | 78 | 39 | | | | -9.8 | -99.5 | 264.4 |
| 100 1111 | 79 | | | | | -4.9 | -99.9 | 267.2 |

Step Sequence in 1/2, 1/4, 1/8, 1/16 and 1/32 step Modes – continued

| MSP[6:0] | Step Mode {SM2, MODE1 xor SM1, MODE0 xor SM0} | | | | | % of I _{max} | | Step angle [°] |
|----------|--|------|-----|-----|-----------|-----------------------|--------|-------------------|
| | 111 | 011 | 010 | 110 | 101 / 001 | Coil 1 | Coil 2 | |
| | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | | | |
| 101 0000 | 80 | 40 | 20 | 10 | 5 | 0.0 | -100.0 | 270.0 |
| 101 0001 | 81 | | | | | 4.9 | -99.9 | 272.8 |
| 101 0010 | 82 | 41 | | | | 9.8 | -99.5 | 275.6 |
| 101 0011 | 83 | | | | | 14.7 | -98.9 | 278.5 |
| 101 0100 | 84 | 42 | 21 | | | 19.5 | -98.1 | 281.2 |
| 101 0101 | 85 | | | | | 24.3 | -97.0 | 284.1 |
| 101 0110 | 86 | 43 | | | | 29.0 | -95.7 | 286.9 |
| 101 0111 | 87 | | | | | 33.7 | -94.2 | 289.7 |
| 101 1000 | 88 | 44 | 22 | 11 | | 38.3 | -92.4 | 292.5 |
| 101 1001 | 89 | | | | | 42.8 | -90.4 | 295.3 |
| 101 1010 | 90 | 45 | | | | 47.1 | -88.2 | 298.1 |
| 101 1011 | 91 | | | | | 51.4 | -85.8 | 300.9 |
| 101 1100 | 92 | 46 | 23 | | | 55.6 | -83.1 | 303.8 |
| 101 1101 | 93 | | | | | 59.6 | -80.3 | 306.6 |
| 101 1110 | 94 | 47 | | | | 63.4 | -77.3 | 309.4 |
| 101 1111 | 95 | | | | | 67.2 | -74.1 | 312.2 |
| 110 0000 | 96 | 48 | 24 | 12 | 6 | 70.7 | -70.7 | 315.0 |
| 110 0001 | 97 | | | | | 74.1 | -67.2 | 317.8 |
| 110 0010 | 98 | 49 | | | | 77.3 | -63.4 | 320.6 |
| 110 0011 | 99 | | | | | 80.3 | -59.6 | 323.4 |
| 110 0100 | 100 | 50 | 25 | | | 83.1 | -55.6 | 326.2 |
| 110 0101 | 101 | | | | | 85.8 | -51.4 | 329.1 |
| 110 0110 | 102 | 51 | | | | 88.2 | -47.1 | 331.9 |
| 110 0111 | 103 | | | | | 90.4 | -42.8 | 334.7 |
| 110 1000 | 104 | 52 | 26 | 13 | | 92.4 | -38.3 | 337.5 |
| 110 1001 | 105 | | | | | 94.2 | -33.7 | 340.3 |
| 110 1010 | 106 | 53 | | | | 95.7 | -29.0 | 343.1 |
| 110 1011 | 107 | | | | | 97.0 | -24.3 | 345.9 |
| 110 1100 | 108 | 54 | 27 | | | 98.1 | -19.5 | 348.8 |
| 110 1101 | 109 | | | | | 98.9 | -14.7 | 351.5 |
| 110 1110 | 110 | 55 | | | | 99.5 | -9.8 | 354.4 |
| 110 1111 | 111 | | | | | 99.9 | -4.9 | 357.2 |

Function Description – continued

Drive Mode and Hold Mode

The IC has a drive mode and a hold mode and the peak current for each mode can be set by SPI.

The drive mode = Not (hold mode) and this mode is determined by exclusive OR of the RHB pin and RHBP register.

The peak current in drive mode is determined by IRUN[3:0] register, and the peak current in hold mode is determined by IHOLD[3:0] register. The percentage of peak current for each register value is shown below

| IRUN[3:0] | Peak Motor Current IRUN [%] | IHOLD[3:0] | Peak Motor Current IHOLD [%] |
|-----------|-----------------------------|------------|------------------------------|
| 0000 | 9.1 | 0000 | 0.0 <i>(Note 1)</i> |
| 0001 | 10.1 | 0001 | 9.1 |
| 0010 | 11.6 | 0010 | 10.1 |
| 0011 | 13.0 | 0011 | 11.6 |
| 0100 | 15.1 | 0100 | 13.0 |
| 0101 | 17.4 | 0101 | 15.1 |
| 0110 | 20.3 | 0110 | 17.4 |
| 0111 | 24.0 | 0111 | 20.3 |
| 1000 | 30.4 | 1000 | 24.0 |
| 1001 | 36.1 | 1001 | 30.4 |
| 1010 | 42.9 | 1010 | 36.1 |
| 1011 | 50.0 | 1011 | 42.9 |
| 1100 | 59.5 | 1100 | 50.0 |
| 1101 | 70.8 | 1101 | 59.5 |
| 1110 | 83.9 | 1110 | 70.8 |
| 1111 | 100.0 | 1111 | 83.9 |

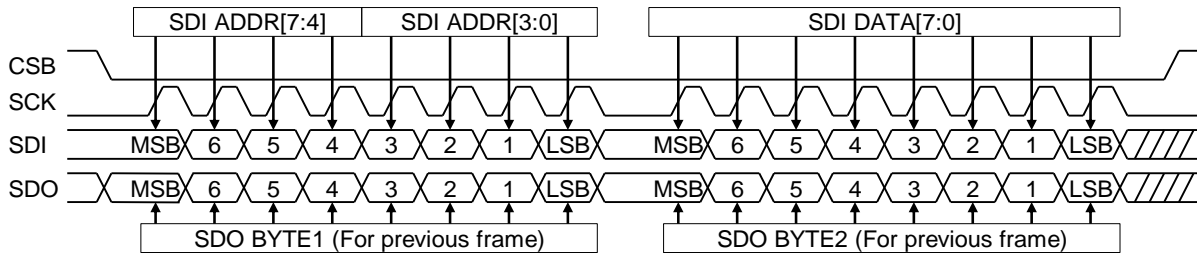
(Note 1) Open detection is disabled under this condition.

Function Description – continued

SPI Interface

This IC supports Serial Peripheral Interface (SPI) to set parameter into IC and to read out status data from IC.

SPI frame structure is as follows,



The SPI transfer data length is 16 bits.

When CSB is 'L', the SPI is active and IC latches SDI data at the rising of SCK.

During CSB is 'L', the frame data is stored at every multiples of 16 SCK pulses.

The frame data is not latched internally if the number of SCK pulses is less than 16 after CSB becomes 'L' or after latching frame data.

The structure of SPI address, data input and data output is described below,

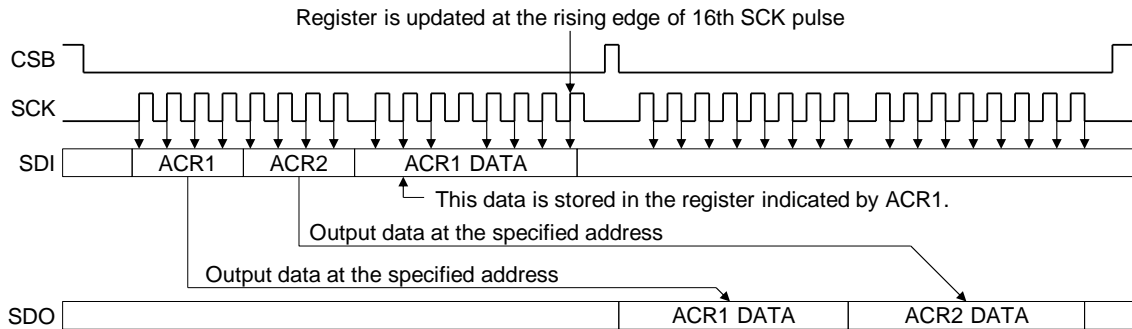
| SDI ADDR[7:4] | SDI ADDR[3:0] | SDI DATA[7:0] | SDO BYTE1 | SDO BYTE2 | Comment on Use |
|---------------|---------------|---------------|-----------|-----------|---|
| ACR1 | ACR2 | SDICR1 | SDOCR1 | SDOCR2 | Control Register CR1 Data Input Data Output of CR1 and CR2 |
| ACR1 | ASR1 | SDICR1 | SDOCR1 | SDOSR1 | Control Register CR1 Data Input Data Output of CR1 and SR1 |
| ACR1 | NOP | SDICR1 | SDOCR1 | 00h | Control Register CR1 Data Input Data Output of CR1 |
| ASR1 | ACR1 | XXh | SDOSR1 | SDOCR1 | Data Output of SR1 and CR1 |
| ASR1 | ASR2 | XXh | SDOSR1 | SDOSR2 | Data Output of SR1 and SR2 |
| ASR1 | NOP | XXh | SDOSR1 | 00h | Data Output of SR1 |
| NOP | ACR1 | XXh | 00h | SDOCR1 | Data Output of CR1 |
| NOP | ASR2 | XXh | 00h | SDOSR2 | Data Output of SR2 |
| NOP | NOP | XXh | 00h | 00h | Dummy/Placeholder |

- ACR1, ACR2 : Control Register Address. Refer to [P32 Control Register](#).
- ASR1, ASR2 : Status Register Address. Refer to [P36 Status Register](#).
- SDICR1 : Control Register Data Input
- SDOCR_x, SDOSR_x : Data Output (x = 1, 2)
- NOP : Register Address outside the range
- XXh : Any Value

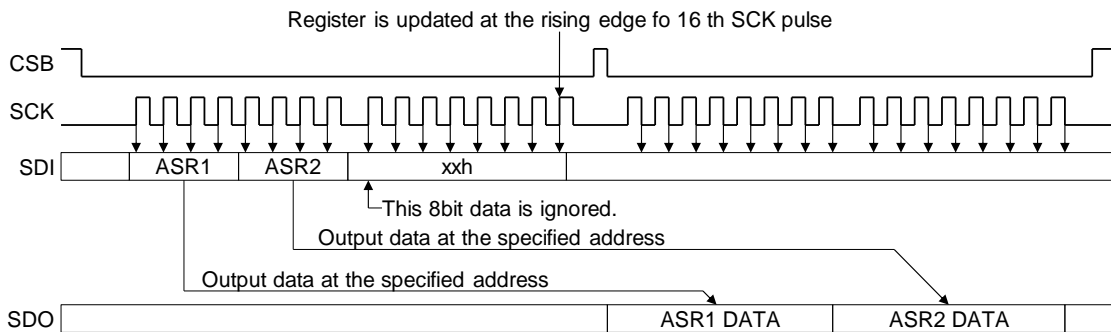
SPI Interface - continued

Examples of SPI Input / Output Sequence

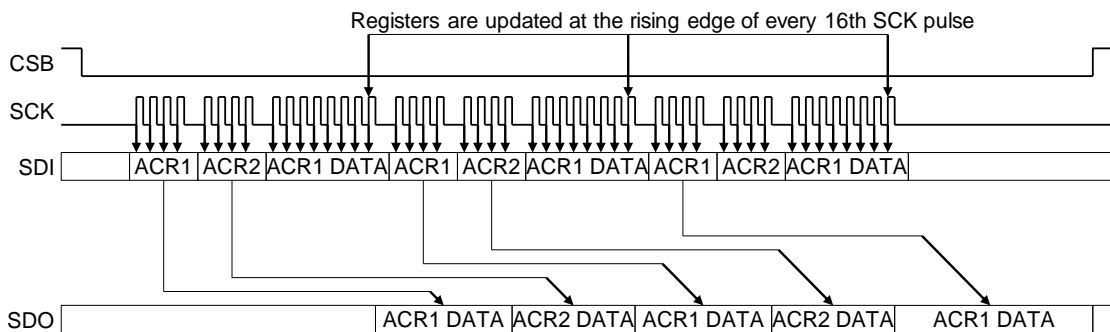
In writing data to Control Register, the addresses are specified by the first 4 bits, and the data in the last 8bits is stored. Output data is output in 16 bit of the next frame from SDO. The data corresponding to the address indicated in the first 4 bits is output in the first 8 bits of the next frame. The data corresponding to the address indicated in the next 4 bits is output in the last 8 bits of the next frame.



In reading data from Status Register, the address is indicated in the first 4 bits and the next 4 bits. It is not necessary to input values to the last 8 bits. Output data is output in 16 bit of the next frame from SDO. The data corresponding to the address indicated in the first 4 bits is output in the first 8 bits of the next frame. And the data corresponding to the address indicated in the next 4 bits is output in the last 8 bits of the next frame.



This IC supports a burst transfer. MCU can write data to registers continuously by inputting data in multiple of 16 to SCK and SDI with CSB = 'L'.

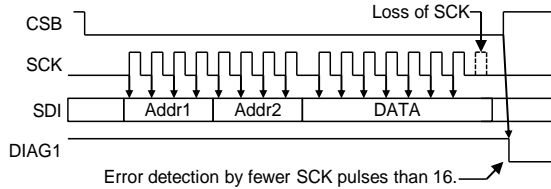


SPI Interface - continued

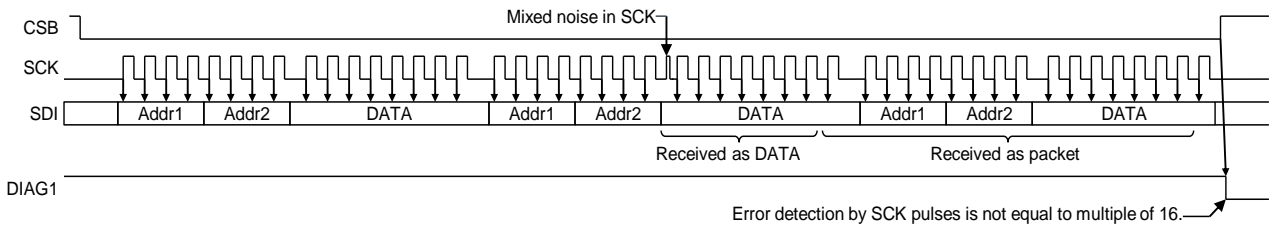
SPI Bit Count Error Detection

This IC supports SPI error check function. Then IC counts the SCK pulses during CSB = L and checks the count at the rising edge of CSB. If the count is not a multiple of 16, SPI bit count error is detected.
(If there are no SCK pulses during CSB = L, any SPI bit count errors are not detected because of no effect for register access.)

In case of single packet transfer



In case of burst transfer



Multi IC connection example

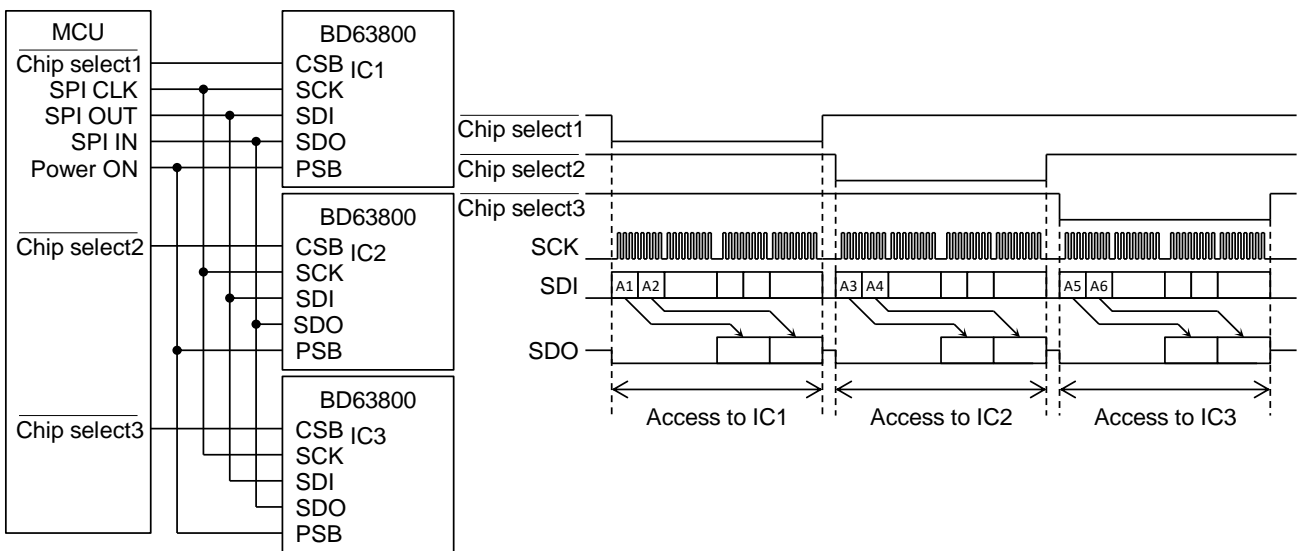


Figure 11. Example of Multi IC Connection

The Figure 11 shows the connection diagram and the access timing chart where three ICs are connected in parallel. The pins SCK, SDI, SDO can be shorted to each other. The MCU can select the specific IC to write to Control Register and to read from Status Register by controlling each CSB pin. The SDO pin is CMOS type. But it switches to HiZ state during CSB = H. Therefore, the MCU can read data from specific IC even if all SDOs are shorted. If the MCU send command two or more ICs at the same time, each IC may output different levels. Note that large current flows in the SDO pin in that case. Also, the MCU input from SDO becomes HiZ when CSB pins of all ICs are set to 'H'. Ensure that there is enough time of CSB = H so that each IC's output does not overlap. (Refer to $t_{BCSBSDO1}$, $t_{BCSBSDO2}$ in SPI timing table in [P43 Electrical Characteristics](#))

Function Description – continued

Protection/Detection Functions

Malfunction Prevention Function w/o Power Supply (Ghost Supply Prevention Function)

This function prevents IC malfunction when there is no power supplied to the IC and a control signal^(Note 1) is input to the IC. The voltage supplied to the power supply of this IC or other IC in the system is shorted through the electrostatic destruction prevention diode from these input pins to the VCC. Therefore, there is no malfunction of the circuit even when voltage is supplied to these input pins while there is no power supply.

(Note 1) control signal: Logic signals, MTH, RREF

Thermal Shutdown Function (TSD)

This IC has a built-in Thermal Shutdown circuit for protection against overheating. If the chip temperature of the IC is above +175 °C (Typ), the motor output will become open. It will automatically return to normal operation when the temperature goes below +150 °C (Typ). However, even when TSD is in operation, if heat is continuously applied externally, it will result in thermal runaway and can lead to destruction of the IC.

Thermal Warning Function (TW)

This IC has a built-in temperature warning circuit to detect overheating. When the chip temperature of the IC is above the level set by SPI, a temperature warning is output to the SDO and DIAG1/DIAG2 pins. The warning is cleared when temperature goes down under the level set by SPI. Unlike Thermal Shutdown Function (TSD), IC keeps the motor control operation even in Thermal Warning Function.

| TWThr[3:0] | TW Threshold Level ON/OFF [°C] (Typ) | | |
|------------|--------------------------------------|---|-------|
| 0000 | 65.7 | / | 33.8 |
| 0001 | 71.4 | / | 39.8 |
| 0010 | 77.1 | / | 45.9 |
| 0011 | 82.8 | / | 51.9 |
| 0100 | 88.4 | / | 58.0 |
| 0101 | 94.1 | / | 64.0 |
| 0110 | 99.8 | / | 70.1 |
| 0111 | 105.4 | / | 76.1 |
| 1000 | 111.1 | / | 82.2 |
| 1001 | 116.8 | / | 88.2 |
| 1010 | 122.4 | / | 94.2 |
| 1011 | 128.1 | / | 100.3 |
| 1100 | 133.8 | / | 106.3 |
| 1101 | 139.5 | / | 112.4 |
| 1110 | 145.1 | / | 118.4 |
| 1111 | 150.8 | / | 124.5 |

Over Current Protection Function (OCP)

This IC has a built-in over current protection circuit as a countermeasure against destruction when the motor outputs are shorted to each other, to VCC or to GND. This circuit latches the motor output to open state when the current is above the specified level (reference value: 3 A in 25 °C, Typ) for 4 μs (Typ). The IC can only recover by power-on again or reset by the PSB pin.

The overcurrent protection circuit is designed to prevent the breakdown of IC caused by overcurrent in abnormal conditions such as shorted motor outputs. This protection is not intended to guarantee the protection of application circuit. Therefore, do not design the protection of the system using this circuit function. After detecting over current, then power-on again or recovery by reset while IC is still in abnormal state, the OCP operates repeatedly ('latch → recover → latch'). Note that the IC may generate heat and may lead to deterioration of the IC.

If the L value of the wiring is large, such as when the wiring during a shorted circuit to each other, to VCC or to GND is long, there is a possibility of destruction of the IC after the over current has flowed and the output pin voltage suddenly jumps to a value that is over the absolute maximum ratings.

If the current is below the OCP detection current level and above the output current rating level, the IC can heat up, exceed $T_{jmax} = 150\text{ °C}$ and then deteriorate, so current which exceeds the output rating should not be applied.

Over Voltage Lock-out Function (OVLO)

This IC has a built-in over voltage lock-out circuit to protect the IC output and the motor during power supply over voltage. When the applied voltage to the VCC pin goes up to 32 V (Typ) or more, the motor output is set to OPEN. To prevent false operation by noise, etc., the switching voltage has a 1 V (Typ) hysteresis and there is a 4 μs (Typ) mask time for the detection time

Although the overvoltage lock out circuit is built-in, there is a possibility of destruction if the absolute maximum value for power supply voltage is exceeded. Avoid to exceed the absolute maximum rating. Note that this circuit does not operate during power save state.

Protection/Detection Functions – continued

Under Voltage Lock-out (UVLO) / Under Voltage Motor Hold Function

This IC has a built-in under voltage lock-out circuit to prevent malfunction of IC output caused by low level power supply to IC. When the VCC pin is lower than the level set by SPI, IC set the motor output to open. Under voltage motor hold mode can also be selected. In this mode, when IC detects low level of power supply, IC keeps motor hold although the detected results are output to DIAG1/DIAG2 and Status Register.

These modes can be selected by setting UVM3 to UVM0 in the control register.

| UVM3 | UVM2 | UVM1 | UVM0 | Mode | Operation |
|--------|------|------|------|------------|--|
| 0 | 0 | 0 | 0 | Protection | Motor output: Open during low voltage in VCC |
| 1 | 1 | 0 | 1 | Hold | Motor output: Hold during low voltage in VCC |
| Others | | | | Prohibited | _(Note 1) |

(Note 1) In this mode, IC keeps the operation. But there is a possibility that the following status occurs. If each of protection/hold is set to UVM3 to UVM0, SDO output normally.

- SDO output unexpected logical value.
- Protection/Detection function are turned off.

This switching voltage has hysteresis to prevent false operation by noise etc. Note that this circuit does not operate during power save mode.

| UVThr[3:0] | UV Threshold Level ON/OFF [V] (Typ) |
|------------|-------------------------------------|
| 0000 | 3.92 / 4.53 |
| 0001 | 4.29 / 4.96 |
| 0010 | 4.67 / 5.39 |
| 0011 | 5.04 / 5.82 |
| 0100 | 5.41 / 6.24 |
| 0101 | 5.78 / 6.67 |
| 0110 | 6.15 / 7.10 |
| 0111 | 6.52 / 7.53 |
| 1000 | 6.89 / 7.96 |
| 1001 | 7.26 / 8.39 |
| 1010 | 7.64 / 8.82 |
| 1011 | 8.01 / 9.24 |
| 1100 | 8.38 / 9.67 |
| 1101 | 8.75 / 10.10 |
| 1110 | 9.12 / 10.53 |
| 1111 | 9.49 / 10.96 |

Open Detection Function

This IC has a built-in open detection function. When an open state is detected, the reception of advanced CLK is stopped and the excitation position is not changed until the open state is resolved. Open status is determined by whether or not the H-bridge output is chopping. It outputs open detection result to the SDO and DIAG1/DIAG2 pins when any of H-bridge output pins (OUT1A, OUT1B, OUT2A, and OUT2B) become open. The open detection is asserted when the open(chopping not working) status keeps over 5.12 ms (Typ). The open detection is not asserted in the following conditions because an internal timer counting the open period will be stopped. If the open state continues after recovering from the following conditions, the timer starts to count-up again and the open detection will be asserted.

- (1) In detection of TSD, OCP, UVLO^(Note 1), OVLO
 - (2) In Hold mode with IHOLD = '0000'
 - (3) When Electric angle is 0°/180° (Stopping detection Only in OUT2 side), 90°/270° (Stopping detection Only in OUT1 side)
- (Note 1) The open detection is available when under voltage motor hold mode is selected.

In case of fast motor rotation without chopping operation, the open status is detected even if the outputs are not open.

Protection/Detection Functions – continued

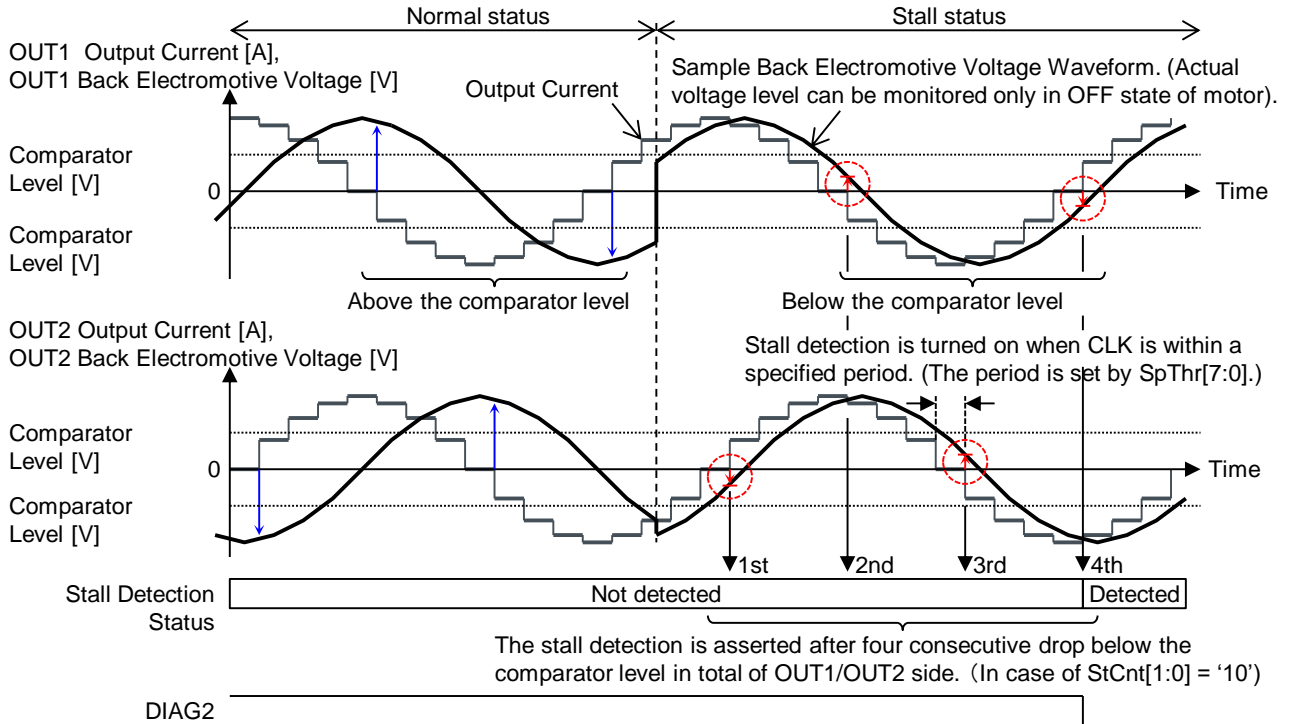
Stall Detection Function

This IC has a built-in stall detection circuit.

Stall is detected by monitoring the back electromotive voltages at zero cross points.

If the back electromotive force to be monitored is significantly affected by the chopping operation of other phases, insert a Schottky diode between the OUT pin and GND.

If the motor gets stalled, the IC outputs the Status register value from the SDO pin by SPI and Stall detection result from the DIAG1/DIAG2 pins.



Comparator Voltage Level: Set StThr[7:0] and BeGain2/BeGain referring to the table below
Unit [V] (all values are typical)

| StThr[7:0] | n | BeGain2/BeGain | | | |
|---------------------|-----|---------------------------|-------------------------|-------------------------|-------------------------|
| | | '0'/'0' | '0'/'1' | '1'/'0' | '1'/'1' |
| 0000 0000 | 0 | Stall detection: Disabled | | | |
| 0000 0001 | 1 | 0.20 | 0.15 | 0.06 | 0.03 |
| 0000 0010 | 2 | 0.39 | 0.29 | 0.12 | 0.06 |
| 0000 0011 | 3 | 0.59 | 0.44 | 0.18 | 0.09 |
| 0000 0100 | 4 | 0.78 | 0.59 | 0.24 | 0.12 |
| : | : | : | : | : | : |
| 1111 1110 | 254 | 49.80 | 37.35 | 14.94 | 7.47 |
| 1111 1111 | 255 | 50.00 | 37.50 | 15.00 | 7.50 |
| Calculation Formula | | $\frac{10}{51} \times n$ | $\frac{5}{34} \times n$ | $\frac{2}{34} \times n$ | $\frac{1}{34} \times n$ |

Comparator Hysteresis: Hysteresis is the share for Comparator Voltage Level. Set StHys[3:0] referring to the table below.

| StHys[3:0] | m | Hysteresis (Typ) |
|---------------------|----|--------------------|
| 0000 | 0 | 4 % |
| 0001 | 1 | 8 % |
| 0010 | 2 | 12 % |
| : | : | : |
| 1110 | 14 | 60 % |
| 1111 | 15 | 64 % |
| Calculation Formula | | $4 \times (m + 1)$ |

Stall Detection Function – continued

CLK-IN period condition where stall detection is enabled: Set SpThr[7:0] referring to the table below. Stall detection is enabled when CLK-IN period is less than or equal to the values in the table.

| SpThr[7:0] | Threshold setting of CLK-IN Period for Stall detection (Typ) |
|------------|--|
| 0000 0000 | Stall detection: Disabled |
| 0000 0001 | 20 μ s |
| 0000 0010 | 40 μ s |
| : | : |
| 1111 1110 | 5,080 μ s |
| 1111 1111 | 5,100 μ s |

Total count of asserting Stall detection: Set StCnt[1:0] referring to the table below. Stall detection is asserted when the back electromotive voltage falls below the comparator level in consecutive certain times indicated in the table below.

| StCnt[1:0] | Total times of stall status for asserting stall detection |
|------------|---|
| 00 | 1 time stall status |
| 01 | 2 times consecutive stall status |
| 10 | 4 times consecutive stall status |
| 11 | 8 times consecutive stall status |

Stall detection is available in 1/2, 1/4, 1/8, 1/16 and 1/32 step modes.

Protection/Detection Functions – continued**DIAG Output Selection Function**

This IC has DIAG output function.

The following detection results are output from the DIAG1/DIAG2 pins.

- (1) Over Current Detection
- (2) Open Detection
- (3) Thermal Warning (TW)
- (4) Thermal Shutdown (TSD)
- (5) Stall Detection
- (6) Under Voltage Detection
- (7) Over Voltage Detection
- (8) SPI Bit Count Error Detection

MCU can freely select detection/protection to output to the DIAG1 and DIAG2 pins by setting Control Register CR5A/CR6A. In the initial state after the IC resets, DIAG1 outputs logical OR of all detection results mentioned above and DIAG2 outputs only stall detection result. Refer to [P35 CR5A \(0x15\) CR6A \(0x16\)](#).

Function Description – continued

Control Register

Control Register Map

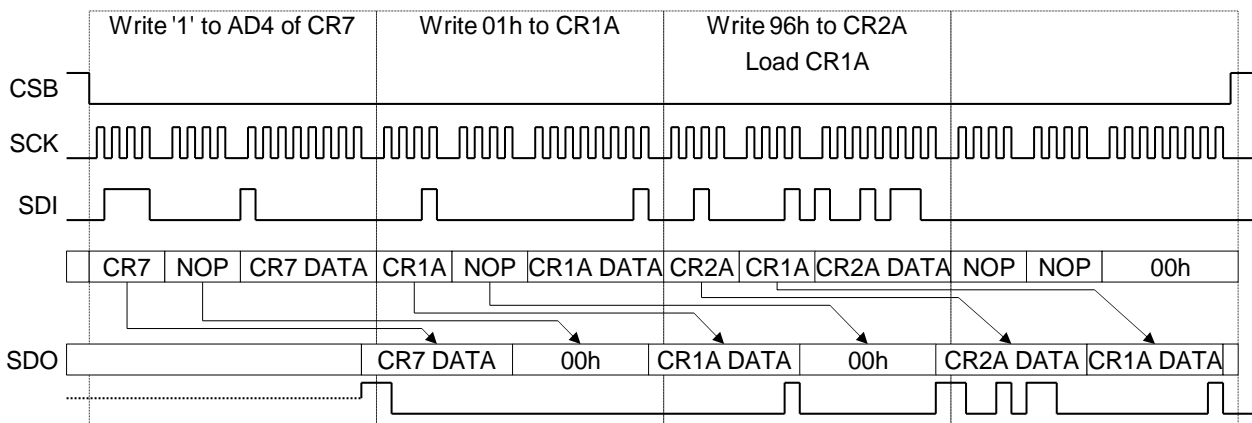
Values in the bottom row are the default value after reset.

The register address is determined by 5 bits, which is the sum of AD4 value of register x7h (CR7) Bit 7 and 4 bits of SPI input.

Specify the address only for x7h (CR7) regardless of the value of AD4. Please note that writing to CR7 is valid regardless of the value of AD4, but reading from CR7 is valid only when AD4 = '0'.

| 5-bit Address | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------------|-----------|---------|------------|-----------|--------|---------|------------|--------|--------|
| AD4 | 4bit | | | | | | | | |
| 0 | 1h (CR1) | CWBP | RHBP | CLKP | MOTEN | StThr7 | StThr6 | StThr5 | StThr4 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 2h (CR2) | IHOLD3 | IHOLD2 | IHOLD1 | IHOLD0 | IRUN3 | IRUN2 | IRUN1 | IRUN0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 3h (CR3) | - | - | EMC1 | EMC0 | UVM3 | SM2 | SM1 | SM0 |
| | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 5h (CR5) | SpThr7 | SpThr6 | SpThr5 | SpThr4 | SpThr3 | SpThr2 | SpThr1 | SpThr0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 6h (CR6) | UVThr3 | UVThr2 | UVThr1 | UVThr0 | - | - | - | - | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 1 | 1h (CR1A) | UVM0 | BeGain2 | StCnt1 | StCnt0 | TwThr3 | TwThr2 | TwThr1 | TwThr0 |
| | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 2h (CR2A) | StHys3 | StHys2 | StHys1 | StHys0 | StThr3 | StThr2 | StThr1 | StThr0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 5h (CR5A) | SelSPI1 | SelSHOR T1 | SelOPEN 1 | SelTW1 | SelTSD1 | SelSTALL 1 | SelUV1 | SelOV1 |
| | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | 6h (CR6A) | SelSPI2 | SelSHORT2 | SelOPEN 2 | SelTW2 | SelTSD2 | SelSTALL 2 | SelUV2 | SelOV2 |
| | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| x | 7h (CR7) | AD4 | BeGain | UVM2 | UVM1 | - | - | - | - |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Example of writing and reading using AD4



Control Register - continued

Definition of each Control Register Bit

CR1 (0x01)

| Symbol | Bit | Description |
|------------|-------|--|
| CWBP | 7 | Motor rotation direction selection. When CWBP = 1, the CWB pin logic is inverted. Refer to P7 CWB (Motor Rotation Direction Selection Pin) |
| RHBP | 6 | Drive/Hold mode selection. When RHBP = 1, the RHB pin logic is inverted. In RHB xor RHBP = 0, Hold mode is selected Refer to P7 RHB (Drive/Hold Mode Selection Pin) |
| CLKP | 5 | CLKIN input. It's recognized as CLKIN input to set '1' to this bit. Internally the value is cleared to '0' automatically after receiving next rising edge of SCK. (Note that the external CLK input is ignored during this period) Refer to P6 CLK (Clock Input Pin for Micro Step) |
| MOTEN | 4 | Enable of H-bridge. Motor driving operation starts after '1' is set to this bit. H-bridge is open after '0' is set to this bit. Refer to P15 Translator Circuit Operation |
| StThr[7:4] | [3:0] | Threshold setting for Stall detection. Stall detection is disabled in StThr[7:0]='0000 0000'. When other values are set, Stall detection is enabled. Refer to P29 Stall Detection Function |

CR2 (0x02)

| Symbol | Bit | Description |
|------------|-------|--|
| IHOLD[3:0] | [7:4] | Current ratio setting for the hold mode. Refer to P23 Drive Mode and Hold Mode |
| IRUN[3:0] | [3:0] | Current ratio setting for the drive mode. Refer to P23 Drive Mode and Hold Mode |

CR3 (0x03)

| Symbol | Bit | Description |
|----------|-------|--|
| EMC[1:0] | [5:4] | Switching slew rate setting for motor driver. '00': 12 V/μs, '01': 24 V/μs, '10': 96 V/μs, '11': 192 V/μs If the slew rate is lowered, the transition of the H-bridge output voltage will be longer than the minimum on-time, and chopping may not occur at the correct current setting value, so be sure to check with the actual device. |
| SM[2:0] | [2:0] | Excitation mode selector. Refer to P6 MODE0, MODE1 (Motor Excitation Mode Selection Pin) . |
| UVM3 | 3 | Selection bit for Protection /Hold mode in Under Voltage state. Refer to P28 Under Voltage Lock-out (UVLO) / Under Voltage Motor Hold Function . |

CR5 (0x05)

| Symbol | Bit | Description |
|------------|-------|--|
| SpThr[7:0] | [7:0] | Threshold setting of stepping speed for Stall detection. 1 step = 20 μs (Typ). Stall detection is enabled when the CLKIN period is smaller than this register. Stall detection is disabled in SpThr[7:0]='0000 0000'. Refer to P29 Stall Detection Function . |

CR6 (0x06)

| Symbol | Bit | Description |
|------------|-------|--|
| UVThr[3:0] | [7:4] | Threshold setting for UVLO Refer to P28 Under Voltage Lock-out (UVLO) / Under Voltage Motor Hold Function . |

Definition of each Control Register Bit – continued

CR7 (0x07)

| Symbol | Bit | Description |
|------------|-------|--|
| AD4 | 7 | Address setting bit. AD4 = '0': Access to following registers is available. CR1, CR2, CR3, CR5, CR6, SR1, SR2, SR3, SR5 and SR6 AD4 = '1': Access to following registers is available. CR1A, CR2A, CR5A, CR6A, SR7A and SR8A Note that writing access to CR7 is available both in AD4 = '0'/'1' but reading access to CR7 is available only in AD4 = '0'. |
| BeGain | 6 | Gain setting for back electromotive voltage for Stall detection. Refer to P29 Stall Detection Function . |
| UVM2, UVM1 | [5:4] | Selection bit for Protection /Hold mode in Under Voltage state. Refer to P28 Under Voltage Lock-out (UVLO) / Under Voltage Motor Hold Function . |

CR1A (0x11)

| Symbol | Bit | Description |
|------------|-------|---|
| UVM0 | 7 | Selection bit for Protection /Hold mode in Under Voltage state. Refer to P28 Under Voltage Lock-out (UVLO) / Under Voltage Motor Hold Function . |
| BeGain2 | 6 | Gain setting for back electromotive voltage for Stall detection. Refer to P29 Stall Detection Function . |
| StCnt[1:0] | [5:4] | Counter setting for Stall detection. Refer to P29 Stall Detection Function . |
| TwThr[3:0] | [3:0] | Threshold setting for Thermal warning Refer to P27 Thermal Warning Function (TW) . |

CR2A (0x12)

| Symbol | Bit | Description |
|------------|-------|--|
| StHys[3:0] | [7:4] | Hysteresis setting for Stall detection. Refer to P29 Stall Detection Function . |
| StThr[3:0] | [3:0] | Threshold setting for Stall detection. Refer to P29 Stall Detection Function . |

Definition of each Control Register Bit – continued

CR5A (0x15)

| Symbol | Bit | Description |
|-----------|-----|--|
| SelSPI1 | 7 | DIAG1 output selector for SPI bit count error detection result '1': the detection result output to DIAG1. Refer to P31 DIAG Output Selection Function . |
| SelSHORT1 | 6 | DIAG1 output selector for Over current protection '1': the detection result output to DIAG1. Refer to P31 DIAG Output Selection Function . |
| SelOPEN1 | 5 | DIAG1 output selector for Open detection result '1': the detection result output to DIAG1. Refer to P31 DIAG Output Selection Function . |
| SelTW1 | 4 | DIAG1 output selector for Thermal warning (TW) '1': the detection result output to DIAG1. Refer to P31 DIAG Output Selection Function . |
| SelTSD1 | 3 | DIAG1 output selector for Thermal shutdown (TSD) '1': the detection result output to DIAG1. Refer to P31 DIAG Output Selection Function . |
| SelSTALL1 | 2 | DIAG1 output selector for Stall detection result '1': the detection result output to DIAG1. Refer to P31 DIAG Output Selection Function . |
| SelUV1 | 1 | DIAG1 output selector for Under voltage detection result '1': the detection result output to DIAG1. Refer to P31 DIAG Output Selection Function . |
| SelOV1 | 0 | DIAG1 output selector for Over voltage detection result '1': the detection result output to DIAG1. Refer to P31 DIAG Output Selection Function . |

CR6A (0x16)

| Symbol | Bit | Description |
|-----------|-----|--|
| SelSPI2 | 7 | DIAG2 output selector for SPI bit count error detection result '1': the detection result output to DIAG2. Refer to P31 DIAG Output Selection Function . |
| SelSHORT2 | 6 | DIAG2 output selector for Over current protection '1': the detection result output to DIAG2. Refer to P31 DIAG Output Selection Function . |
| SelOPEN2 | 5 | DIAG2 output selector for Open detection result '1': the detection result output to DIAG2. Refer to P31 DIAG Output Selection Function . |
| SelTW2 | 4 | DIAG2 output selector for Thermal warning (TW) '1': the detection result output to DIAG2. Refer to P31 DIAG Output Selection Function . |
| SelTSD2 | 3 | DIAG2 output selector for Thermal shutdown (TSD) '1': the detection result output to DIAG2. Refer to P31 DIAG Output Selection Function . |
| SelSTALL2 | 2 | DIAG2 output selector for Stall detection result '1': the detection result output to DIAG2. Refer to P31 DIAG Output Selection Function . |
| SelUV2 | 1 | DIAG2 output selector for Under voltage detection result '1': the detection result output to DIAG2. Refer to P31 DIAG Output Selection Function . |
| SelOV2 | 0 | DIAG2 output selector for Over voltage detection result '1': the detection result output to DIAG2. Refer to P31 DIAG Output Selection Function . |

Function Description – continued

Status Register

Status Register Map

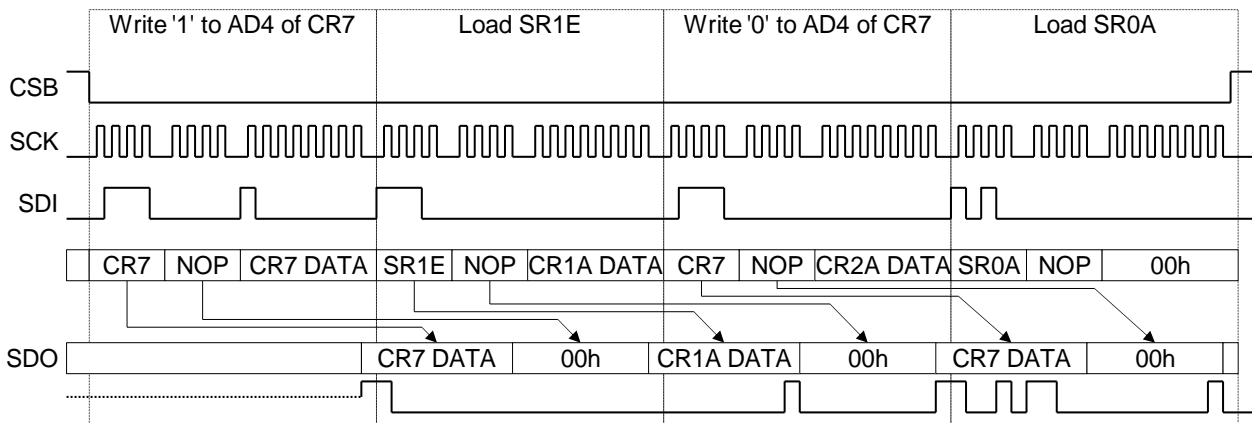
Values in the bottom row are the default value after reset.

The register address is determined by 5 bits, which is the sum of AD4 value of register x7h (CR7) Bit 7 and 4 bits of SPI input.

Specify the address only for x7h (CR7) regardless of the value of AD4. Please note that writing to CR7 is valid regardless of the value of AD4, but reading from CR7 is valid only when AD4 = '0'.

| 5-bit Address | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------------------|-----------------------|------|-------|----------|----------|----------|----------|----------|----------|
| AD4 | 4bit | | | | | | | | |
| 0 | 8h(SR1) Errors1 | PAR | SPI | SHORT | OPEN | TSD | TW | STALL | Reserved |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 9h(SR2) Errors2 | PAR | ORErr | OV | UV | Reserved | Reserved | Reserved | Reserved |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Ah(SR3) Position | PAR | MSP6 | MSP5 | MSP4 | MSP3 | MSP2 | MSP1 | MSP0 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Ch(SR5) Speed | Sp7 | Sp6 | Sp5 | Sp4 | Sp3 | Sp2 | Sp1 | Sp0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Dh(SR6) StepLoss | PAR | SI6 | SI5 | SI4 | SI3 | SI2 | SI1 | SI0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 1 | Eh(SR7A) In&Short1 | PAR | OPEN1 | MODE0pin | MODE1pin | SHRT1AB | SHRT1BB | SHRT1AT | SHRT1BT |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Fh(SR8A) In&Short2 | PAR | OPEN2 | RHBpin | CWBpin | SHRT2AB | SHRT2BB | SHRT2AT | SHRT2BT |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Example of writing and reading using AD4



Status Register - continued

Definition of each Status Register Bit

SR1 (0x08)

| Symbol | Bit | Description |
|--------|-----|--|
| PAR | 7 | Parity bit for Status Register SR1. PAR value is calculated so that total of '1' in SR1 is even. |
| SPI | 6 | SPI input bit count check result. '1' is set when total bit number during CSB = 'L' is not multiple of 16. This bit is cleared by setting(can be overwriting) CLKP = '0' and MOTEN = '1' in CR1. Refer to P26 SPI Bit Count Error Detection . |
| SHORT | 5 | OCP detection status. '1' is set when over current status is detected. This bit is cleared by PSB = L or VCC power down. SR7A[3:0] and SR8A[3:0] show the positions where over current actually flows. Refer to P27 Over Current Protection Function (OCP) . |
| OPEN | 4 | Open detection status. '1' is set when the open status is detected. This bit is cleared by setting(can be overwriting) CLKP = '0' and MOTEN = '1' in CR1. SR7A[6] and SR8A[6] show which of OUT1/OUT2 is open. Refer to P28 Open Detection Function . |
| TSD | 3 | Thermal shutdown status. '1' is set when TSD is detected. This bit is cleared by setting(can be overwriting) CLKP = '0' and MOTEN = '1' in CR1. Refer to P27 Thermal Shutdown Function (TSD) . |
| TW | 2 | Thermal warning status. '1' is set when temperature of IC chip is over the threshold set by SPI. This bit is cleared by setting(can be overwriting) CLKP = '0' and MOTEN = '1' in CR1. Refer to P27 Thermal Warning Function (TW) . |
| STALL | 1 | Stall detection status. '1' is set when stall is detected. This bit is cleared by setting(can be overwriting) CLKP = '0' and MOTEN = '1' in CR1. Refer to P29 Stall Detection Function . |

SR2 (0x09)

| Symbol | Bit | Description |
|--------|-----|--|
| PAR | 7 | Parity bit for Status Register SR2. PAR value is calculated so that total of '1' in SR2 is even. |
| ORErr | 6 | OR output of bit 6 to bit0 in SR1 |
| OV | 5 | Over voltage lock-out status. '1' is set when 'over voltage' is detected. This bit is cleared by setting(can be overwriting) CLKP = '0' and MOTEN = '1' in CR1. Refer to P27 Over Voltage Lock-out Function (OVLO) . |
| UV | 4 | Under voltage lock-out status. '1' is set when 'under voltage' is detected. This bit is cleared by setting(can be overwriting) CLKP = '0' and MOTEN = '1' in CR1. Refer to P28 Under Voltage Lock-out (UVLO) / Under Voltage Motor Hold Function . |

Definition of each Status Register Bit – continued

SR3 (0x0A)

| Symbol | Bit | Description |
|----------|-------|---|
| PAR | 7 | Parity bit for Status Register SR3. PAR value is calculated so that total of '1' in SR3 is even. |
| MSP[6:0] | [6:0] | Micro step position. MSP is updated by CLK-IN input based on the excitation mode and CW setting. But MSP is not updated when CLK-IN is input during TSD, OCP, OVLO, UVLO and Open detection because the motor is turned off. And MSP is also not updated in the hold mode (including under voltage motor hold mode.) where CLK-IN is ignored. Refer to P18 Step Sequence . |

SR5 (0x0C)

| Symbol | Bit | Description |
|---------|-------|--|
| Sp[7:0] | [7:0] | CLK-IN stepping period. Sp shows the period between the rising edge of last two CLK-IN. 1 step is 20 us (Typ) and the maximum period is 5.1 ms (Typ) at Sp[7:0] = '1111 1111'. IC keeps the maximum value if the period is longer than it. |

SR6 (0x0D)

| Symbol | Bit | Description |
|---------|-------|--|
| PAR | 7 | Parity bit for Status Register SR6. PAR value is calculated so that total of '1' in SR6 is even. |
| SI[6:0] | [6:0] | Step Loss Counter. IC counts CLK-IN input while the motor is in open state by TSD/OCP/UVLO/OVLO. The maximum number is 127 pulses (SI[6:0] = '111 1111'). IC keeps the maximum value if more CLK-IN pulses are input. In the hold mode where CLK-IN is no available, SI is not updated even in the protected state. This bit is cleared by setting (can be overwriting) CLKP = '0' and MOTEN = '1' in CR1. |

Definition of each Status Register Bit – continued

SR7A (0x1E)

| Symbol | Bit | Description |
|----------|-----|---|
| PAR | 7 | Parity bit for Status Register SR7A. PAR value is calculated so that total of '1' in SR7A is even. |
| OPEN1 | 6 | Output of Open detection result for OUT1. '1' is set when the open status is detected. This bit goes back '0' when the open state is cleared. |
| MODE0pin | 5 | Output of the MODE0 pin logic level |
| MODE1pin | 4 | Output of the MODE1 pin logic level |
| SHRT1AB | 3 | Short status of OUT1A - GND. '1' is set when the short status is detected. This bit is cleared by PSB = L or VCC power down. |
| SHRT1BB | 2 | Short status of OUT1B - GND. '1' is set when the short status is detected. This bit is cleared by PSB = L or VCC power down. |
| SHRT1AT | 1 | Short status of OUT1A - VCC. '1' is set when the short status is detected. This bit is cleared by PSB = L or VCC power down. |
| SHRT1BT | 0 | Short status of OUT1B - VCC. '1' is set when the short status is detected. This bit is cleared by PSB = L or VCC power down. |

SR8A (0x1F)

| Symbol | Bit | Description |
|---------|-----|---|
| PAR | 7 | Parity bit for Status Register SR8A. PAR value is calculated so that total of '1' in SR8A is even. |
| OPEN2 | 6 | Output of Open detection result for OUT2. '1' is set when the open status is detected. This bit goes back '0' when the open state is cleared. |
| RHBpin | 5 | Output of the RHB pin logic level |
| CWBpin | 4 | Output of the CWB pin logic level |
| SHRT2AB | 3 | Short status of OUT2A - GND. '1' is set when the short status is detected. This bit is cleared by PSB = L or VCC power down. |
| SHRT2BB | 2 | Short status of OUT2B - GND. '1' is set when the short status is detected. This bit is cleared by PSB = L or VCC power down. |
| SHRT2AT | 1 | Short status of OUT2A - VCC. '1' is set when the short status is detected. This bit is cleared by PSB = L or VCC power down. |
| SHRT2BT | 0 | Short status of OUT2B - VCC. '1' is set when the short status is detected. This bit is cleared by PSB = L or VCC power down. |

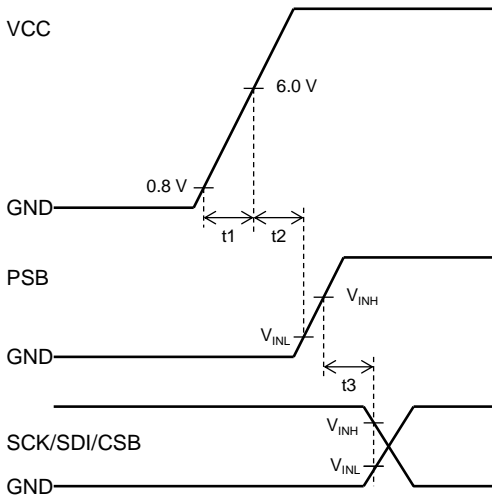
Power-on Sequence

To initialize this IC completely in power-on, follow the sequences shown below.

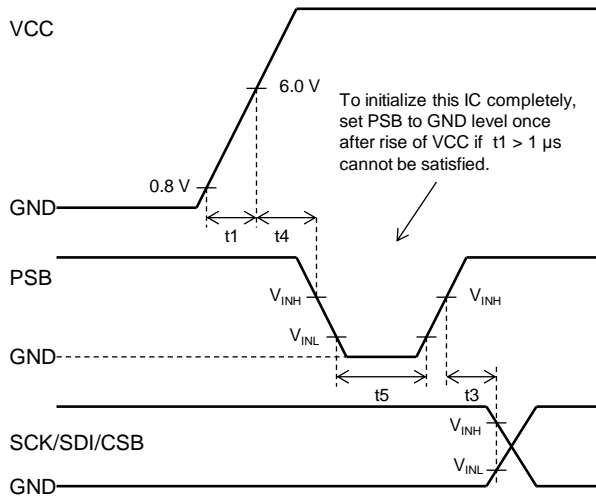
$t_1 > 1 \mu\text{s}$, $t_2 > 0 \mu\text{s}$, $t_4 > 0 \mu\text{s}$ (all Typ). Refer to [P16 Control Input Timing](#) for t_3 and t_5 .

If $t_1 > 1 \mu\text{s}$ is not satisfied, there is a possibility that IC is not initialized completely because of no power-on reset operation by steep rise of VCC. In that case, PSB should be set to GND level once after the rise of VCC.

Case of power-on with PSB = L



Case of power-on with PSB = H



Power Dissipation

In consideration of the IC's power consumption (W), thermal resistance (θ_{JA}), and ambient temperature (T_a), confirm that the IC's chip temperature T_j is not over 150 °C. When $T_j = 150$ °C is exceeded, the functions as a semiconductor do not operate and problems such as parasitism and leaks occur. Constant use under these circumstances leads to deterioration and eventually destruction of the IC. $T_{jmax} = 150$ °C must be strictly obeyed under all circumstances.

Thermal Calculation

The power consumption of this IC can be estimated roughly. The calculation formula in case of Full step mode in slow decay mode is shown below:

Self-power consumption in V_{CC} :

$$V_{CC} \times I_{CC} \quad [W] \quad (1)$$

Output DMOS power consumption during output ON:

$$(R_{ONH} + R_{ONL}) \times I_{OUT}^2 \times 2 \times on_duty \quad [W] \quad (2)$$

Output DMOS power consumption during decay:

$$2 \times R_{ONL} \times I_{OUT}^2 \times 2 \times (1 - on_duty) \quad [W] \quad (3)$$

IC total power consumption:

$$W_{TOTAL} = (1) + (2) + (3) \quad [W]$$

Junction temperature:

$$T_j = T_a + \theta_{JA} \times W_{TOTAL} \quad [^{\circ}C]$$

Where

V_{CC} is the power supply voltage [V].

I_{CC} is the circuit current [A] without motor load.

I_{OUT} is the motor output current [A].

R_{ONH} is the Upper Pch DMOS ON Resistance [Ω]. 0.45 Ω in BD63800MUF-C (Typ).

R_{ONL} is the Lower Nch DMOS ON Resistance [Ω]. 0.30 Ω in BD63800MUF-C (Typ).

$$on_duty = \frac{t_{ON}}{t_{CHOP}}$$

t_{CHOP} is the chopping cycle time [s], which depends on the CR pin. Refer [P10 PWM Constant Current control](#) for details.

t_{ON} is the CR charging period during t_{CHOP} [s], which depends on the L and R values of the motor coil and the current setting. Confirm by actual measurement, or make an approximate calculation.

T_a is the ambient temperature [$^{\circ}C$].

θ_{JA} is the thermal resistance from junction to ambient [$^{\circ}C/W$].

Note that the thermal resistance value θ_{JA} [$^{\circ}C/W$] differs greatly depending on circuit board conditions. ROHM provides a service to measure the thermal resistance θ_{JA} with a PCB which customers actually designed. Contact us about this service. The calculated values above are only theoretical. For actual thermal design, perform sufficient thermal evaluation for the application board used, and make the thermal design with enough margin so as not to exceed $T_{jmax} = 150$ °C.

Consider attaching an external Schottky diode between the motor output pin and the GND pin / the VCC pin to abate heat from the IC if the IC is used under particularly severe heat conditions. (This counter measure is not necessary for normal use)

Absolute Maximum Rating

(Ta = 25 °C)

| Item | Symbol | Rated Value | Unit |
|---|----------------------|--------------------------|---------|
| Supply Voltage | V _{CC} | -0.2 to +40.0 | V |
| Input Voltage for Control Pin | V _{IN} | -0.2 to +7.0 | V |
| Output Voltage for Control Pin | V _{OUT} | -0.2 to +7.0 | V |
| Output Current (Steady-state) | I _{OUT} | 1.21 ^(Note 1) | A/Phase |
| Output Current (Peak) ^(Note 2) | I _{OUTPEAK} | 1.35 ^(Note 1) | A/Phase |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |
| Maximum Junction Temperature | T _{jmax} | +150 | °C |

(Note 1) Do not exceed T_{jmax} = 150 °C.

(Note 2) Pulse width tw ≤ 1 ms, duty 20 %

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Recommended Operating Condition

| Item | Symbol | Min | Typ | Max | Unit |
|-----------------------|-----------------|-----|------|------|------|
| Operating Temperature | Topr | -40 | +25 | +125 | °C |
| Supply Voltage | V _{CC} | 6.0 | 12.0 | 28.0 | V |

Thermal Resistance (Note 1)

| Parameter | Symbol | Thermal Resistance (Typ) | | Unit |
|--|-----------------|--------------------------|--------------------------|------|
| | | 1s ^(Note 3) | 2s2p ^(Note 4) | |
| VQFN32FBV050 | | | | |
| Junction to Ambient | θ _{JA} | 89.20 | 30.80 | °C/W |
| Junction to Top Characterization Parameter ^(Note 2) | Ψ _{JT} | 10.00 | 7.00 | °C/W |

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

| Layer Number of Measurement Board | Material | Board Size |
|-----------------------------------|----------|-------------------------------|
| Single | FR-4 | 114.3 mm x 76.2 mm x 1.57 mmt |

| Top | |
|-----------------------|-----------|
| Copper Pattern | Thickness |
| Footprints and Traces | 70 μm |

| Layer Number of Measurement Board | Material | Board Size | Thermal Via ^(Note 5) | |
|-----------------------------------|----------|------------------------------|---------------------------------|----------|
| | | | Pitch | Diameter |
| 4 Layers | FR-4 | 114.3 mm x 76.2 mm x 1.6 mmt | 1.20 mm | Φ0.30 mm |

| Top | | 2 Internal Layers | | Bottom | |
|-----------------------|-----------|-------------------|-----------|-------------------|-----------|
| Copper Pattern | Thickness | Copper Pattern | Thickness | Copper Pattern | Thickness |
| Footprints and Traces | 70 μm | 74.2 mm x 74.2 mm | 35 μm | 74.2 mm x 74.2 mm | 70 μm |

(Note 5) This thermal via connects with the copper pattern of all layers.

Electrical Characteristics(Unless otherwise specified $V_{CC} = 8.0\text{ V}$ to 28.0 V , $T_a = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$)

| Item | Symbol | Limit | | | Unit | Conditions |
|--|--------------|-------|-------|------|------------------|--|
| | | Min | Typ | Max | | |
| Whole | | | | | | |
| Standby Circuit Current | I_{CCST} | - | 0.1 | 10.0 | μA | PSB = L |
| Circuit Current | I_{CC} | - | 3.5 | - | mA | PSB = H, RREF = 6.2 k Ω |
| Control input (CLK, CWB, MODE0, MODE1, RHB, PSB, SCK, SDI, CSB) | | | | | | |
| H Level Input Voltage | V_{INH} | 2.0 | - | - | V | |
| L Level Input Voltage | V_{INL} | - | - | 0.8 | V | |
| H Level Input Current | I_{INH} | 35 | 50 | 100 | μA | $V_{IN} = 5.0\text{ V}$ |
| L Level Input Current | I_{INL} | -10 | 0 | - | μA | $V_{IN} = 0.0\text{ V}$ |
| Output(OUT1A, OUT1B, OUT2A, OUT2B) | | | | | | |
| Output On Resistance | R_{ON} | - | 0.75 | 1.50 | Ω | $I_{OUT} = \pm 0.5\text{ A}$, Total of upper and lower side |
| Output Leakage Current | I_{LEAK} | - | 0.1 | 10.0 | μA | |
| Output Rising Slew Rate | t_R | - | 2.0 | - | μs | $V_{CC} = 24\text{ V}$ |
| Output Falling Slew Rate | t_F | - | 2.0 | - | μs | EMC[1:0] = '00' |
| Current Control Unit | | | | | | |
| Maximum Output Current | I_{OMAX} | 0.99 | 1.10 | 1.21 | A | RREF = 6.2 k Ω |
| PWM Frequency | f_{PWM} | - | 24.7 | - | kHz | C = 1000 pF, R = 39 k Ω |
| RREF Outflow Current | I_{RREF} | - | 74 | - | μA | RREF = 6.2 k Ω |
| RREF Output Voltage | V_{RREF} | - | 0.457 | - | V | |
| MTH Input Current | I_{MTH} | -10 | -5 | - | μA | MTH = 0 V |
| MTH Input Voltage Range | V_{MTH} | 0 | - | 3.5 | V | |
| Minimum ON Time (Blank Time) | t_{ONMIN} | 0.3 | 0.8 | 1.5 | μs | C = 1000 pF, R = 39 k Ω |
| DIAG Output (DIAG1, DIAG2) | | | | | | |
| Output L Voltage | V_{OLD} | - | 0.15 | 0.50 | V | $I_{LOAD} = -1\text{ mA}$ |
| Output Leakage Current | I_{OD} | - | 0 | 10 | μA | $V_{DG} = 5\text{ V}$ |
| SDO Output | | | | | | |
| Output H Voltage | V_{OHS} | 4.50 | 4.85 | - | V | $I_{LOAD} = +1\text{ mA}$ |
| Output L Voltage | V_{OLS} | - | 0.15 | 0.50 | V | $I_{LOAD} = -1\text{ mA}$ |
| Output Leakage Current | I_{OS} | - | 0 | 10 | μA | $V_{SDO} = 5\text{ V}$ |
| Protection circuit | | | | | | |
| Thermal Shutdown ON Temperature | T_{TSDON} | - | 175.0 | - | $^\circ\text{C}$ | |
| Thermal Shutdown OFF Temperature | T_{TSDOFF} | - | 150.0 | - | $^\circ\text{C}$ | |
| Thermal Warning ON Ambient Temp | T_{TAON} | - | 150.8 | - | $^\circ\text{C}$ | TWThr = '1111' |
| Thermal Warning OFF Ambient Temp | T_{TAOFF} | - | 124.5 | - | $^\circ\text{C}$ | TWThr = '1111' |
| Low Voltage Protection ON Voltage | V_{UVON} | - | 5.04 | - | V | UVThr = '0011' |
| Low Voltage Protection OFF Voltage | V_{UVOFF} | - | 5.82 | - | V | UVThr = '0011' |
| Over Voltage Protection ON Voltage | V_{OVON} | - | 32.0 | - | V | |
| Over Voltage Protection OFF Voltage | V_{OVOFF} | - | 31.0 | - | V | |
| Output Load Open Detection Time | t_{LOPEN} | - | 5.12 | - | ms | |

Electrical Characteristics - continued

(Unless otherwise specified $V_{CC} = 8.0\text{ V}$ to 28.0 V , $T_a = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$)

| Item | Symbol | Specification | | | Unit | Conditions |
|-------------------------------------|----------------|---------------|-----|-----|---------------|---|
| | | Min | Typ | Max | | |
| SPI Timing | | | | | | |
| SPI Clock Cycle | t_{SCK} | 1 | - | - | μs | |
| SPI Clock High Time Range | t_{HSCK} | 200 | - | - | ns | |
| SPI Clock Rise Time | t_{RSCK} | - | - | 1 | μs | |
| SPI Clock Fall Time | t_{FSCK} | - | - | 1 | μs | |
| SPI Clock Low Time Range | t_{LSCK} | 200 | - | - | ns | |
| SDI Setup Time for SCK | t_{STSDI} | 50 | - | - | ns | |
| SDI Hold Time for SCK | t_{HDSDI} | 50 | - | - | ns | |
| CSB High Time | t_{HCSB} | 200 | - | - | ns | |
| CSB Low Setup Time for SCK | t_{STLCSB} | 1 | - | - | μs | |
| CSB High Hold Time for SCK | t_{HDHCSB} | 200 | - | - | ns | |
| SDO Delay Time for CSB Rising Edge | $t_{DCSBSDO1}$ | - | - | 250 | ns | $R_L = 1.5\text{ k}\Omega$, $C_L = 10\text{ pF}$ |
| SDO Delay Time for CSB Falling Edge | $t_{DCSBSDO2}$ | - | - | 250 | ns | $R_L = 1.5\text{ k}\Omega$, $C_L = 10\text{ pF}$ |
| SDO Delay Time for SCK | $t_{DSCKSDO}$ | - | - | 100 | ns | $R_L = 1.5\text{ k}\Omega$, $C_L = 10\text{ pF}$ |

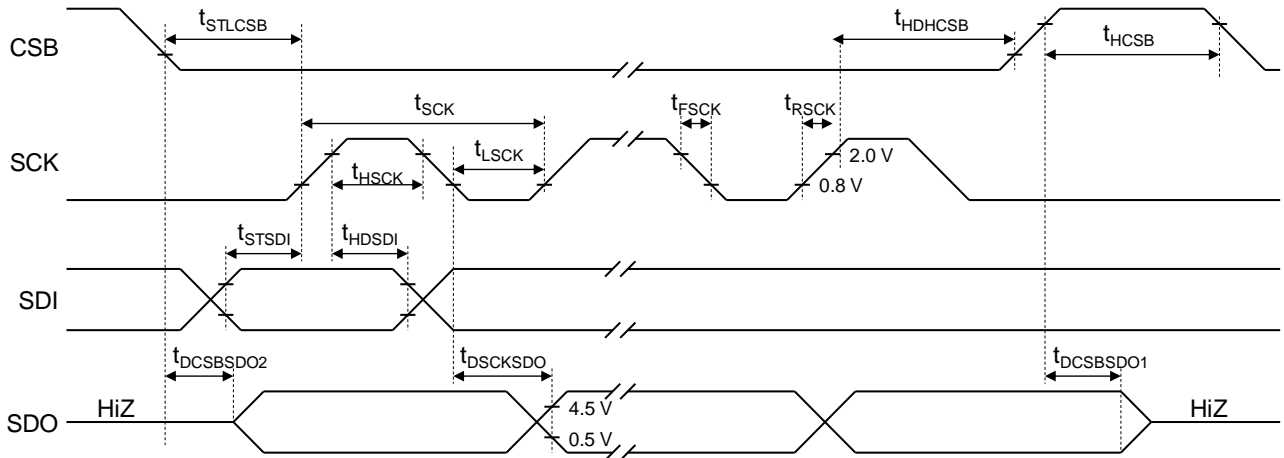


Figure 12. SPI Timing Chart

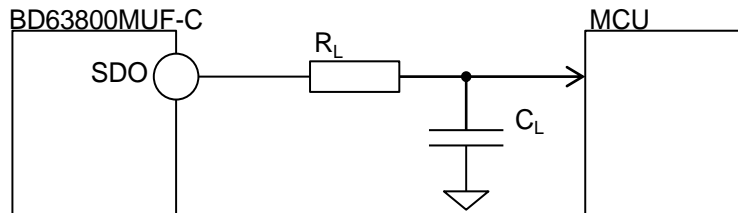
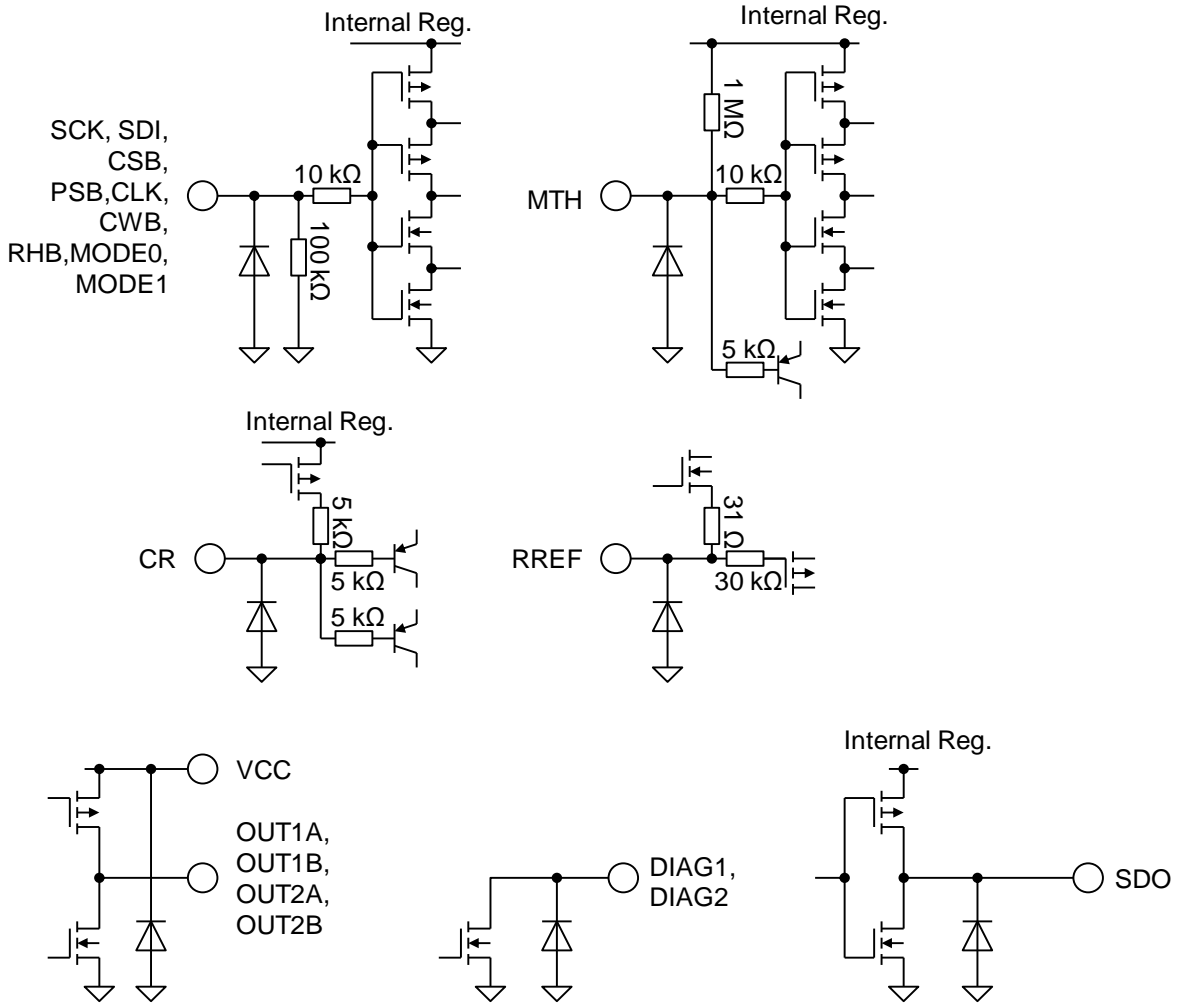


Figure 13. SDO Load Model

I/O Equivalence Circuit



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

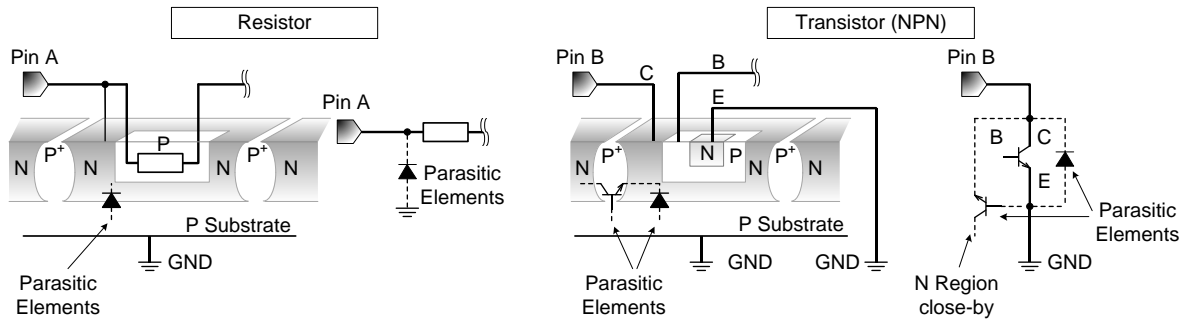


Figure 14. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

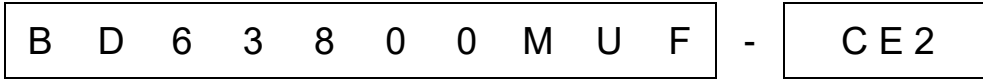
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

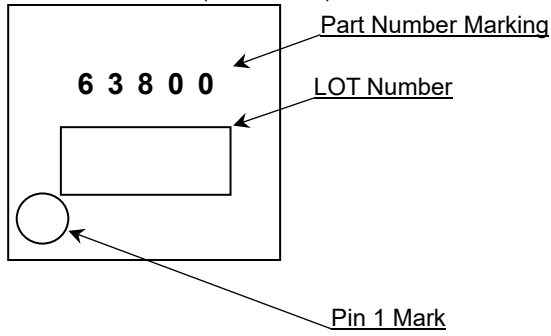


Package
MUF: VQFN32FBV050

Product Rank
C: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

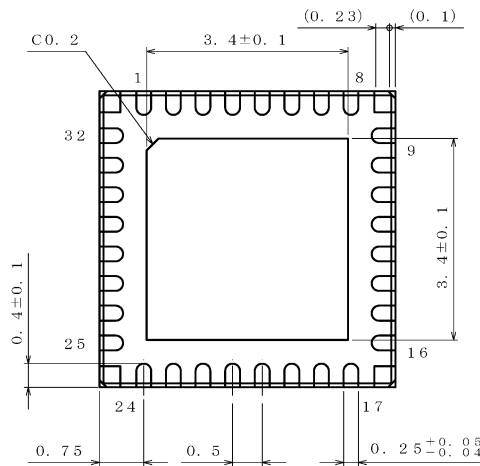
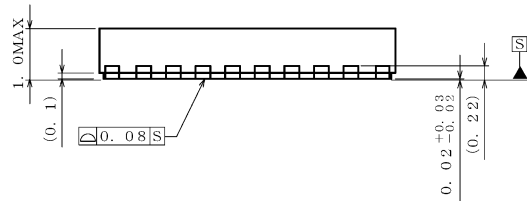
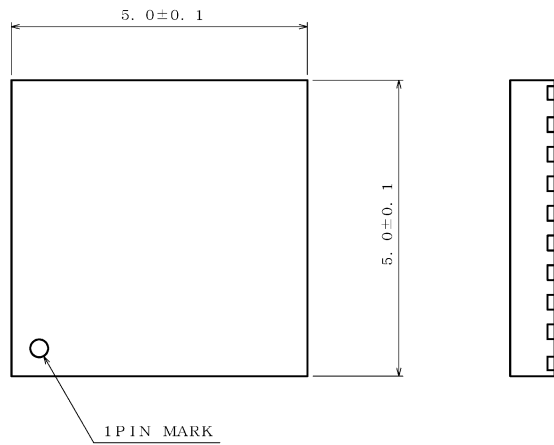
Marking Diagram

VQFN32FBV050 (TOP VIEW)



Physical Dimension and Packing Information

| | |
|--------------|--------------|
| Package Name | VQFN32FBV050 |
|--------------|--------------|



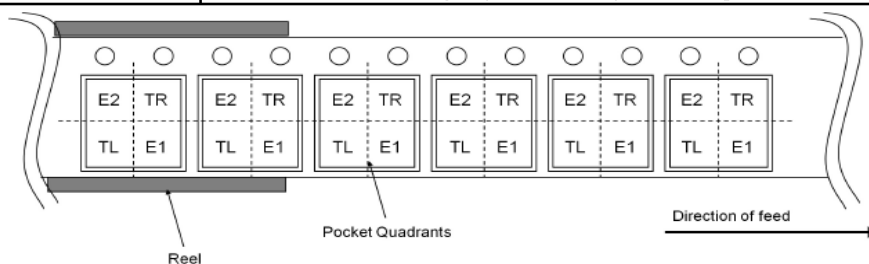
(UNIT : mm)

PKG : VQFN32FBV050
Drawing No. EX416-5001

NOTE: Dimensions in () for reference only.

< Tape and Reel Information >

| | |
|-------------------|--|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand |



Revision History

| Date | Revision | Changes |
|-------------|----------|---|
| 10.Feb.2021 | 001 | The first edition |
| 29.Jan.2024 | 002 | <p>P7, P15, P16 Change the description</p> <p>P8 IOOUT calculation formula changed</p> <p>P9, P10 External CR range change</p> <p>P11 Added about the current distortion threshold when the minimum ON time is shortened</p> <p>P11, P12 Add graph</p> <p>P17 Correction of typographical errors in diagrams</p> <p>P18 Added that the excitation position inside the IC cannot be changed without moving the motor.</p> <p>P26 Change of IC parallel connection diagram</p> <p>P28 Added about open detection</p> <p>P29 Addendum regarding cases where the back electromotive force is significantly affected</p> <p>P32, P36 Added about register map address</p> <p>P33 Added the relationship between slew rate and minimum ON time</p> <p>P37, P38 Added overwriting possible</p> <p>P43 PWM frequency change</p> <p>P45 Add resistance value to input/output equivalent circuit diagram</p> <p>Figure number updated</p> |

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - [a] Installation of protection circuits or other protective devices to improve system safety
 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
 - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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General Precaution







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