THE DATASHEET OF

ASGTX-C-100.000MHZ-2

Configurable High Performance SMD TCXO/VCTCXO

ASGTX

Request Samples | Check Inventory | ESD Sensitive | Pb

9.0 x 7.0 x 2.24 mm
RoHS/RoHS II Compliant
MSL Level = 1

Overview

ASGTX temperature compensated Crystal Oscillators are designed to accommodate a broad breadth of Precision TCXO requirements, without NRE and extended lead-times. This oscillator series is designed and manufactured by Abracon Corporation and is available to order from 1pc to high volume production quantities.

- **Quick-turn availability of a TCXO/VCTCXO with LVCMOS output, Any frequency between 10MHz and 250MHz**

  For example, if a reference oscillator requirement calls out 49.7521MHz; ±1.00 ppm TCXO/VCTCXO with **LVCMOS** output, ASGTX can be configured and shipped within days. Customers with low-to-mid annual volume requirements find it difficult to procure custom frequency TCXO/VCTXCO's without costly NRE charges and/or long lead-times (≥ 12 weeks).

- **Quick turn availability of a TCXO/VCTXCO requiring LVDS or LVPECL Differential output, Any frequency between 10MHz to 1.50GHz**

  ASGTX is available with either **LVDS or LVPECL** output, from **10MHz to 1.50GHz**; at any desired frequency, such as 149.875MHz, 1.00GHz, 1.5GHz, etc. with as tight as ±1.00 ppm stability over temperature. No other solution in the marketplace currently offers such capability, especially in a small form-factor of 9.0x7.0x2.24 mm.

ASGTX is suitable for a wide variety of precision timing applications where TCXO/VCTXO's are typically employed. In addition, for high frequency LO requirements, traditionally customers have relied on SAW based oscillators. Such devices are only available at a few fixed frequencies, such as 915MHz, 1.0GHz, etc. They are typically in 9x14mm or bigger packages and vary as much as ±100 ppm over temperature.

Although ASGTX series will be slightly less favorable in phase noise performance compared to SAW based oscillators, it offers the following key advantages:

- One device can be used for both TCXO or VCTCXO configurations
- ±1.00 ppm stability over -30ºC to +70ºC and ±2.00 ppm stability over -40ºC to +85ºC
- Any carrier frequency between 10MHz and 1.50GHz
- LVCMOS / LVDS / LVPECL Output
- Small form-factor of 9.0x7.0x2.24 mm
- No NRE, reduced lead-time

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Features

- 10MHz to 1.50GHz, any Carrier Frequency in differential mode (LVDS or LVPECL)
- 10MHz to 250MHz, any Carrier Frequency in LVCMOS mode
- -40ºC to +85ºC operating temperature range
- ±1.0ppm stability over -30ºC to +70ºC and ±2.0ppm stability over -40ºC to +85ºC
- Minimum guaranteed pull ability of ± 10ppm minimum (VCTCXO)
- Good Phase Noise, excellent Harmonics and Spurious content
- Immediate availability, quick-turn lead-time for small quantities

Applications

- 40G and 100G Ethernet
- WiMax,
- LTE, BTS
- CATV, LAN, LMDS
- Point-to-Point communication network

Key Electrical Specifications

Parameters		Min.	Typ.	Max.	Units	Notes
Frequency:	LVCMOS	10		250	MHz	
	LVDS	10		1500		
	LVPECL	10		1500		
Operating Temperature:		-40		+85	°C	
Storage Temperature:		-40		+85	°C	
Frequency Stability:						
Initial Set Tolerance:		-1.50	≤ ±1.00	+1.50	ppm	TCXO configuration*
		-1.50	≤ ±1.00	+1.50	ppm	VCTCXO configuration**
Stability over operating temperature	-30°C to +70°C	-1.00		+1.00	ppm	Option "1"
	-40°C to +85°C	-2.00		+2.00		Option "2"
Supply Voltage (Vdd):		3.135	3.300	3.465	V	
Startup Time:				3	ms	
Voltage Control Function (Vcon)		0	1.17	2.5	V	VCTCXO configuration
Frequency Tuning Range:				-10	ppm	At Vcon(min), V_{DD}=3.3Vdc
		+10				At Vcon(max), V_{DD}=3.3Vdc
Phase jitter RMS [$t_{jit(\varphi)}$] *** (12kHz to 20MHz)			1.0	3.0	ps	Frequency dependent, see Table 1 below

Notes

* **Reference to fo, at 25°C ±2°C, 24 hours after reflow, one time , nominal Vdd**

** **Reference to fo, at 25°C ±2°C, 24 hours after reflow, one time , nominal Vdd, and Vcon = 1.17V +- 0.2V**

*** **1.8ps max is guaranteed for LVCMOS and LVDS output modes. For LVPECL mode at carrier frequency greater than 1.289GHz, the maximum RMS jitter is 3.0ps**

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Electrical Specifications-LVCMOS

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (I_{dd})				45	mA	Frequency dependent With CMOS output load
Output Load:				15	pF	
Output Logic Level	V_{OH}	0.9*V_{dd}			V	
	V_{OL}			0.1*V_{dd}	V	
Rise Time (Tr):				1000	ps	
Fall Time (Tf):				1000	ps	
Duty Cycle:		45		55	%	@1/2Vdd

Electrical Specifications-LVPECL

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (I_{dd})				60	mA	With LVPECL output termination
Output Logic Level	V_{OH}	V_{dd}-1.03		V_{dd}-0.60	V	
	V_{OL}	V_{dd}-1.85		V_{dd}-1.60	V	
Rise Time (Tr):				350	ps	
Fall Time (Tf):				350	ps	
Differential Duty Cycle:		45		55	%	$DODC_{LVPECL}$

Electrical Specifications-LVDS

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Current (I_{dd})			40	mA	With LVDS output termination
Differential Output Voltage (V_{OD})	175	350		mV	
V_{OD} Magnitude Change (ΔV_{OD})			50	mV	
Offset Voltage (V_{OS})		1.25		V	
V_{OS} Magnitude Change (ΔV_{OS})			50	mV	
Rise Time (Tr):			350	ps	
Fall Time (Tf):			450	ps	
Differential Duty Cycle:	45		55	%	ODC_{LVDS}

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Options and Part Identification

ASGTX-[ ]-[ ]MHZ-[ ]-[ ]

Output Type
C = LVCMOS
P = LVPECL
D = LVDS

Frequency in MHz
Please specify the Frequency in MHz e.g. 100.000 MHz

Freq. Stability
1 = ±1ppm over -30 to +70°C
2 = ±2ppm over -40 to +85°C

Packaging
Blank = Bulk
T2 = 250pcs/Reel

C = LVCMOS	Any Carrier Frequency between 10MHz minimum to 250MHz maximum
P = LVPECL	Any Carrier Frequency between 10MHz minimum to 1.50GHz maximum
D = LVDS	Any Carrier Frequency between 10MHz minimum to 1.50GHz maximum

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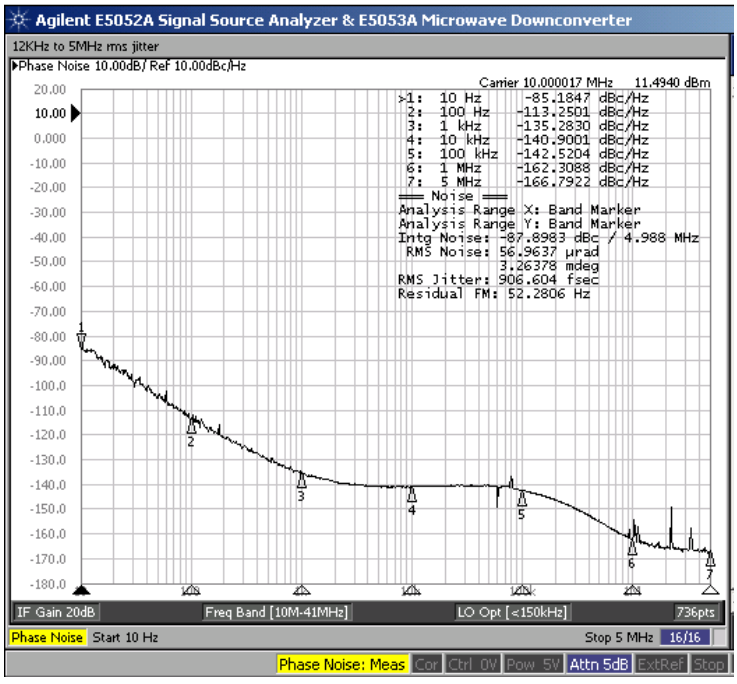
RoHS/RoHS II Compliant
MSL Level = 1

Typical Phase Jitter Characteristics (Table 1) Integration Bandwidth: 12kHz to 20Mhz

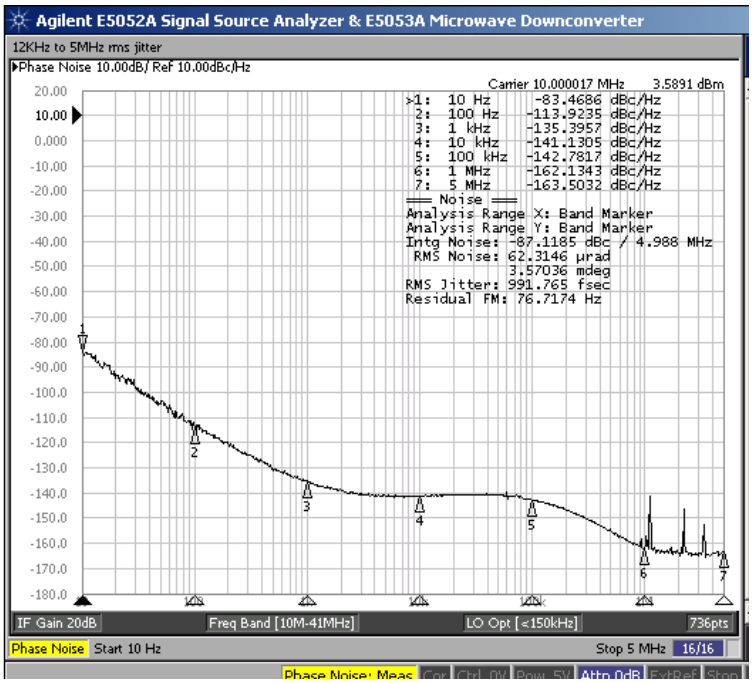
Carrier	RF Output	*rms* Phase Jitter
10.00MHz	LVDS	992 fs
10.00MHz	LVCMOS	906 fs
25.00MHz	LVDS	774 fs
25.00MHz	LVCMOS	754 fs
50.00MHz	LVDS	768 fs
50.00MHz	LVCMOS	999 fs
120.00MHz	LVCMOS	1.1 ps
500.00MHz	LVPECL	956 fs
1.00GHz	LVDS	911 fs
1.2890625GHz	LVDS	1.03 ps
1.50GHz	LVDS	1.55 ps

Typical Phase Noise Characteristics

LVCMOS Output; 10MHz Carrier



LVDS Output; 10MHz Carrier



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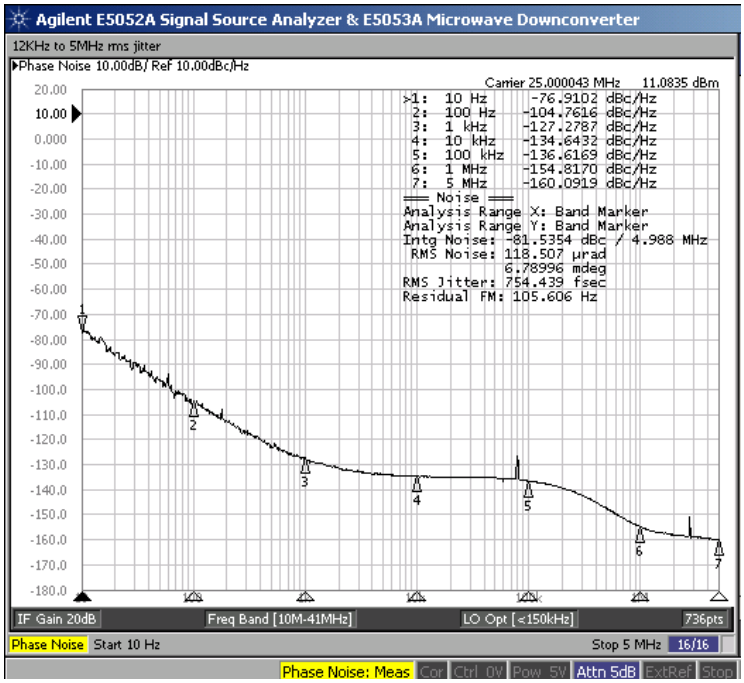
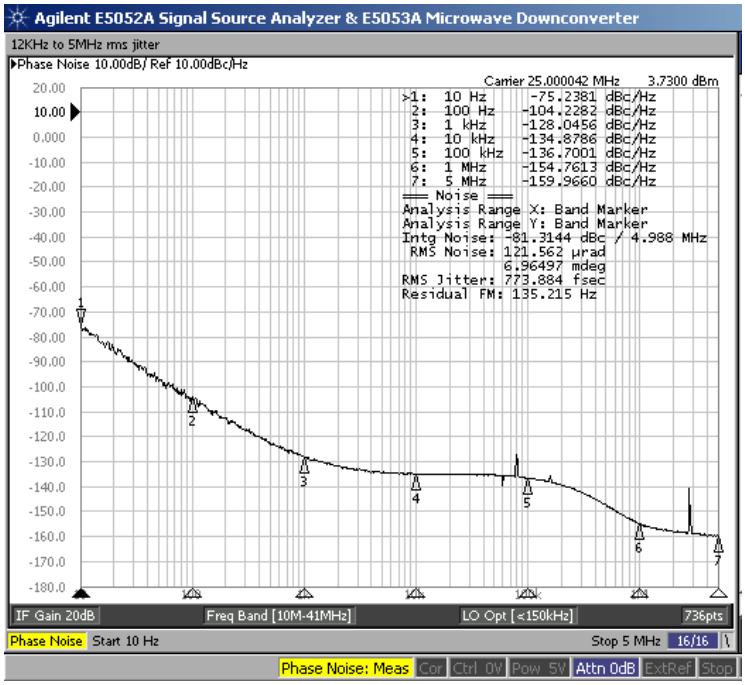
MSL Level = 1

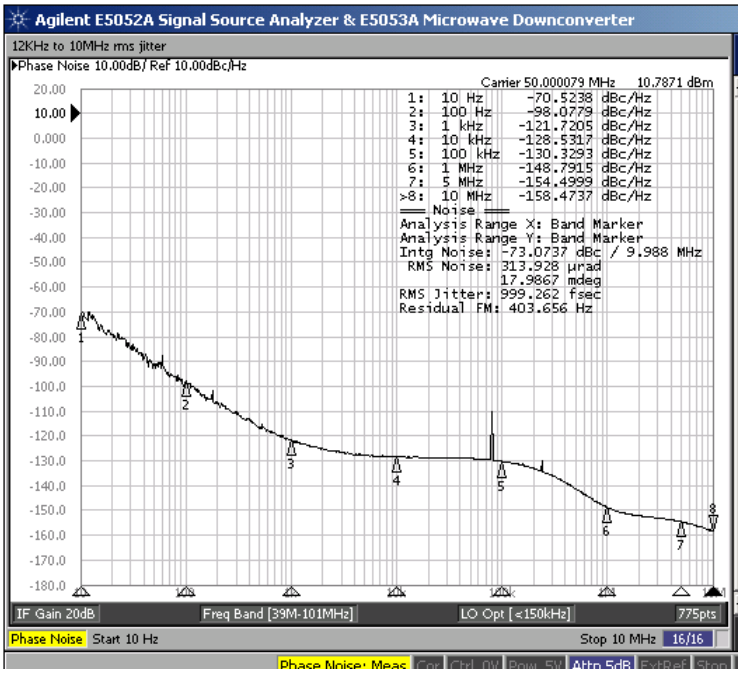
LVCMOS Output; 25MHz Carrier



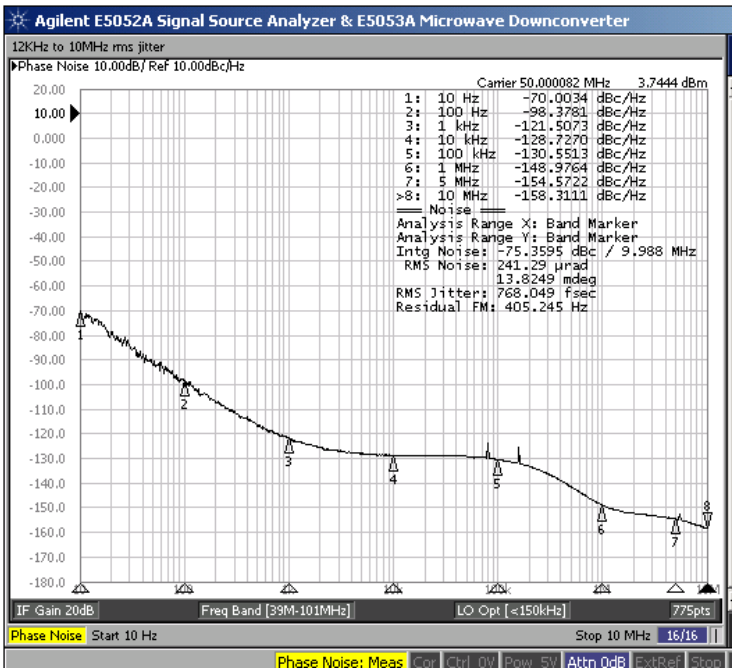
LVDS Output; 25MHz Carrier



LVCMOS Output; 50MHz Carrier



LVDS Output; 50MHz Carrier



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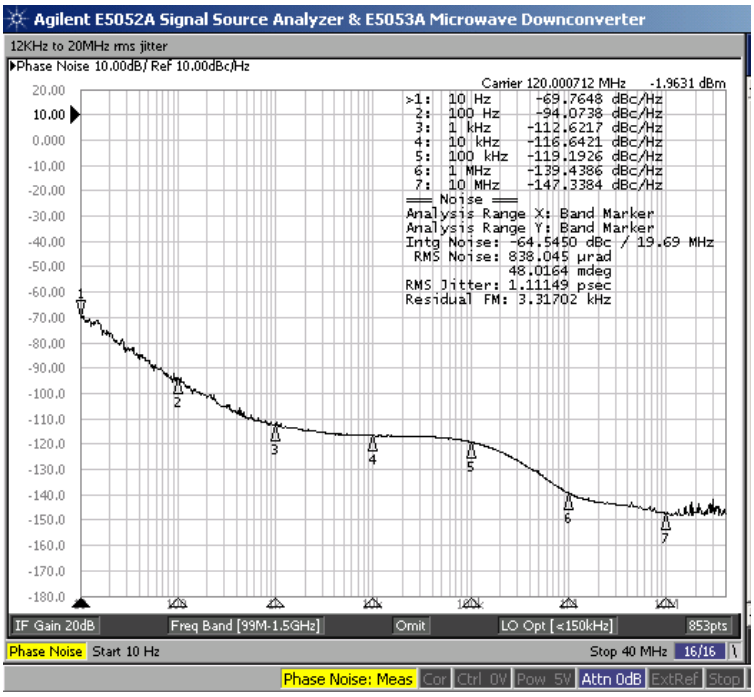
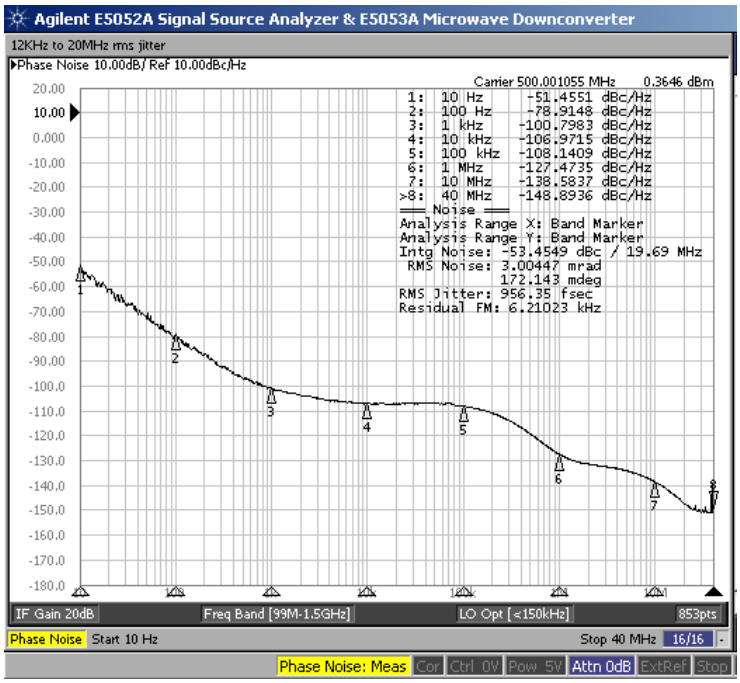
MSL Level = 1

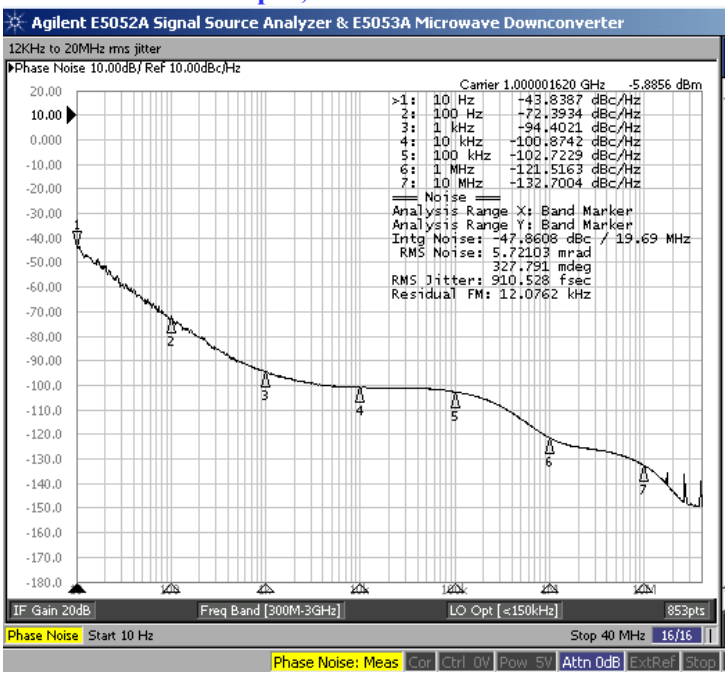
LVCMOS Output; 120MHz Carrier



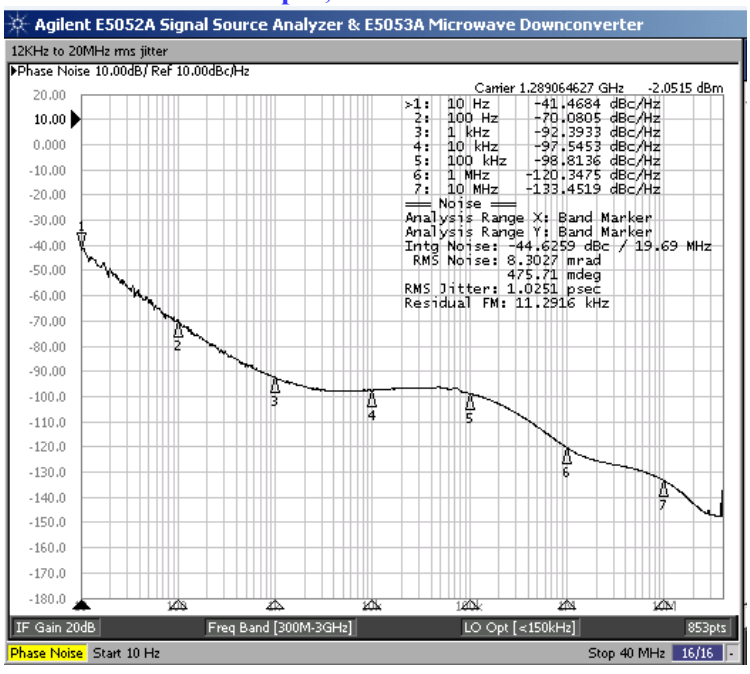
LVPECL Output; 500MHz Carrier



LVDS Output; 1.00GHz Carrier



LVDS Output; 1.2890625GHz Carrier



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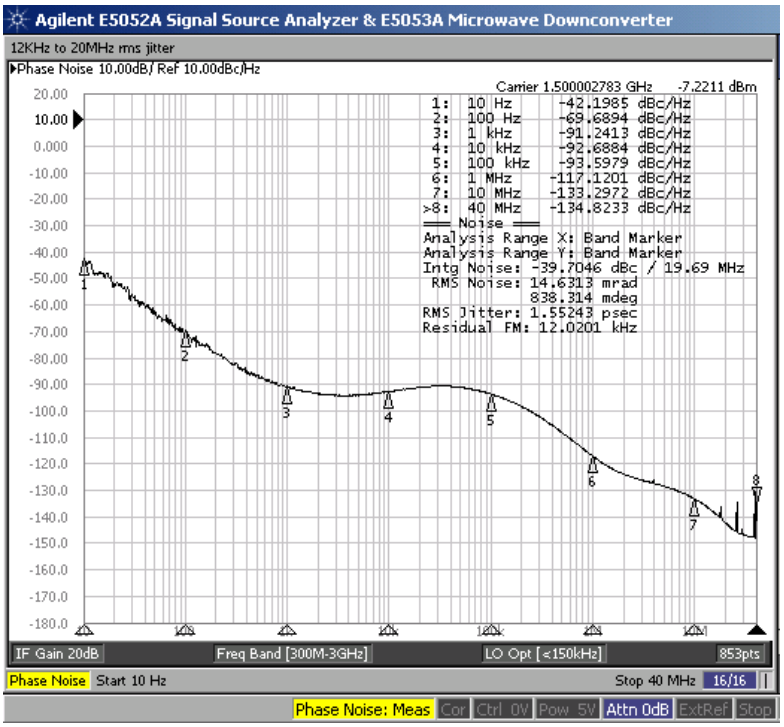
MSL Level = 1

LVDS Output; 1.50GHz Carrier



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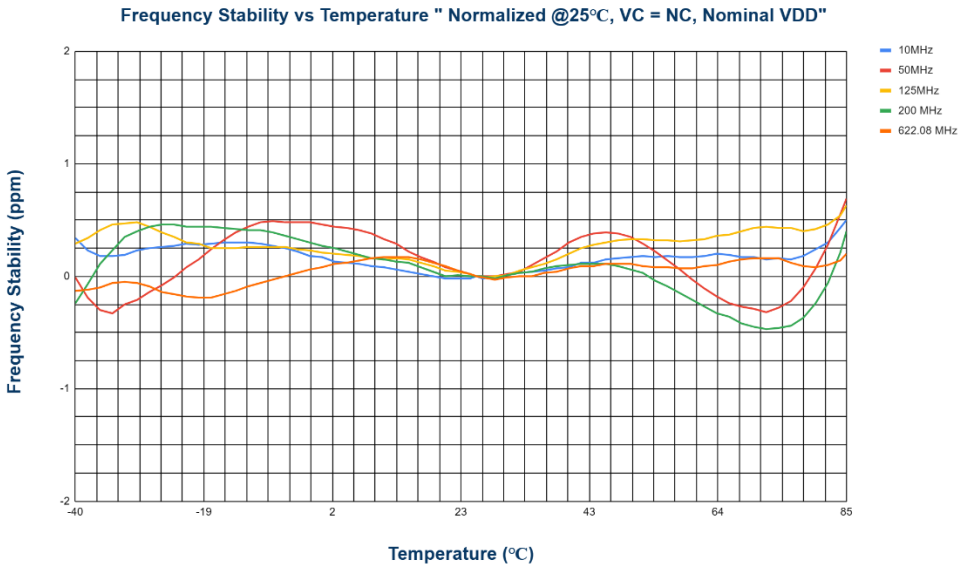
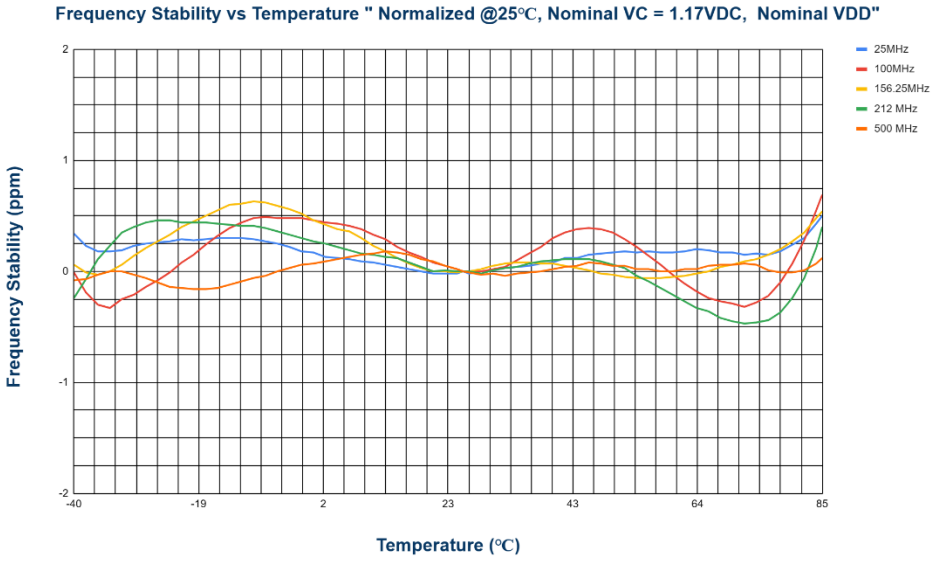
MSL Level = 1

Frequency Stability vs. Temperature ****

TCXO Configuration



VCTCXO Configuration



Notes

**** **The following conditions are applicable to all output logic types.**

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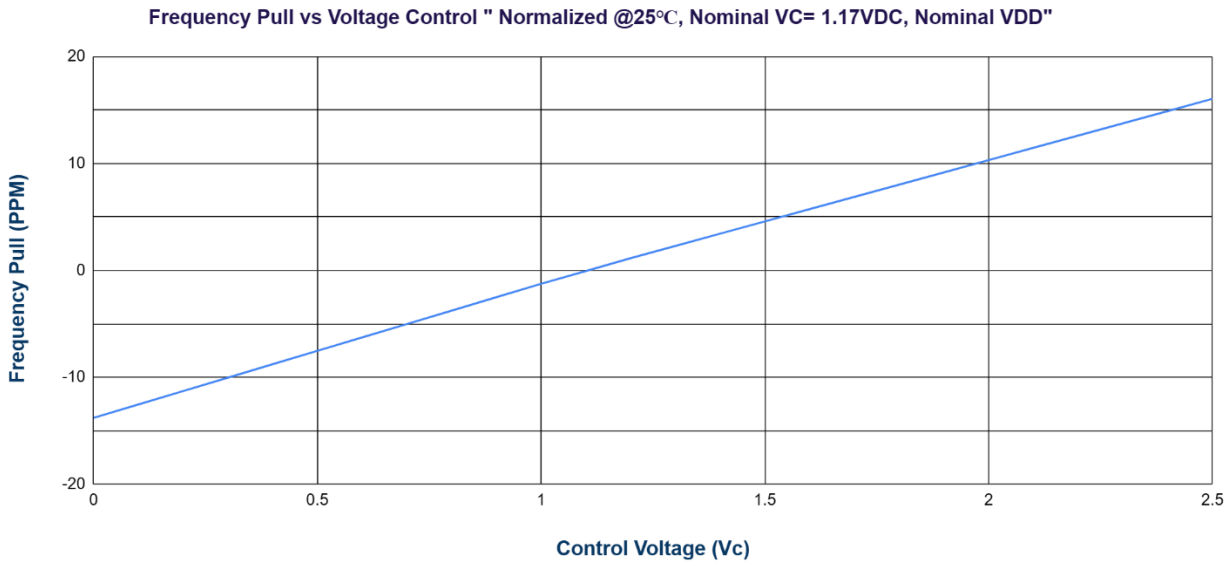
Frequency Pull vs. Control Voltage (VCTCXO Configuration)



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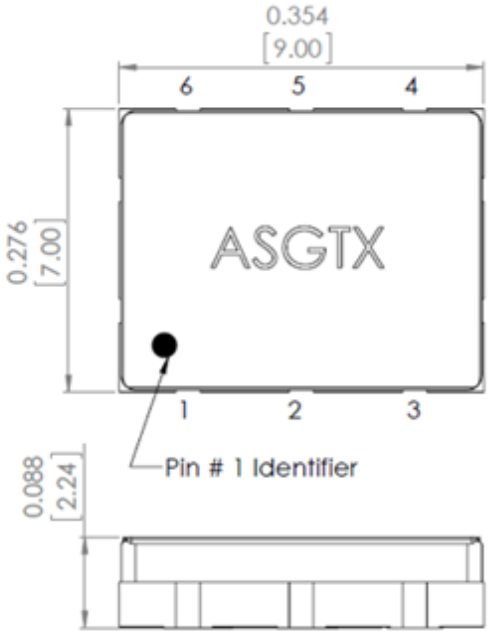
Mechanical Dimensions

LVCMOS output

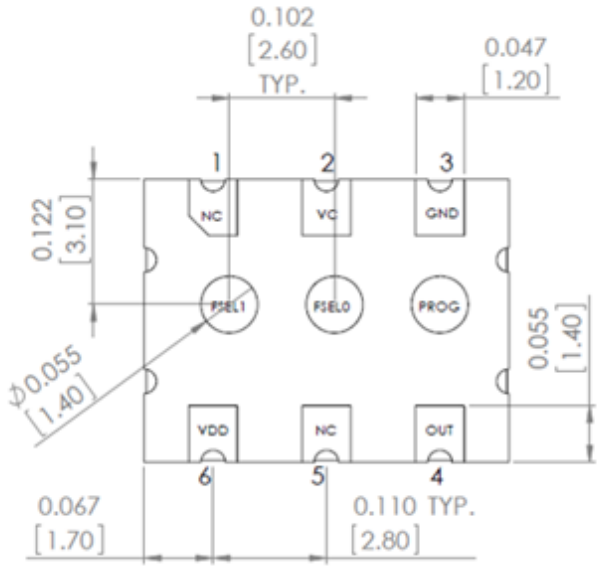


Pin #	Pin Description	
	TCXO	VCTCXO
1	N/C (1)	
2	By-Pass (2)	Vc (3)
3	GND	
4	RF Output	
5	N/C (1)	
6	Vdd	

N/C (1) = Please leave these pins electrically floating on the end-PCB

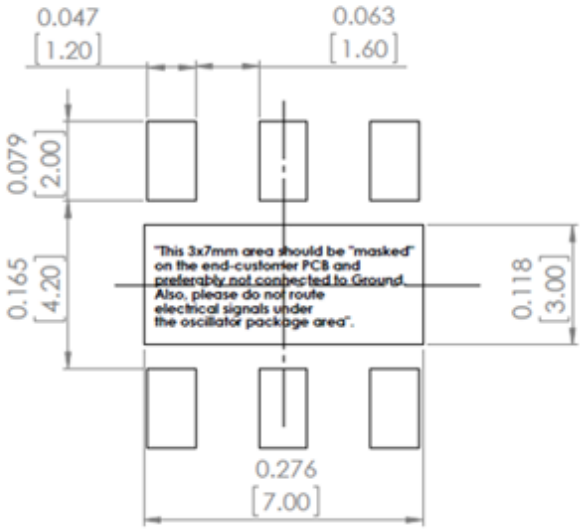
By-Pass (2) = In TCXO configuration, it is recommended that a 1,000pF COG by-pass capacitor is connected between Pin#2 and GND

Vc (3) = In VCTCXO configuration, please connect external voltage to pull the oscillator frequency



Note: Pads PROG, FSEL0 & FSEL1 are factory configuration pins. Do Not Connect.

Recommended Land Pattern



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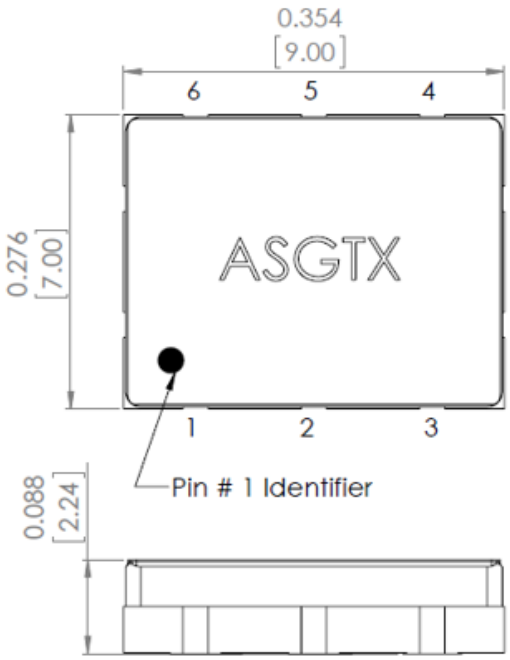
LVDS/LVPECL output

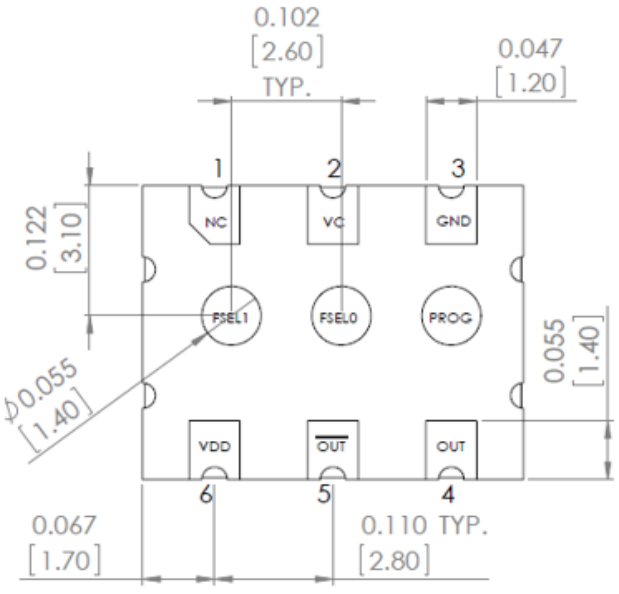


Pin #	Pin Description	
	TCXO	VCTCXO
1	N/C (1)	
2	By-Pass (2)	Vc (3)
3	GND	
4	RF Output	
5	Complimentary RF Output	
6	Vdd	

N/C (1) = Please leave these pins electrically floating on the end-PCB

By-Pass (2) = In TCXO configuration, it is recommended that a 1,000pF COG by-pass capacitor is connected between Pin#2 and GND

Vc (3) = In VCTCXO configuration, please connect external voltage to pull the oscillator frequency



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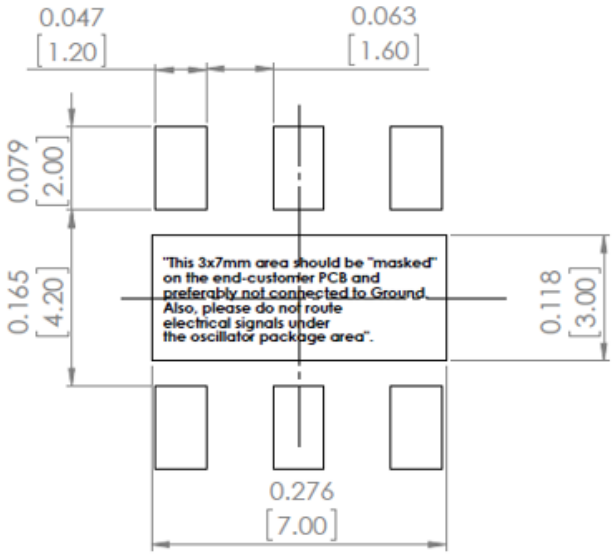
Recommended Land Pattern



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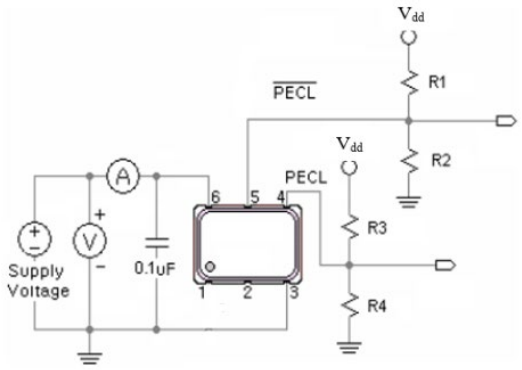
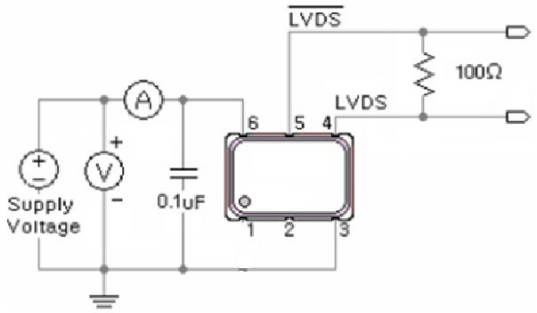
Recommended Test Circuit

LVPECL

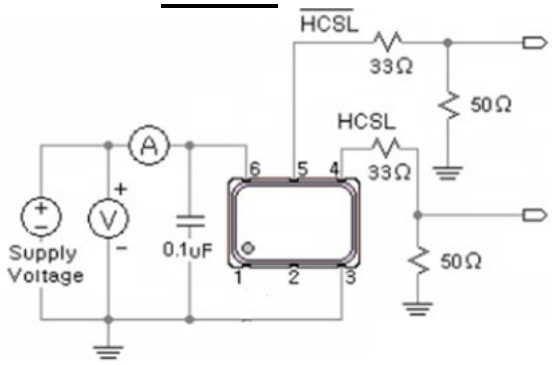


Vdd=3.3V: R1=R3=127Ω; R2=R4=82.5 Ω
Vdd=2.5V: R1=R3=250Ω; R2=R4=62.5 Ω

LVDS



HCSL



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Reflow Profile [JEDEC J-STD-020]

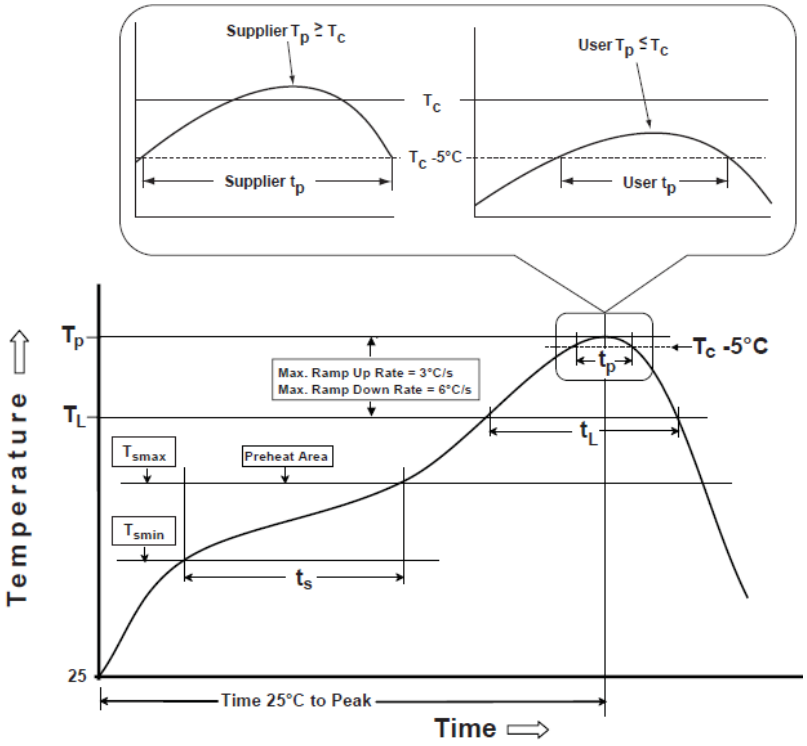

Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_P)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_P)*	**see Table 1**	**see Table 2**
Time (t_p)** within 5°C of the specified classification temperature (T_C)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.

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Configurable High Performance SMD TCXO/VCTCXO

ASGTX

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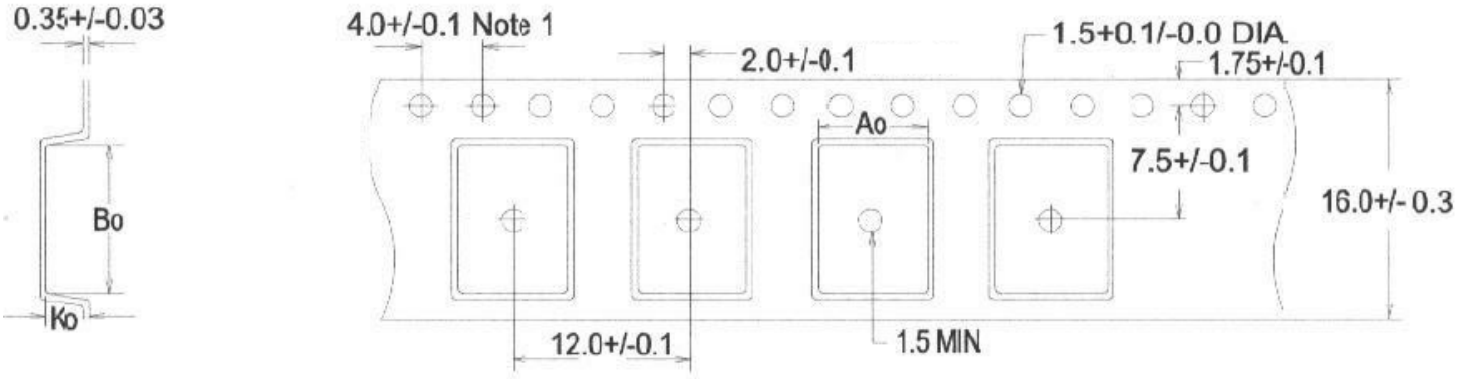
ESD Sensitive | Pb

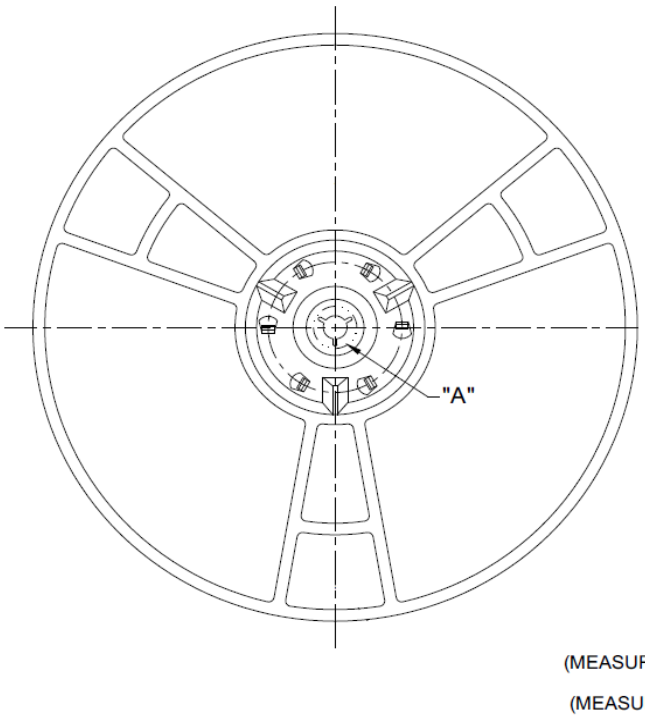
9.0 x 7.0 x 2.24 mm
RoHS/RoHS II Compliant
MSL Level = 1

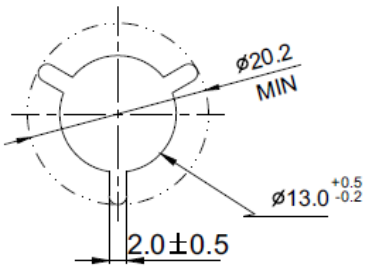
Packaging

250pcs/reel



A0	B0	K0
7.10±0.1	9.60±0.1	3.00±0.1





Detail "A"

W1	W2
16.8+0.6/-0.4	22.2 max.

Dimensions: mm

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