



**THE DATASHEET OF  
AS7C1024C-12TJINTR**





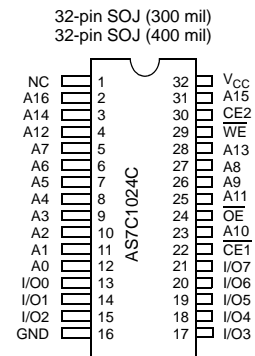
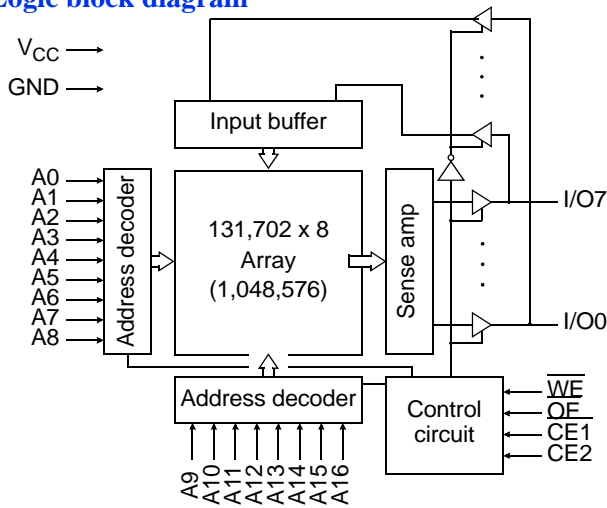
5V 128K X 8 CMOS SRAM

**Features**

- Industrial (-40° to 85°C) temperature
- Organization: 131,072 x 8 bits
- High speed
  - 12 ns address access time
  - 6 ns output enable access time
- Low power consumption via chip deselect
- Easy memory expansion with  $\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{OE}$  inputs
- TTL/LVTTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
  - 300 mil SOJ
  - 400 mil SOJ
- ESD protection  $\geq$  2000 volts

**Pin arrangement**

**Logic block diagram**





## Functional description

The AS7C1024C is a 5V high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) device organized as 131,072 words x 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 12 ns with output enable access times ( $t_{OE}$ ) of 6 ns are ideal for high performance applications. Active high and low chip enables ( $\overline{CE1}$ , CE2) permit easy memory expansion with multiple-bank systems.

When  $\overline{CE1}$  is high or CE2 is low, the devices enter standby mode. If inputs are still toggling, the device will consume  $I_{SB}$  power. If the bus is static, then full standby power is reached ( $I_{SB1}$ ).

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and both chip enables ( $\overline{CE1}$ , CE2). Data on the input pins I/O0 through I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or the active-to-inactive edge of  $\overline{CE1}$  or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{OE}$ ) and both chip enables ( $\overline{CE1}$ , CE2), with write enable ( $\overline{WE}$ ) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable is inactive, output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

## Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on $V_{CC}$ relative to GND	$V_{t1}$	-0.50	+7.0	V
Voltage on any pin relative to GND	$V_{t2}$	-0.50	$V_{CC} + 0.50$	V
Power dissipation	$P_D$	–	1.25	W
Storage temperature (plastic)	$T_{stg}$	-55	+125	°C
Ambient temperature with $V_{CC}$ applied	$T_{bias}$	-55	+125	°C
DC current into outputs (low)	$I_{OUT}$	–	50	mA

### Note:

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
X	L	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
L	H	H	H	High Z	Output disable ( $I_{CC}$ )
L	H	H	L	$D_{OUT}$	Read ( $I_{CC}$ )
L	H	L	X	$D_{IN}$	Write ( $I_{CC}$ )

Key: X = don't care, L = low, H = high.



### Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input Voltage	$V_{IH}$	2.2	-	$V_{CC} + 0.5$	V
	$V_{IL}^{(1)}$	$-0.5^{(1)}$	-	0.8	V
Ambient operating temperature (Industrial)	$T_A$	-40	-	85	°C

**Note:**

1  $V_{IL}$  min = -1.5V for pulse width less than 10ns, once per cycle.

### DC operating characteristics (over the operating range)<sup>1</sup>

Parameter	Symbol	Test conditions	AS7C1024C-12		Unit
			Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{IN} = \text{GND to } V_{CC}$	-	5	$\mu\text{A}$
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}, \overline{CE1} = V_{IH}$ or $CE2 = V_{IL}, V_{OUT} = \text{GND to } V_{CC}$	-	5	$\mu\text{A}$
Operating power supply current	$I_{CC}$	$V_{CC} = \text{Max}, \overline{CE1} \leq V_{IL},$ $CE2 \geq V_{IH}, f = f_{\text{Max}},$ $I_{OUT} = 0 \text{ mA}$	-	160	mA
Standby power supply current <sup>1</sup>	$I_{SB}$	$V_{CC} = \text{Max}, \overline{CE1} \geq V_{IH}$ and/or $CE2 \leq V_{IL}, f = f_{\text{Max}}$	-	40	mA
	$I_{SB1}$	$V_{CC} = \text{Max}, \overline{CE1} \geq V_{CC} - 0.2\text{V}$ and/or $CE2 \leq 0.2\text{V}$ $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}, f = 0$	-	10	mA
Output voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	-	0.4	V
	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4	-	V

### Capacitance ( $f = 1 \text{ MHz}, T_a = 25^\circ \text{ C}, V_{CC} = \text{NOMINAL}$ )<sup>2</sup>

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	A, $\overline{CE1}$ , CE2, $\overline{WE}$ , $\overline{OE}$	$V_{IN} = 3\text{dV}$	7	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{OUT} = 3\text{dV}$	8	pF

**Note:**

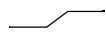
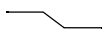

This parameter is guaranteed by device characterization, but is not production tested.



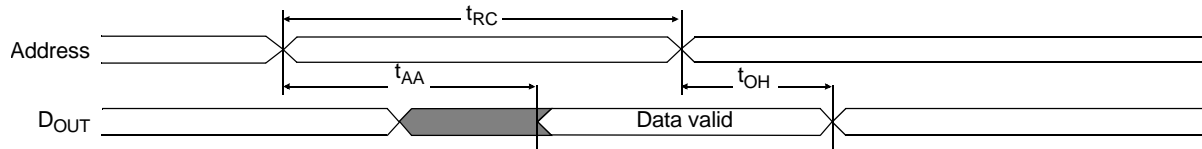
### Read cycle (over the operating range)<sup>3,9</sup>

Parameter	Symbol	AS7C1024C-12		Unit	Notes
		Min	Max		
Read cycle time	$t_{RC}$	12	–	ns	
Address access time	$t_{AA}$	–	12	ns	3
Chip enable ( $\overline{CE1}$ ) access time	$t_{ACE1}$	–	12	ns	3, 12
Chip enable (CE2) access time	$t_{ACE2}$	–	12	ns	3, 12
Output enable ( $\overline{OE}$ ) access time	$t_{OE}$	–	6	ns	
Output hold from address change	$t_{OH}$	4	–	ns	5
$\overline{CE1}$ Low to output in low Z	$t_{CLZ1}$	3	–	ns	4, 5, 12
CE2 High to output in low Z	$t_{CLZ2}$	3	–	ns	4, 5, 12
$\overline{CE1}$ Low to output in high Z	$t_{CHZ1}$	0	6	ns	4, 5, 12
CE2 Low to output in high Z	$t_{CHZ2}$	–	5	ns	4, 5, 12
$\overline{OE}$ Low to output in low Z	$t_{OLZ}$	0	–	ns	4, 5
$\overline{OE}$ High to output in high Z	$t_{OHZ}$	–	5	ns	4, 5
Power up time	$t_{PU}$	0	–	ns	4, 5, 12
Power down time	$t_{PD}$	–	12	ns	4, 5, 12

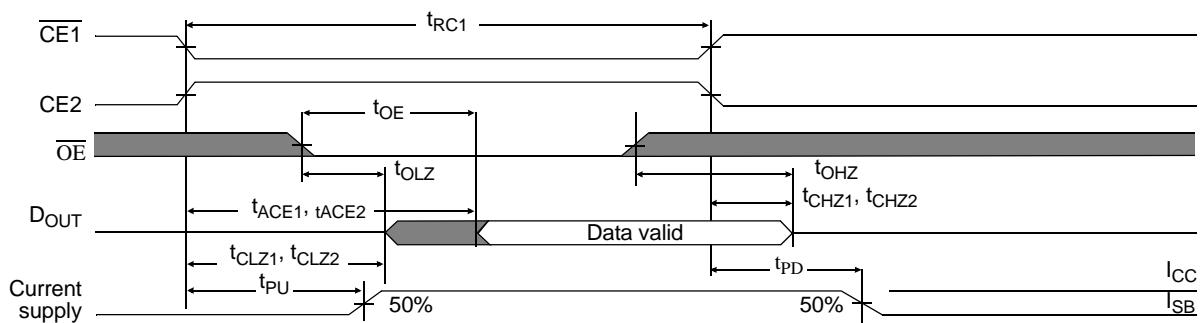
### Key to switching waveforms

 Rising input     
  Falling input     
  Undefined/don't care

### Read waveform 1 (address controlled)<sup>3,6,7,9</sup>



### Read waveform 2 ( $\overline{CE1}$ , CE2, and $\overline{OE}$ controlled)<sup>3,6,8,9,12</sup>

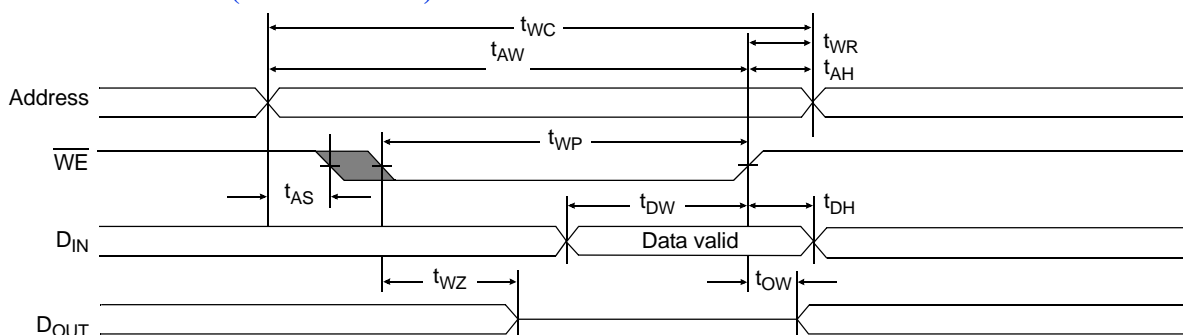




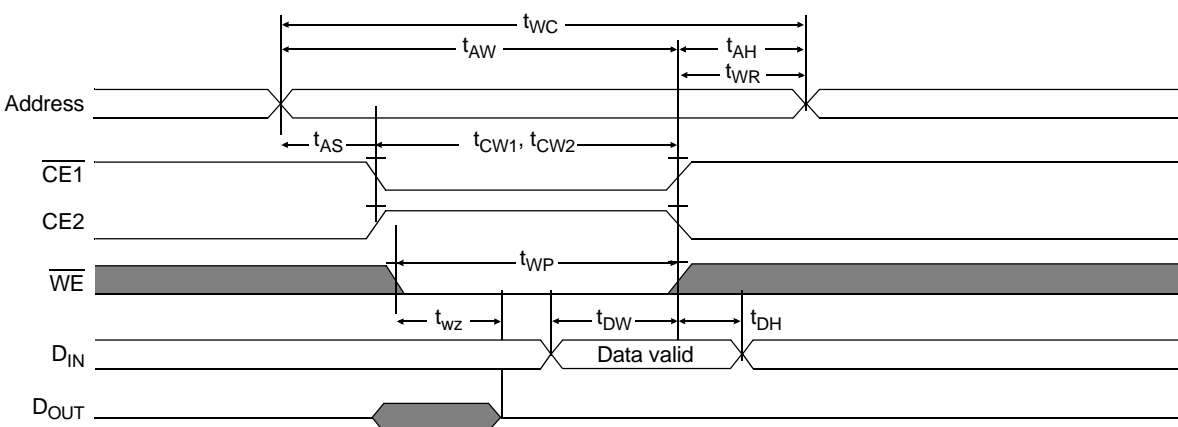
### Write cycle (over the operating range)<sup>11</sup>

Parameter	Symbol	AS7C1024C-12		Unit	Notes
		Min	Max		
Write cycle time	$t_{WC}$	12	–	ns	
Chip enable ( $\overline{CE1}$ ) to write end	$t_{CW1}$	10	–	ns	12
Chip enable (CE2) to write end	$t_{CW2}$	10	–	ns	12
Address setup to write end	$t_{AW}$	10	–	ns	
Address setup time	$t_{AS}$	0	–	ns	12
Write pulse width	$t_{WP}$	8	–	ns	
Write recovery time	$t_{WR}$	0	–	ns	
Address hold from end of write	$t_{AH}$	0	–	ns	
Data valid to write end	$t_{DW}$	7	–	ns	
Data hold time	$t_{DH}$	0	–	ns	4, 5
Write enable to output in high Z	$t_{WZ}$	0	5	ns	4, 5
Output active from write end	$t_{OW}$	3	–	ns	4, 5

### Write waveform 1 ( $\overline{WE}$ controlled)<sup>10,11</sup>



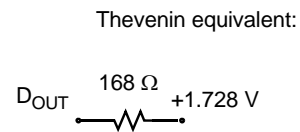
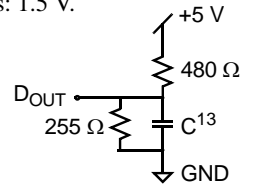
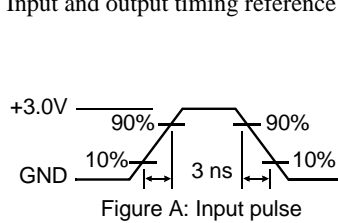
### Write waveform 2 ( $\overline{CE1}$ and CE2 controlled)<sup>10,11,12</sup>





### AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0 V. See Figure A.
- Input rise and fall times: 3 ns. See Figure A.
- Input and output timing reference levels: 1.5 V.



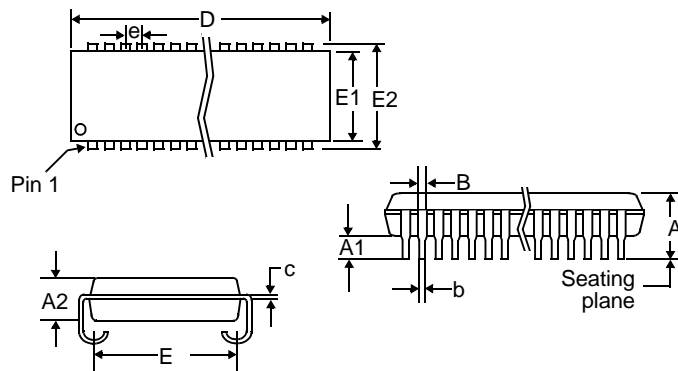
### Notes

- 1 During  $V_{CC}$  power-up, a pull-up resistor to  $V_{CC}$  on  $\overline{CE}$  is required to meet  $I_{SB}$  specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see *AC Test Conditions*, Figures A and B.
- 4  $t_{CLZ}$  and  $t_{CHZ}$  are specified with  $C_L = 5$  pF, as in Figure B. Transition is measured  $\pm 200$  mV from steady-state voltage.
- 5 This parameter is guaranteed, but not 100% tested.
- 6  $\overline{WE}$  is high for read cycle.
- 7  $\overline{CE}$  and  $\overline{OE}$  are low for read cycle.
- 8 Address is valid prior to or coincident with  $\overline{CE}$  transition low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 N/A
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 N/A.
- 13  $C = 30$  pF, except all high Z and low Z parameters where  $C = 5$  pF.



## Package dimensions

32-pin SOJ  
300/400 mil



	32-pin SOJ 300 mil		32-pin SOJ 400 mil	
	Min	Max	Min	Max
A	0.128	0.145	0.132	0.146
A1	0.025	-	0.025	-
A2	0.095	0.105	0.105	0.115
B	0.026	0.032	0.026	0.032
b	0.016	0.020	0.015	0.020
c	0.007	0.010	0.007	0.013
D	0.820	0.830	0.820	0.830
E	0.255	0.275	0.354	0.378
E1	0.295	0.305	0.395	0.405
E2	0.330	0.340	0.435	0.445
e	0.050 BSC		0.050 BSC	

Note: This part is compatible with both pin numbering conventions used by various manufacturers.

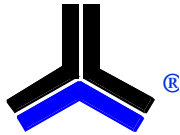


### Ordering Codes

Package	Volt/Temp	12 ns
Plastic SOJ, 300 mil	5V industrial	AS7C1024C-12TJIN
Plastic SOJ, 400 mil	5V industrial	AS7C1024C-12JIN

### Part numbering system

AS7C	1024C	-XX	X	X	X
SRAM prefix	Device number	Access time	Package: J = SOJ 400 mil TJ = SOJ 300 mil	Temperature range I = industrial, -40° C to 85° C	N = LEAD FREE PART



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Part Number: AS7C1024C  
Document Version: v. 1.0

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