



**THE DATASHEET OF  
ADG5423BRMZ-RL7**



## FEATURES

Latch-up immune under all circumstances  
 Human body model (HBM) ESD rating: 8 kV  
 Low on resistance: 13.5  $\Omega$   
 $\pm 9$  V to  $\pm 22$  V dual-supply operation  
 9 V to 40 V single-supply operation  
 48 V supply maximum ratings  
 Fully specified at  $\pm 15$  V,  $\pm 20$  V, +12 V, and +36 V  
 $V_{DD}$  to  $V_{SS}$  analog signal range

## APPLICATIONS

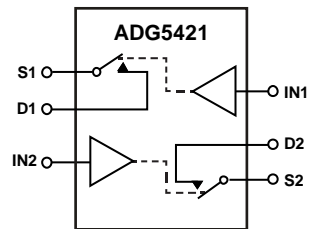
High voltage signal routing  
 Automatic test equipment  
 Analog front-end circuits  
 Precision data acquisition  
 Industrial instrumentation  
 Amplifier gain select  
 Relay replacement

## GENERAL DESCRIPTION

The [ADG5421/ADG5423](#) are monolithic industrial, complementary metal oxide semiconductor (CMOS) analog switches containing two independent latch-up immune single-pole/single-throw (SPST) switches. Each switch conducts equally well in both directions when on, and has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. Both [ADG5421](#) switches are turned on with a Logic 1 input, whereas the [ADG5423](#) has one switch turned on and one switch turned off for a Logic 1 input. The [ADG5423](#) exhibits break-before-make action for use in multiplexer applications.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. The latch-up immune construction and high ESD rating make these switches more robust in harsh environments.

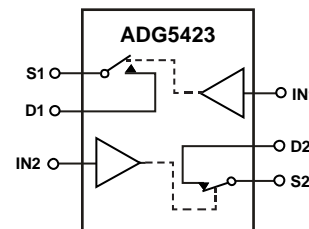
## FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC 0 INPUT

 Figure 1. [ADG5421](#)

11369-001



SWITCHES SHOWN FOR A LOGIC 0 INPUT

 Figure 2. [ADG5423](#)

11369-002

## PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P channel and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.
2. Low  $R_{ON}$  of 13.5  $\Omega$ .
3. Dual-supply operation. For applications where the analog signal is bipolar, the [ADG5421/ADG5423](#) can operate from dual supplies up to  $\pm 22$  V.
4. Single-supply operation. For applications where the analog signal is unipolar, the [ADG5421/ADG5423](#) can operate from a single-rail power supply up to 40 V.
5. 3 V logic compatible digital inputs:  $V_{INH} = 2.0$  V,  $V_{INL} = 0.8$  V.
6. No  $V_L$  logic power supply required.
7. Available in 10-lead MSOP and 10-lead 3 mm  $\times$  3 mm LFCSP packages.

Rev. A

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## REVISION HISTORY

### 1/15—Rev. 0 to Rev. A

Added 10-Lead LFCSP Package.....	Universal
Changes to Table 5.....	7
Added Figure 3, Renumbered Sequentially; Changes to Table 7.....	9
Changes to Figure 5.....	10
Changes to Figure 30.....	14
Updated Outline Dimensions .....	17
Changes to Ordering Guide .....	17

### 9/13—Revision 0: Initial Version

## SPECIFICATIONS

## ±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	13.5			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 25
	15	19	23	$\Omega$ max	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.1			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	0.8	1.3	1.4	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.8			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	2.2	2.7	3.1	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.05$			nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	$\pm 0.25$	$\pm 1$	$\pm 10$	nA max	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ ; see Figure 24
Drain Off Leakage, $I_D$ (Off)	$\pm 0.05$			nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ ; see Figure 24
	$\pm 0.25$	$\pm 1$	$\pm 10$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.1$			nA typ	$V_S = V_D = \pm 10\text{ V}$ ; see Figure 23
	$\pm 0.4$	$\pm 4$	$\pm 20$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	6			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	185			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	220	273	313	ns max	$V_S = 10\text{ V}$ ; see Figure 30
$t_{OFF}$	163			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	196	219	242	ns max	$V_S = 10\text{ V}$ ; see Figure 30
Break-Before-Make Time Delay, $t_D$ (ADG5423 Only)	73			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			21	ns min	$V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 32
Charge Injection, $Q_{INJ}$	95			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 31
Off Isolation	-55			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
Channel-to-Channel Crosstalk	-85			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 29
Total Harmonic Distortion + Noise	0.01			% typ	$R_L = 1\text{ k}\Omega$ , 15 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 27
-3 dB Bandwidth	250			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 28
Insertion Loss	-1			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 28
$C_S$ (Off)	12			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	13			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (On), $C_S$ (On)	44			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	45			$\mu\text{A}$ typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	55		70	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{SS}$	0.001			$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
			1	$\mu\text{A}$ max	
$V_{DD}/V_{SS}$			$\pm 9/\pm 22$	V min/V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

**±20 V DUAL SUPPLY**

$V_{DD} = +20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

**Table 2.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	12.5 14	18	22	$\Omega$ typ $\Omega$ max	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 25 $V_{DD} = +18\text{ V}$ , $V_{SS} = -18\text{ V}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.1			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.8	1.3	1.4	$\Omega$ max	
	2.3 2.7	3.3	3.7	$\Omega$ typ $\Omega$ max	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.05$ $\pm 0.25$	$\pm 1$	$\pm 10$	nA typ nA max	$V_{DD} = +22\text{ V}$ , $V_{SS} = -22\text{ V}$ $V_S = \pm 15\text{ V}$ , $V_D = \mp 15\text{ V}$ ; see Figure 24
Drain Off Leakage, $I_D$ (Off)	$\pm 0.05$ $\pm 0.25$	$\pm 1$	$\pm 10$	nA typ nA max	$V_S = \pm 15\text{ V}$ , $V_D = \mp 15\text{ V}$ ; see Figure 24
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.1$ $\pm 0.4$	$\pm 4$	$\pm 20$	nA typ nA max	$V_S = V_D = \pm 15\text{ V}$ ; see Figure 23
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{GND}$ or $V_{DD}$
Digital Input Capacitance, $C_{IN}$	6			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	168			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 10\text{ V}$ ; see Figure 30
$t_{OFF}$	199	243	276	ns max	$V_S = 10\text{ V}$ ; see Figure 30
	156			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
Break-Before-Make Time Delay, $t_D$ (ADG5423 Only)	184	204	218	ns max	$V_S = 10\text{ V}$ ; see Figure 30
	65			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
Charge Injection, $Q_{INJ}$	120		38	ns min	$V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 32
				pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 31
Off Isolation	-55			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
Channel-to-Channel Crosstalk	-85			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 29
Total Harmonic Distortion + Noise	0.01			% typ	$R_L = 1\text{ k}\Omega$ , 20 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 27
-3 dB Bandwidth	250			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 28
Insertion Loss	-0.8			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 28
$C_S$ (Off)	11			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	12			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (On), $C_S$ (On)	44			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	50		110	$\mu\text{A}$ typ	$V_{DD} = +22\text{ V}$ , $V_{SS} = -22\text{ V}$
	70			$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{SS}$	0.001		1	$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
				$\mu\text{A}$ max	
$V_{DD}/V_{SS}$			$\pm 9/\pm 22$	V min/V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

**12 V SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 3.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	26			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 25
On-Resistance Match Between Channels, $\Delta R_{ON}$	30	38	44	$\Omega$ max	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
	0.1			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	1	1.5	1.6	$\Omega$ max	
	5.5			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	6.8	8.3	12.3	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.05$			nA typ	$V_{DD} = +13.2\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.25$	$\pm 1$	$\pm 10$	nA max	$V_S = 1\text{ V to }10\text{ V}$ , $V_D = 10\text{ V to }1\text{ V}$ ; see Figure 24
Drain Off Leakage, $I_D$ (Off)	$\pm 0.05$			nA typ	$V_S = 1\text{ V to }10\text{ V}$ , $V_D = 10\text{ V to }1\text{ V}$ ; see Figure 24
	$\pm 0.25$	$\pm 1$	$\pm 10$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.1$			nA typ	$V_S = V_D = 1\text{ V to }10\text{ V}$ ; see Figure 23
	$\pm 0.4$	$\pm 4$	$\pm 20$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	6			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	295			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	370	470	540	ns max	$V_S = 8\text{ V}$ ; see Figure 30
$t_{OFF}$	192			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	235	273	295	ns max	$V_S = 8\text{ V}$ ; see Figure 30
Break-Before-Make Time Delay, $t_D$ (ADG5423 Only)	142			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			78	ns min	$V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 32
Charge Injection, $Q_{INJ}$	55			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 31
Off Isolation	-55			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
Channel-to-Channel Crosstalk	-85			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 29
Total Harmonic Distortion + Noise	0.03			% typ	$R_L = 1\text{ k}\Omega$ , $6\text{ V p-p}$ , $f = 20\text{ Hz to }20\text{ kHz}$ ; see Figure 27
-3 dB Bandwidth	290			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 28
Insertion Loss	-1.7			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 28
$C_S$ (Off)	14			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	15			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (On), $C_S$ (On)	38			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	40			$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$
	50		65	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$V_{DD}$			9/40	V min/V max	$GND = 0\text{ V}$ , $V_{SS} = 0\text{ V}$

<sup>1</sup> Guaranteed by design; not subject to production test.

**36 V SINGLE SUPPLY**

$V_{DD} = 36\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 4.**

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analogue Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	14.5			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 25
	16	20	24	$\Omega$ max	$V_{DD} = 32.4\text{ V}$ , $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.1			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$
	0.8	1.3	1.4	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	3.5			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$
	4.3	5.5	6.5	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.05$			nA typ	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V to }30\text{ V}$ , $V_D = 30\text{ V to }1\text{ V}$ ; see Figure 24
	$\pm 0.25$	$\pm 1$	$\pm 10$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.05$			nA typ	$V_S = 1\text{ V to }30\text{ V}$ , $V_D = 30\text{ V to }1\text{ V}$ ; see Figure 24
	$\pm 0.25$	$\pm 1$	$\pm 10$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.1$			nA typ	$V_S = V_D = 1\text{ V to }30\text{ V}$ ; see Figure 23
	$\pm 0.4$	$\pm 4$	$\pm 20$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	6			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	181			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	210	245	280	ns max	$V_S = 18\text{ V}$ ; see Figure 30
$t_{OFF}$	170			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	192	205	220	ns max	$V_S = 18\text{ V}$ ; see Figure 30
Break-Before-Make Time Delay, $t_D$ (ADG5423 Only)	66			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			37	ns min	$V_{S1} = V_{S2} = 18\text{ V}$ ; see Figure 32
Charge Injection, $Q_{INJ}$	110			pC typ	$V_S = 18\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 31
Off Isolation	−55			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
Channel-to-Channel Crosstalk	−85			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 29
Total Harmonic Distortion + Noise	0.01			% typ	$R_L = 1\text{ k}\Omega$ , 18 V p-p, $f = 20\text{ Hz to }20\text{ kHz}$ ; see Figure 27
−3 dB Bandwidth	260			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 28
Insertion Loss	−0.9			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 28
$C_S$ (Off)	13			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	16			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (On), $C_S$ (On)	38			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	80			$\mu\text{A}$ typ	$V_{DD} = 39.6\text{ V}$
	100		130	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$V_{DD}$			9/40	V min/V max	$GND = 0\text{ V}$ , $V_{SS} = 0\text{ V}$

<sup>1</sup> Guaranteed by design; not subject to production test.

**CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx**

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx					$\theta_{JA} = 133.1^{\circ}\text{C/W}$
10-Lead MSOP					
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$	84	58	39	mA maximum	
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$	89	60	41	mA maximum	
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$	67	47	32	mA maximum	
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$	87	59	40	mA maximum	
10-Lead LFCSP					$\theta_{JA} = 48.7^{\circ}\text{C/W}$
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$	129	80	48	mA maximum	
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$	135	83	50	mA maximum	
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$	103	37	43	mA maximum	
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$	132	82	49	mA maximum	

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 6.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	48 V
$V_{DD}$ to GND	-0.3 V to +48 V
$V_{SS}$ to GND	+0.3 V to -48 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	300 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx <sup>2</sup>	Data + 15%
Temperature Range	
Operating	-40°C to +125°C
Storage	-65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, $\theta_{JA}$	
10-Lead MSOP (4-Layer Board)	133.1°C/W
10-Lead LFCSP	48.7°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
Human Body Model (HBM) ESD	8 kV

<sup>1</sup> Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes.  
Limit current to the maximum ratings given.

<sup>2</sup> See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

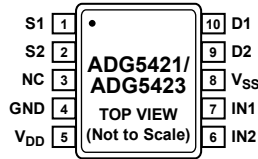
### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

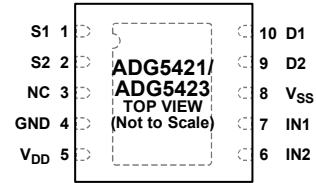
# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES  
1. NC = NO CONNECT. NOT INTERNALLY CONNECTED.

Figure 3. MSOP Pin Configuration

11369-033



NOTES  
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.  
2. EXPOSED PAD TIED TO SUBSTRATE, VSS.

Figure 4. LFCSP Pin Configuration

11369-033

Table 7. Pin Function Descriptions

MSOP Pin No. <sup>1</sup>	LFCSP Pin No.	Mnemonic	Description
1	1	S1	Source Terminal 1. This pin can be an input or output.
2	2	S2	Source Terminal 2. This pin can be an input or output.
3	3	NC	No Connect. Not internally connected.
4	4	GND	Ground (0 V) Reference.
5	5	V <sub>DD</sub>	Most Positive Power Supply Potential.
6	6	IN2	Logic Control Input.
7	7	IN1	Logic Control Input.
8	8	V <sub>SS</sub>	Most Negative Power Supply Potential.
9	9	D2	Drain Terminal 2. This pin can be an input or output.
10	10	D1	Drain Terminal 1. This pin can be an input or output.
N/A	EPAD		Exposed Pad. The exposed pad is tied to substrate, V <sub>SS</sub> .

<sup>1</sup> N/A means not applicable.

Table 8. ADG5421 Truth Table

IN <sub>x</sub>	Switch Conditions
0	Off
1	On

Table 9. ADG5423 Truth Table

IN <sub>x</sub>	Switch 1 Condition	Switch 2 Condition
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

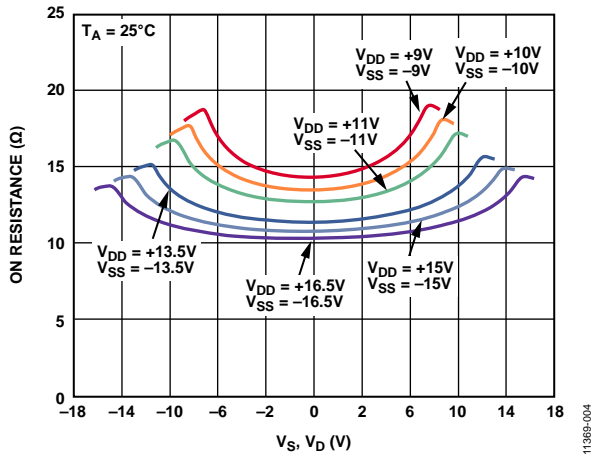


Figure 5. On Resistance as a Function of  $V_S, V_D$  (Dual Supply:  $\pm 10\text{ V}, \pm 15\text{ V}$ )

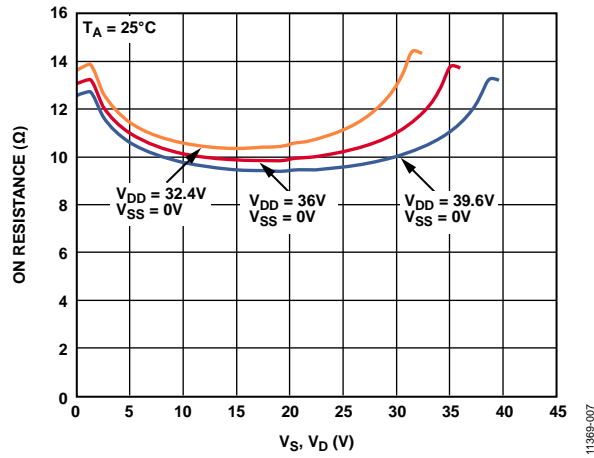


Figure 8. On Resistance as a Function of  $V_S, V_D$  (Single Supply:  $36\text{ V}$ )

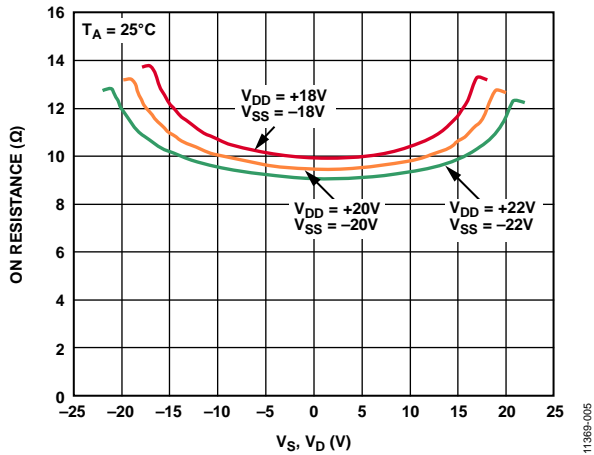


Figure 6. On Resistance as a Function of  $V_S, V_D$  (Dual Supply:  $\pm 20\text{ V}$ )

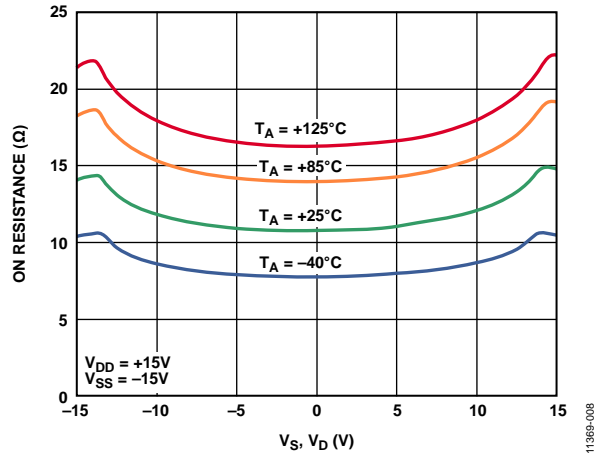


Figure 9. On Resistance as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures,  $\pm 15\text{ V}$  Dual Supply

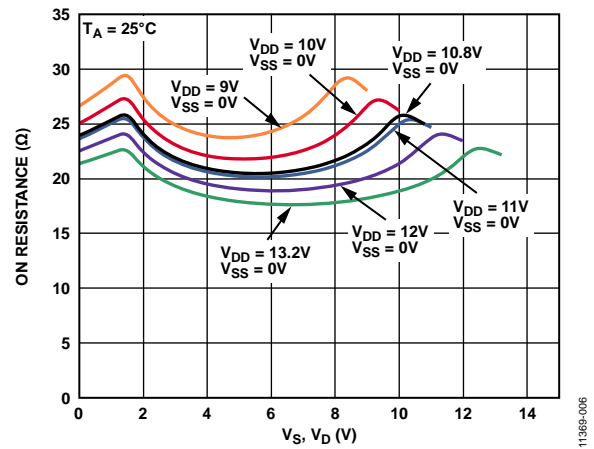


Figure 7. On Resistance as a Function of  $V_S, V_D$  (Single Supply:  $10\text{ V}, 12\text{ V}$ )

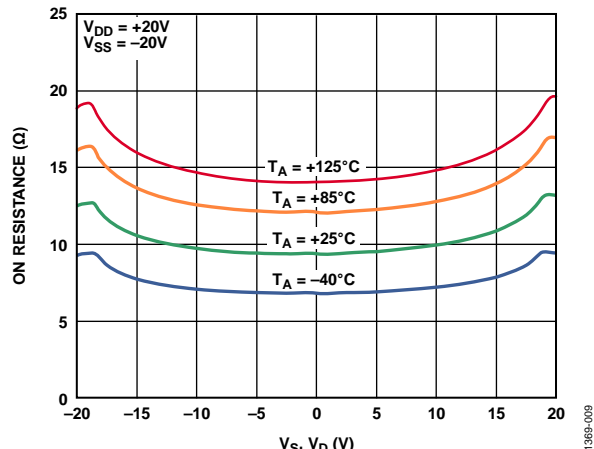


Figure 10. On Resistance as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures,  $\pm 20\text{ V}$  Dual Supply

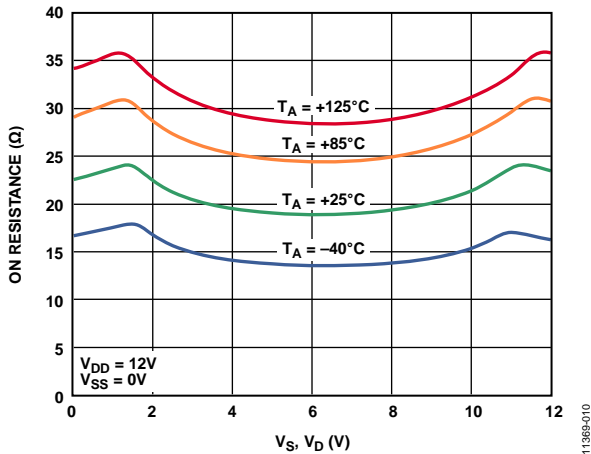


Figure 11. On Resistance as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures, 12 V Single Supply

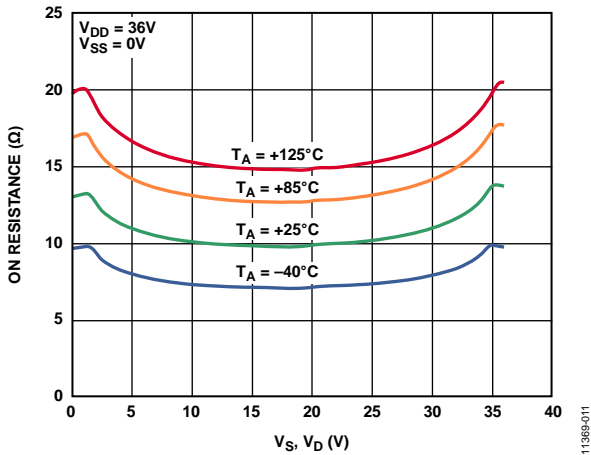


Figure 12. On Resistance as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures, 36 V Single Supply

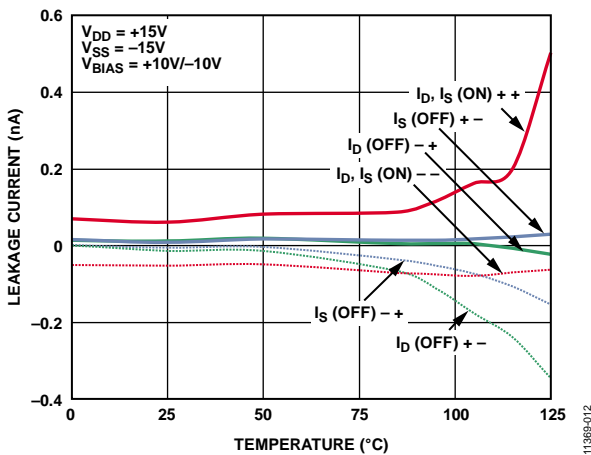


Figure 13. Leakage Currents as a Function of Temperature,  $\pm 15$  V Dual Supply

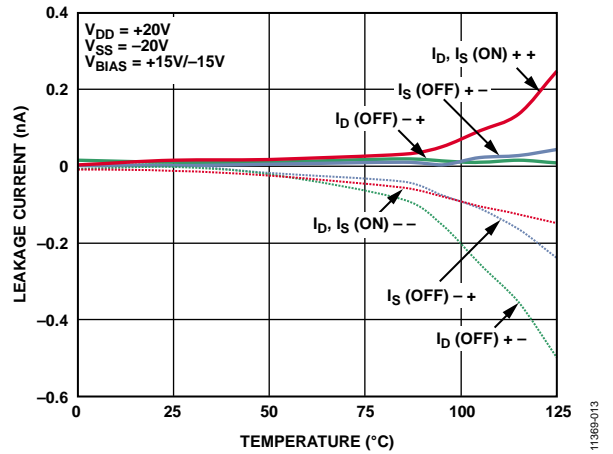


Figure 14. Leakage Currents as a Function of Temperature,  $\pm 20$  V Dual Supply

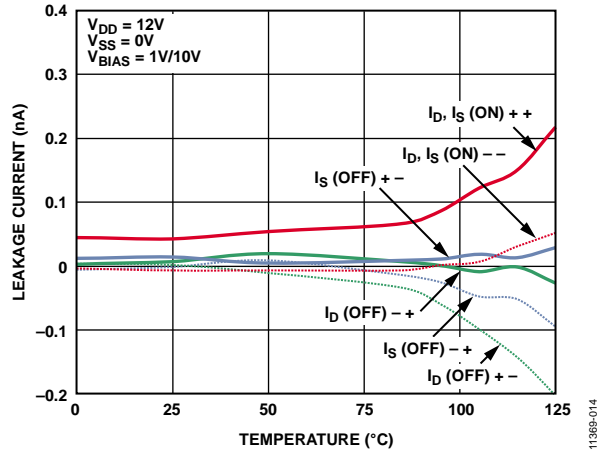


Figure 15. Leakage Currents as a Function of Temperature, 12 V Single Supply

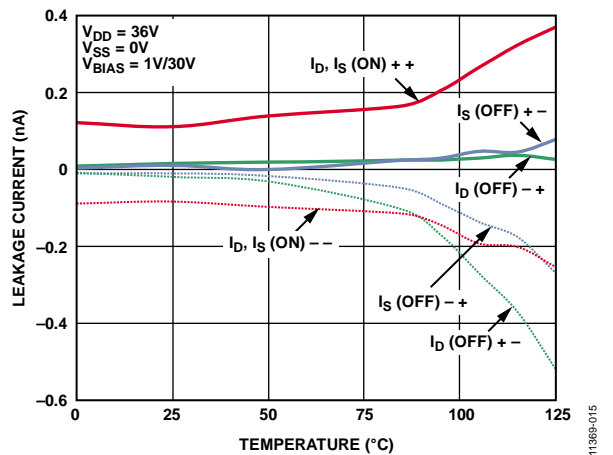


Figure 16. Leakage Currents as a Function of Temperature, 36 V Single Supply

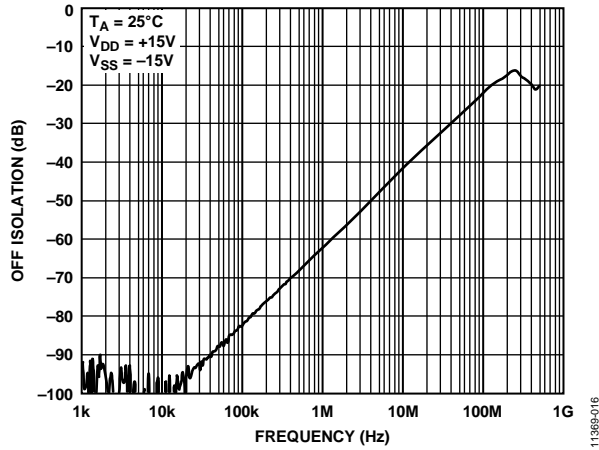


Figure 17. Off Isolation vs. Frequency

11369-016

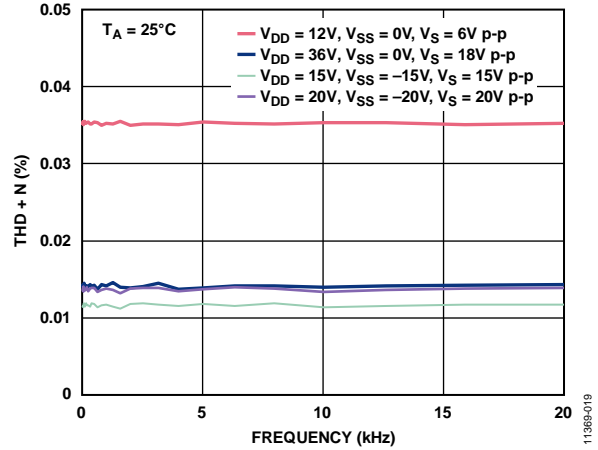


Figure 20. THD + N vs. Frequency

11369-019

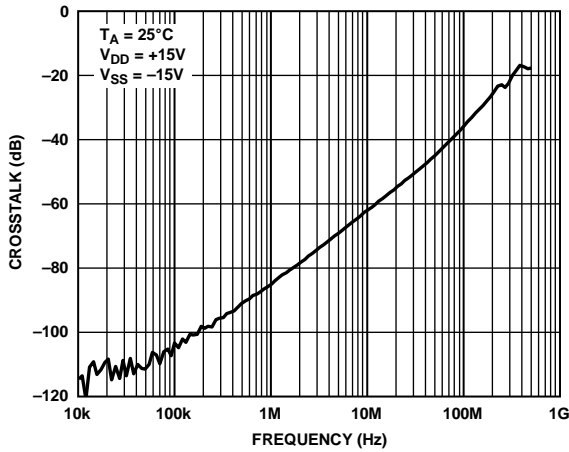


Figure 18. Crosstalk vs. Frequency

11369-017

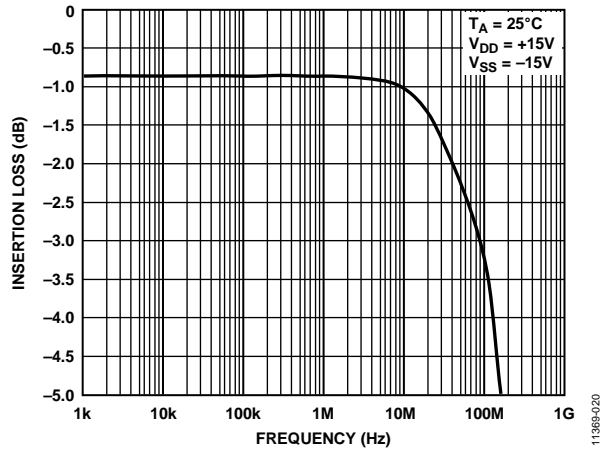


Figure 21. Bandwidth

11369-020

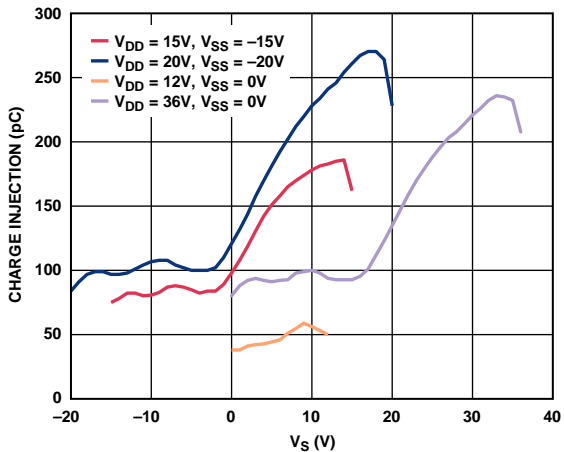


Figure 19. Charge Injection vs. Source Voltage ( $V_S$ )

11369-018

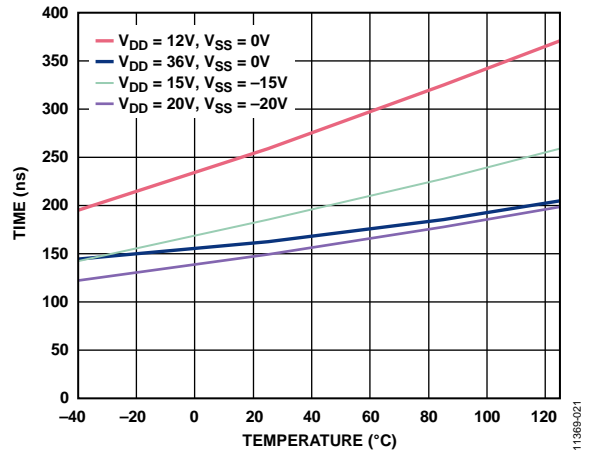


Figure 22.  $t_{\text{TRANSITION}}$  Times vs. Temperature

11369-021

TEST CIRCUITS

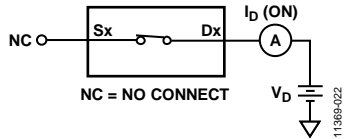


Figure 23. On Leakage

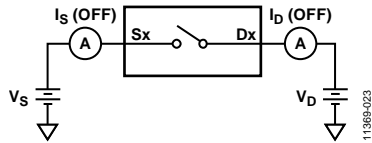


Figure 24. Off Leakage

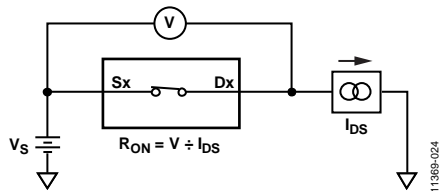


Figure 25. On Resistance

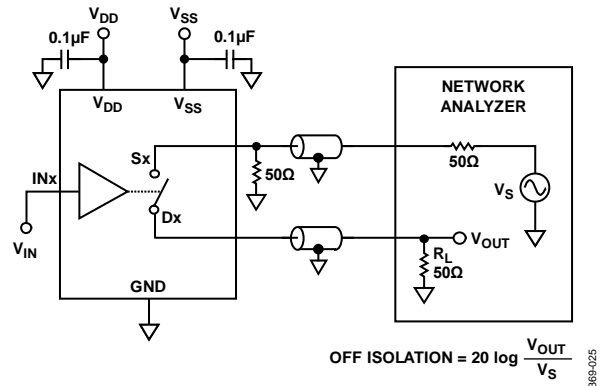


Figure 26. Off Isolation

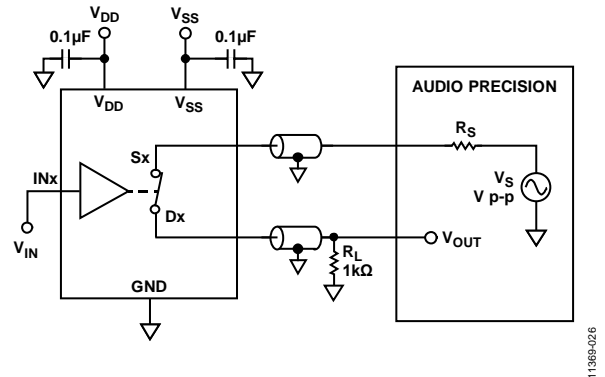


Figure 27. THD + Noise

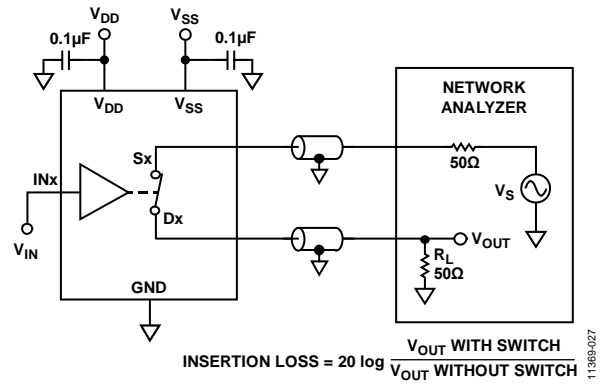
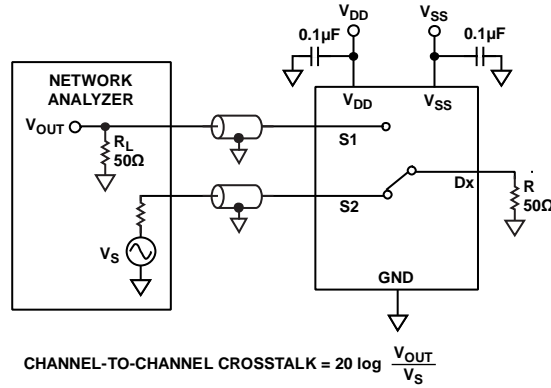
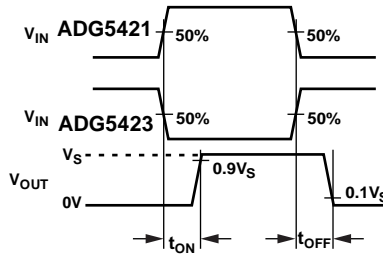
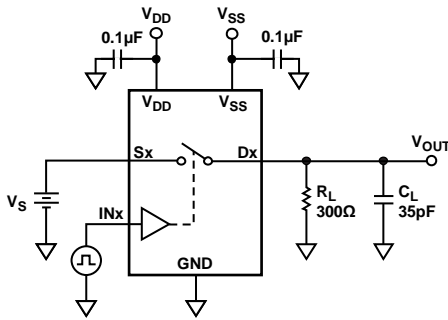


Figure 28. Bandwidth



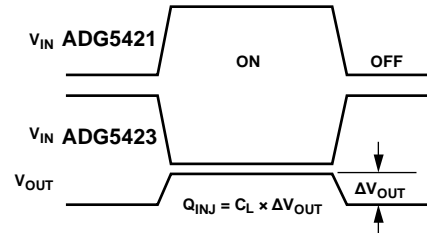
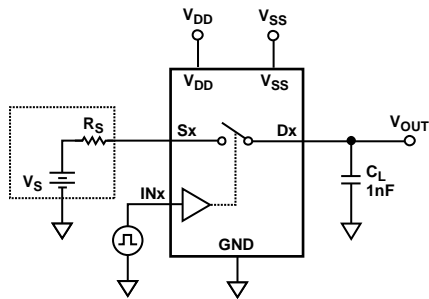
08487-028

Figure 29. Channel-to-Channel Crosstalk



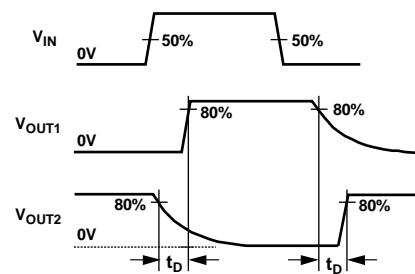
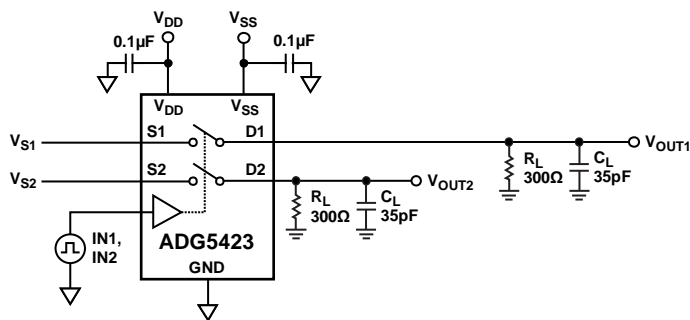
11389-029

Figure 30. Switching Times,  $t_{\text{ON}}$  and  $t_{\text{OFF}}$



11389-030

Figure 31. Charge Injection



11389-031

Figure 32. Break-Before-Make Time Delay

## TERMINOLOGY

### **I<sub>DD</sub>**

I<sub>DD</sub> represents the positive supply current.

### **I<sub>SS</sub>**

I<sub>SS</sub> represents the negative supply current.

### **V<sub>D</sub>, V<sub>S</sub>**

V<sub>D</sub> and V<sub>S</sub> represent the analog voltage on Terminal D and Terminal S, respectively.

### **R<sub>ON</sub>**

R<sub>ON</sub> is the ohmic resistance between Terminal D and Terminal S.

### **ΔR<sub>ON</sub>**

ΔR<sub>ON</sub> represents the difference between the R<sub>ON</sub> of any two channels.

### **R<sub>FLAT (ON)</sub>**

R<sub>FLAT (ON)</sub> represents the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

### **I<sub>S</sub> (Off)**

I<sub>S</sub> (Off) is the source leakage current with the switch off.

### **I<sub>D</sub> (Off)**

I<sub>D</sub> (Off) is the drain leakage current with the switch off.

### **I<sub>D</sub> (On), I<sub>S</sub> (On)**

I<sub>D</sub> (On) and I<sub>S</sub> (On) represent the channel leakage currents with the switch on.

### **V<sub>INL</sub>**

V<sub>INL</sub> is the maximum input voltage for Logic 0.

### **V<sub>INH</sub>**

V<sub>INH</sub> is the minimum input voltage for Logic 1.

### **I<sub>INL</sub>, I<sub>INH</sub>**

I<sub>INL</sub> and I<sub>INH</sub> represent the low and high input currents of the digital inputs.

### **C<sub>D</sub> (Off)**

C<sub>D</sub> (Off) represents the off switch drain capacitance, which is measured with reference to ground.

### **C<sub>S</sub> (Off)**

C<sub>S</sub> (Off) represents the off switch source capacitance, which is measured with reference to ground.

### **C<sub>D</sub> (On), C<sub>S</sub> (On)**

C<sub>D</sub> (On) and C<sub>S</sub> (On) represent on switch capacitances, which are measured with reference to ground.

### **C<sub>IN</sub>**

C<sub>IN</sub> represents digital input capacitance.

### **t<sub>ON</sub>**

t<sub>ON</sub> represents the delay time between the 50% and 90% points of the digital input and switch on condition.

### **t<sub>OFF</sub>**

t<sub>OFF</sub> represents the delay time between the 50% and 90% points of the digital input and switch off condition.

### **t<sub>D</sub>**

t<sub>D</sub> represents the off time measured between the 80% point of both switches when switching from one address state to another.

### **Off Isolation**

Off isolation is a measure of unwanted signal coupling through an off channel.

### **Charge Injection**

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

### **Crosstalk**

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### **Bandwidth**

Bandwidth is the frequency at which the output is attenuated by 3 dB from its dc level.

### **Total Harmonic Distortion + Noise (THD + N)**

The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

## APPLICATIONS INFORMATION

The [ADG54xx](#) family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The [ADG5421/ADG5423](#) high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from  $\pm 9$  V to  $\pm 22$  V. The [ADG5421/ADG5423](#) (as well as other select devices within this family) achieve an 8 kV human body model ESD rating, which provides a robust solution, eliminating the need for separate protection circuitry designs in some applications.

### TRENCH ISOLATION

In the [ADG5421/ADG5423](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated, and the result is a completely latch-up immune switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. The two transistors form a silicon-controlled rectifier (SCR) type circuit, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up immune switch.

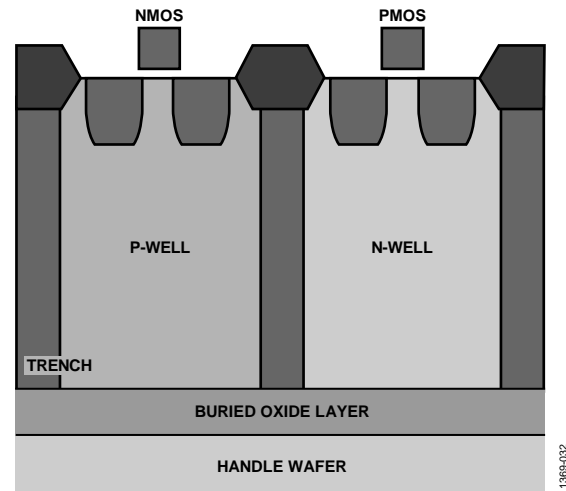


Figure 33. Trench Isolation

11389-032



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