THE DATASHEET OF

AD9094BCPZ-1000

www.win-source.net 0086-755-83957316

8-Bit, 1 GSPS, JESD204B, Quad ADC

Data Sheet **AD9094**

FEATURES

- JESD204B (Subclass 1 and Subclass 0) coded serial digital outputs
  - Lane rates up to 15 Gbps
- 1.6 W total power at 1 GSPS
  - 400 mW per ADC channel
- SFDR: 71 dBFS at 611 MHz (1.44 V p-p input range)
- SNR: 48.6 dBFS at 611 MHz (1.44 V p-p input range)
- SINAD: 48.5 dBFS at 611 MHz (1.44 V p-p input range)
- 0.9 V, 1.8 V, and 2.5 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Analog input buffer
- On-chip dithering to improve small signal linearity
- Flexible differential input voltage range
  - 1.44 V p-p to 2.16 V p-p (1.44 V p-p default)
- 1.4 GHz analog input full power bandwidth
- Fast detect bits for efficient AGC implementation
- Differential clock input
- Integer input clock divide by 1, 2, 4, or 8
- On-chip temperature diode
- Flexible JESD204B lane configurations

APPLICATIONS

- Laser imaging, detection, and ranging (LIDAR)
- Communications
- Digital oscilloscope (DSO)
- Ultrawideband satellite receivers
- Instrumentation

GENERAL DESCRIPTION

The AD9094 is an 8-bit, 1 GSPS, quad analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. The device is designed to sample wide bandwidth analog signals up to 1.4 GHz. The AD9094 is optimized for wide input bandwidth, a high sampling rate, high works linearity, and low power in a small package.

The quad-ADC cores feature multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs that support a variety of user-selectable input ranges. An integrated voltage reference facilitates design considerations. The analog inputs and clock signals are differential inputs.

Users can configure each pair of intermediate frequency (IF) receiver outputs onto either one or two lanes of JESD204B Subclass 1 or Subclass 0, high speed, serialized outputs, depending on the sample rate and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF±, SYNCINB±AB, and SYNCINB±CD input pins.

The AD9094 has flexible power-down options that allow significant power savings when desired. To program the power down options, use the 1.8 V capable, serial port interface (SPI).

The AD9094 is available in a Pb-free, 72-lead, lead frame chip scale package (LFCSP) and is specified over a junction temperature range of −40°C to +105°C. This product may be protected by one or more U.S. or international patents.

Note that throughout this data sheet, multifunction pins, such as PDWN/STBY, are referred to either by the entire pin name or by a single function of the pin, for example, PDWN, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Low power consumption per channel.
2. JESD204B lane rate support up to 15 Gbps.
3. Wide, full power bandwidth that supports IF sampling of signals up to 1.4 GHz.
4. Buffered inputs that ease filter design and implementation.
5. Programmable, fast overrange detection.
6. On-chip temperature diode for system thermal management.

Rev. A Document Feedback

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REVISION HISTORY

7/2024—Rev. 0 to Rev. A

Updated Outline Dimensions ... 67

10/2020—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

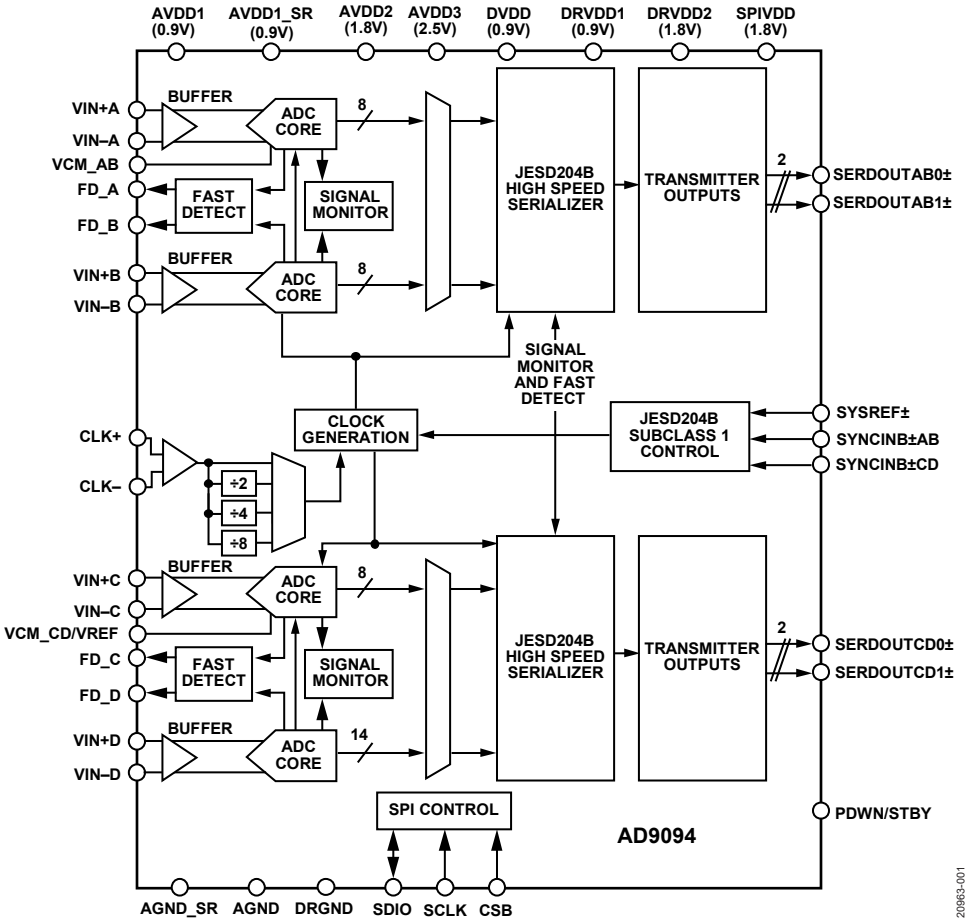


Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = AVDD1_SR = DVDD = DRVDD1 = 0.9 V, AVDD2 = DRVDD2 = SPIVDD = 1.8 V, AVDD3 = 2.5 V, 1 GSPS, clock divider = 2, 1.44 V p-p full-scale differential input, 0.5 V internal reference, analog input amplitude (A_{IN}) = −1.0 dBFS, and default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating T_J range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	8			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error		0		% FSR
Offset Matching		0		% FSR
Gain Error	−5.6		+5.6	% FSR
Gain Matching		1.0	3.7	% FSR
Differential Nonlinearity (DNL)	−0.1	±0.0	+0.1	LSB
Integral Nonlinearity (INL)	−0.3	±0	+0.3	LSB
TEMPERATURE DRIFT				
Offset Error		49.5		ppm/°C
Gain Error		172.7		ppm/°C
INTERNAL VOLTAGE REFERENCE		0.5		V
INPUT REFERRED NOISE		2.6		LSB rms
ANALOG INPUTS				
Differential Input Voltage Range (Programmable)	1.44	1.44	2.16	V p-p
Common-Mode Voltage (V_{CM})		1.43		V
Differential Input Capacitance[1]		1.75		pF
Differential Input Resistance		200		Ω
Analog Input Full Power Bandwidth		1.4		GHz
POWER SUPPLY				
AVDD1	0.877	0.9	0.923	V
AVDD1_SR	0.877	0.9	0.923	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.877	0.9	0.923	V
DRVDD1	0.877	0.9	0.923	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
AVDD1 Current, I_{AVDD1}		420	575	mA
AVDD1_SR Current, I_{AVDD1_SR}		25	60	mA
AVDD2 Current, I_{AVDD2}		440	520	mA
AVDD3 Current, I_{AVDD3}		60	71	mA
DVDD Current, I_{DVDD}[2]		110	196	mA
DRVDD1 Current, I_{DRVDD1}[1]		85	205	mA
DRVDD2 Current, I_{DRVDD2}[1]		30	38	mA
SPIVDD Current, I_{SPIVDD}		0.65	0.80	mA

Parameter	Min	Typ	Max	Unit
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)[2]		1.6	2.0	W
Power-Down Dissipation		0.3		mW
Standby[3]		1.2		W

[1] All lanes are running. Power dissipation on DRVDD1 changes with the lane rate and number of lanes used.
[2] Full bandwidth mode.
[3] Standby mode is controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = AVDD1_SR = DVDD = DRVDD1 = 0.9 V, AVDD2 = DRVDD2 = SPIVDD = 1.8 V, AVDD3 = 2.5 V, 1 GSPS, clock divider = 2, 1.44 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, and default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the T_J range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 2.

	Analog Input Full Scale = 1.44 V p-p			Analog Input Full Scale = 1.80 V p-p			Analog Input Full Scale = 2.16 V p-p			
Parameter[1, 2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		1.44			1.80			2.16		V p-p
NOISE DENSITY[3]		−136.1			−136.1			−136.2		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[4]										
f_{IN} = 10 MHz		49.1			49.2			49.2		dBFS
f_{IN} = 155 MHz		49.1		47.4	49.2			49.2		dBFS
f_{IN} = 451 MHz		49.1			49.2			49.2		dBFS
f_{IN} = 611 MHz		48.6			48.7			48.6		dBFS
f_{IN} = 871 MHz		48.5			48.5			48.5		dBFS
f_{IN} = 1391 MHz		48.4			48.5			48.4		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)										
f_{IN} = 10 MHz		49.1			49.2			49.2		dBFS
f_{IN} = 155 MHz		49.1		46.2	49.2			49.2		dBFS
f_{IN} = 451 MHz		49.1			49.2			49.2		dBFS
f_{IN} = 611 MHz		48.5			48.7			48.5		dBFS
f_{IN} = 871 MHz		48.5			48.4			48.3		dBFS
f_{IN} = 1391 MHz		48.4			48.4			48.2		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)										
f_{IN} = 10 MHz		7.9			7.9			7.9		Bits
f_{IN} = 155 MHz		7.9		7.4	7.9			7.9		Bits
f_{IN} = 451 MHz		7.9			7.9			7.9		Bits
f_{IN} = 611 MHz		7.8			7.8			7.8		Bits
f_{IN} = 871 MHz		7.8			7.7			7.7		Bits
f_{IN} = 1391 MHz		7.7			7.7			7.7		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)										
f_{IN} = 10 MHz		71			72			71		dBFS
f_{IN} = 155 MHz		71		60	72			70		dBFS
f_{IN} = 451 MHz		71			72			71		dBFS
f_{IN} = 611 MHz		71			66			63		dBFS
f_{IN} = 871 MHz		70			65			63		dBFS
f_{IN} = 1391 MHz		70			67			65		dBFS

Parameter[1, 2]	Analog Input Full Scale = 1.44 V p-p			Analog Input Full Scale = 1.80 V p-p			Analog Input Full Scale = 2.16 V p-p			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
WORST OTHER, EXCLUDING SECOND AND THIRD HARMONIC										
f_{IN} = 10 MHz		−70			−71			−70		dBFS
f_{IN} = 155 MHz		−70			−72	−64		−70		dBFS
f_{IN} = 451 MHz		−71			−72			−71		dBFS
f_{IN} = 611 MHz		−72			−74			−72		dBFS
f_{IN} = 871 MHz		−73			−72			−73		dBFS
f_{IN} = 1391 MHz		−75			−72			−75		dBFS
CROSSTALK[5]		82			82			82		dB
FULL POWER BANDWIDTH[6]		1.4			1.4			1.4		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] f_{IN} is the analog input frequency.
[3] Noise density is measured at a low analog input frequency (f_A) of 30 MHz.
[4] See Table 9 for recommended settings for the buffer current setting.
[5] Crosstalk is measured at 155 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[6] Full power bandwidth is measured with the circuit shown in Figure 44.

DIGITAL SPECIFICATIONS

AVDD1 = 0.9 V, AVDD1_SR = 0.9 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.9 V, DRVDD1 = 0.9 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 1 GSPS, clock divider = 2, 1.44 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, and default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the T_J range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK±)				
Logic Compliance		LVDS/LVPECL[1]		
Differential Input Voltage	600	800	1600	mV p-p
Input V_{CM}		0.69		V
Differential Input Resistance		32		kΩ
Input Capacitance			0.9	pF
SYSTEM REFERENCE (SYSREF) INPUTS (SYSREF±)[2]				
Logic Compliance		LVDS/LVPECL[1]		
Differential Input Voltage	400	800	1800	mV p-p
Input V_{CM}	0.6	0.69	2.2	V
Differential Input Resistance	18	22		kΩ
Input Capacitance (Single-Ended per Pin)		0.7		pF
LOGIC INPUTS (PDWN/STBY)				
Logic Compliance		CMOS[1]		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		10		MΩ

Parameter	Min	Typ	Max	Unit
LOGIC INPUTS (SDIO, SCLK, AND CSB)				
Logic Compliance		CMOS[1]		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		56		kΩ
LOGIC OUTPUT (SDIO)				
Logic Compliance		CMOS[1]		
Logic 1 Voltage (I_{OH} = 800 µA)[3]	SPIVDD − 0.45 V			V
Logic 0 Voltage (I_{OL} = 50 µA)[3]	0		0.45	V
SYNCIN INPUT (SYNCINB±AB AND SYNCINB±CD)				
Logic Compliance		LVDS/LVPECL/CMOS[1]		
Differential Input Voltage	400	800	1800	mV p-p
Input V_{CM}	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		kΩ
Input Capacitance (Single-Ended per Pin)		0.7		pF
LOGIC OUTPUTS (FD_A, FD_B, FD_C, AND FD_D)				
Logic Compliance		CMOS[1]		
Logic 1 Voltage	0.8 × SPIVDD			V
Logic 0 Voltage	0		0.5	V
Input Resistance		56		kΩ
DIGITAL OUTPUTS (SERDOUTABx± AND SERDOUTCDx±, x = 0 OR 1)				
Logic Compliance		CML[1]		
Differential Output Voltage		455.8		mV p-p
Short-Circuit Current ($I_{D\ SHORT}$)		15		mA
Differential Termination Impedance		100		Ω

[1] LVDS is low voltage differential signaling, LVPECL is low voltage positive/pseudo emitter coupled logic, CMOS is complementary metal-oxide semiconductor, and CML is current mode logic.
[2] DC-coupled input only.
[3] I_{OH} is the sinking current when the pin has a logic level = 0, and I_{OL} is sourcing current when the pin has a logic level = 1.

SWITCHING SPECIFICATIONS

AVDD1 = 0.9 V, AVDD1_SR = 0.9 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.9 V, DRVDD1 = 0.9 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 1 GSPS, clock divider = 2, 1.44 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, and default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the T_J range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate (at CLK± Pins)	0.3		2.4	GHz
Maximum Sample Rate[1]	1000			MSPS
Minimum Sample Rate[2]	240			MSPS
Clock Pulse Width High	125			ps
Clock Pulse Width Low	125			ps
OUTPUT				
Unit Interval (UI)[3]	66.67	100	593	ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		31.25		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		31.37		ps
Phase-Locked Look (PLL) Lock Time		5		ms
Data Rate per Channel (Nonreturn to Zero (NRZ))[4]	1.6875	10	15	Gbps

Parameter	Min	Typ	Max	Unit
LATENCY[5]				
Pipeline Latency		45		Sample clock cycles
Fast Detect Latency			30	Sample clock cycles
WAKE-UP TIME				
From Standby		3		ms
From Power-Down		10		ms
APERTURE				
Aperture Delay (t_A)		160		ps
Aperture Uncertainty (Jitter, t_j)		44		fs rms
Out of Range Recovery Time		1		Sample clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 240 MSPS with L = 2 or L = 1. Use SPI Register 0x011A to reduce the threshold of the clock detection circuit.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] The default is L = 2 for each link. This number can be changed based on the sample rate and decimation ratio.
[5] L = 2, M = 2, F = 2 for each link. See the Setting Up the AD9094 Digital Interface section for more information.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		–44.8		ps
t_{H_SR}	Device clock to SYSREF+ hold time		64.4		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	SCLK period	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum SCLK period required in a logic high state	10			ns
t_{LOW}	Minimum SCLK period required in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

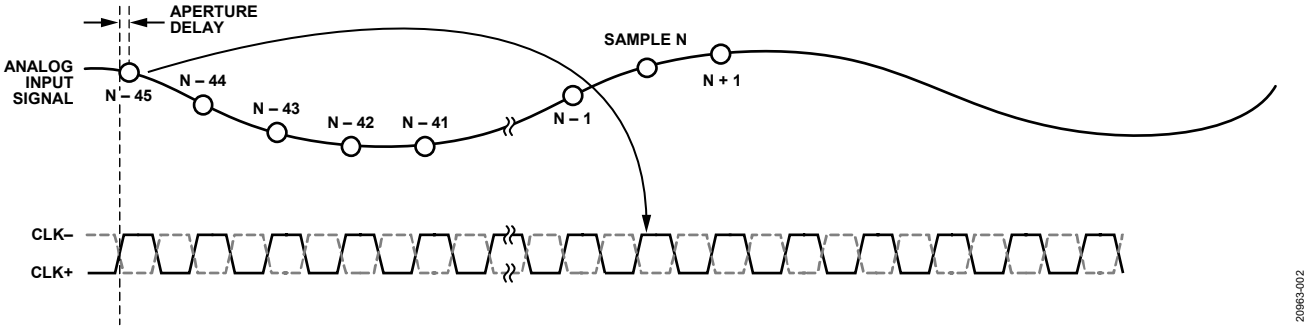


Figure 2. Data Output Timing (Full Bandwidth Mode; L = 2, M = 2, F = 2), N = Sample Number

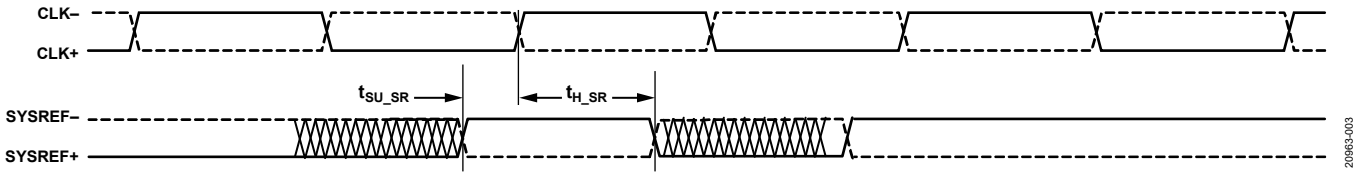


Figure 3. SYSREF± Setup and Hold Timing

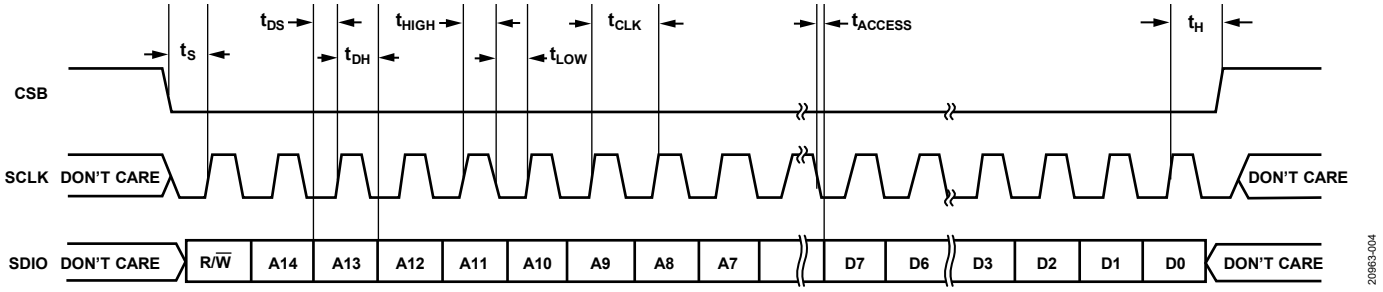


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to AGND	2.00 V
VIN±x to AGND	−0.3 V to AVDD3 + 0.3 V
CLK± to AGND	−0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	−0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND_SR	0 V to 2.5 V
SYNCINB±AB/SYNCINB±CD to DRGND	0 V to 2.5 V
Environmental	
Operating Junction Temperature Range	−40°C to +105°C
Maximum Junction Temperature	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_BOT} is the bottom junction to case thermal resistance.

Table 7. Thermal Resistance

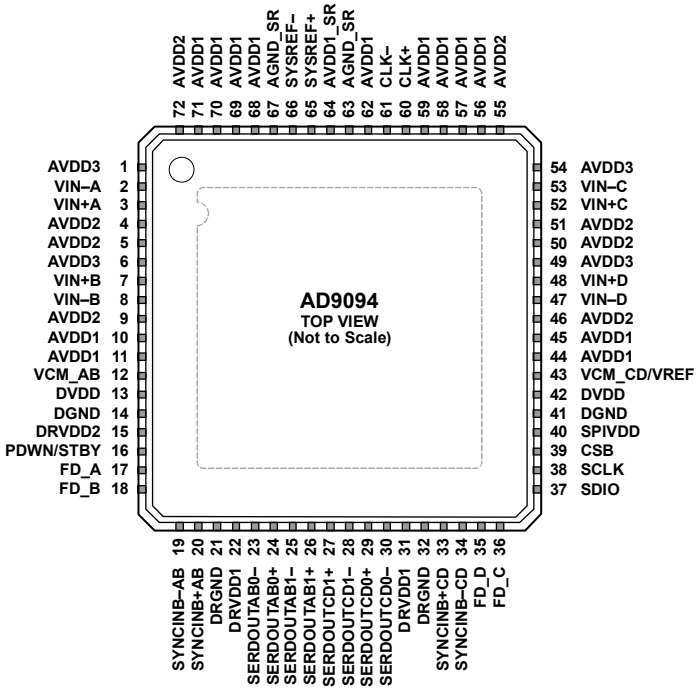
Package Type	PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_BOT}	Unit
CP-72-10	JEDEC 2s2p Board	0.0	21.58[1, 2]	1.95[1, 3]	°C/W
		1.0	17.94[1, 2]	N/A[4]	°C/W
		2.5	16.58[1, 2]	N/A[4]	°C/W
	10-Layer Board	0.0	9.74	1.00	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD 883, Method 1012.1.
[4] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. ANALOG GROUND. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFERENCE FOR AVDDx, SPIVDD, DVDD, DRVDD1, AND DRVDD2. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

20963-005

Figure 5. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 6, 49, 54	AVDD3	Supply	Analog Power Supply (2.5 V Nominal).
2, 3	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
4, 5, 9, 46, 50, 51, 55, 72	AVDD2	Supply	Analog Power Supply (1.8 V Nominal).
7, 8	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
10, 11, 44, 45, 56 to 59, 62, 68 to 71	AVDD1	Supply	Analog Power Supply (0.9 V Nominal).
12	VCM_AB	Output	Common-Mode Level Bias Output for Analog Input Channel A and Channel B.
13, 42	DVDD	Supply	Digital Power Supply (0.9 V Nominal).
14, 41	DGND	Ground	Ground Reference for DVDD and SPIVDD.
15	DRVDD2	Supply	Digital Power Supply for JESD204B PLL (1.8 V Nominal).
16	PDWN/STBY	Input	Power-Down Input/Standby (Active High). The operation of PDWN/STBY depends on the mode that the device is placed in through the SPI and can be configured as either power-down or standby. PDWN/STBY requires an external 10 kΩ pull-down resistor.
17, 18, 35, 36	FD_A, FD_B, FD_D, FD_C	Output	Fast Detect Outputs for Channel A, Channel B, Channel C, and Channel D, Respectively.
19	SYNCINB−AB	Input	Active Low JESD204B LVDS Sync Input Complement for Channel A and Channel B.
20	SYNCINB+AB	Input	Active Low JESD204B LVDS/CMOS Sync Input True for Channel A and Channel B.
21, 32	DRGND	Ground	Ground Reference for DRVDD1 and DRVDD2.
22, 31	DRVDD1	Supply	Digital Power Supply for SERDOUTABx± and SERDOUTCDx± (0.9 V Nominal).

Pin No.	Mnemonic	Type	Description
23, 24	SERDOUTAB0−, SERDOUTAB0+	Output	Lane 0 Output Data Complement/True for Channel A and Channel B.
25, 26	SERDOUTAB1−, SERDOUTAB1+	Output	Lane 1 Output Data Complement/True for Channel A and Channel B.
27, 28	SERDOUTCD1+, SERDOUTCD1−	Output	Lane 1 Output Data True/Complement for Channel C and Channel D.
29, 30	SERDOUTCD0+, SERDOUTCD0−	Output	Lane 0 Output Data True/Complement for Channel C and Channel D.
33	SYNCINB+CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input True for Channel C and Channel D.
34	SYNCINB−CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input Complement for Channel C and Channel D.
37	SDIO	Input/ Output	SPI Serial Data Input/Output.
38	SCLK	Input	SPI Serial Clock.
39	CSB	Input	SPI Chip Select (Active Low).
40	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V Nominal).
43	VCM_CD/VREF	Output/ Input	Common-Mode Level Bias Output for Analog Input Channel C and Channel D or 0.5 V Reference Voltage Input. VCM_CD/VREF is configurable through the SPI as an output or an input. Use VCM_CD/VREF as the common-mode level bias output when using the internal reference. VCM_CD/VREF requires a 0.5 V reference voltage input when using an external voltage reference source.
47, 48	VIN−D, VIN+D	Input	ADC D Analog Input Complement/True.
52, 53	VIN+C, VIN−C	Input	ADC C Analog Input True/Complement.
60, 61	CLK+, CLK−	Input	Clock Input True/Complement.
63, 67	AGND_SR	Ground	Ground Reference for SYSREF±.
64	AVDD1_SR	Supply	Analog Power Supply for SYSREF± (0.9 V Nominal).
65, 66	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement. DC-coupled input only.
	AGND/EPAD		Exposed Pad. Analog ground. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx, SPIVDD, DVDD, DRVDD1, and DRVDD2. This exposed pad must be connected to ground for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = AVDD1_SR = DVDD = DRVDD1 = 0.9 V, AVDD2 = DRVDD2 = SPIVDD = 1.8 V, AVDD3 = 2.5 V, 1 GSPS, clock divider = 2, 1.44 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, and default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the T_J range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

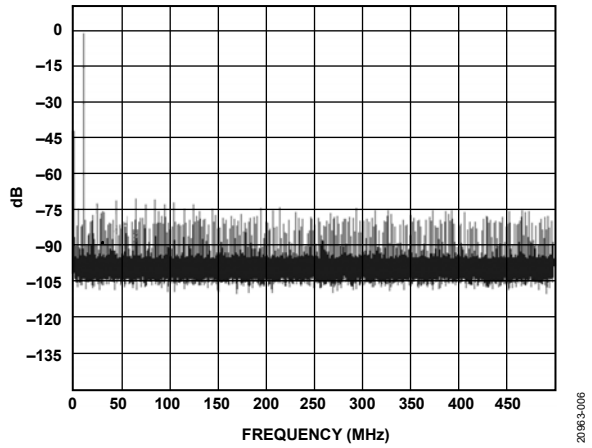


Figure 6. Single-Tone Fast Fourier Transform (FFT) with f_{IN} = 10 MHz, Signal to Noise Ratio Full Scale (SNRFS) = 49.1 dBFS, SFDR = 71 dBFS, SINAD = 49.1 dBFS

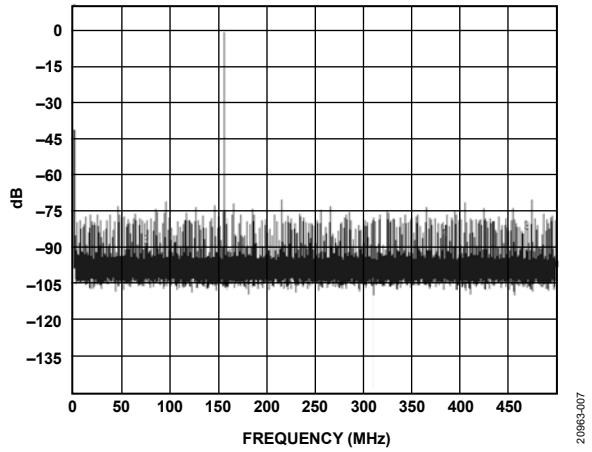


Figure 7. Single-Tone FFT with f_{IN} = 155 MHz, SNRFS = 49.1 dBFS, SFDR = 71 dBFS, SINAD = 49.1 dBFS

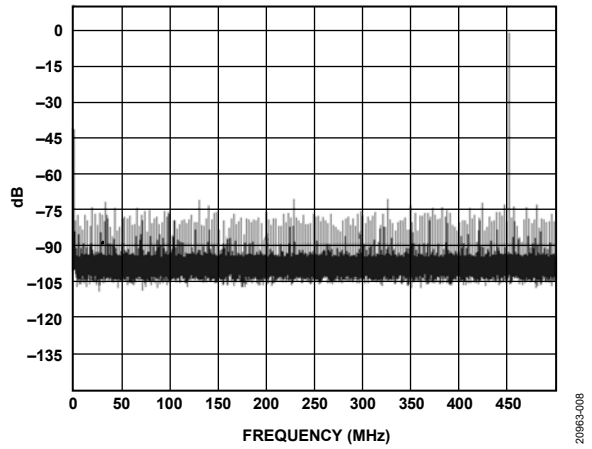


Figure 8. Single-Tone FFT with f_{IN} = 451 MHz, SNRFS = 49.1 dBFS, SFDR = 71 dBFS, SINAD = 49.1 dBFS

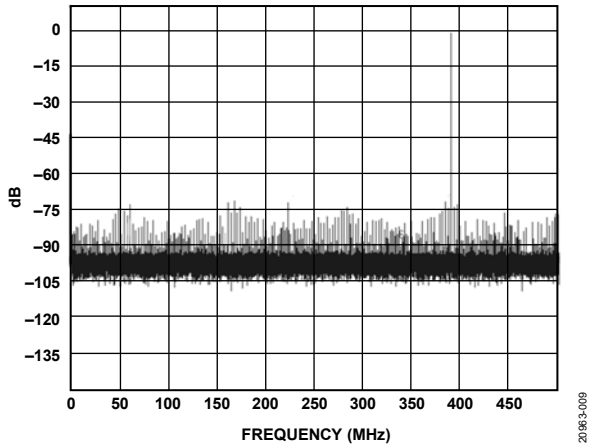


Figure 9. Single-Tone FFT with f_{IN} = 611 MHz, SNRFS = 48.6 dBFS, SFDR = 71 dBFS, SINAD = 48.5 dBFS

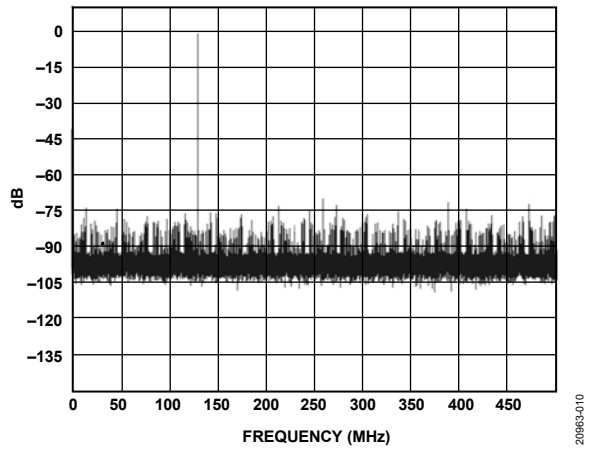


Figure 10. Single-Tone FFT with f_{IN} = 871 MHz, SNRFS = 48.5 dBFS, SFDR = 70 dBFS, SINAD = 48.5 dBFS

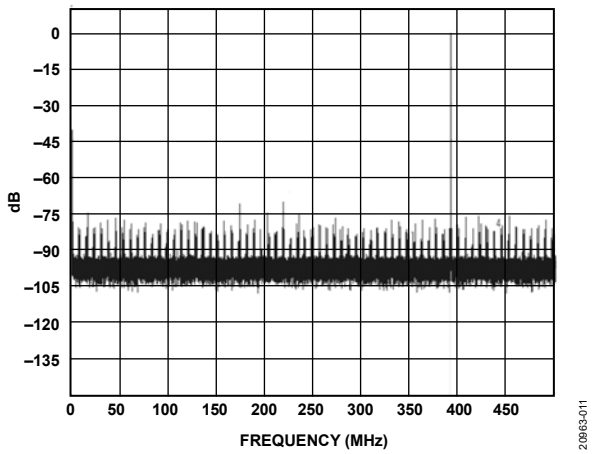


Figure 11. Single-Tone FFT with f_{IN} = 1391 MHz, SNRFS = 48.4 dBFS, SFDR = 70 dBFS, SINAD = 48.4 dBFS

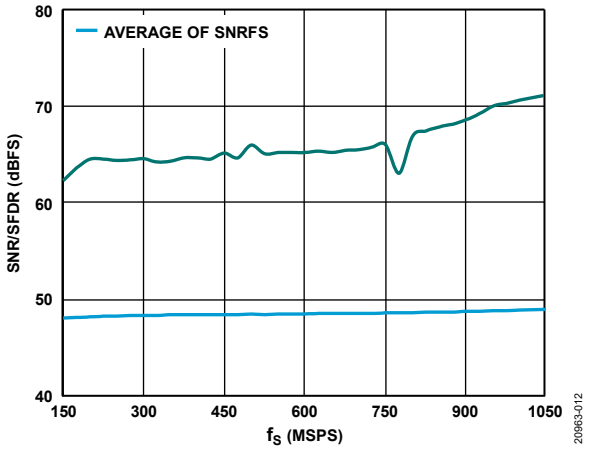


Figure 12. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 155 MHz

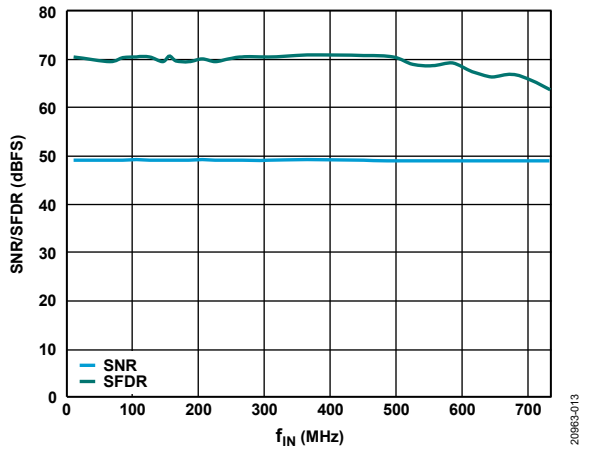


Figure 13. SNR/SFDR vs. f_{IN}, A_{IN} < 735MHz, Buffer Current = 160 µA

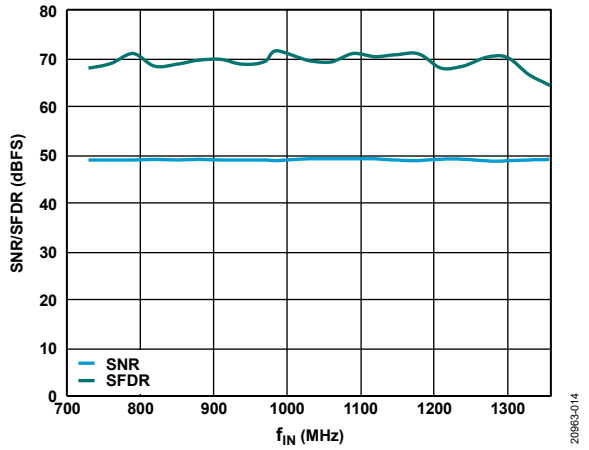


Figure 14. SNR/SFDR vs. f_{IN}, A_{IN} ≥ 735 MHz, Buffer Current = 320 µA

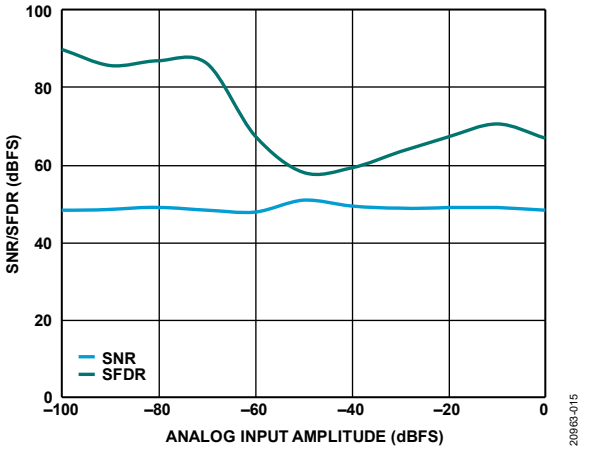


Figure 15. SNR/SFDR vs. Analog Input Amplitude, f_{IN} = 155 MHz

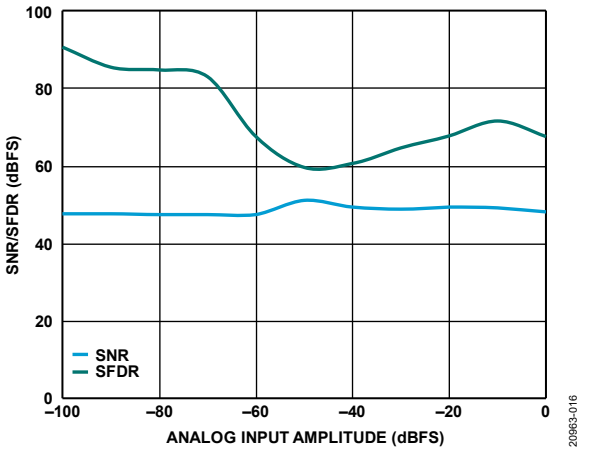


Figure 16. SNR/SFDR vs. Analog Input Amplitude, f_{IN} = 611 MHz

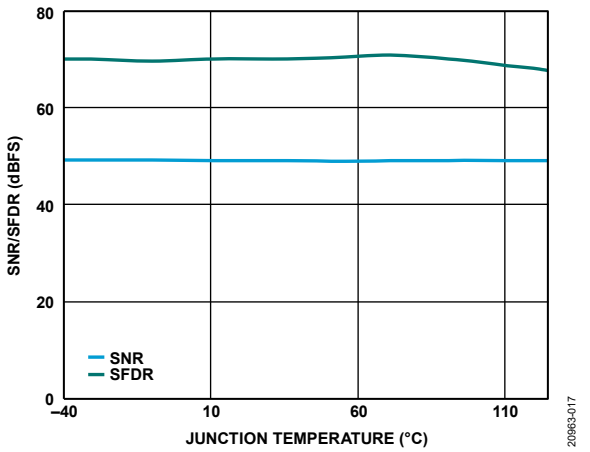


Figure 17. SNR/SFDR vs. Junction Temperature, f_{IN} = 155 MHz

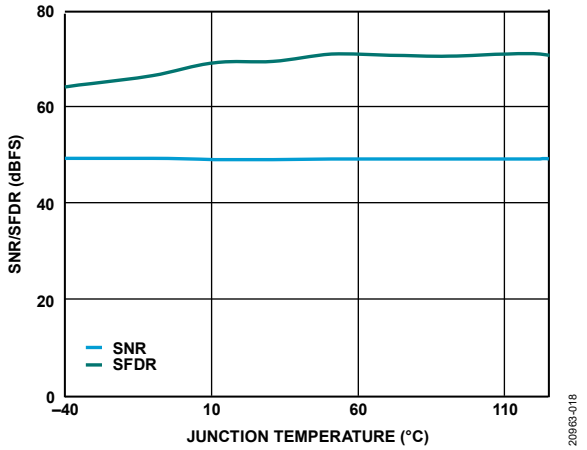


Figure 18. SNR/SFDR vs. Junction Temperature, f_{IN} = 611 MHz

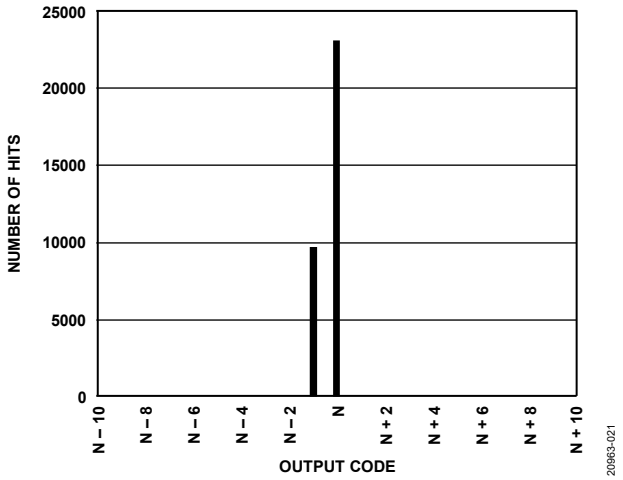


Figure 21. Input Referred Noise Histogram

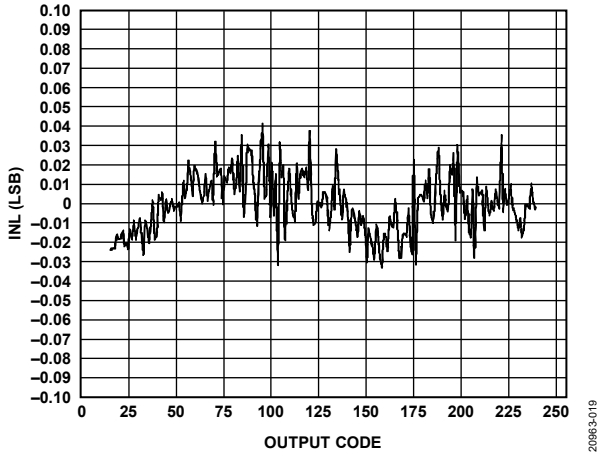


Figure 19. INL, f_{IN} = 10.3 MHz

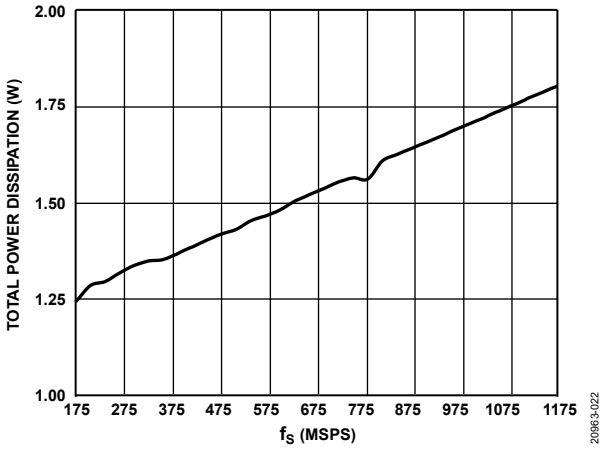


Figure 22. Total Power Dissipation vs. f_S

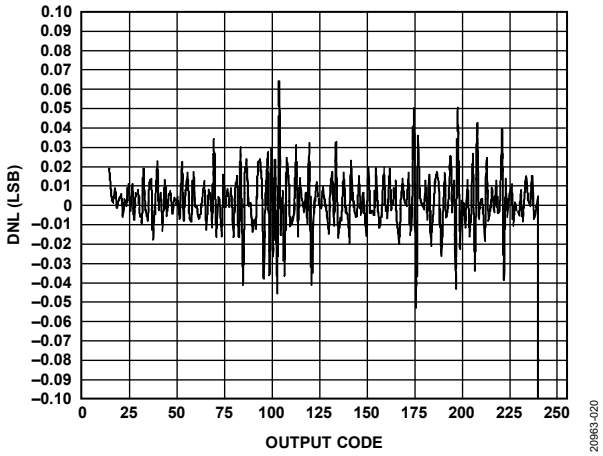


Figure 20. DNL, f_{IN} = 10.3 MHz

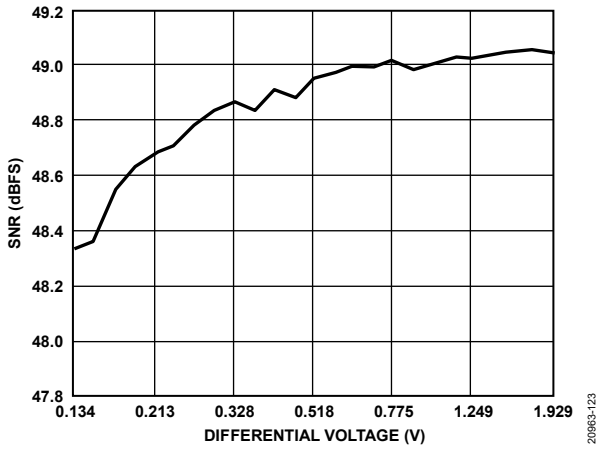


Figure 23. SNR vs. Differential Voltage (Clock Amplitude), f_{IN} = 155.3 MHz

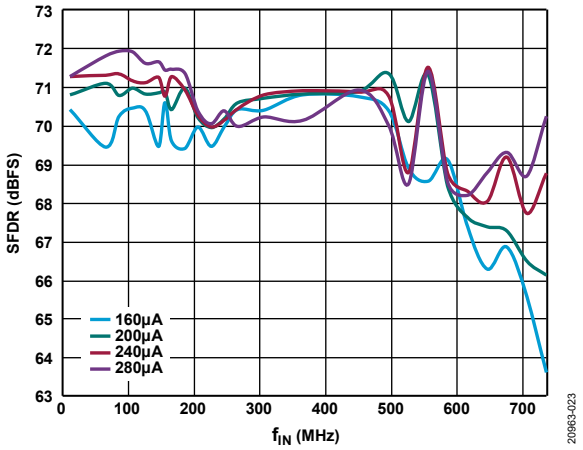


Figure 24. SFDR vs. f_{IN} with Different Buffer Current Settings, A_{IN} < 735 MHz

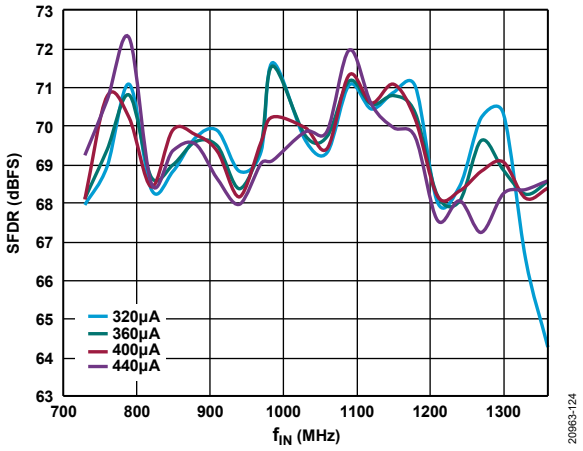


Figure 25. SFDR vs. f_{IN} with Different Buffer Current Settings, A_{IN} ≥ 735 MHz

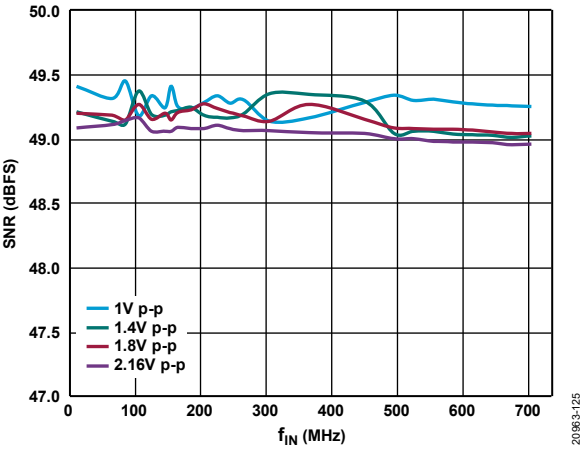


Figure 26. SNR vs. f_{IN} with Different Analog Input Full Scales, A_{IN} < 735 MHz

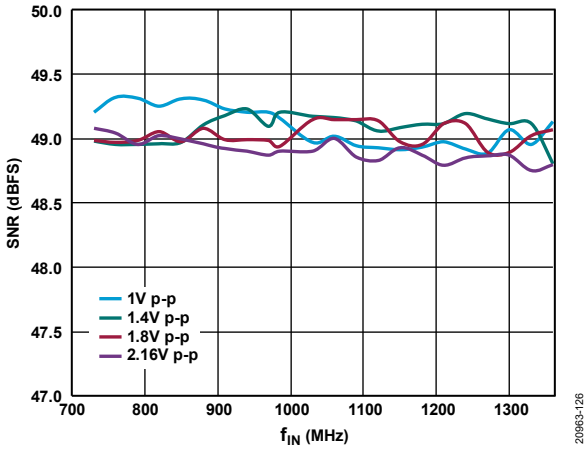


Figure 27. SNR vs. f_{IN} with Different Analog Input Full Scales, A_{IN} ≥ 735 MHz, Buffer Current = 320 µA

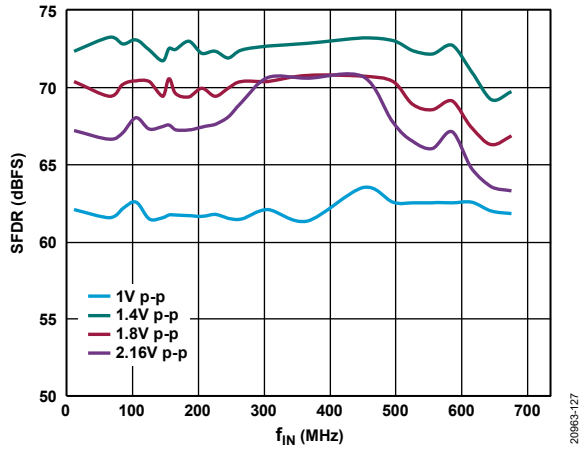


Figure 28. SFDR vs. f_{IN} with Different Analog Input Full Scales, A_{IN} < 735 MHz

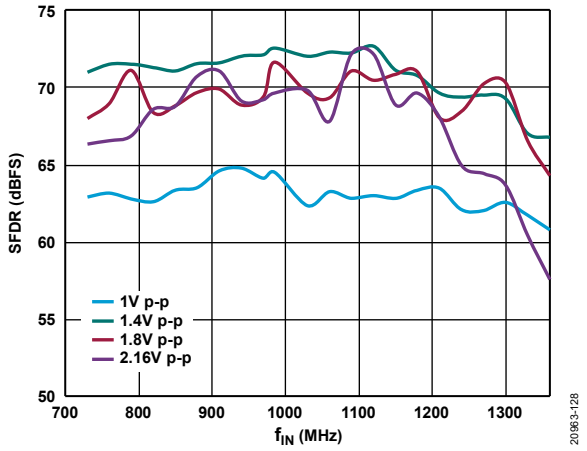


Figure 29. SFDR vs. f_{IN} with Different Analog Input Full Scales, A_{IN} ≥ 735 MHz, Buffer Current = 320 µA

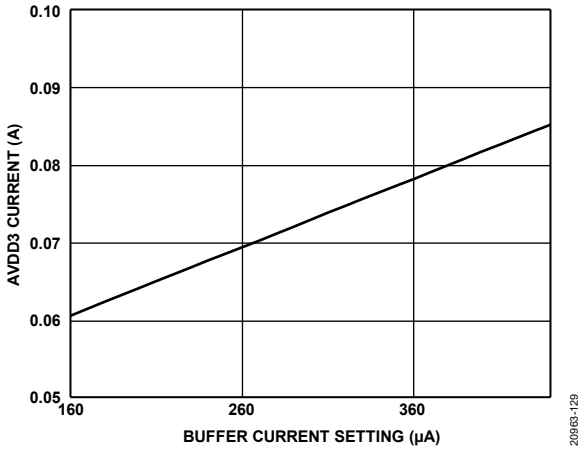


Figure 30. AVDD3 Current vs. Buffer Current Setting

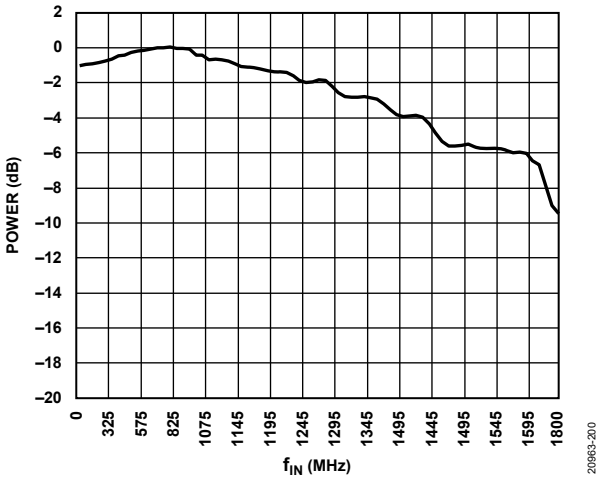


Figure 31. Full Power Bandwidth

EQUIVALENT CIRCUITS

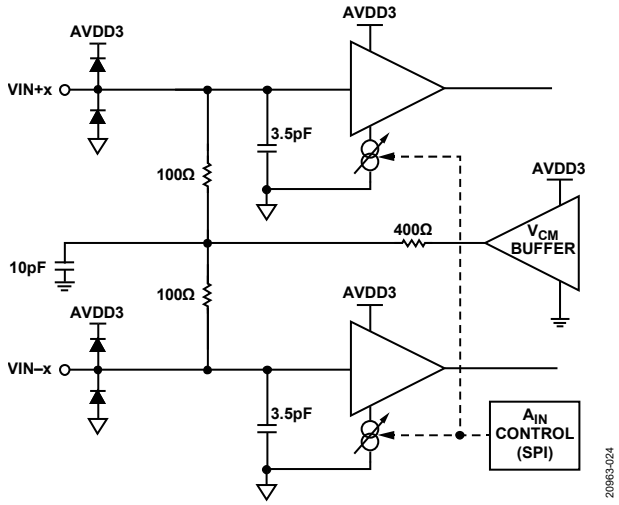


Figure 32. Analog Inputs

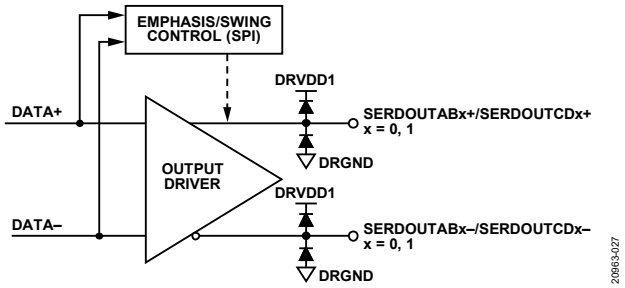


Figure 35. Digital Outputs

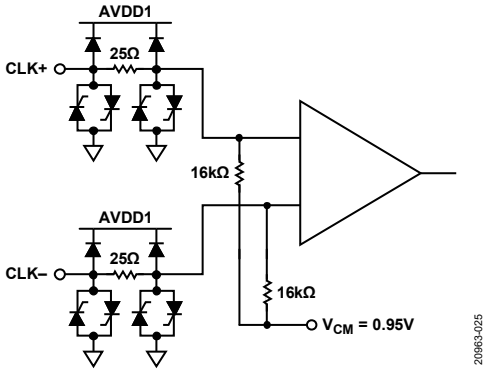


Figure 33. Clock Inputs

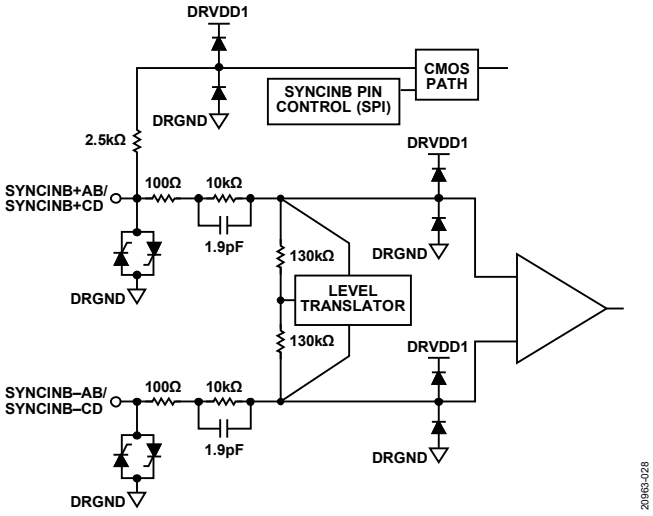


Figure 36. SYNCINB±AB, SYNCINB±CD Inputs

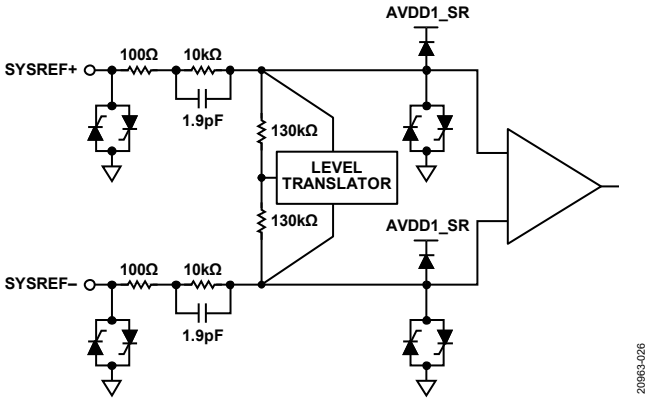


Figure 34. SYSREF± Inputs

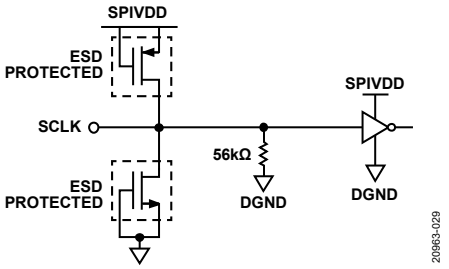


Figure 37. SCLK Input

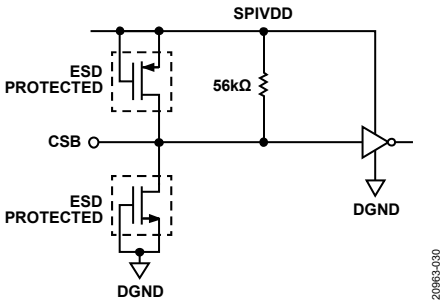


Figure 38. CSB Input

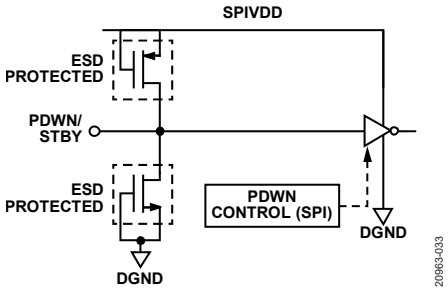


Figure 41. PDWN/STBY Input

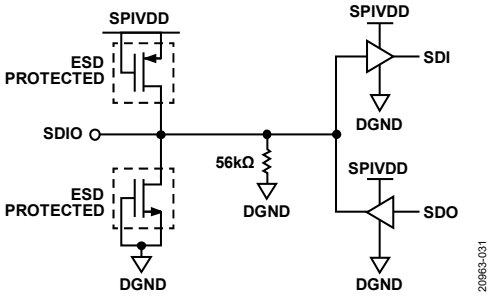


Figure 39. SDIO Input

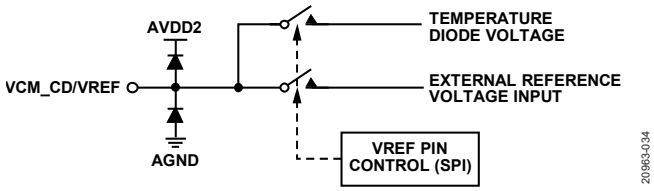


Figure 42. VCM_CD/VREF Input/Output

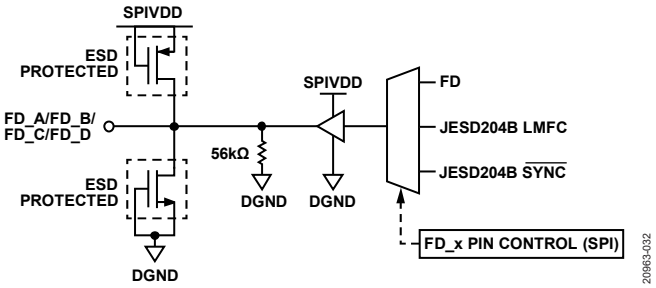


Figure 40. FD_A, FD_B, FD_C, or FD_D Outputs

THEORY OF OPERATION

ADC ARCHITECTURE

The AD9094 architecture consists of an input buffered, pipelined ADC. The input buffer of the ADC provides a 200 Ω termination impedance to the analog input signal. The equivalent circuit diagram of the analog input termination is shown in Figure 32.

The input buffer provides a linear, high input impedance (for ease of drive) and reduces kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 8-bit result in the digital correction logic. The pipelined architecture allows the first stage to operate with a new input sample while the remaining stages operate with the preceding samples at the same time. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9094 is a differential buffer with an internal V_{CM} of 1.43 V. The clock signal alternately switches the input circuit between sample mode and hold mode. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input that limits unwanted broadband noise. See Figure 43 and Figure 44 for details on input network recommendations.

For optimal dynamic performance, match the source impedances driving VIN+x and VIN−x such that the common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

To achieve maximum SNR performance, set the ADC to the largest span in a differential configuration. For the AD9094, the available span is programmable through the SPI from 1.44 V p-p to 2.16 V p-p differential with 1.44 V p-p differential as the default.

Dither

The AD9094 has internal on-chip dither circuitry that improves the ADC linearity and SFDR, particularly at smaller signal levels. A known but random amount of white noise is injected into the AD9094 input. This dither improves the small signal linearity within the ADC transfer function and is precisely subtracted out digitally. The dither is turned on by default and does not reduce the ADC input dynamic range. The specifications and limits in this data sheet are obtained with the dither turned on. To disable the dither, use the SPI writes to Register 0x0922. Disabling the dither can slightly improve the SNR (by about 0.2 dB) at the expense of the small signal SFDR.

Differential Input Configurations

There are several ways to drive the AD9094 actively or passively. However, to achieve optimum performance, drive the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 43 and Figure 44) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9094.

For low to midrange frequencies, a double balun or double transformer network is recommended for optimum performance of the AD9094 (see Figure 43). For higher frequencies in the third or fourth Nyquist zones, remove some of the front-end passive components to ensure wideband operation (see Figure 44).

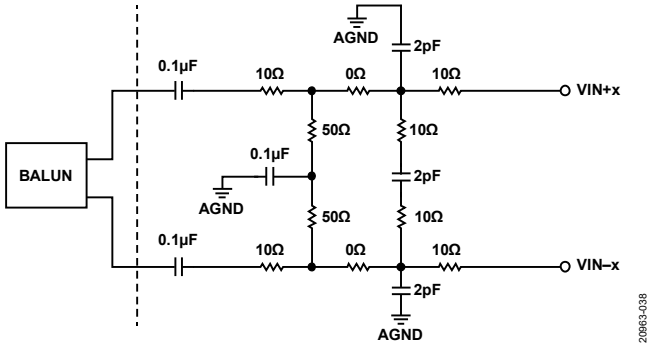


Figure 43. Differential Transformer Coupled Configuration A_{IN} ≤ 735 MHz

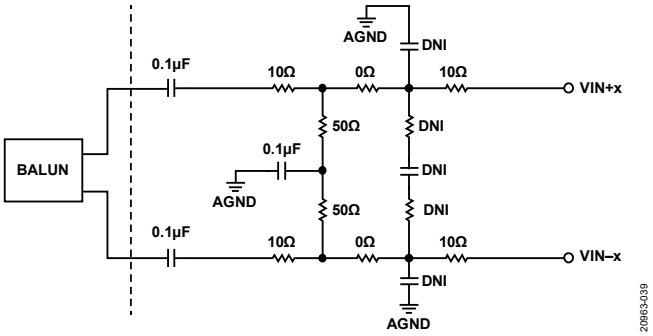


Figure 44. Differential Transformer Coupled Configuration for A_{IN} > 735 MHz

Input Common Mode

The analog inputs of the AD9094 are internally biased to the common mode, as shown in Figure 45.

For dc-coupled applications, use the SPI writes listed in this section to export the V_{CM} to the VCM_CD/VREF pin. Use Register 0x1908 to disconnect the internal V_{CM} buffer from the analog input.

When performing SPI writes for dc coupling operation, use the following register settings in order:

1. Set Register 0x1908, Bit 2 to 1 to disconnect the internal common-mode buffer from the analog input.
2. Set Register 0x18A6 to 0x00 to turn off the voltage reference.
3. Set Register 0x18E6 to 0x00 to turn off the temperature diode export.
4. Set Register 0x18E0 to 0x04.
5. Set Register 0x18E1 to 0x1C.
6. Set Register 0x18E2 to 0x14.
7. Set Register 0x18E3, Bit 6 to 0x01 to turn on the V_{CM} buffer to export the internal common-mode voltage.
8. Set Register 0x18E3, Bits[5:0] to the buffer current setting (copy the buffer current setting from Register 0x1A4C and Register 0x1A4D to improve the accuracy of the common-mode export).

Analog Input Controls and SFDR Optimization

The AD9094 offers flexible controls for the analog inputs, such as buffer current and input full-scale adjustment. All available controls are shown in Figure 45.

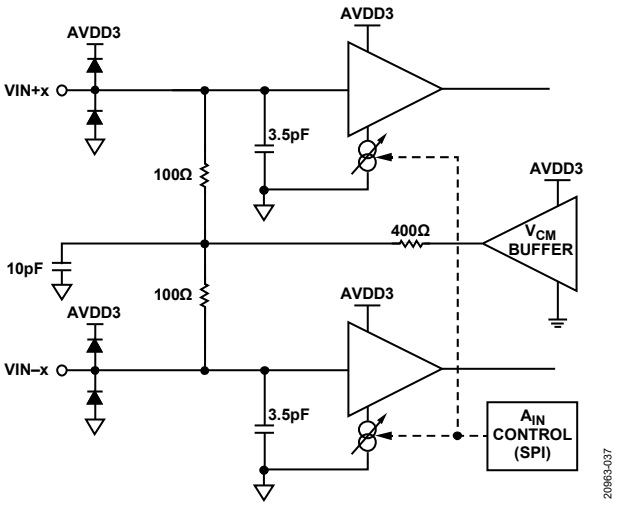


Figure 45. Analog Input Controls

Use Register 0x1A4C and Register 0x1A4D to scale the buffer currents on each channel to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 46. For a complete list of buffer current settings, see Table 23.

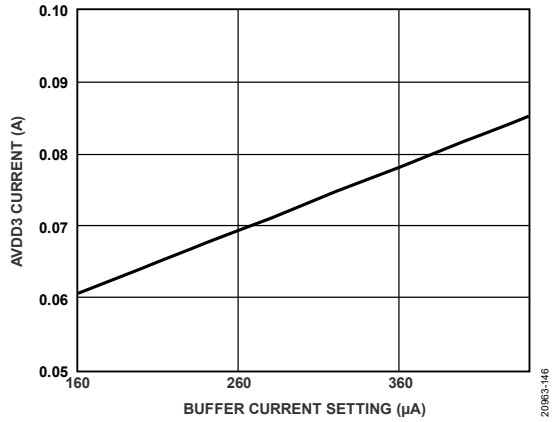


Figure 46. AVDD3 Power vs. Buffer Current Setting

In certain high frequency applications, the SFDR can be improved by reducing the full-scale setting.

Table 9 shows the recommended buffer current settings for the different analog input frequency (f_A) ranges.

Table 9. SFDR Optimization for Input Frequencies

Analog Input Frequencies	Input Buffer Current Control Settings, Register 0x1A4C and Register 0x1A4D
A_{IN} < 500 MHz	160 µA (Register 0x1A4C, Bits[5:0] = Register 0x1A4D, Bits[5:0] = 01000)
A_{IN} ≥ 500 MHz, A_{IN} < 735 MHz	280 µA (Register 0x1A4C, Bits[5:0] = Register 0x1A4D, Bits[5:0] = 01110)
A_{IN} ≥ 735 MHz	320 µA (Register 0x1A4C, Bits[5:0] = Register 0x1A4D, Bits[5:0] = 10000)

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the AD9094 inputs is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9094. This internal 0.5 V reference sets the full-scale input range of the ADC. The full-scale input range can be adjusted via Register 0x1910. For more information on adjusting the input swing, see Table 23. Figure 47 shows the block diagram of the internal 0.5 V reference controls.

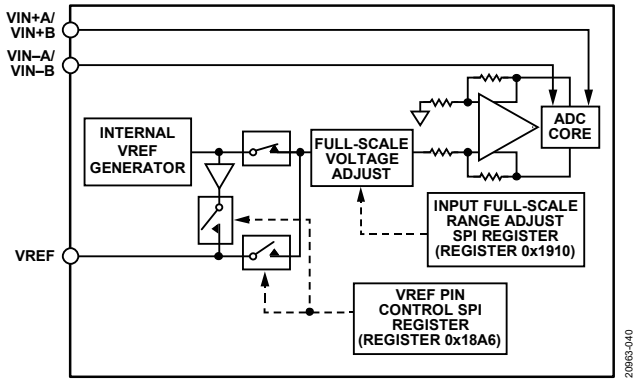


Figure 47. Internal Reference Configuration and Controls

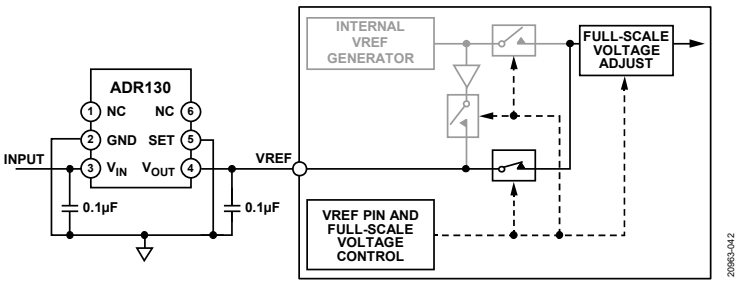


Figure 48. External Reference Using the ADR130

Use Register 0x18A6 to either use the internal 0.5 V reference or to provide an external 0.5 V reference. When using an external voltage reference, always provide a 0.5 V reference. The full-scale adjustment is made using the SPI and is irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD9094, refer to Table 23.

The SPI writes required to use the external voltage reference, in order, are as follows:

1. Set Register 0x18E3 to 0x00 to turn off V_{CM} export.
2. Set Register 0x18E6 to 0x00 to turn off temperature diode export.
3. Set Register 0x18A6 to 0x01 to turn on the external voltage reference.

The use of an external reference can be necessary in some applications to enhance the gain accuracy of the ADC or to improve thermal drift characteristics.

The external reference must be a stable 0.5 V reference. The ADR130 is a sufficient option for providing the 0.5 V reference. Figure 48 shows how the ADR130 provides the external 0.5 V reference to the AD9094. The dashed lines show unused blocks within the AD9094 while using the ADR130 to provide the external reference.

DC OFFSET CALIBRATION

The AD9094 contains a digital filter to remove the dc offset from the output of the ADC. To enable this filter for ac-coupled applications, set Register 0x0701, Bit 7 to 1 and set Register 0x073B, Bit 7 to 0. The filter computes the average dc signal that is digitally subtracted from the ADC output. As a result, the dc offset is improved to better than 70 dBFS at the output. Because the filter does not distinguish between the source of dc signals, this feature can be used when the signal content at dc is not of interest. The filter corrects dc up to ±512 codes and saturates beyond that.

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9094 sample clock inputs (CLK±) with a differential signal. This signal is typically ac-coupled to the CLK± pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 49 shows a preferred method for clocking the AD9094. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

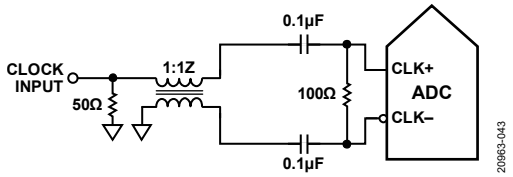


Figure 49. Transformer Coupled Differential Clock (Z is the Impedance Ratio)

Another option for clocking the AD9094 is to ac couple a differential or LVDS signal to the sample clock input pins, as shown in Figure 50.

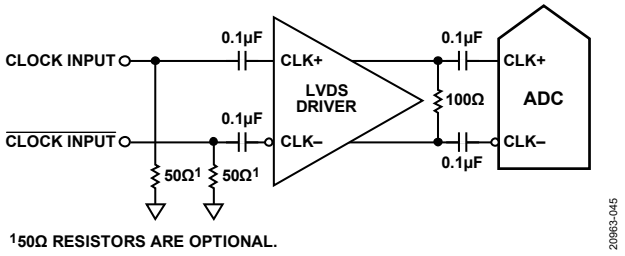


Figure 50. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. The AD9094 contains an internal clock divider and a duty cycle stabilizer (DCS). In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock with the usage of the clock divider is recommended. When providing a higher frequency clock is not possible, users are recommended to turn on the DCS. The divider output offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. The following SPI writes are required to turn on DCS (see the Memory Map section for more details on using this feature):

1. Write 0x81 to Register 0x011F.
2. Write 0x09 to Register 0x011C.
3. Write 0x09 to Register 0x011E.
4. Write 0x0B to Register 0x011C.
5. Write 0x0B to Register 0x011E.

Input Clock Divider

The AD9094 contains an input clock divider with the ability to divide the input clock by 1, 2, 4, or 8. To select the divider ratios, use Register 0x0108 (see Figure 51).

In applications where the clock input is a multiple of the sample clock, take care to program the appropriate divider ratio into the clock divider before applying the clock signal to ensure that the current transients during device startup are controlled.

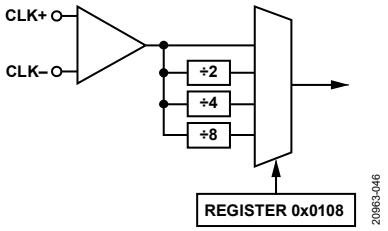


Figure 51. Clock Divider Circuit

The AD9094 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± causes the clock divider to reset to a programmable state. This synchronization feature allows multiple devices to have the corresponding clock dividers aligned to guarantee simultaneous input sampling.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. Calculate the degradation in SNR at a given f_A only in relation to t_J with the following equation:

$$SNR = -20 \times \log(2 \times \pi \times f_A \times t_J)$$

In this equation, the rms t_J represents the root mean square of all jitter sources including the clock input, analog input signal, and ADC t_J specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 52).

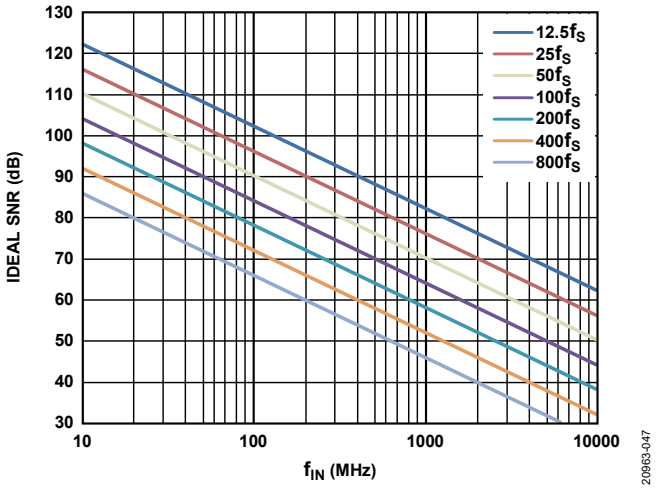


Figure 52. Ideal SNR vs. f_{IN} over Jitter

Treat the clock input as an analog signal in cases where t_J can affect the dynamic range of the AD9094. Separate the power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by using the original clock at the last step. Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance* and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter* for more in depth information about jitter performance as it relates to ADCs.

Figure 53 shows the estimated SNR of the AD9094 across f_A for different clock induced jitter values. To estimate the SNR, use the following equation:

$$SNR(\text{dBFS}) = -10\log\left(10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right)$$

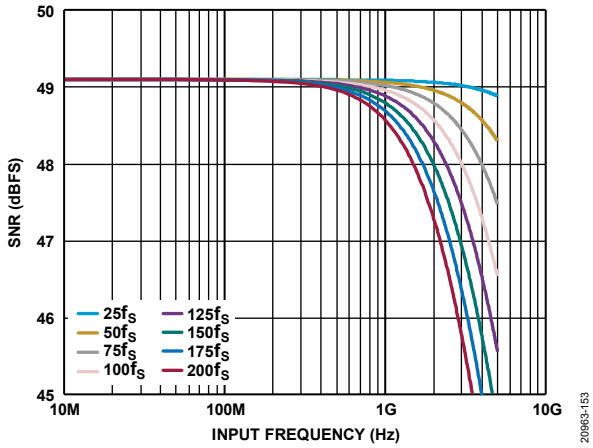


Figure 53. Estimated SNR Degradation vs. Analog Input Frequency over RMS Jitter

Input Clock Detect

The AD9094 contains input clock detection circuitry to detect the signal on the CLK± input clock pins. If the clock amplitude or f_S is lower than the specified minimum value, the AD9094 enters power-down mode. When the input clock detect bit in Register 0x011B is set to 0, the input clock is not detected. See Register 0x011A and Register 0x011B in Table 23 for more details on the input clock detect feature.

Power-Down and Standby Mode

The AD9094 PDWN/STBY pin configures the device when in power-down or standby mode. The default operation is power-down. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x003F and Register 0x0040.

In standby mode, the JESD204B link is not disrupted and transmits zeros for all converter samples. To change this state, use Register 0x0571, Bit 7 to select /K/ characters.

Temperature Diode

The AD9094 contains a diode-based temperature sensor to measure the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

To output the temperature diode voltage to the VCM_CD/VREF pin, use the SPI. Use Register 0x18E6 to enable or disable the diode. Register 0x18E6 is a local register. Both cores must be selected in the pair index register (Register 0x0009 = 0x03) to enable the temperature diode readout. Note that other voltages may be exported to the same pin at the same time, which can result in undefined behavior. Therefore, to ensure a proper readout, switch off all other voltage exporting circuits as detailed in the following steps.

The SPI writes required to export the temperature diode are as follows (see Table 23 for more information):

1. Set Register 0x0009 to 0x03 to select both cores.
2. Set Register 0x18E3 to 0x00 to turn off V_{CM} export.
3. Set Register 0x18A6 to 0x00 to turn off voltage reference export.
4. Set Register 0x18E6 to 0x01 to turn on the voltage export of the central 1× temperature diode. The typical voltage response of the temperature diode is shown in Figure 54. Although this voltage represents the die temperature, take measurements from a pair of diodes for improved accuracy.
5. To enable the 20× diode , set Register 0x18E6 to 0x02 to turn on the second central temperature diode of the pair, which is 20× the size of the first. When using two diodes simultaneously to achieve a more accurate result, see the AN-1432 Application Note, *Practical Thermal Modeling and Measurements in High Power ICs* for more information.

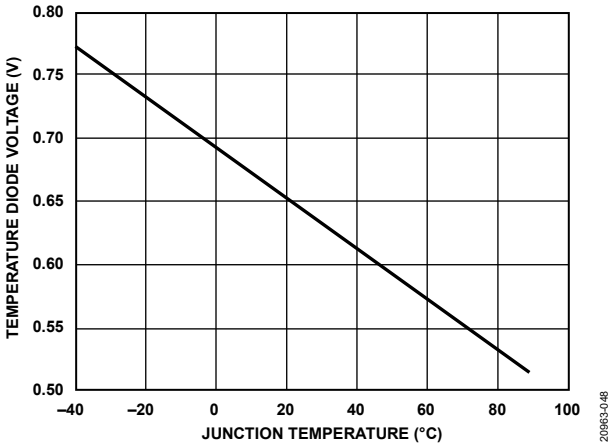


Figure 54. Temperature Diode Voltage vs. Junction Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, a mechanism to reliably determine when the converter is about to be clipped is beneficial. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs is helpful. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9094 contains fast detect circuitry for individual channels to monitor the threshold and to assert the FD_A, FD_B, FD_C, and FD_D pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the ADC input. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

FAST THRESHOLD DETECTION (FD_A, FD_B, FD_C, AND FD_D)

The fast detect FD_x bits in Register 0x0040 immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD_x bits clear only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD_x bits from excessively toggling.

The operation of the upper threshold and lower threshold registers with the dwell time registers is shown in Figure 55.

The fast detect indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers located at Register 0x0247 and Register 0x0248. The selected threshold register is compared with the signal magnitude at the ADC output. The fast upper threshold detection has a latency of 30 clock cycles (maximum). The approximate upper threshold magnitude (in dBFS) is defined by the following equation:

$$Upper\ Threshold\ Magnitude = 20\log(Threshold\ Magnitude/2^{13})$$

The fast detect indicators do not clear until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers located at Register 0x0249 and Register 0x024A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the ADC output. This comparison is subject to the ADC pipeline latency, however, the comparison is accurate in terms of converter resolution. The lower threshold magnitude (in dBFS) is defined by the following equation:

$$Lower\ Threshold\ Magnitude = 20\log(Threshold\ Magnitude/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x0247 and Register 0x0248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x0249 and Register 0x024A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles. To program the dwell time, pace the desired value in the fast detect dwell time registers located at Register 0x024B and Register 0x024C (see Table 23 for more details).

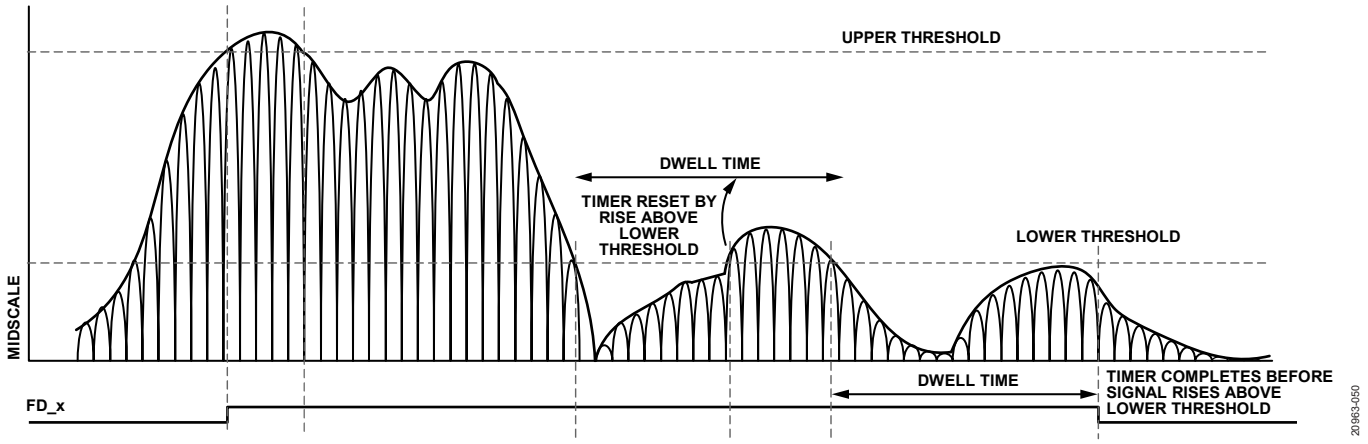


Figure 55. Threshold Settings for the FD_x Signals

SIGNAL MONITOR

The signal monitor block provides additional information on the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can drive an automatic gain control (AGC) loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 56 shows the simplified block diagram of the signal monitor block.

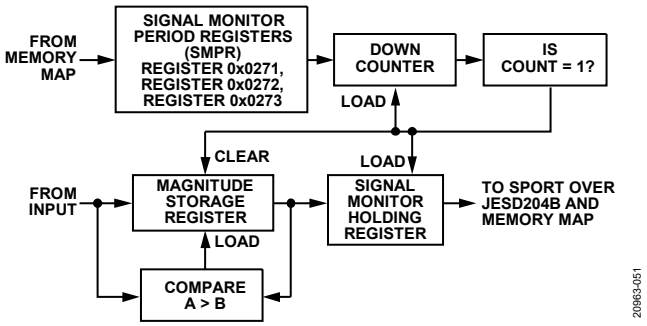


Figure 56. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value, and the observation period is 24 bits and represents converter output samples. To derive the peak magnitude (in dBFS), use the following equation:

$$Peak\ Magnitude = 20\log(Peak\ Detector\ Value/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period that is determined by the signal monitor period register (SMPR). To enable the peak detector function, set Bit 1 of Register 0x0270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

When peak detection mode is enabled, the value in the SMPR is loaded into a monitor period timer that decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user) and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT interface over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR and the countdown restarts. The magnitude of the first input sample is also updated in the magnitude storage register, and the comparison and update procedure, as described in the Fast Threshold Detection (FD_A, FD_B, FD_C, and FD_D) section, continues.

SPORT OVER JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. To enable the signal control monitor function, set Bit 0 of Register 0x0279 and Bit 1 of Register 0x027A. Figure 57 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. A maximum of three control bits can be inserted into the JESD204B samples. However, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (number of control bits per sample (CS) = 1), only the most significant control bit is used (see the Example Configuration 1 and the Example Configuration 2 in Figure 57). To select the SPORT over JESD204B (signal monitor) option, program Register 0x0559, and Register 0x058F accordingly. See Table 23 for more information on setting these bits.

Figure 58 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 59 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

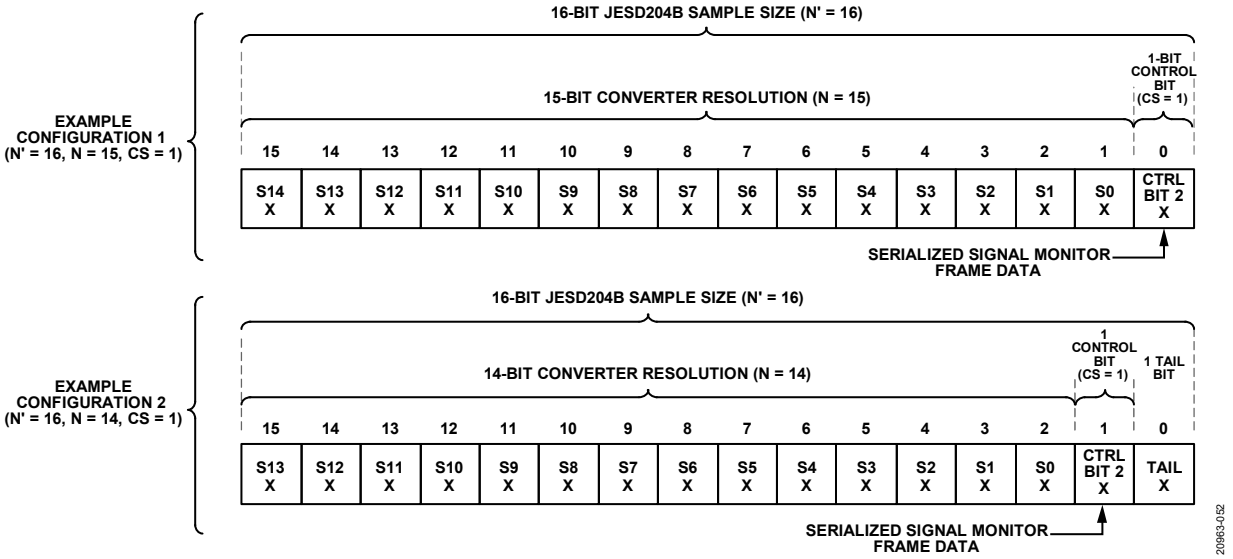


Figure 57. Signal Monitor Control Bit Locations

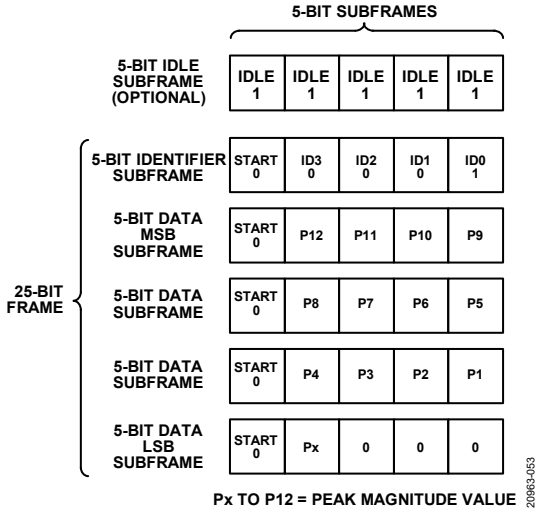


Figure 58. SPORT over JESD204B Signal Monitor Frame Data

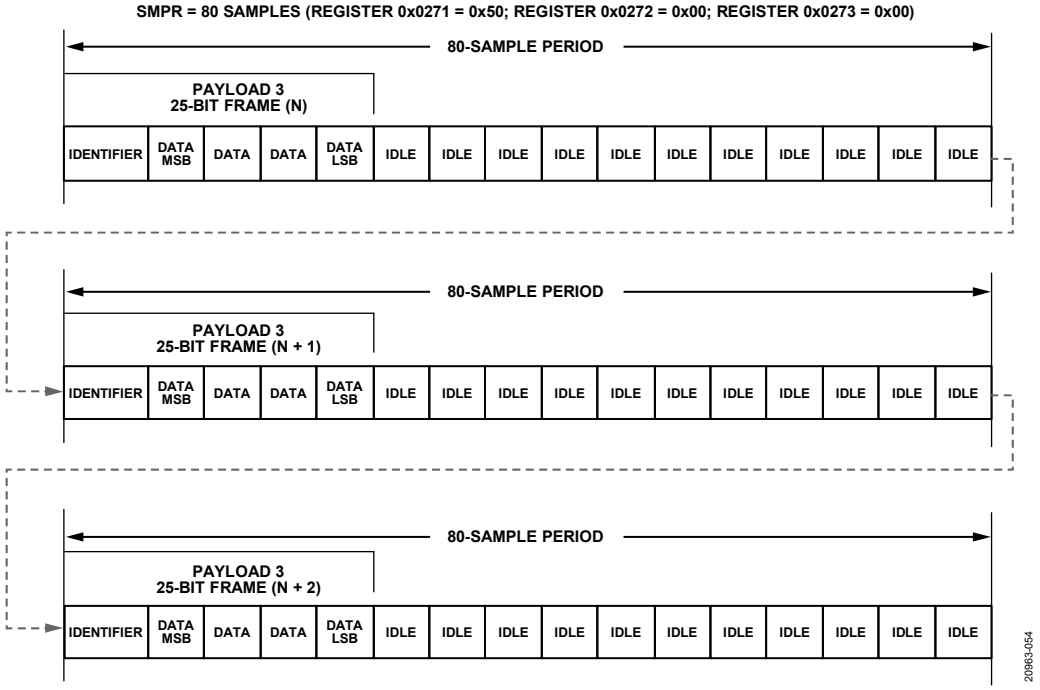


Figure 59. SPORT over JESD204B Signal Monitor Data Example with Period Timer = 80 Samples

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD9094 digital outputs are designed to the JEDEC standard, JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD9094 to a digital processing device over a serial interface with lane rates up to 15 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing and an ability to enable smaller packages for converter and logic devices.

SETTING UP THE AD9094 DIGITAL INTERFACE

The following SPI writes are required for the AD9094 at startup and each time the ADC is reset (datapath reset, soft reset, link power-down or power-up, or hard reset):

1. Write 0x4F to Register 0x1228.
2. Write 0x0F to Register 0x1228.
3. Write 0x04 to Register 0x1222.
4. Write 0x00 to Register 0x1222.
5. Write 0x08 to Register 0x1262.
6. Write 0x00 to Register 0x1262.

The JESD204B data transmit block, JTX, assembles the parallel data from the ADC into frames and uses 8-bit or 10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial link establishment. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The JESD204B data transmit blocks in the AD9094 map up to two physical ADCs over each of the two JESD204B links. Each link can be configured to use one or two JESD204B lanes for up to a total of four lanes for the AD9094 chip. The JESD204B specification refers to a number of parameters to define the link. These parameters must match between the JESD204B transmitter (the AD9094 output) and the JESD204B receiver (the logic device input). The JESD204B outputs of the AD9094 function effectively as two individual JESD204B links. The two JESD204B links can be synchronized, if desired, using the SYSREF± input.

Each JESD204B link is described according to the following parameters:

- L is the number of lanes per converter device (lanes per link) (AD9094 value = 1 or 2).
- M is the number of converters per converter device (virtual converters per link) (AD9094 value = 1 or 2).
- F is the number of octets per frame (AD9094 value = 1, 2, 4, or 8).
- N′ is the number of bits per sample (JESD204B word size) (AD9094 value = 8).
- N is the converter resolution (AD9094 value = 7 to 8).
- CS is the number of control bits per sample (AD9094 value = 0 or 1).
- K is the number of frames per multiframe (AD9094 value = 4, 8, 12, 16, 20, 24, 28, or 32).
- S is the samples transmitted per single converter per frame cycle (AD9094 value is set automatically based on L, M, F, and N′).
- HD is high density mode (AD9094 value is set automatically based on L, M, F, and N′).
- CF is the number of control words per frame clock cycle per converter device (AD9094 value = 0).

Figure 60 shows a simplified block diagram of the AD9094 JESD204B transmit link. By default, the AD9094 is configured to use four converters and four lanes. The Converter A and Converter B data is output to the SERDOUTAB0± and SERDOUTAB1± pins, and the Converter C and Converter D data is output to the SERDOUTCD0± and SERDOUTCD1± pins. The AD9094 allows other configurations, such as combining the outputs of each pair of converters into a single lane or changing the mapping of the digital output paths. These modes are set up via a quick configuration register in the SPI register map, which includes additional customizable options.

By default in the AD9094, the 8-bit converter word from each converter is placed into an octet (eight bits of data).

By default, no tail bit is enabled. If enabled, the tail bits can be configured as zeros or a pseudorandom number sequence. The tail bits can also be replaced with control bits that indicate overrange, SYSREF±, or fast detect output.

The resulting octet can be scrambled. Scrambling is optional, however, avoiding spectral peaks when transmitting similar digital data patterns is recommended. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self synchronizing version of the scrambler polynomial.

After the octet is scrambled The octet is then encoded with an 8-bit or 10-bit encoder. The 8-bit or 10-bit encoder takes eight bits of data (an octet) and encodes the bits into a 10-bit symbol. Figure 61 shows how the 8-bit data is taken from the ADC, the tail bits are added (if enabled), the octet is scrambled, and the octet is encoded into a 10-bit symbol. Figure 61 shows the default data format.

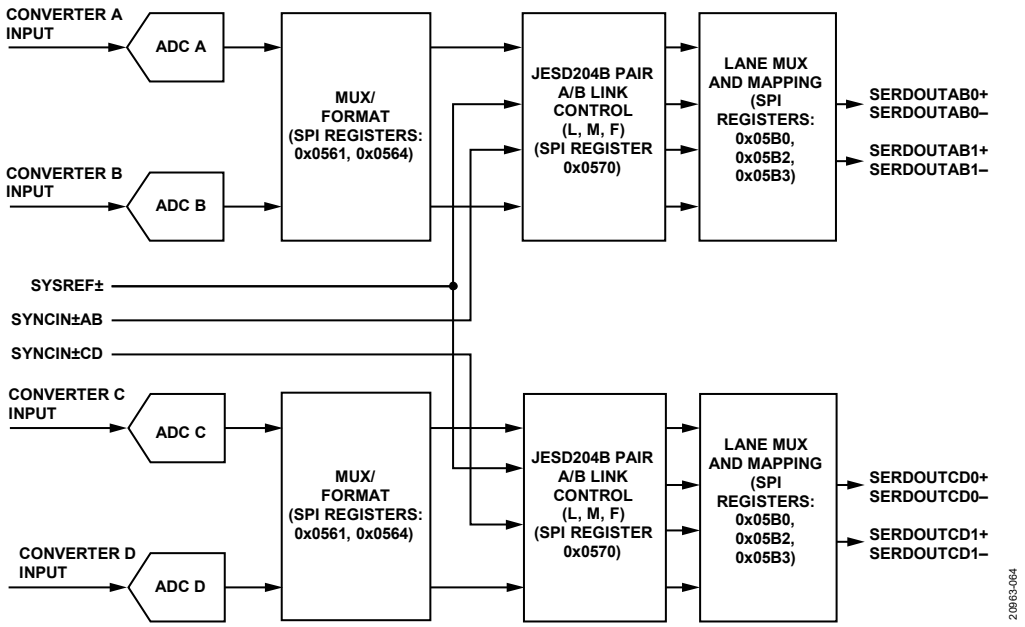


Figure 60. Transmit Link Simplified Block Diagram with Full Bandwidth Mode

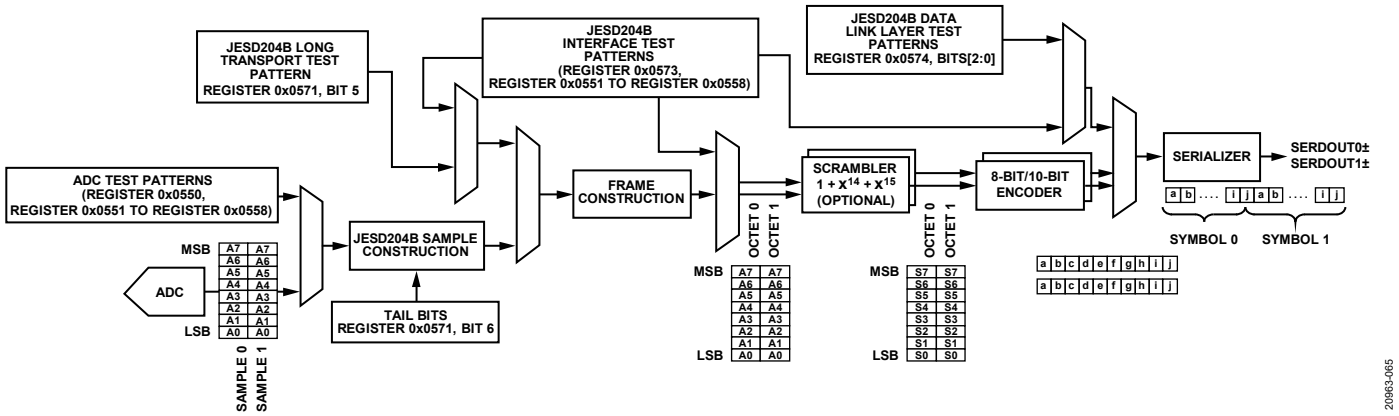


Figure 61. ADC Output Datapath with Data Framing

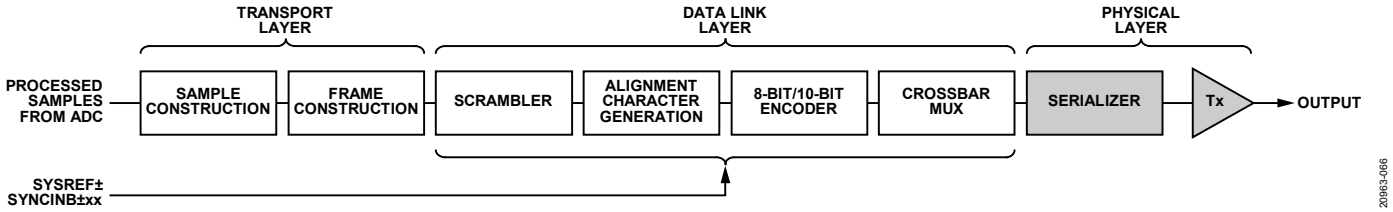


Figure 62. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 62 shows the flow of data through each of the two JESD204B links from the sample input to the physical output. The processing can be divided into layers that are derived from the open source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (PHY) (serializer and output driver).

Transport Layer

The transport layer packs the data, which consists of samples and optional control bits, into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. Use the following equation to determine the number of tail bits (T) within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These functions include optionally scrambling the data, inserting control characters for multichip synchronization, lane alignment, or monitoring, as well as encoding 8-bit octets into 10-bit symbols. The data link layer also sends the initial lane alignment sequence (ILAS) that contains the link configuration data used by the receiver to verify the settings in the transport layer.

PHY

The PHY consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, or four lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD9094 JESD204B transmitter interface operates in Subclass 1, as defined in the JEDEC Standard 204B. The link establishment process is divided into the following steps: code group synchronization (CGS) and SYNCINB±AB and/or SYNCINB±CD, ILAS, and user data and error correction.

CGS and SYNCINB±xx

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must use clock and data recovery (CDR) techniques to locate /K28.5/ characters in the input data stream.

The receiver asserts the SYNCINB±AB and SYNCINB±CD pins of the AD9094 low to issue a synchronization request. The JESD204B transmitter then begins sending /K/ characters. When the receiver synchronizes, the receiver waits for the correct reception of at least four consecutive /K/ symbols. The receiver then deasserts SYNCINB±AB and SYNCINB±CD, and the AD9094 transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the CGS phase, refer to the JEDEC JESD204B standard.

The SYNCINB±AB and SYNCINB±CD pin operation can also be controlled by the SPI. The SYNCINB±AB and SYNCINB±CD signals are differential LVDS mode signals by default. However, these signals can also be driven as single-ended. For more information on configuring the SYNCINB±AB and SYNCINB±CD pin operation, refer to Table 23.

ILAS

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. When the ILAS begins, it sends an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS construction is shown in Figure 63. The four multiframes include the following:

- Multiframe 1 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2 begins with an /R/ character followed by a /Q/ (/K28.4/) character, followed by link configuration parameters over 14 configuration octets (see Table 10), and ends with an /A/ character. Many parameter values are of the value − 1 notation.
- Multiframe 3 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

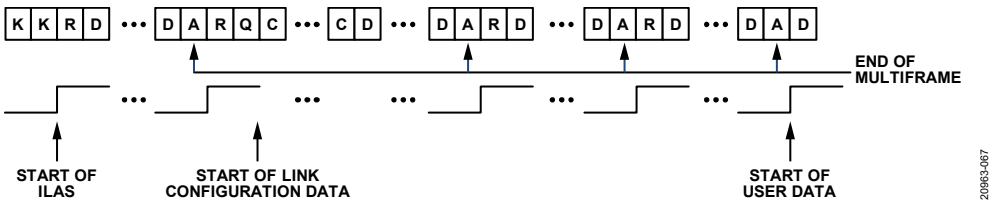


Figure 63. ILAS Construction

User Data and Error Detection

When the ILAS is complete, the user data is sent. Normally, within a frame, all characters are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default but can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/ character, and any 0xFD character at the end of a multiframe is replaced with an /A/ character. The JESD204B receiver checks for /F/ and /A/ characters in the received data stream and verifies that the characters only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver uses dynamic realignment or asserts the SYNCINB±xx signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames are equal, the second character is replaced with an /F/ character if the character is at the end of a frame, and an /A/ character if the character is at the end of a multiframe.

Insertion of alignment characters can be modified using the SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Table 23.

8-Bit and 10-Bit Encoder

The 8-bit and 10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 10. The 8-bit and 10-bit encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8-bit and 10-bit interface has bypass and invert options that can be controlled via the SPI. These options are troubleshooting tools for the verification of the digital front end (DFE). Refer to Table 23 for information on configuring the 8-bit and 10-bit encoder.

PHY (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD9094 PHY consists of drivers that are defined in the JEDEC JESD204B standard. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 300 mV p-p swing at the receiver (see Figure 64). Alternatively, single-ended 50 Ω termination resistors can be used. When single-ended termination resistors are used, the termination voltage is DRVDD1/2. Otherwise, 0.1 µF ac coupling capacitors can be used to terminate to any single-ended voltage.

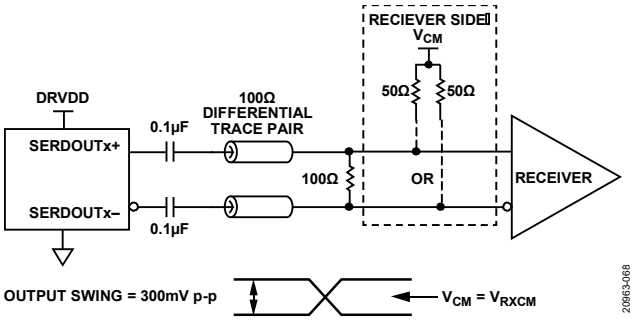


Figure 64. AC-Coupled Digital Output Termination Example (V_{RXCM} is the Receive Side V_{CM})

The AD9094 digital outputs can interface with custom application-specific integrated circuits (ASICs) and field programmable gate array (FPGA) receivers to provide superior switching performance in noisy environments. Single point to point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible. The V_{CM} of the digital output automatically biases to half the DRVDD1 supply of 1.25 V (V_{CM} = 0.6 V). See Figure 65 for an example of dc coupling the outputs to the receiver logic.

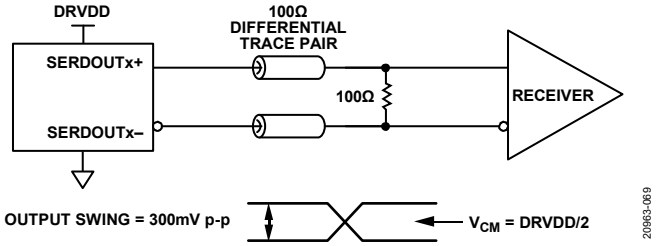


Figure 65. DC-Coupled Digital Output Termination Example

Table 10. AD9094 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

If there is no far end receiver termination, or if there is poor differential trace routing, timing errors can occur. To avoid such timing errors, ensure that the trace length is less than 6 inches, and that the differential output traces are close together and at equal lengths.

Figure 66 through Figure 68 show examples of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve, respectively, for one AD9094 lane running at 15 Gbps. The format of the output data is twos complement by default. To change the output data format, see Table 23.

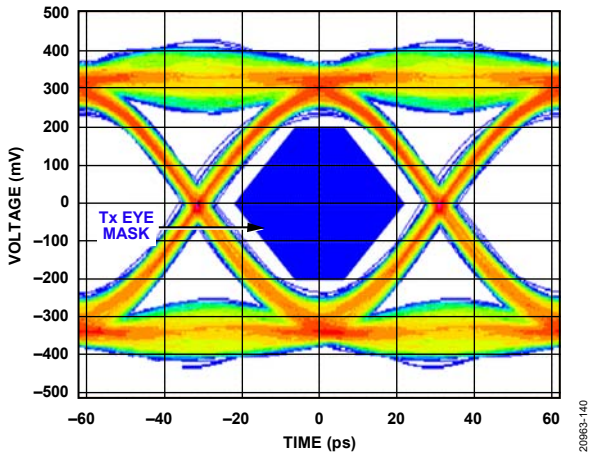


Figure 66. Digital Outputs Data Eye Diagram, External 100 Ω Terminations at 15 Gbps

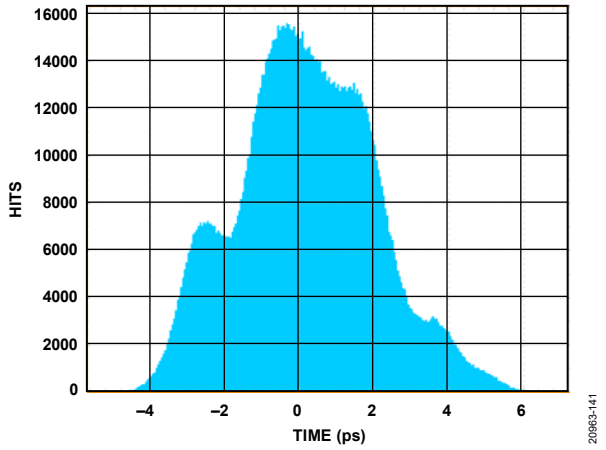


Figure 67. Digital Output TIE Jitter Histogram, External 100 Ω Terminations at 15 Gbps

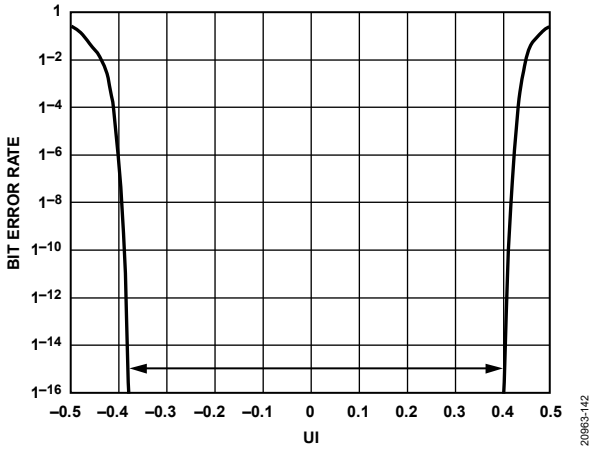


Figure 68. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 15 Gbps

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock because of excessive insertion loss. Under normal conditions, this feature is disabled to conserve power. Additionally, enabling and setting a de-emphasis value too high on a short link can cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because this feature can increase electromagnetic interference (EMI). See Table 23 for more details.

PLL

The PLL generates the serializer clock that operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL lock status bit (Register 0x056F, Bit 7). This read-only bit alerts the user when the PLL achieves a lock for the specific setup. The JESD204B lane rate control bits, Bits[7:4] of Register 0x056E, must be set to correspond with the lane rate.

JESD204B TRANSMITTER CONVERTER MAPPING

To support the different chip operating modes, the AD9094 design treats each sample stream as originating from separate virtual converters.

CONFIGURING THE JESD204B LINK

The AD9094 has two JESD204B links. The device offers a simplified way to set up the JESD204B link through the JESD204B JTX quick configuration register (Register 0x0570). One link consists of the SERDOUTAB0± and SERDOUTAB1± serial outputs and the second link consists of the SERDOUTCD0± and SERDOUTCD1± serial outputs. The basic parameters that determine the link setup are L, M, and F (see the Setting Up the AD9094 Digital Interface section).

M represents the number of virtual converters. The virtual converter mapping setup is shown in Table 11.

The maximum lane rate allowed by the JESD204B specification is 15 Gbps. The lane line rate is related to the JESD204B parameters using the following equation:

$$Lane\ Line\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{ADC_CLOCK}}{L}$$

where f_{ADC_CLOCK} is the sample rate of the converter.

Use the following steps to configure the output:

1. Power down the link.
2. Select the quick configuration options.
3. Configure any detailed options.
4. Set the output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane line rate calculated is less than 6.75 Gbps, select the low line rate option. To select this option, program a value of 0x10 to Register 0x056E. Table 12 shows the JESD204B output configurations supported for N′ = 8 for a given number of virtual converters. Ensure that the serial line rate for a given configuration is within the supported range of 1.6875 Gbps to 15 Gbps.

See the Example: Full Bandwidth Mode section for an example describing which JESD204B transport layer settings are valid for a given chip mode.

Table 11. Virtual Converter Mapping (Per Link)

	Virtual Converter Mapping	
Number of Virtual Converters Supported	**0**	**1**
1 to 2	ADC A and ADC C samples	ADC B and ADC D samples

Table 12. JESD204B Output Configurations for N′ = 8 (Per Link)

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (Register 0x0570)	Serial Lane Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x00	10 × f_{OUT}	1	1	1	1	0	7 to 8	8	0 to 1	Only valid K values divisible by 4 are supported
	0x01	10 × f_{OUT}	1	1	2	2	0	7 to 8	8	0 to 1	
	0x40	5 × f_{OUT}	2	1	1	2	0	7 to 8	8	0 to 1	
	0x41	5 × f_{OUT}	2	1	2	4	0	7 to 8	8	0 to 1	
	0x42	5 × f_{OUT}	2	1	4	8	0	7 to 8	8	0 to 1	
2	0x09	20 × f_{OUT}	1	2	2	1	0	7 to 8	8	0 to 1	Only valid K values divisible by 4 are supported
	0x48	10 × f_{OUT}	2	2	1	1	0	7 to 8	8	0 to 1	
	0x49	10 × f_{OUT}	2	2	2	2	0	7 to 8	8	0 to 1	

[1] f_{OUT} is the output sample rate, which is the ADC sample rate and chip decimation ratio. The JESD204B serial line rate must be ≥1687.5 Mbps and ≤15,000 Mbps. When the serial lane rate is ≤15 Gbps and >13.5 Gbps, set Bits[7:4] to 0x3 in Register 0x056E. When the serial lane rate is ≤13.5 Gbps and > 6.75 Gbps, set Bits[7:4] to 0x0 in Register 0x056E. When the serial lane rate is ≤6.75 Gbps and >3.375 Gbps, set Bits[7:4] to 0x1 in Register 0x056E. When the serial lane rate is ≤3.375 Gbps and ≥1687.5 Mbps, set Bits[7:4] to 0x5 in Register 0x056E.

[2] For more information on the JESD204B transport layer descriptions, see the Setting Up the AD9094 Digital Interface section.

[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

Example: Full Bandwidth Mode

In this example, the chip application mode is full bandwidth mode (see Figure 69) with two 8-bit converters at 1 GSPS.

The JESD204B output configuration is as follows:

- Two virtual converters are required (see Table 12)
- f_{OUT} = 1000/1 = 1000 MSPS

The JESD204B supported output configurations (see Table 12) include the following:

- N′ = 8 bits
- N = 8 bits
- L = 2, M = 2, and F = 2 (quick configuration = 0x48)
- CS = 0
- K = 32
- Output serial line rate = 10 Gbps per lane

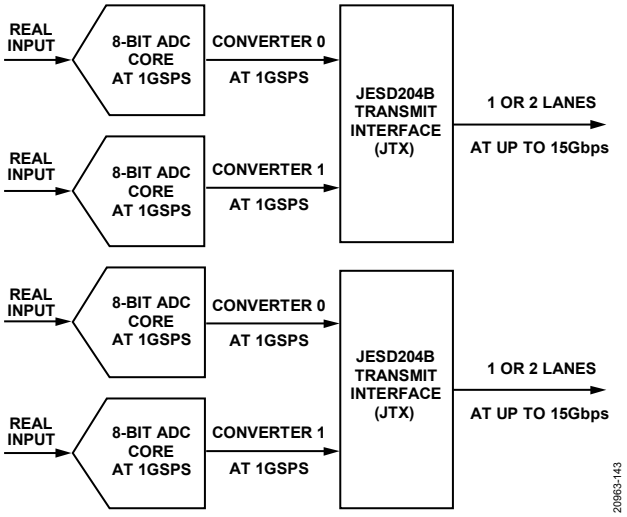


Figure 69. Full Bandwidth Mode

LATENCY

END TO END TOTAL LATENCY

Total latency in the AD9094 depends on the chip application mode and the JESD204B configuration. For any given combination of these parameters, the latency is deterministic, however, the value of this deterministic latency must be calculated as described in the Example Latency Calculations section.

Table 13 shows the combined latency through the ADC and serializer and deserializer (SERDES) blocks on the AD9094. Table 14 shows the latency through the JESD204B block based on the number of converters divided by the number of lanes for the configuration (the M/L ratio). For both Table 13 and Table 14, latency is typical and is measured in units of the encode clock.

To determine the total latency, select the appropriate ADC + SERDES latency from Table 13 and add the value to the appropriate JESD204B latency from Table 14. Example calculations are provided in the Example Latency Calculations section.

EXAMPLE LATENCY CALCULATIONS

In this example, the ADC application mode is full bandwidth mode with the following conditions:

- L = 2, M = 2, F = 2, and S = 1 (JESD204B mode)
- M/L ratio = 1
- Latency = 31 + 14 = 45 encode clocks

LMFC REFERENCED LATENCY

Some FPGA vendors may require the end user to know the LMFC referenced latency to make the appropriate deterministic latency adjustments. If this is required, the latency values in Table 13 and Table 14 can be used for the analog input to LMFC latency value and the LMFC to data output latency value.

Table 13. Latency Through the ADC + SERDES Blocks (Number of Sample Clocks)

Chip Application Mode	ADC + SERDES Latency
Full Bandwidth	31

Table 14. Latency Through JESD204B Block (Number of Sample Clocks) when N' = 8

	M/L Ratio		
Chip Application Mode	**0.5**	**1**	**2**
Full Bandwidth	23	14	7

DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to nonrepeatable latencies across the link from one power cycle or link reset to the next. See the JESD204B for more information on deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9094 supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x0590, Bits[7:5] set the subclass mode for the AD9094 and the default is set for Subclass 1 operating mode (Register 0x590, Bits[7:5] = 001). If deterministic latency is not a system requirement, Subclass 0 operation is recommended, and the SYSREF± signal may not be required. The SYSREF± signal may still be required in Subclass 0 mode in an application where multiple AD9094 devices must be synchronized with each other (for more information, see the Timestamp Mode section).

SUBCLASS 0 OPERATION

If there is no requirement for multichip synchronization while operating in Subclass 0 mode (Register 0x0590, Bits[7:5] = 000), the SYSREF± input can be left disconnected. In this mode, the relationships of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary but do not affect the ability of the receiver to capture and align the lanes within the link.

SUBCLASS 1 OPERATION

The JESD204B protocol organizes data samples into octets, frames, and multiframes, as described in the Transport Layer section. The LMFC is synchronous with the beginnings of these multiframes. In Subclass 1 operation, the SYSREF± signal is used to synchronize the LMFCs for each device in a link or across multiple links (within the AD9094, SYSREF± also synchronizes the internal sample dividers) (see Figure 70). The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and to achieve a fixed latency between power cycles and link reset conditions.

Deterministic Latency Requirements

The key factors required for achieving deterministic latency in a JESD204B Subclass 1 system include the following:

- The SYSREF± signal distribution skew within the system must be less than the desired uncertainty for the system.
- The SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links, and devices must be ≤1 LMFC (t_{LMFC}) period (see Figure 70). This total latency includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Setting Deterministic Latency Registers

The JESD204B receive buffer in the logic device buffers data starting on the LMFC boundary. If the total link latency in the system is near an integer multiple of the LMFC period, the data arrival time at the receive buffer may overlap an LMFC boundary from one power cycle to the next. To ensure deterministic latency in this case, perform a phase adjustment of the LMFC at either the transmitter or the receiver. Typically, adjustments to accommodate the receive buffer are made to the LMFC of the receiver. In the AD9094, this adjustment can be made using the JTX LMFC offset register (Register 0x0578, Bits[4:0]). This register delays the LMFC in frame clock increments, depending on the F parameter (number of octets per lane per frame). For F = 1, every fourth setting (0, 4, 8, …) results in a one frame clock shift. For F = 2, every other setting (0, 2, 4, …) results in a one frame clock shift. For all other values of F, each setting results in a one frame clock shift. Figure 71 shows that when the link latency is near an LMFC boundary, the local LMFC of the AD9094 can be delayed, delaying the data arrival time at the receiver. Figure 72 shows how the LMFC of the receiver is delayed to accommodate the receive buffer timing. Consult the applicable JESD204B receiver user guide for details on making this adjustment.

If the total latency in the system is not near an integer multiple of the LMFC period, or if the appropriate adjustments have been made to the LMFC phase at the clock source, variable latency from one power cycle to the next is still possible. In this case, check whether the setup and hold time requirements for the SYSREF± are being met. To check these requirements, read the SYSREF± setup and hold monitor register (Register 0x0128). This function is fully described in the SYSREF± Setup and Hold Window Monitor section.

If the Register 0x0128 read indicates a timing issue, the following adjustments can be made in the AD9094:

- Use the SYSREF± transition select bit (Register 0x0120, Bit 4) to change the SYSREF± level that is used for alignment.
- Use the CLK± edge select bit (Register 0x0120, Bit 3) to change the edge of CLK± that is used to capture SYSREF±.

Both of these options are described in further detail in the SYSREF± Control Features section. If neither of these measures achieve an acceptable setup and hold time, the user may need to adjust the phase of SYSREF± and/or the device clock (CLK±) .

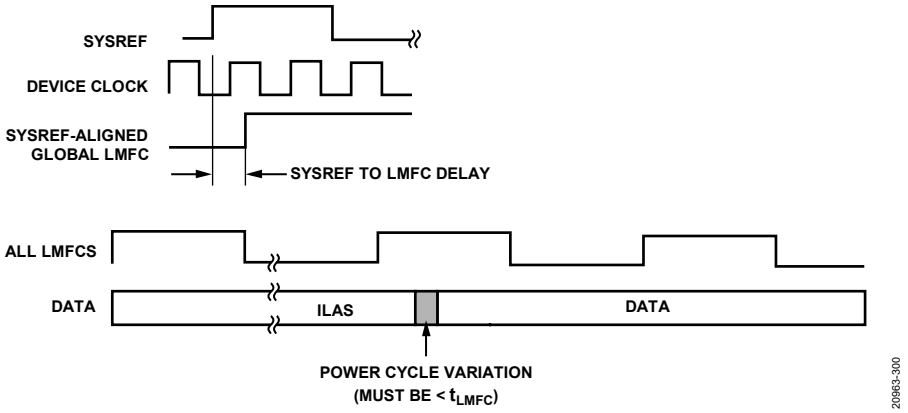


Figure 70. SYSREF± and LMFC

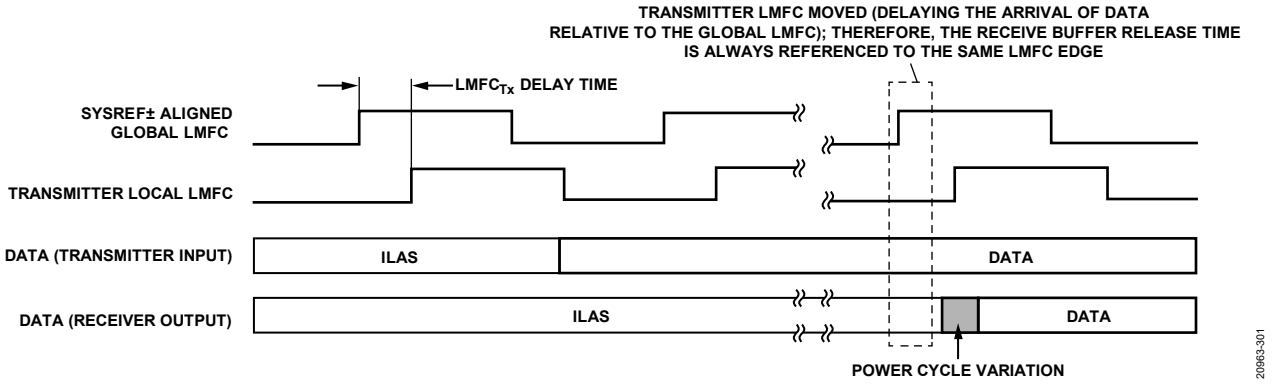


Figure 71. Adjusting the JESD204B Transmitter LMFC in the AD9094

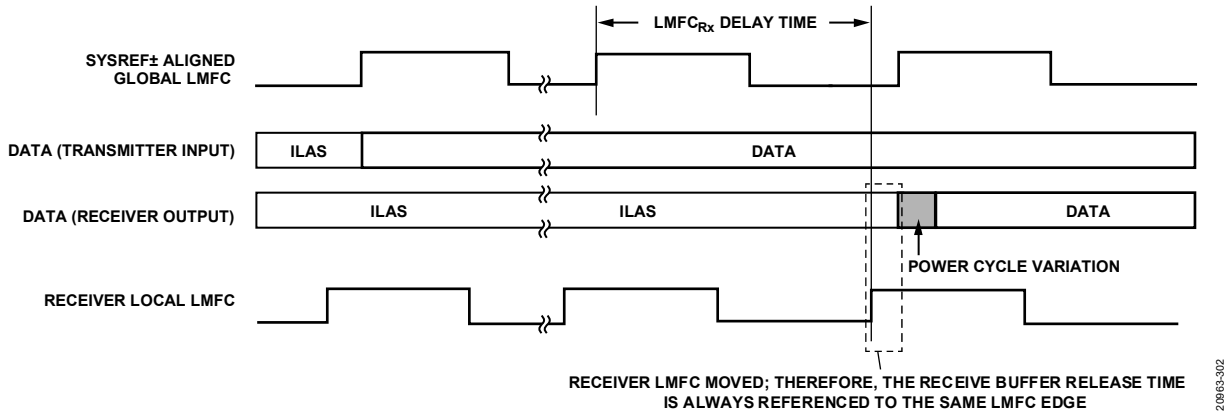


Figure 72. Adjusting the JESD204B Receiver LMFC in the Logic Device

MULTICHIP SYNCHRONIZATION

The flowchart in Figure 74 describes the internal mechanism for multichip synchronization in the AD9094. There are two methods by which multichip synchronization can take place (normal mode and timestamp mode), as determined by the synchronization mode bit in Register 0x01FF, Bit 0. Each method involves different applications of the SYSREF± signal.

NORMAL MODE

The default state of the synchronization mode bit is 0x0, which configures the AD9094 for sample chip synchronization. The JESD204B standard specifies the use of SYSREF± to provide for deterministic latency within a single link. The same concept, when applied to a system with multiple converters and logic devices, can also provide multichip synchronization. In Figure 74, this synchronization mode is referred to as normal mode. Follow the process outlined in Figure 74 to ensure that the AD9094 is configured appropriately. Users are recommended to consult the user intellectual property guide of the logic devices to ensure the JESD204B receivers are configured appropriately.

TIMESTAMP MODE

For all AD9094 full bandwidth operating modes, the SYSREF± input can also be used to timestamp samples. Timestamping is another method by which multiple channels and multiple devices can achieve synchronization. Timestamping is especially effective when synchronizing multiple devices to one or more logic devices. The logic devices buffer the data streams, identify the timestamped samples, and align the samples. When the synchronization mode bit (Register 0x01FF, Bit 0) is set to 0x1, the timestamp method is used for the synchronization of multiple channels and/or devices. In this mode, SYSREF± resets the sample dividers and the JESD204B clocking. When the synchronization mode is set to 0x1, the clocks are not reset. Instead, the coinciding sample is timestamped with the JESD204B control bits of that sample. To operate in timestamp mode, the following additional settings are required:

- Continuous or N shot SYSREF± enabled (Register 0x0120, Bits[2:1] = 01 or 10).
- At least one control bit must be enabled (Register 0x058F, Bits[7:6] = 00, 01, or 10.
- Set the function for one of the control bits to SYSREF±, as Register 0x0559, Bits[2:0] = 101 if using Control Bit 0.

Figure 73 shows how the input sample that coincides with SYSREF± is timestamped and ultimately output from the ADC. In this example, there are two control bits and Control Bit 0 indicates which sample coincides with the SYSREF± rising edge. The pipeline latencies for each channel are identical. If desired, the SYSREF± timestamp delay bits in Register 0x0123 (Bits[6:0]) can be used to adjust the timing of the sample that is timestamped.

Timestamping is not supported by any AD9094 operating modes that use decimation.

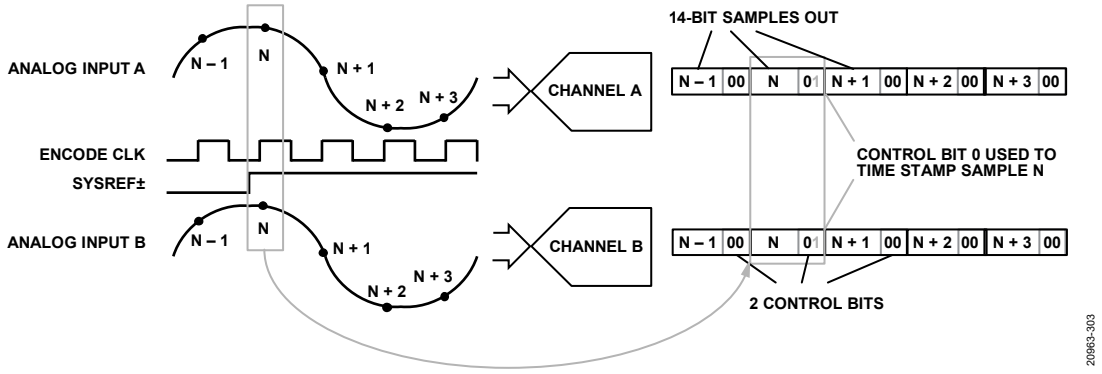


Figure 73. Timestamping, CS = 1 (Register 0x058F, Bits[7:6] = 1 Decimal), Control Bit 0 is SYSREF± (Register 0x0559, Bits[2:0] = 101)

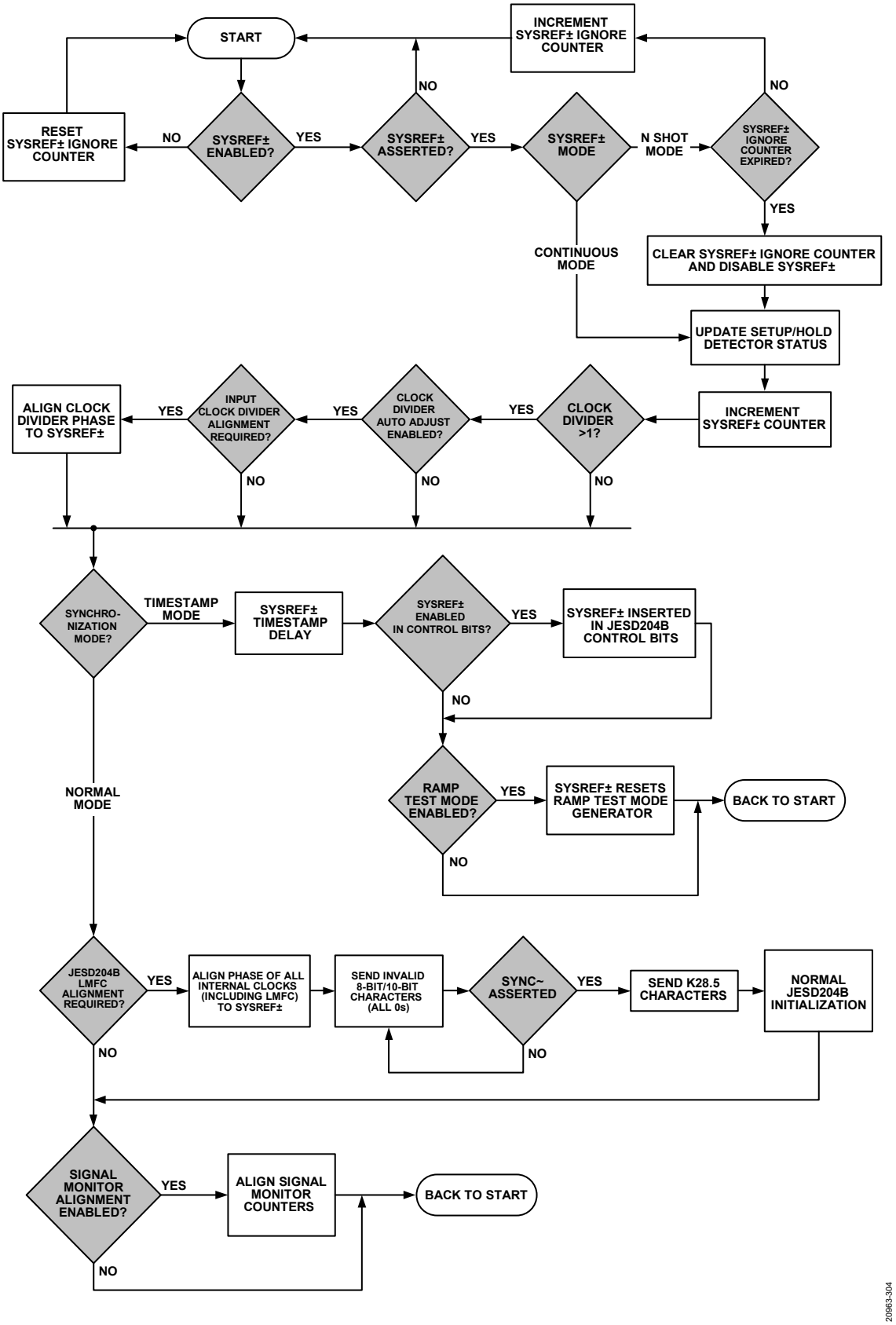


Figure 74. SYSREF± Capture Scenarios and Multichip Synchronization

SYSREF± INPUT

The SYSREF± input signal is used as a high accuracy system reference for deterministic latency and multichip synchronization. The AD9094 accepts a single-shot or periodic input signal. The SYSREF± mode select bits (Register 0x0120, Bits[2:1]) select the input signal type and activate the SYSREF± state machine when set. If in single- (or N) shot mode (Register 0x0120, Bits[2:1] = 10), the SYSREF± mode select bit self clears when the appropriate SYSREF± transition is detected. The pulse width must have a minimum width of two CLK± periods. If the clock divider (Register 0x010B, Bits[2:0]) is set to a value other than divide by 1, multiply this minimum pulse width requirement by the divide ratio. For example, if set to divide by 8, the minimum pulse width is 16 CLK± cycles. When using a continuous SYSREF± signal (Register 0x0120, Bits[2:1] = 01), the SYSREF± signal period must be an integer multiple of the LMFC. The LMFC can be derived using the following formula:

$$LMFC = ADC\ Clock/S \times K$$

A continuous SYSREF± signal is not recommended because the periodic SYSREF± signal can couple with the sampling path and create spurs in the spectrum.

The input clock divider, signal monitor block, and JESD204B link are all synchronized with the SYSREF± input when in sample synchronization mode (normal mode) (Register 0x01FF, Bit 0 = 0x0). The SYSREF± input can also be used to timestamp an ADC sample or provide a mechanism for synchronizing multiple AD9094 devices in a system. For the highest level of timing accuracy, SYSREF± must meet setup and hold requirements relative to the CLK± input. Several features in the AD9094 can ensure that these requirements are met. These features are described in the SYSREF± Control Features section.

SYSREF± Control Features

SYSREF± is used with the CLK± input as part of a source synchronous timing interface and requires setup and hold timing requirements of −44.8 ps and +64.4 ps relative to CLK± (see Figure 75). The AD9094 has three features that help meet these requirements.

First, the SYSREF± sample event can be defined as either a synchronous low to high transition or synchronous high to low transition.

Second, the AD9094 allows the SYSREF± signal to be sampled using either the rising edge or falling edge of the input clock CLK±. Figure 75, Figure 76, Figure 77, and Figure 78 show the four possible sampling combinations.

Third, the AD9094 has the ability to ignore a programmable number (up to 16) of SYSREF± events. To enable this SYSREF± ignore feature, set the SYSREF± mode register (Register 0x0120, Bits[2:1]) to 10 (N shot mode). This feature is useful to handle periodic SYSREF± signals that need time to settle after startup. Ignoring SYSREF± until the clocks in the system have settled can avoid an inaccurate SYSREF± trigger. Figure 79 shows an example of the SYSREF± ignore feature when ignoring three SYSREF± events.

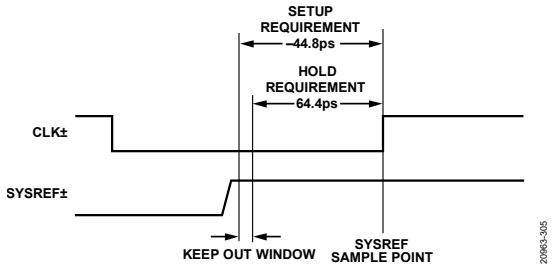


Figure 75. SYSREF± Setup and Hold Time Requirements, SYSREF± Low to High Transition Using Rising Edge CLK± (Default)

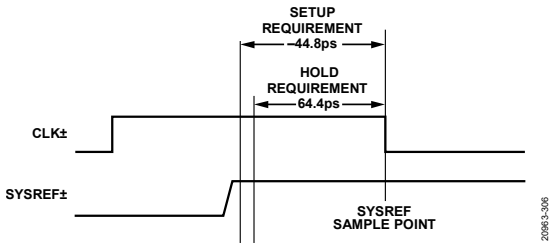


Figure 76. SYSREF± Low to High Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4 = 0, Register 0x0120, Bit 3 = 1)

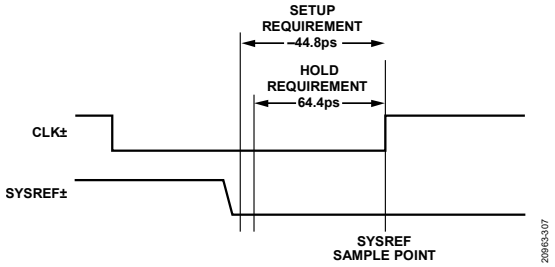


Figure 77. SYSREF± High to Low Transition Using Rising Edge Clock Capture (Register 0x0120, Bit 4 = 1, Register 0x0120, Bit 3 = 0)

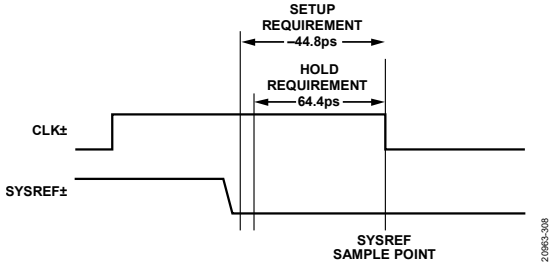


Figure 78. SYSREF± High to Low Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4 = 1, Register 0x0120, Bit 3 = 1)

SYSREF± SETUP AND HOLD WINDOW MONITOR

To ensure a valid SYSREF signal capture, the AD9094 has a SYSREF± setup and hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup and hold margin on the interface through the memory map. Figure 80 and Figure 81 show the setup and hold status values for different phases of SYSREF±. The setup detector returns the status of the SYSREF± signal before the CLK± edge, and the hold detector returns the status of the SYSREF signal after the CLK± edge. Register 0x0128 stores the status of SYSREF± and lets the user know if the SYSREF± signal is captured by the ADC.

Table 15 shows the description of the contents of Register 0x128 and how to interpret them.

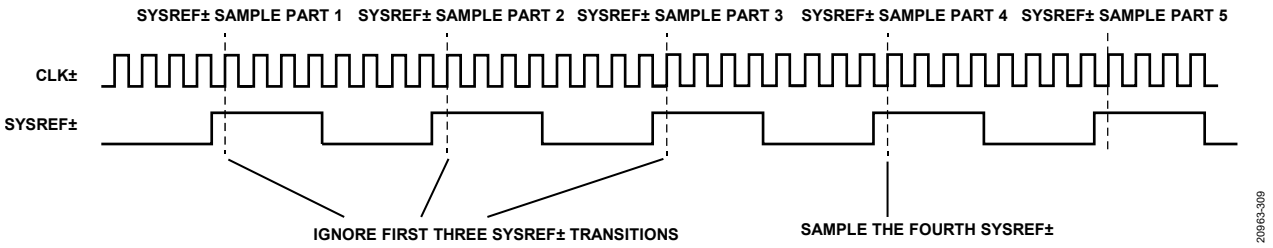


Figure 79. SYSREF± Ignore Example (SYSREF± N Shot Ignore Counter Select, Register 0x0121, Bits[3:0] = 0011)

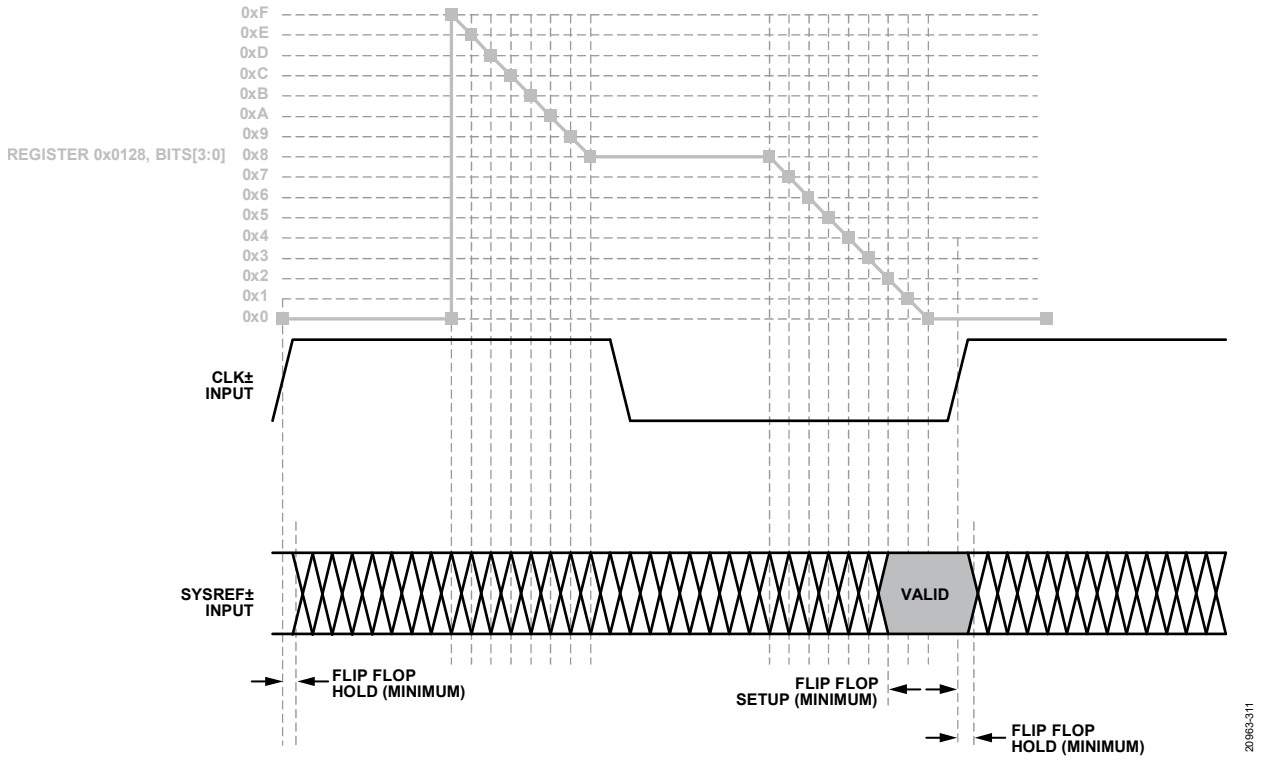


Figure 80. SYSREF± Setup Detector

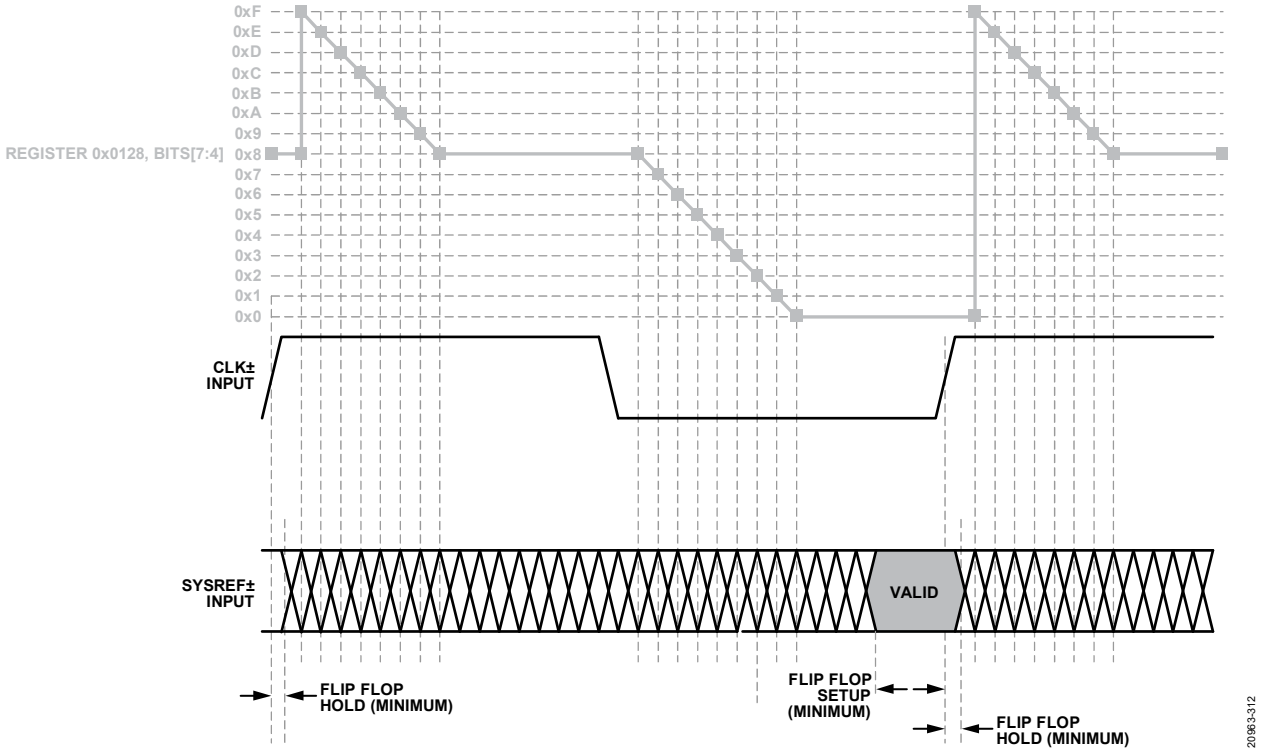


Figure 81. SYSREF± Hold Detector

Table 15. SYSREF± Setup/Hold Monitor, Register 0x0128

Register 0x0128, Bits[7:4], Hold Status	Register 0x0128, Bits[3:0], Setup Status	Description
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

TEST MODES

ADC TEST MODES

The AD9094 has various test options that assist in the system level implementation. The AD9094 has ADC test modes that are available in Register 0x0550. These test modes are described in Table 16. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some test patterns are subject to output formatting and some are not. To reset the pseudorandom noise (PN) generators from the PN sequence, set Bit 4 or Bit 5 of Register 0x0550. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), however, the test does require an encode clock.

For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Table 16. ADC Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/Seed Value	Sample (N, N + 1, N + 2, ...)
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	00 0000 0000 0000	Not applicable	Not applicable
0010	Positive full-scale short	01 1111 1111 1111	Not applicable	Not applicable
0011	Negative full-scale short	10 0000 0000 0000	Not applicable	Not applicable
0100	Checkerboard	10 1010 1010 1010	Not applicable	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One word, zero word toggle	11 1111 1111 1111	Not applicable	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x0551 to Register 0x0558	Not applicable	User Pattern 1 (Bits[15:2]), User Pattern 2 (Bits[15:2]), User Pattern 3 (Bits[15:2]), User Pattern 4 (Bits[15:2]), User Pattern 1 (Bits[15:2]) … for repeat mode User Pattern 1 (Bits[15:2]), User Pattern 2 (Bits[15:2]), User Pattern 3 (Bits[15:2]), User Pattern 4 (Bits[15:2]), 0x0000 … for single mode
1111	Ramp output	(x) % 2^{14}	Not applicable	(x) % 2^{14}, (x + 1) % 2^{14}, (x + 2) % 2^{14}, (x + 3) % 2^{14}

JESD204B BLOCK TEST MODES

In addition to the ADC pipeline test modes, the AD9094 has flexible test modes in the JESD204B block. These test modes are listed in Register 0x0573 and Register 0x0574. The test patterns can be injected at various points along the output datapath. These test injection points are shown in Figure 61. Table 17 describes the various test modes available in the JESD204B block. For the AD9094, a transition from test modes (Register 0x0573 ≠ 0x00) to normal mode (Register 0x0573 = 0x00) requires an SPI soft reset. To perform this reset, write 0x81 to Register 0x0000 (self cleared).

Transport Layer Sample Test Mode

The transport layer samples are implemented in the AD9094 as defined in the JEDEC JESD204B specification. These tests are shown in Register 0x0571, Bit 5. The test pattern is equivalent to the raw samples from the ADC.

Interface Test Modes

The interface test modes are described in Register 0x0573, Bits[3:0], and in Table 17. The interface tests can be injected at various points along the data. See Figure 61 for more information on the test injection points. Register 0x0573, Bits[5:4] show where these tests are injected.

Table 18, Table 19, and Table 20 show examples of some test modes when injected at the JESD204B sample input, PHY 10-bit input, and scrambler 8-bit input. In Table 18 through Table 20, UPx represents the user pattern control bits from the customer register map.

Data Link Layer Test Modes

The data link layer test modes are implemented in the AD9094 as defined in the JEDEC JESD204B specification. These tests are shown in Register 0x0574, Bits[2:0]. The test patterns inserted at the data link layer are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, write 0xC0 to Register 0x0572 to disable SYNCINB±x.

Table 17. JESD204B Interface Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checkerboard	0x5555, 0xAAAA, 0x5555, …	Not applicable
0010	1/0 word toggle	0x0000, 0xFFFF, 0x0000, …	Not applicable
0011	31-bit PN sequence	$x^{31} + x^{28} + 1$	0x0003AFFF
0100	23-bit PN sequence	$x^{23} + x^{18} + 1$	0x003AFF
0101	15-bit PN sequence	$x^{15} + x^{14} + 1$	0x03AF
0110	9-bit PN sequence	$x^{9} + x^{5} + 1$	0x092
0111	7-bit PN sequence	$x^{7} + x^{6} + 1$	0x07
1000	Ramp output	(x) % 2^{16}	Ramp size depends on test injection point
1110	Continuous/repeat user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then zeros

Table 18. JESD204B Sample Input for M = 2, S = 2, N' = 8 (Register 0x0573, Bits[5:4] = 0)

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	9-Bit PN	23-Bit PN	User Repeat	User Single
0	0	0	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
0	0	1	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
0	1	0	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
0	1	1	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0	0	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
1	0	1	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
1	1	0	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
1	1	1	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0	0	0x55	0x00	(x + 2) % 2^{8}	0xC9	0x00	UP3[15:9]	UP3[15:9]
2	0	1	0x55	0x00	(x + 2) % 2^{8}	0xC9	0x00	UP3[15:9]	UP3[15:9]

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	9-Bit PN	23-Bit PN	User Repeat	User Single
2	1	0	0x55	0x00	(x + 2) % 2^8	0xC9	0x00	UP3[15:9]	UP3[15:9]
2	1	1	0x55	0x00	(x + 2) % 2^8	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0	0	0xAA	0xFF	(x + 3) % 2^8	0xA9	0x29	UP4[15:9]	UP4[15:9]
3	0	1	0xAA	0xFF	(x + 3) % 2^8	0xA9	0x29	UP4[15:9]	UP4[15:9]
3	1	0	0xAA	0xFF	(x + 3) % 2^8	0xA9	0x29	UP4[15:9]	UP4[15:9]
3	1	1	0xAA	0xFF	(x + 3) % 2^8	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0	0	0x55	0x00	(x + 4) % 2^8	0x98	0xB8	UP1[15:9]	0x0000
4	0	1	0x55	0x00	(x + 4) % 2^8	0x98	0xB8	UP1[15:9]	0x0000
4	1	0	0x55	0x00	(x + 4) % 2^8	0x98	0xB8	UP1[15:9]	0x0000
4	1	1	0x55	0x00	(x + 4) % 2^8	0x98	0xB8	UP1[15:9]	0x0000

Table 19. Physical Layer 10-Bit Input (Register 0x0573, Bits[5:4] = 1)

10-Bit Symbol Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	9-Bit PN	23-Bit PN	User Repeat	User Single
0	0x155	0x000	(x) % 2^{10}	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	(x + 1) % 2^{10}	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	(x + 2) % 2^{10}	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	(x + 3) % 2^{10}	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	(x + 4) % 2^{10}	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	(x + 5) % 2^{10}	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	(x + 6) % 2^{10}	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	(x + 7) % 2^{10}	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	(x + 8) % 2^{10}	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	(x + 9) % 2^{10}	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	(x + 10) % 2^{10}	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	(x + 11) % 2^{10}	0x3DD	0x008	UP4[15:6]	0x000

Table 20. Scrambler 8-Bit Input (Register 0x0573, Bits[5:4] = 10)

8-Bit Octet Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	9-Bit PN	23-Bit PN	User Repeat	User Single
0	0x55	0x00	(x) % 2^8	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	(x + 1) % 2^8	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	(x + 2) % 2^8	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	(x + 3) % 2^8	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	(x + 4) % 2^8	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	(x + 5) % 2^8	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	(x + 6) % 2^8	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	(x + 7) % 2^8	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	(x + 8) % 2^8	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	(x + 9) % 2^8	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	(x + 10) % 2^8	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	(x + 11) % 2^8	0xAC	0xFF	UP4[15:9]	0x00

SPI

The AD9094 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 21). The SCLK (serial clock) pin is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input and output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 21. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface, reads, and writes.
SDIO	Serial data input and output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 4 and Table 5.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device (streaming). The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This bit allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

HARDWARE INTERFACE

The pins described in Table 21 comprise the physical interface between the user programming device and the serial port of the AD9094. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9094 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 22 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 1.0). The AD9094 device specific features are described in the Memory Map section.

Table 22. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock divider via the SPI.
Test Input and Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
SERDES Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Analog Devices SPI registers (Register 0x0000 to Register 0x000D and Register 0x18A6 to Register 0x1A4D), the ADC function registers (Register 0x003F to Register 0x027A, Register 0x0701, and Register 0x073B), and the digital outputs and test modes registers (Register 0x0550 to Register 0x1262).

Unassigned and Reserved Locations

Some address and bit locations are not included in Table 23 and are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x0561). If the entire address location is open (for example, Address 0x0013), do not write to this address location.

Default Values

After the AD9094 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table (see Table 23).

Logic Levels

Logic level terminology is as follows:

- Bit is set is synonymous with bit is set to Logic 1 or writing Logic 1 for the bit.
- Clear a bit is synonymous with bit is set to Logic 0 or writing Logic 0 for the bit.
- X denotes a don't care bit.

ADC Pair Addressing

The AD9094 functionally operates as two pairs of dual IF receiver channels. There are two ADCs in each pair for a total of four each for the AD9094 device. To access the SPI registers for each pair, write the pair index in Register 0x0009. The pair index register must be written prior to any other SPI write to the AD9094.

Channel Specific Registers

Some channel setup functions, such as the fast detect control (Register 0x0247), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 23 as local. To access these local registers and bits, set the appropriate Channel A and Channel C or Channel B and Channel D bits in Register 0x0008. The particular channel that is addressed depends on the pair selection written to Register 0x0009. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A and Channel C or Channel B and Channel D to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. If both pairs and both channels are selected via Register 0x0009 and Register 0x0008, the device returns the value for Channel A.

The register names listed in Table 23 are prefixed with either global map, channel map, JESD204B map, or pair map. Registers in the pair map and JESD204B map apply to a pair of channels, either Pair A and Pair B or Pair C and Pair D. To write registers in the pair map and JESD204B map, the pair index register (Register 0x0009) must be written to address the appropriate pair. The SPI Configuration A (Register 0x0000), SPI Configuration B (Register 0x0001), and pair index (Register 0x0009) registers are the only registers that reside in the global map. Registers in the channel map are local to each channel: Channel A, Channel B, Channel C, or Channel D. To write registers in the channel map, the pair index register (Register 0x0009) must be written first to address the desired pair (Pair A and Pair B or Pair C and Pair D) followed by writing the device index register (Register 0x0008) to select the desired channel (Channel A and Channel C or Channel B and Channel D).

For example, to write Channel A to a test mode (set by Register 0x0550), write 0x01 to Register 0x0009 to select Pair A and Pair B and then write 0x01 to Register 0x0008 to select Channel A. Next, write Register 0x0550 to the value for the desired test mode. To write all channels to a test mode (set by Register 0x0550), write Register 0x0009 to a value of 0x03 to select both Pair A and Pair B and Pair C and Pair D and then write Register 0x0008 to a value of 0x03 to select Channel A, Channel B, Channel C, and Channel D. Next, write Register 0x0550 to the value for the desired test mode.

SPI Soft Reset

When 0x81 is programmed to Register 0x0000 and a soft reset is issued, the AD9094 requires 5 ms to recover. When programming the AD9094 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP REGISTER

All address locations that are not included in Table 23 are not currently supported for this device and must not be written.

Table 23. Memory Map Register Details

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0000	Global Map SPI Configuration A	7	Soft reset (self clearing)		When a soft reset is issued, the user must wait 5 ms before writing to any other register. This wait provides sufficient time for the boot loader to complete.	0x0	R/W
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
		6	LSB first mirror			0x0	R/W
				1	LSB is shifted first for all SPI operations.		
				0	MSB is shifted first for all SPI operations.		
		5	Address ascension mirror	0	Multibyte SPI operations cause addresses to autoincrement.	0x0	R/W
				1	Multibyte SPI operations cause addresses to autoincrement.		
		4	Reserved		Reserved.	0x0	R
		3	Reserved		Reserved.	0x0	R
		2	Address ascension	0	Multibyte SPI operations cause addresses to autoincrement.	0x0	R/W
				1	Multibyte SPI operations cause addresses to autoincrement.		
		1	LSB first	1	MSB is shifted first for all SPI operations.	0x0	R/W
				0	MSB is shifted first for all SPI operations.		
		0	Soft reset (self clearing)		When a soft reset is issued, the user must wait 5 ms before writing to any other register. This wait provides sufficient time for the boot loader to complete.	0x0	R/W
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
0x0001	Global Map SPI Configuration B	7	Single instruction	0	SPI streaming is enabled.	0x0	R/W
				1	Streaming (multibyte read/write) is disabled. Only one read or write operation is performed regardless of the state of the CSB line.		
		[6:2]	Reserved		Reserved.	0x0	R
		1	Datapath soft reset (self clearing)	0	Normal operation.	0x0	R/W
				1	Datapath soft reset (self clearing).		
		0	Reserved		Reserved.	0x0	R
0x0002	Channel Map Chip Configuration	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Channel power modes		Channel Power Modes.	0x0	R/W
				00	Normal mode (power-up).		
				10	Standby mode. The digital datapath clocks are disabled, the JESD204B interface is enabled, and the outputs are enabled.		
				11	Power-down mode. The digital datapath clocks are disabled, the digital datapath is held in reset, the JESD204B interface is disabled, and the outputs are disabled.		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0003	Pair Map Chip Type	[7:0]	CHIP_TYPE		Chip Type.	0x3	R
				0x3	High speed ADC.		
0x0004	Pair Map Chip ID LSB	[7:0]	CHIP_ID		Chip ID.	0xDB	R
0x0006	Pair Map Chip Grade	[7:4]	CHIP_SPEED_GRADE		Chip Speed Grade.	0x0	R
				0101	500 MHz.		
		[3:0]	Reserved		Reserved.	0x0	R
0x0008	Pair Map Device Index	[7:2]	Reserved		Reserved.	0x0	R
		1	Channel B/Channel D	0	ADC Core B and ADC Core D does not receive the next SPI command.	0x1	R/W
				1	ADC Core B and ADC Core D receives the next SPI command.		
		0	Channel A/Channel C	0	ADC Core A and ADC Core C does not receive the next SPI command.	0x1	R/W
				1	ADC Core A and ADC Core C receives the next SPI command.		
0x0009	Global Map Pair Index	[7:2]	Reserved		Reserved.	0x0	R
		1	Pair C/D	0	ADC Pair C and ADC Pair D does not receive the next read/write command from the SPI interface.	0x1	R/W
				1	ADC Pair C and ADC Pair D does not receive the next read/write command from the SPI interface.		
		0	Pair A/B	0	ADC Pair A and ADC Pair B does not receive the next read/write command from the SPI interface.	0x1	R/W
				1	ADC Pair A and ADC Pair B does receive the next read/write command from the SPI interface.		
0x000A	Pair Map Scratch Pad	[7:0]	Scratch pad		Chip Scratch Pad Register. This register provides a consistent memory location for software debug.	0x7	R/W
0x000B	Pair Map SPI Revision	[7:0]	SPI_REVISION		SPI Revision Register (0x01 = Revision 1.0).	0x1	R
				00000001	Revision 1.0.		
0x000C	Pair Map Vendor ID LSB	[7:0]	CHIP_VENDOR_ID[7:0]		Vendor ID.	0x56	R
0x000D	Pair Map Vendor ID MSB	[7:0]	CHIP_VENDOR_ID[15:8]		Vendor ID.	0x4	R
0x003F	Channel Map Chip Power-Down Pin	7	PDWN/STBY disable		This register is used in conjunction with Register 0x0040.	0x0	R/W
				0	Power-down pin (PDWN/STBY) is enabled and global pin control selection is enabled (default).		
				1	Power-down pin (PDWN/STBY) is disabled and ignored and global pin control selection is ignored.		
		[6:0]	Reserved		Reserved.	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0040	Pair Map Chip Pin Control 1	[7:6]	PDWN/STBY function	00	Power-down pin. Assertion of the external power-down pin (PDWN/STBY) causes the chip to enter full power-down mode.	0x0	R/W
				01	Standby pin. Assertion of the external power-down (PDWN/STBY) causes the chip to enter standby mode.		
				10	Pin disabled. Assertion of the external power-down pin (PDWN/STBY) is ignored.		
		[5:3]	Fast Detect B/D (FD_B/FD_D)	000	Fast Detect B and Fast Detect D output.	0x7	R/W
				001	JESD204B LMFC output.		
				010	JESD204B internal SYNC~ output.		
				111	Disabled (configured as an input with a weak pull-down resistor).		
		[2:0]	Fast Detect A/C (FD_A/FD_C)	000	Fast Detect A and Fast Detect C output.	0x7	R/W
				001	JESD204B LMFC output.		
				010	JESD204B internal SYNC~ output.		
				111	Disabled (configured as an input with a weak pull-down resistor.		
0x0108	Pair Map Clock Divider Control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Clock divider	000	Divide by 1.	0x1	R/W
				001	Divide by 2.		
				011	Divide by 4.		
				111	Divide by 8.		
0x0109	Channel Map Clock Divider Phase	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase offset	0000	0 input clock cycles delayed.	0x0	R/W
				0001	½ input clock cycles delayed (invert clock).		
				0010	1 input clock cycle delayed.		
				0011	1 ½ input clock cycles delayed.		
				0100	2 input clock cycles delayed.		
				0101	2 ½ input clock cycles delayed.		
				0110	3 input clock cycles delayed.		
				0111	3 ½ input clock cycles delayed.		
				1000	4 input clock cycles delayed.		
				1001	4 ½ input clock cycles delayed.		
				1010	5 input clock cycles delayed.		
				1011	5 ½ input clock cycles delayed.		
				1100	6 input clock cycles delayed.		
				1101	6 ½ input clock cycles delayed.		
				1110	7 input clock cycles delayed.		
				1111	7 ½ input clock cycles delayed.		
0x010A	Pair Map Clock Divider SYSREF± Control	7	Clock divider autophase adjust	0	Clock divider phase is not changed by SYSREF± (disabled).	0x0	R/W
				1	Clock divider phase is automatically adjusted by SYSREF± (enabled).		
		[6:4]	Reserved		Reserved.	0x0	R
		[3:2]	Clock divider negative skew window	00	No negative skew. SYSREF± must be captured accurately.	0x0	R/W
				01	½ device clocks of negative skew.		
				10	1 device clock of negative skew.		
				11	1 ½ device clocks of negative skew.		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
		[1:0]	Clock divider positive skew window	00	No positive skew. SYSREF± must be captured accurately.	0x0	R/W
				01	½ device clocks of positive skew.		
				10	1 device clock of positive skew.		
				11	1 ½ device clocks of positive skew.		
0x0110	Pair Map Clock Delay Control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Clock delay mode select		Clock Delay Mode Select. This register is used in conjunction with Register 0x0111 and Register 0x0112.	0x0	R/W
				000	No clock delay.		
				001	Reserved.		
				010	Fine delay. Only Delay Step 0 to Delay Step 16 are valid.		
				011	Fine delay (lowest jitter). Only Delay Step 0 to Delay Step 16 are valid.		
				100	Fine delay. All 192 delay steps are valid.		
				101	Reserved (same as 100).		
				110	Fine delay enabled (all 192 delay steps are valid), and super fine delay enabled (all 128 delay steps are valid).		
0x0111	Channel Map Clock Super Fine Delay	[7:0]	Clock super fine delay adjust		Clock Super Fine Delay Adjust. This register is an unsigned control to adjust the super fine sample clock delay in 0.25 ps steps.	0x0	R/W
				0x00	0 delay steps.		
				…	…		
				0x08	8 delay steps.		
				…	…		
				0x08	128 delay steps.		
0x0112	Channel Map Clock Fine Delay	[7:0]	Clock fine delay adjust		Clock Fine Delay Adjust. This register is an unsigned control to adjust the fine sample clock skew in 1.725 ps steps.	0xC0	R/W
				0x00	0 delay steps.		
				…	…		
				0x08	8 delay steps.		
				…	…		
				0xC0	192 delay steps.		
0x011A	Clock Detection Control	[7:5]	Reserved		Reserved.	0x0	R/W
		[4:3]	Clock detection threshold		Clock Detection Threshold.	0x1	R/W
				01	Threshold 1 for $f_S \geq 300$ MSPS.		
				11	Threshold 2 for $f_S < 300$ MSPS.		
		[2:0]	Reserved		Reserved.	0x1	R/W
0x011B	Pair Map Clock Status	[7:1]	Reserved		Reserved.	0x0	R
		0	Input clock detect		Clock Detection Status.	0x0	R
				0	Input clock not detected.		
				1	Input clock detected and locked.		
0x011C	Clock DCS Control 1	[7:3]	Reserved		Reserved.	0x1	R/W
		1	Clock DCS 1 enable	0	DCS 1 bypassed.	0x0	R/W
				1	DCS 1 enabled.		
		0	Clock DCS 1 power-up	0	DCS 1 powered down.	0x0	R/W
				1	DCS 1 powered up. The DCS must be powered up before being enabled.		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x011E	Clock DCS Control 2 (this register must be set to the same value as DCS Control 1)	[7:3]	Reserved		Reserved.	0x11	R/W
		1	Clock DCS 2 enable	0	DCS 2 bypassed.	0x0	R/W
				1	DCS 2 enabled.		
		0	Clock DCS 2 power-up	0	DCS 2 powered down.	0x0	R/W
				1	DCS 2 powered up. The DCS must be powered up before being enabled.		
0x011F	Clock DCS Control 3	[7:0]	Clock DCS 3 enable	0x84	DCS 3 bypassed.	0x84	R/W
				0x81	DCS 3 enabled.		
0x0120	Pair Map SYSREF Control 1	7	Reserved		Reserved.	0x0	R
		6	SYSREF± flag reset	0	Normal flag operation.	0x0	R/W
				1	SYSREF± flags are held in reset (setup and hold error flags are cleared).		
		5	Reserved		Reserved.	0x0	R
		4	SYSREF± transition select	0	SYSREF± is valid on low to high transitions using the selected CLK± edge. When changing this setting, SYSREF± mode select must be set to disabled.	0x0	R/W
				1	SYSREF± is valid on high to low transitions using the selected CLK± edge. When changing this setting, SYSREF± mode select must be set to disabled.		
		3	CLK± edge select	0	Captured on the rising edge of CLK± input.	0x0	R/W
				1	Captured on the falling edge of CLK± input.		
		[2:1]	SYSREF± mode select	00	Disabled.	0x0	R/W
				01	Continuous.		
				10	N shot.		
		0	Reserved		Reserved.	0x0	R
0x0121	Pair Map SYSREF Control 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	SYSREF± N shot ignore counter select	0000	Next SYSREF± only (do not ignore).	0x0	R/W
				0001	Ignore the first SYSREF± transition.		
				0010	Ignore the first two SYSREF± transitions.		
				0011	Ignore the first three SYSREF± transitions.		
				0100	Ignore the first four SYSREF± transitions.		
				0101	Ignore the first five SYSREF± transitions.		
				0110	Ignore the first six SYSREF± transitions.		
				0111	Ignore the first seven SYSREF± transitions.		
				1000	Ignore the first eight SYSREF± transitions.		
				1001	Ignore the first nine SYSREF± transitions.		
				1010	Ignore the first 10 SYSREF± transitions.		
				1011	Ignore the first 11 SYSREF± transitions.		
				1100	Ignore the first 12 SYSREF± transitions.		
				1101	Ignore the first 13 SYSREF± transitions.		
				1110	Ignore the first 14 SYSREF± transitions.		
				1111	Ignore the first 15 SYSREF± transitions.		
0x0123	Pair Map SYSREF Control 4	7	Reserved		Reserved.	0x0	R
		[6:0]	SYSREF± timestamp delay, Bits[6:0]		SYSREF± Timestamp Delay (in Converter Sample Clock Cycles).	0x40	R/W
				0	0 sample clock cycle delay.		
				1	1 sample clock cycle delay.		
				…	…		
				127	127 sample clock cycle delay.		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0128	Pair Map SYSREF Status 1	[7:4]	SYSREF± hold status, Bits[7:4]		SYSREF± Hold Status. See Table 15 for more information.	0x0	R
		[3:0]	SYSREF± setup status, Bits[3:0]		SYSREF± Setup Status. See Table 15 for more information.	0x0	R
0x0129	Pair Map SYSREF Status 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase when SYSREF± captured		SYSREF± Divider Phase. This register represents the phase of the divider when SYSREF± was captured.	0x0	R
				0000	In phase.		
				0001	SYSREF± is ½ cycle delayed from the clock.		
				0010	SYSREF± is 1 cycle delayed from the clock.		
				0011	1½ input clock cycles are delayed.		
				0100	2 input clock cycles are delayed.		
				0101	2½ input clock cycles are delayed.		
				…	…		
				1111	7½ input clock cycles are delayed.		
0x012A	Pair Map SYSREF Status 3	[7:0]	SYSREF counter, Bits[7:0] increments when SYSREF± captured		SYSREF± count. This register is a running counter that increments whenever a SYSREF± event is captured and is reset by Register 0x0120, Bit 6. This register wraps around at 255. Read these bits only while Register 0x0120, Bits[2:1] are set to disabled.	0x0	R
0x01FF	Pair Map Chip Sync	[7:1]	Reserved		Reserved.	0x0	R
		0	Synchronization mode	0x0	Sample synchronization mode. The SYSREF± signal resets all internal sample dividers. Use this mode when synchronizing multiple chips, as specified in the JESD204B standard. If the phase of any of the dividers must change, the JESD204B link goes down.	0x0	R/W
				0x1	Partial synchronization/timestamp mode. The SYSREF± signal does not reset sample internal dividers. In this mode, the JESD204B link, the signal monitor, and the parallel interface clocks are not affected by the SYSREF± signal. The SYSREF± signal timestamps a sample as the signal passes through the ADC.		
0x0228	Channel Map Custom Offset	[7:0]	Offset adjust in LSBs from +127 to −128		Digital Datapath Offset. The twos complement offset adjustment aligns with least significant converter resolution bit.	0x0	R/W
0x0245	Channel Map Fast Detect Control	[7:4]	Reserved		Reserved.	0x0	R
		3	Force FD_A/FD_B/ FD_C/FD_D pins	0	Normal operation of the fast detect pins.	0x0	R/W
				1	Force a value on the fast detect pins (see Bit 2).		
		2	Force value of FD_A/ FD_B/FD_C/FD_D pins (if force pins are true, this value is output on FD_x pins)		The fast detect output pin for this channel is set to this value when the output is forced.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	Enable fast detect output	0	Fine fast detect disabled.	0x0	R/W
				1	Fine fast detect enabled.		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0247	Channel Map Fast Detect Upper Threshold LSB	[7:0]	Fast detect upper threshold, Bits[7:0]		LSBs of Fast Detect Upper Threshold. These are the 8 LSBs of the programmable 13-bit upper threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x0248	Channel Map Fast Detect Upper Threshold MSB	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect upper threshold, Bits[12:8]		MSBs of Fast Detect Upper Threshold. These are the 8 MSBs of the programmable 13-bit upper threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x0249	Channel Map Fast Detect Lower Threshold LSB	[7:0]	Fast detect lower threshold, Bits[7:0]		LSBs of Fast Detect Lower Threshold. These are the 8 LSBs of the programmable 13-bit lower threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x024A	Channel Map Fast Detect Lower Threshold MSB	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect lower threshold, Bits[12:8]		MSBs of Fast Detect Lower Threshold. These are the 8 MSBs of the programmable 13-bit lower threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x024B	Channel Map Fast Detect Dwell Time LSB	[7:0]	Fast detect dwell time, Bits[7:0]		LSBs of Fast Detect Dwell Time Counter Target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD_x pins are reset to 0.	0x0	R/W
0x024C	Channel Map Fast Detect Dwell Time MSB	[7:0]	Fast detect dwell time, Bits[15:8]		MSBs of Fast Detect Dwell Time Counter Target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD_x pins are reset to 0.	0x0	R/W
0x026F	Pair Map Signal Monitor Sync Control	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Signal monitor synchronization mode	0 1	Synchronization disabled. Only the next valid edge of the SYSREF± pin is used to synchronize the signal monitor block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF± is received, this bit is cleared. The SYSREF± input pin must be enabled to synchronize the signal monitor blocks.	0x0	R/W
0x0270	Channel Map Signal Monitor Control	[7:2]	Reserved		Reserved.	0x0	R
		1	Peak detector	0 1	Peak detector disabled. Peak detector enabled.	0x0	R/W
		0	Reserved		Reserved.	0x0	R
0x0271	Channel Map Signal Monitor Period 0	[7:0]	Signal monitor period, Bits[7:0]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs the operation. Bit 0 is ignored.	0x80	R/W
0x0272	Channel Map Signal Monitor Period 1	[7:0]	Signal monitor period, Bits[15:8]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Bit 0 is ignored.	0x0	R/W
0x0273	Channel Map Signal Monitor Period 2	[7:0]	Signal monitor period, Bits[23:16]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Bit 0 is ignored.	0x0	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0274	Channel Map Signal Monitor Status Control	[7:5]	Reserved		Reserved.	0x0	R
		4	Result update	1	Status update based on Bits[2:0] (self clearing).	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	Result selection	001	Peak detector placed on status readback signals.	0x1	R/W
0x0275	Channel Map Signal Monitor Status 0	[7:0]	Signal monitor result, Bits[7:0]		Signal Monitor Status Result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0276	Channel Map Signal Monitor Status 1	[7:0]	Signal monitor result, Bits[15:8]		Signal Monitor Status Result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0277	Channel Map Signal Monitor Status 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Signal monitor result, Bits[19:16]		Signal Monitor Status Result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0278	Channel Map Signal Monitor Status Frame Counter	[7:0]	Period count result, Bits[7:0]		Signal Monitor Frame Counter Status Bits. The frame counter increments whenever the period counter expires.	0x0	R
0x0279	Channel Map Signal Monitor Serial Framer Control	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Signal monitor SPORT over JESD204B enable	0 1	Disabled. Enabled.	0x0	R/W
0x027A	SPORT over JESD204B Input Selection (Local)	[7:6]	Reserved		Reserved.	0x0	R
		1	SPORT over JESD204B input selection		Signal Monitor Serial Framer Input Selection. When each individual bit is a 1, the corresponding signal statistics information is sent within the frame. 0 Disabled. 1 Peak detector data inserted in the serial frame.	0x1	R/W
		0	Reserved			0x0	R
0x0550	Channel Map Test Mode Control	7	User pattern selection	0 1	Continuous repeat. Single pattern.	0x0	R/W
		6	Reserved		Reserved.	0x0	R
		5	Reset PN long generator	0 1	Long PN enabled. Long PN held in reset.	0x0	R/W
		4	Reset PN short generator	0 1	Short PN enabled. Short PN held in reset.	0x0	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
		[3:0]	Test mode selection	0000	Off, normal operation.	0x0	R/W
				0001	Midscale short.		
				0010	Positive full scale.		
				0011	Negative full scale.		
				0100	Alternating checkerboard.		
				0101	PN sequence, long.		
				0110	PN sequence, short.		
				0111	1/0 word toggle.		
				1000	User pattern test mode (used with the test mode pattern selection and the User Pattern 1 through User Pattern 4 registers).		
				1111	Ramp output.		
0x0551	Pair Map User Pattern 1 LSB	[7:0]	User Pattern 1, Bits[7:0]		User Test Pattern 1 Least Significant Byte.	0x0	R/W
0x0552	Pair Map User Pattern 1 MSB	[7:0]	User Pattern 1, Bits[15:8]		User Test Pattern 1 Most Significant Byte.	0x0	R/W
0x0553	Pair Map User Pattern 2 LSB	[7:0]	User Pattern 2, Bits[7:0]		User Test Pattern 2 Least Significant Byte.	0x0	R/W
0x0554	Pair Map User Pattern 2 MSB	[7:0]	User Pattern 2, Bits[15:8]		User Test Pattern 2 Most Significant Byte.	0x0	R/W
0x0555	Pair Map User Pattern 3 LSB	[7:0]	User Pattern 3, Bits[7:0]		User Test Pattern 3 Least Significant Byte.	0x0	R/W
0x0556	Pair Map User Pattern 3 MSB	[7:0]	User Pattern 3, Bits[15:8]		User Test Pattern 3 Most Significant Byte.	0x0	R/W
0x0557	Pair Map User Pattern 4 LSB	[7:0]	User Pattern 4, Bits[7:0]		User Test Pattern 4 Least Significant Byte.	0x0	R/W
0x0558	Pair Map User Pattern 4 MSB	[7:0]	User Pattern 4, Bits[15:8]		User Test Pattern 4 most Significant Byte.	0x0	R/W
0x0559	Pair Map Output Control Mode 0	7	Reserved		Reserved.	0x0	R
		[6:4]	Reserved		Reserved.	0x0	R
		3	Reserved		Reserved.	0x0	R
		[2:0]	Converter Control Bit 0 selection	000	Tie low (1'b0).	0x0	R/W
				001	Overrange bit.		
				010	Signal monitor (SMON) bit.		
				011	Fast detect (FD) bit.		
				101	SYSREF±.		
				100	Reserved.		
				110	Reserved.		
				111	Reserved.		
0x0561	Pair Map Output Sample Mode	[7:3]	Reserved		Reserved.	0x0	R
		2	Sample invert	0	ADC sample data is not inverted.	0x0	R/W
				1	ADC sample data is inverted.		
		[1:0]	Data format select	00	Offset binary.	0x1	R/W
				01	Twos complement (default).		
0x0564	Pair Map Output Channel Select	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Converter channel swap control	0	Normal channel ordering.	0x0	R/W
				1	Channel swap enabled.		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x056E	JESD204B Map PLL Control	[7:4]	JESD204B lane rate control	0000	Lane rate = 6.75 Gbps to 13.5 Gbps.	0x0	R/W
				0001	Lane rate = 3.375 Gbps to 6.75 Gbps.		
				0011	Lane rate = 13.5 Gbps to 15 Gbps.		
				0101	Lane rate = 1.6875 Gbps to 3.375 Gbps.		
		[3:0]	Reserved		Reserved.	0x0	R
0x056F	JESD204B Map PLL Status	7	PLL lock status	0	Not locked.	0x0	R
				1	Locked.		
		[6:4]	Reserved		Reserved.	0x0	R
		3	Reserved		Reserved.	0x0	R
		[2:0]	Reserved		Reserved.	0x0	R
0x0570	JESD204B Map JTX Quick Configuration	[7:6]	Quick Configuration L		Number of Lanes (L) = $2^{0x0570[7:6]}$.	0x1	R/W
				0	L = 1.		
				1	L = 2.		
		[5:3]	Quick Configuration M		Number of Converters (M) = $2^{0x0570[5:3]}$.	0x1	R/W
				0	M = 1.		
				1	M = 2.		
				10	M = 4.		
		[2:0]	Quick Configuration F		Number of Octets/Frame (F) = $2^{0x0570[2:0]}$.	0x1	R/W
				0	F = 1.		
				1	F = 2.		
				10	F = 4.		
				11	F = 8.		
0x0571	JESD204B Map JTX Link Control 1	7	Standby mode	0	Standby mode forces zeros for all converter samples.	0x0	R/W
				1	Standby mode forces CGS (/K28.5/ characters).		
		6	Tail bit (t) PN	0	Disable.	0x0	R/W
				1	Enable.		
		5	Long transport layer test	0	JESD204B test samples disabled.	0x0	R/W
				1	JESD204B test samples enabled, long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) is sent on all link lanes.		
		4	Lane synchronization	0	Disable FACI uses /K28.7/.	0x1	R/W
				1	Enable FACI uses /K28.3/ and /K28.7/.		
		[3:2]	ILAS sequence mode	00	Initial lane alignment sequence disabled, (JESD204B 5.3.3.5).	0x1	R/W
				01	Initial lane alignment sequence enabled, (JESD204B 5.3.3.5).		
				11	Initial lane alignment sequence always on test mode, JESD204B data link layer test mode where the repeated lane alignment sequence (as specified in JESD204B 5.3.3.8.2) is sent on all lanes.		
		1	FACI	0	Frame alignment character insertion enabled (JESD204B 5.3.3.4).	0x0	R/W
				1	Frame alignment character insertion disabled for debug only (JESD204B 5.3.3.4).		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Link control	0	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for CGS is controlled by the SYNCINB±xx pin.	0x0	R/W
				1	JESD204B serial transmit link powered down (held in reset and clock gated).		
0x0572	JESD204B Map JTX Link Control 2	[7:6]	SYNCINB±xx pin control	00	Normal mode.	0x0	R/W
				10	Ignore SYNCINB±xx (force CGS).		
				11	Ignore SYNCINB±xx (force ILAS/user data).		
		5	SYNCINB±xx pin invert	0	SYNCINB±xx pin not inverted.	0x0	R/W
				1	SYNCINB±xx pin inverted.		
		4	SYNCINB±xx pin type	0	LVDS differential pair SYNC~ input.	0x0	R/W
				1	CMOS single-ended SYNC~ input.		
		3	Reserved		Reserved.	0x0	R
		2	8-bit/10-bit bypass	0	8-bit/10-bit enabled.	0x0	R/W
				1	8-bit/10-bit bypassed (most significant two bits are 0).		
		1	8-bit/10-bit invert	0	Normal.	0x0	R/W
				1	Invert symbol.		
		0	Reserved		Reserved.	0x0	R/W
0x0573	JESD204B Map JTX Link Control 3	[7:6]	Checksum mode	00	Checksum is the sum of all 8-bit registers in the link configuration table.	0x0	R/W
				01	Checksum is the sum of all individual link configuration fields (LSB aligned).		
				10	Checksum is disabled (set to zero). This setting is for test purposes only.		
				11	Unused.		
		[5:4]	Test injection point	0	N' sample input.	0x0	R/W
				1	10-bit data at 8-bit/10-bit output (for PHY testing).		
				10	8-bit data at scrambler input.		
		[3:0]	JESD204B test mode patterns	0	Normal operation (test mode disabled).	0x0	R/W
				1	Alternating checkerboard.		
				10	1/0 word toggle.		
				11	31-bit PN sequence: $x^{31} + x^{28} + 1$.		
				100	23-bit PN sequence: $x^{23} + x^{18} + 1$.		
				101	15-bit PN sequence: $x^{15} + x^{14} + 1$.		
				110	9-bit PN sequence: $x^{9} + x^{5} + 1$.		
				111	7-bit PN sequence: $x^{7} + x^{6} + 1$.		
				1000	Ramp output.		
				1110	Continuous and repeat user test.		
				1111	Single user test.		
0x0574	JESD204B Map JTX Link Control 4	[7:4]	ILAS delay	0	Transmit the ILAS on the first LMFC after SYNCINB±xx is deasserted.	0x0	R/W
				1	Transmit the ILAS on the second LMFC after SYNCINB±xx is deasserted.		
				10	Transmit the ILAS on the third LMFC after SYNCINB±xx is deasserted.		
				11	Transmit the ILAS on the fourth LMFC after SYNCINB±xx is deasserted.		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
				100	Transmit the ILAS on the fifth LMFC after SYNCINB±xx is deasserted.		
				101	Transmit the ILAS on the sixth LMFC after SYNCINB±xx is deasserted.		
				110	Transmit the ILAS on the seventh LMFC after SYNCINB±xx is deasserted.		
				111	Transmit the ILAS on the eighth LMFC after SYNCINB±xx is deasserted.		
				1000	Transmit the ILAS on the ninth LMFC after SYNCINB±xx is deasserted.		
				1001	Transmit the ILAS on the 10th LMFC after SYNCINB±xx is deasserted.		
				1010	Transmit the ILAS on the 11th LMFC after SYNCINB±xx is deasserted.		
				1011	Transmit the ILAS on the 12th LMFC after SYNCINB±xx is deasserted.		
				1100	Transmit the ILAS on the 13th LMFC after SYNCINB±xx is deasserted.		
				1101	Transmit the ILAS on the 14th LMFC after SYNCINB±xx is deasserted.		
				1110	Transmit the ILAS on the 15th LMFC after SYNCINB±xx is deasserted.		
				1111	Transmit the ILAS on the 16th LMFC after SYNCINB±xx is deasserted.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Data Link layer test mode	000	Normal operation (link layer test mode is disabled).	0x0	R/W
				001	Continuous sequence of /D21.5/ characters.		
				010	Reserved.		
				011	Reserved.		
				100	Modified random pattern (RPAT) test sequence.		
				101	Jitter tolerance and scrambled jitter pattern (JSPAT) test sequence.		
				110	JTSPAT test sequence.		
				111	Reserved.		
0x0578	JESD204B Map JTX LMFC Offset	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	LMFC phase offset value		LMFC Phase Offset Value. This value is the reset value for the LMFC phase counter when SYSREF± is asserted and is used for deterministic delay applications.	0x0	R/W
0x0580	JESD204B Map JTX DID Configuration	[7:0]	JESD204B transmitter DID value		JESD204x Serial Device Identification (DID) Number.	0x0	R/W
0x0581	JESD204B Map JTX BID Configuration	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JESD204B transmitter BID value		JESD204x Serial Bank Identification (BID) Number (Extension to DID).	0x0	R/W
0x0583	JESD204B Map JTX LID 0 Configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 0 LID value		JESD204x Serial Lane Identification (LID) Number for Lane 0.	0x0	R/W
0x0585	JESD204B Map JTX LID 1 Configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 1 LID value		JESD204x Serial Lane Identification (LID) Number for Lane 1.	0x2	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x058B	JESD204B Map JTX SCR L Configuration	7	JESD204B scrambling (SCR)	0	JESD204x scrambler disabled (SCR = 0).	0x1	R/W
				1	JESD204x scrambler enabled (SCR = 1).		
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B lanes (L)	0x0	One lane per link (L = 1).	0x1	R
				0x1	Two lanes per link (L = 2).		
0x058C	JESD204B Map JTX F Configuration	[7:0]	Number of octets per frame (F)		Number of Octets per Frame, F = Register 0x058C, Bits[7:0] + 1.	0x1	R
0x058D	JESD204B Map JTX K Configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Number of frames per multiframe (K)		JESD204x Number of Frames per Multiframe (K = Register 0x058D, Bits[4:0] + 1). Only values where F × K, which are divisible by 4, can be used.	0x1F	R/W
				00011	K = 4.		
				00111	K = 8.		
				01100	K = 12.		
				01111	K = 16.		
				10011	K = 20.		
				10111	K = 24.		
				11011	K = 28.		
				11111	K = 32.		
0x058E	JESD204B Map JTX M Configuration	[7:0]	Number of converters per link			0x1	R
				00000000	Link is connected to one virtual converter (M = 1).		
				00000001	Link is connected to two virtual converters (M = 2).		
				00000011	Link is connected to four virtual converters (M = 4).		
0x058F	JESD204B Map JTX CS N Configuration	[7:6]	Number of control bits (CS) per sample	00	No control bits (CS = 0).	0x0	R/W
				01	One control bit (CS = 1), Control Bit 0 only.		
		5	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)	00110	N = 7-bit resolution.	0xF	R/W
				00111	N = 8-bit resolution.		
				01000	N = 9-bit resolution.		
				01001	N = 10-bit resolution.		
				01010	N = 11-bit resolution.		
				01011	N = 12-bit resolution.		
				01100	N = 13-bit resolution.		
				01101	N = 14-bit resolution.		
				01110	N = 15-bit resolution.		
				01111	N = 16-bit resolution.		
0x0590	JESD204B map JTX Subclass Version NP Configuration	[7:5]	Subclass support	000	Subclass 0.	0x1	R/W
				001	Subclass 1.		
		[4:0]	ADC number of bits per sample (N')	00111	N' = 8.	0xF	R/W
				01111	N' = 16.		
0x0591	JESD204B Map JTX S Configuration	[7:5]	Reserved		Reserved.	0x1	R
		[4:0]	Samples per converter frame cycle (S)		Samples per Converter Frame Cycle (S = Register 0x0591, Bits[4:0] + 1).	0x0	R

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0592	JESD204B Map JTX HD CF Configuration	7	HD value	0	High density format disabled.	0x0	R
				1	High density format enabled.		
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	Control words per frame clock cycle per link (CF)		Number of Control Words per Frame Clock Cycle per Link (CF = Register 0x0592, Bits[4:0]).	0x0	R
0x05A0	JESD204B Map JTX Checksum 0 Configuration	[7:0]	Checksum 0 checksum value for SERDOUTxx0±		Serial Checksum Value for Lane 0. This value is automatically calculated for each lane. The sum (all link configuration parameters for Lane 0) is 256.	0xC3	R
0x05A1	JESD204B Map JTX Checksum 1 Configuration	[7:0]	Checksum 1 checksum value for SERDOUTxx1±		Serial Checksum Value for Lane 1. This value is automatically calculated for each lane. Sum (all link configuration parameters for Lane 1) is 256.	0xC4	R
0x05B0	SERDOUTxx0±/ SERDOUTxx1± Lane Power-Down	7	Reserved		Reserved.	0x1	R/W
		6	Reserved		Reserved.	0x1	R/W
		5	Reserved		Reserved.	0x1	R/W
		4	Reserved		Reserved.	0x1	R/W
		3	Reserved		Reserved.	0x1	R/W
		2	SERDOUTxx1± Lane 1 power-down		Physical Lane 1 Force Power-Down.	0x0	R/W
		1	Reserved		Reserved.	0x1	R/W
		0	SERDOUTxx0± Lane 0 power-down		Physical Lane 0 Force Power-Down.	0x0	R/W
0x05B2	JESD204B Map JTX Lane Assignment 1	7	Reserved		Reserved.	0x0	R
		[6:4]	Reserved		Reserved.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUTxx0± lane assignment	0	Logical Lane 0 (default).	0x0	R/W
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
0x05B3	JESD204B Map JTX Lane Assignment 2	7	Reserved		Reserved.	0x0	R
		[6:4]	Reserved		Reserved.	0x1	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUTx1± lane assignment	0	Logical Lane 0.	0x1	R/W
				1	Logical Lane 1 (default).		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
0x05C0	JESD204B Map JESD204B Serializer Drive Adjust	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Swing voltage SERDOUTxx0±	0	1.0 × DRVDD1 (differential).	0x1	R/W
				1	0.850 × DRVDD1 (differential).		
0x05C1	JESD204B Map JESD204B Serializer Drive Adjust	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Swing voltage SERDOUTxx1±	0	1.0 × DRVDD1 (differential).	0x1	R/W
				1	0.850 × DRVDD1 (differential).		

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x05C4	JESD204B Serializer Preemphasis Selection Register for Logical Lane 0	7	Post tap enable	0 1	Disable. Enable.	0x0	R/W
		[6:4]	Sets post tab level	0 1 10 11 100	0 dB (recommended when insertion loss = 0 dB to 4 dB when voltage swing setting is 0). 3 dB (recommended when insertion loss = 4 dB to 9 dB when voltage swing setting is 0). 6 dB (recommended when insertion loss = 9 dB to 14 dB when voltage swing setting is 0). 9 dB (recommended when insertion loss > 14 dB when voltage swing setting is 0). 12 dB.	0x0	R/W
		[3:0]	Reserved		Reserved.	0x0	R
0x05C6	JESD204B Serializer Preemphasis Selection Register for Logical Lane 1	7	Post tap polarity	0 1	Disable. Enable.	0x0	R/W
		[6:4]	Sets post tab level	0 1 10 11 100	0 dB (recommended when insertion loss = 0 dB to 4 dB when voltage swing setting is 0). 3 dB (recommended when insertion loss = 4 dB to 9 dB when voltage swing setting is 0). 6 dB (recommended when insertion loss = 9 dB to 14 dB when voltage swing setting is 0). 9 dB (recommended when insertion loss > 14 dB when voltage swing setting is 0). 12 dB.	0x0	R/W
		[3:0]	Reserved		Reserved.	0x0	R
0x0922	Large Dither Control	[7:0]	Large dither control	1110000 1110001	Enable. Disable.	0x70	R/W
0x1222	PLL Calibration	[7:0]	PLL calibration	 0x00 0x04	PLL Calibration. Normal operation. PLL calibration.	0x0	R/W
0x1228	JESD204B Start-Up Circuit Reset	[7:0]	JESD204B start-up circuit reset	 0x0F 0x4F	JESD204B Start-Up Circuit Reset. Normal operation. Start-up circuit reset.	0xF	R/W
0x1262	PLL Loss of Lock Control		PLL loss of lock control	 0x00 0x08	PLL Loss of Lock Control. Normal operation. Clear loss of lock.	0x0	R/W
0x0701	DC Offset Calibration	[7:0]	DC offset calibration control	0x06 0x86	Disable dc offset calibration. Enable dc offset calibration.	0x06	R/W
0x073B	DC Offset Calibration Control 2 (local)	7	DC Offset Calibration Enable 2	0 1	Enabled (must set to 0 when Register 0x0701, Bit 7 = 1). Disabled (must set to 1 when Register 0x0701, Bit 7 = 0).	0x1	R/W
		[6:0]	Reserved	111111	Reserved.	0x3F	R
0x18A6	Pair Map VREF Control	[7:5]	Reserved		Reserved.	0x0	R
		4	Reserved		Reserved.	0x0	R/W
		[3:1]	Reserved		Reserved.	0x0	R
		0	VREF control	0 1	Internal reference. External reference.	0x0	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x18E0	External V_{CM} Buffer Control 1	[7:0]	External V_{CM} Buffer Control 1		See the Input Common Mode section for details.	0x0	R/W
0x18E1	External V_{CM} Buffer Control 2	[7:0]	External V_{CM} Buffer Control 2		See the Input Common Mode section for details.	0x0	R/W
0x18E2	External V_{CM} Buffer Control 3	[7:0]	External V_{CM} Buffer Control 3		See the Input Common Mode section for details.	0x0	R/W
0x18E3	External V_{CM} Buffer Control	7	Reserved		Reserved.	0x0	R/W
		6	External V_{CM} buffer	1 0	Enable. Disable.	0x0	R/W
		[5:0]	External V_{CM} buffer current setting		See the Input Common Mode section for details.	0x0	R/W
0x18E6	Temperature Diode Export	[7:1]	Reserved		Reserved.	0x0	R/W
		0	Temperature diode export	1 0	Enable. Disable.	0x0	R/W
0x1908	Channel Map Analog Input Control	[7:6]	Reserved		Reserved.	0x0	R
		[5:4]	Reserved		Reserved.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	Analog input dc coupling control	 0 1	Analog Input DC Coupling Control. AC coupling. DC coupling.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	Reserved		Reserved.	0x0	R/W
0x1910	Channel Map Full-Scale Input Range	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Input full-scale control	0000 1010 1011 1100 1101 1110 1111	2.16 V p-p. 1.44 V p-p. 1.56 V p-p. 1.68 V p-p. 1.80 V p-p. 1.92 V p-p. 2.04 V p-p.	0xD	R/W
0x1A4C	Channel Map Buffer Control 1	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control 1	00110 01000 01010 01100 01110 10000 10010 10100 10110	120 µA. 160 µA. 200 µA. 240 µA. 280 µA. 320 µA. 360 µA. 400 µA. 440 µA.	0x8	R/W

Address	Register Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1A4D	Channel Map Buffer Control 2	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control 2	00110	120 µA.	0x8	R/W
				01000	160 µA.		
				01010	200 µA.		
				01100	240 µA.		
				01110	280 µA.		
				10000	320 µA.		
				10010	360 µA.		
				10100	400 µA.		
				10110	440 µA.		

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD9094 must be powered by the following seven supplies: AVDD1 = AVDD1_SR = 0.9 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.9 V, DRVDD1 = 0.9 V, DRVDD2 = 1.8 V, and SPIVDD = 1.8 V. For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP5054 quad-switching regulator be used to convert the 6.0 V or 12 V input rails to intermediate rails (1.3 V, 2.4 V, and 3.0 V). These intermediate rails are then post regulated by very low noise, low dropout (LDO) regulators (such as the ADP1762, ADP7159, ADP151, and ADP7118). Figure 82 shows the recommended power supply scheme for AD9094.

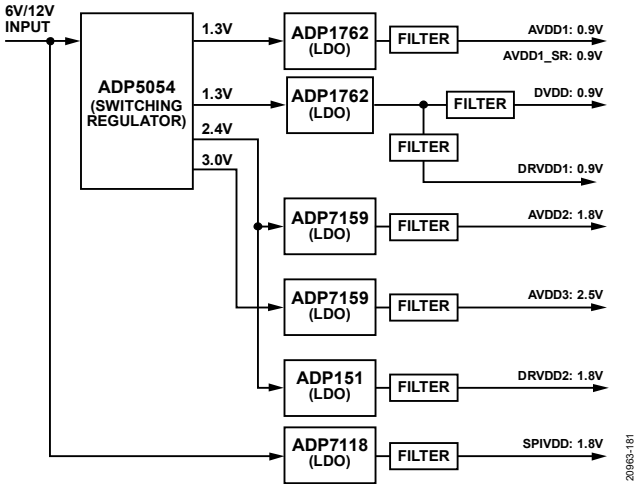


Figure 82. High Efficiency, Low Noise Power Solution for the AD9094

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 82 provides the lowest noise, highest efficiency power delivery system for the AD9094. If only one 0.9 V supply is available, route to AVDD1 first and then tap it off and isolate it with a ferrite bead or a filter choke, preceded by decoupling capacitors for AVDD1_SR, DVDD, and DRVDD1, in that order. The user can employ several different decoupling capacitors to cover both high and low frequencies. These capacitors must be placed close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to AGND to achieve the best electrical and thermal performance of the AD9094. Connect an exposed continuous copper plane on the PCB to the AD9094 exposed pad, Pin 0. The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias must be solder filled or plugged. The number of vias and the fill determine the resultant θ_{JA} measured on the board, which is shown in Table 7.

See Figure 83 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

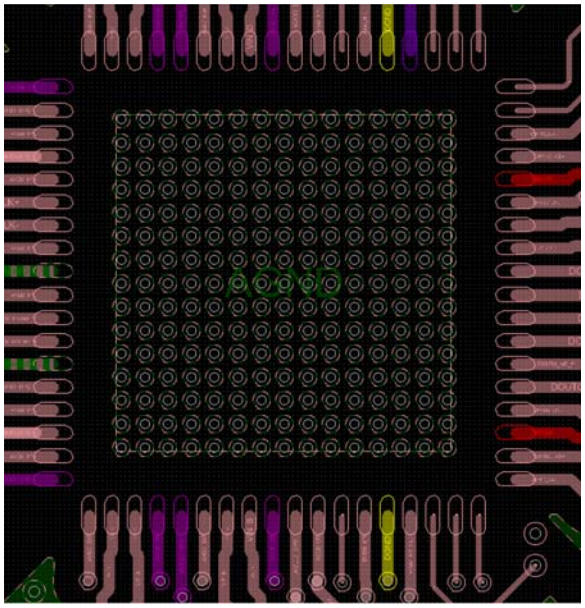


Figure 83. Recommended PCB Layout of Exposed Pad for the AD9094

AVDD1_SR (PIN 64) AND AGND_SR (PIN 63 AND PIN 67)

AVDD1_SR (Pin 64) and AGND_SR (Pin 63 and Pin 67) can provide a separate power supply node to the SYSREF± circuits of AD9094. If running in Subclass 1, the AD9094 can support periodic one shot or gapped signals. To minimize the coupling of this supply into the AVDD1 supply node, adequate supply bypassing is required.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CP-72-10	LFCSP	72-Lead Lead Frame Chip Scale Package [LFCSP]

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Junction Temperature Range	Package Description	Package Option
AD9094BCPZ-1000	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP]	CP-72-10
AD9094BCPZRL7-1000	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP]	CP-72-10

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
AD9094-1000EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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