THE DATASHEET OF

A4964KEVTR-J

A4964

Sensorless Sinusoidal Drive BLDC Controller

FEATURES AND BENEFITS

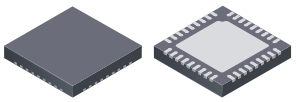
- Three-phase sensorless BLDC motor control FET driver
- Three-phase sinusoidal drive with soft start
- Sensorless start-up and commutation
- Windmill detection and synchronization
- Bootstrap gate drive for N-channel MOSFET bridge
- 5.5 to 50 V supply range
- SPI-compatible interface
- Programmable control modes: speed, voltage, current
- Peak current limiting
- Control via SPI or PWM
- Programmable gate drive for slew rate control
- LIN / PWM physical interface with wake
- Logic supply regulator with current limit
- MCU watchdog and reset
- Ignition switch interface
- Diagnostics, status, current, and speed feedback

APPLICATIONS

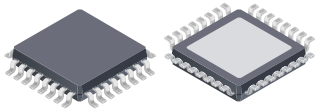
- Automotive fuel, oil, and urea pumps
- Automotive fans and blowers

PACKAGES

36-terminal eQFN
(suffix EV)



32-lead eQFP
(suffix JP)



Not to scale

DESCRIPTION

The A4964 is a three-phase, sensorless, brushless DC (BLDC) motor controller for use with external N-channel power MOSFETs and is specifically designed for automotive applications. It is designed to provide the motor control functions in a system where a small microcontroller provides the communication interface to a central ECU and intelligent fault and status handling. The A4964 provides the supply and watchdog for the microcontroller and the high-voltage interfaces between the microcontroller and the central ECU and ignition switch. The A4964 can also operate as an independent single-chip remote motor controller.

The motor is driven using 3-phase sinusoidal current drive where phase commutation is determined, without the need for independent position sensors, by monitoring the motor back-EMF (bemf). The sensorless start-up scheme includes forward and reverse pre-rotation (windmill) detection and synchronization, and allows the A4964 to operate over a wide range of motor and load combinations.

The A4964 can operate with duty cycle (voltage) control, current (torque limit) control, and closed-loop speed control. Control mode, operating mode, and control parameters are programmed through an SPI-compatible serial interface.

A single current sense amplifier provides peak current limiting and average current measurement through the serial interface.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults and can protect the power switches under most short-circuit conditions.

The A4964 is provided in a 36-terminal QFN and a 32-lead QFP, both with exposed thermal pad.

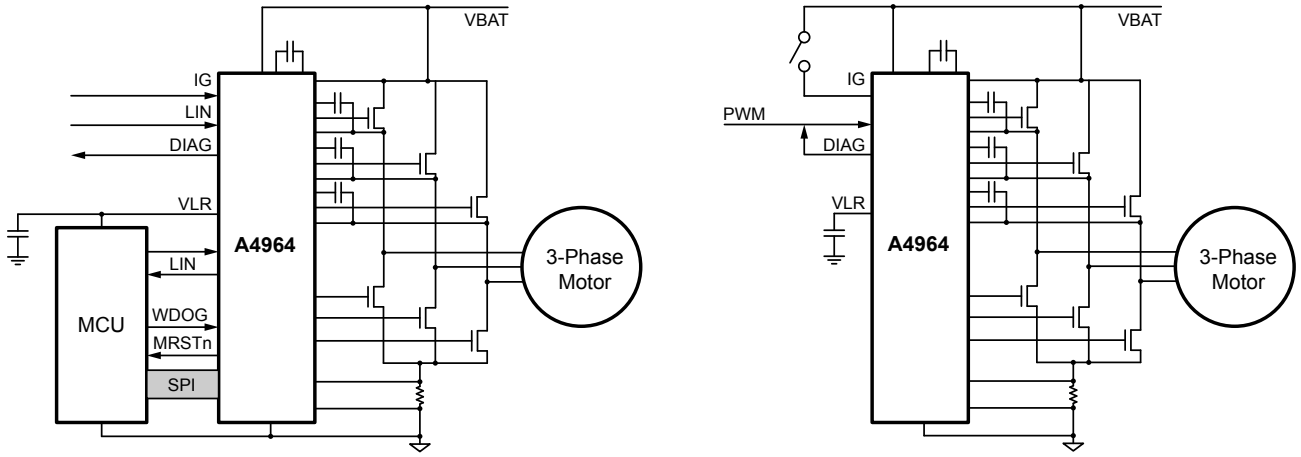


Figure 1: Typical Applications

SELECTION GUIDE

Part Number	Packing	Package
A4964KEVTR-J	1500 pieces per 13 in. reel	6 mm × 6 mm, 1.0 mm max. height, wettable flank 36-lead QFN with exposed thermal pad
A4964KJPTR-T	1500 pieces per 13 in. reel	7 mm × 7 mm, 1.6 mm max. height 32-lead QFP with exposed thermal pad

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}	VBB	–0.3 to 50	V
Pumped Regulator Terminal	V_{REG}	VREG	–0.3 to 16	V
Charge Pump Capacitor Low Terminals	V_{CP}	CP1	–0.3 to 16	V
Charge Pump Capacitor High Terminal	V_{CP2}	CP2	V_{CP1} – 0.3 to V_{REG} + 0.3	V
Logic Regulator Reference	V_{LR}	VLR	–0.3 to 6	V
Battery Compliant Inputs	V_{IG}	IG	–0.3 to 50	V
LIN Bus Interface	V_{LIN}	LIN	–40 to 50	V
Logic Inputs		STRn, SCK, SDI, WDOG, LTX	–0.3 to 6	V
Logic Outputs		SDO, MRSTn, LRX	–0.3 to 6	V
Logic Output		DIAG	–0.3 to 50	V
Bridge Drain Monitor Terminals	V_{BRG}	VBRG	–5 to 55	V
Bootstrap Supply Terminals	V_{CX}	CA, CB, CC	–0.3 to V_{REG} + 50	V
High-Side Gate Drive Output Terminals	V_{GHX}	GHA, GHB, GHC	V_{CX} – 16 to V_{CX} + 0.3	V
Motor Phase Terminals	V_{SX}	SA, SB, SC	V_{CX} – 16 to V_{CX} + 0.3	V
Low-Side Gate Drive Output Terminals	V_{GLX}	GLA, GLB, GLC	V_{REG} – 16 to 18	V
Sense Amplifier Inputs	V_{CSI}	CSP, CSM	–4 to 6	V
Ambient Operating Temperature Range	T_A		–40 to 150	°C
Maximum Continuous Junction Temperature	T_J(max)		165	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	EV package, 4-layer PCB based on JEDEC standard	27	°C/W
		JP package, 4-layer PCB based on JEDEC standard	23	°C/W
		JP package, 2-layer PCB with 3 in.^{2} copper each side	44	°C/W

[2] Additional thermal information available on the Allegro website.

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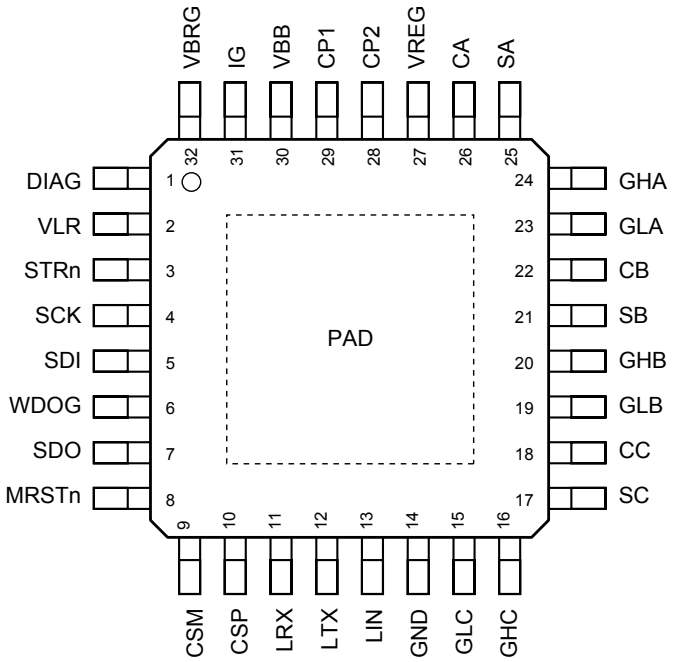
PINOUT DIAGRAMS AND TERMINAL LIST TABLES



32-lead eQFP (suffix JP)

Terminal List Table

Name	Number	Function
CA	26	Phase A Bootstrap Capacitor
CB	22	Phase B Bootstrap Capacitor
CC	18	Phase C Bootstrap Capacitor
CP1	29	Pump Capacitor
CP2	28	Pump Capacitor
CSM	9	Sense Amp Negative Input
CSP	10	Sense Amp Positive Input
DIAG	1	Programmable Diagnostic Output
GHA	24	Phase A HS FET Gate Drive
GHB	20	Phase B HS FET Gate Drive
GHC	16	Phase C HS FET Gate Drive
GLA	23	Phase A LS FET Gate Drive
GLB	19	Phase B LS FET Gate Drive
GLC	15	Phase C LS FET Gate Drive
GND	14	Ground
IG	31	Ignition Switch Input

Name	Number	Function
LIN	13	LIN Bus Connection
LTX	12	LIN Transmit Data Logic Input
LRX	11	LIN Receive Data Logic Output
MRSTn	8	MCU Reset Logic Output
SA	25	Phase A Motor Phase
SB	21	Phase B Motor Phase
SC	17	Phase C Motor Phase
SCK	4	Serial Clock Logic Input
SDI	5	Serial Data Logic Input
SDO	7	Serial Data Logic Output
STRn	3	Serial Strobe (Chip Select) Logic Input
VBB	30	Main Supply
VBRG	32	High-Side Drain Voltage Sense
VLR	2	VLR Logic Regulator Output
VREG	27	Gate Drive Supply Capacitor
WDOG	6	MCU Watchdog Logic Input
PAD	–	Thermal Pad; Connect to GND

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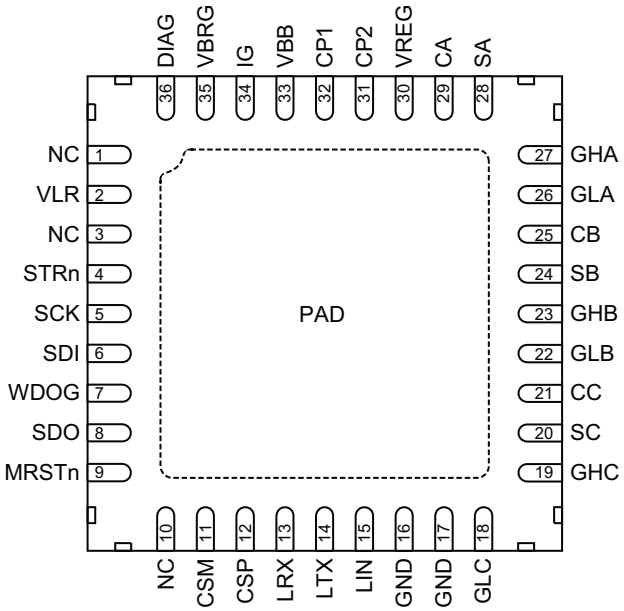

36-terminal eQFN (suffix EV)

Terminal List Table

Name	Number	Function
CA	29	Phase A Bootstrap Capacitor
CB	25	Phase B Bootstrap Capacitor
CC	21	Phase C Bootstrap Capacitor
CP1	32	Pump Capacitor
CP2	31	Pump Capacitor
CSM	11	Sense Amp Negative Input
CSP	12	Sense Amp Positive Input
DIAG	36	Programmable Diagnostic Output
GHA	27	Phase A HS FET Gate Drive
GHB	23	Phase B HS FET Gate Drive
GHC	19	Phase C HS FET Gate Drive
GLA	26	Phase A LS FET Gate Drive
GLB	22	Phase B LS FET Gate Drive
GLC	18	Phase C LS FET Gate Drive
GND	16	Ground; Connect GND Terminals Together
GND	17	Ground; Connect GND Terminals Together
IG	34	Ignition Switch Input

Name	Number	Function
LIN	15	LIN Bus Connection
LTX	14	LIN Transmit Data Logic Input
LRX	13	LIN Receive Data Logic Output
MRSTn	9	MCU Reset Logic Output
NC	3	No Connect
SA	28	Phase A Motor Phase
SB	24	Phase B Motor Phase
SC	20	Phase C Motor Phase
SCK	5	Serial Clock Logic Input
SDI	6	Serial Data Logic Input
SDO	8	Serial Data Logic Output
STRn	4	Serial Strobe (Chip Select) Logic Input
VBB	33	Main Supply
VBRG	35	High-Side Drain Voltage Sense
VLR	2	VLR Logic Regulator Output
VREG	30	Gate Drive Supply Capacitor
WDOG	7	MCU Watchdog Logic Input
PAD	–	Thermal Pad; Connect to GND

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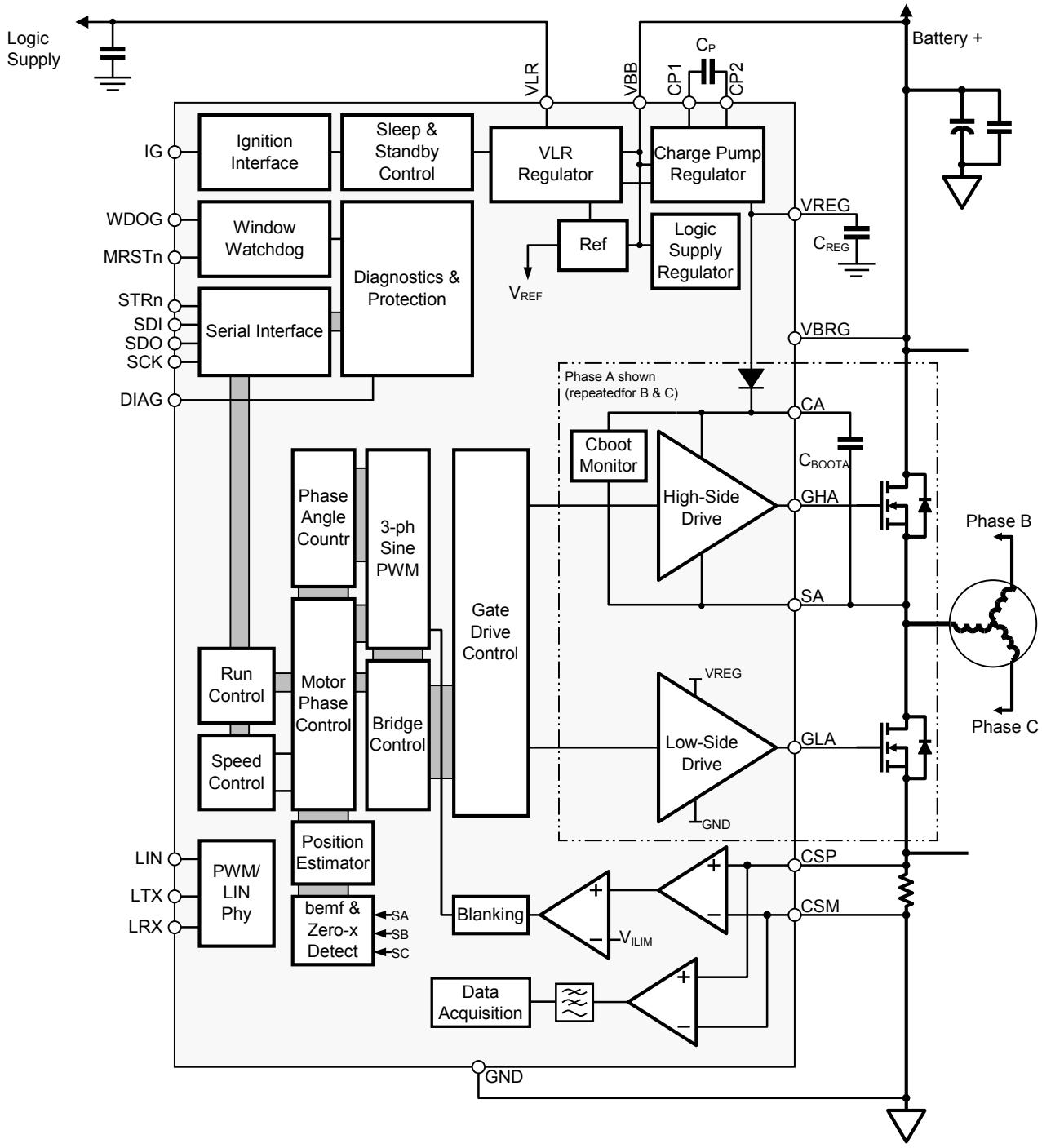
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range	V_{BB}	Operating; outputs active	5.5	–	50	V
		No unsafe states	0	–	50	V
VBB Quiescent Current	I_{BBQ}	RUN = 0, V_{BB} = 12 V	–	13	20	mA
VBB Sleep Current	I_{BBS}	RUN = 0, V_{LIN} = V_{BB} = 12 V, in sleep state	–	10	20	µA
VREG Output Voltage VRG = 0	V_{REG}	V_{BB} ≥ 7.5 V, I_{VREG} = 0 to 30 mA	7.5	8	8.5	V
		6 V ≤ V_{BB} < 7.5 V, I_{VREG} = 0 to 15 mA	7.5	8	8.5	V
		5.5 V ≤ V_{BB} < 6 V, I_{VREG} ≤ 10 mA	7.5	8	8.5	V
VREG Output Voltage VRG = 1	V_{REG}	V_{BB} ≥ 9 V, I_{VREG} = 0 to 30 mA	9	11	11.7	V
		7.5 V ≤ V_{BB} < 9 V, I_{VREG} = 0 to 20 mA	9	11	11.7	V
		6 V ≤ V_{BB} < 7.5 V, I_{VREG} = 0 to 15 mA	7.9	–	–	V
		5.5 V ≤ V_{BB} < 6 V, I_{VREG} ≤ 10 mA	7.9	9.5	–	V
VLR Output Voltage	V_{LR}	VLR = 0; I_{VLR} < 70 mA, V_{BB} > 6 V	3.1	3.3	3.5	V
		VLR = 1; I_{VLR} < 70 mA, V_{BB} > 6 V	4.8	5.0	5.2	V
VLR Regulator Current Limit	I_{LROC}		130	–	260	mA
VLR Regulator Shutdown Voltage Threshold	V_{LROSD}	VLR falling	1.2	–	–	V
VLR Regulator Enable Voltage Threshold	V_{LROE}	VLR rising	–	–	1.5	V
VLR Regulator Shutdown Lockout Period	t_{LRLO}		–	2	–	ms
VLR Regulator Pilot Current	I_{LROP}		–	2	–	mA
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.6	0.8	1.0	V
		I_D = 100 mA	1.5	2.2	2.8	V
Bootstrap Diode Resistance	r_D	$r_{D(100mA)} = (V_{fBOOT(150mA)} - V_{fBOOT(50mA)}) / 100$ mA	6	11	22	Ω
Bootstrap Diode Current Limit	I_{DBOOT}		250	500	750	mA
System Clock Period	t_{OSC}		47.5	50	52.5	ns

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE						
Turn-On Time	t_r	Switched mode, C_{LOAD} = 10 nF, 20% to 80%	–	190	–	ns
Turn-Off Time	t_f	Switched mode, C_{LOAD} = 10 nF, 80% to 20%	–	120	–	ns
Pull-Up On Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_G = -150 mA [1]	4	7	11	Ω
		T_J = 150°C, I_G = –150 mA [1]	9	12	20	Ω
Pull-Up Peak Source Current [1][8]	I_{PUPK}	V_{GS} = 0 V	–500	–600	–	mA
Pull-Down On Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_G = 150 mA	1.5	3	4.5	Ω
		T_J = 150°C, I_G = 150 mA	2.9	4	6	Ω
Pull-Down Peak Sink Current [8]	I_{PDPK}	V_{GS} > 9 V	600	750	–	mA
Turn-On Current 1	I_{R1}	V_{GS} = 0 V, VRG = 1, IR1 = 15	–	–75	–	mA
		Programmable range	–5	–	–75	mA
Turn-On Current 2	I_{R2}	V_{GS} = 0 V, VRG = 1, IR2 = 15	–	–75	–	mA
		Programmable range	–5	–	–75	mA
Turn-Off Current 1	I_{F1}	V_{GS} = 9 V, VRG = 1, IF1 = 15	–	75	–	mA
		Programmable range	5	–	75	mA
Turn-Off Current 2	I_{F2}	V_{GS} = 9 V, VRG = 1, IF2 = 15	–	75	–	mA
		Programmable range	5	–	75	mA
GHx Output Voltage High	V_{GHH}	Bootstrap capacitor fully charged	V_{CX} – 0.2	–	–	V
GHx Output Voltage Low	V_{GHL}	–10 µA < I_{GH} < 10 µA	–	–	V_{SX} + 0.3	V
GLx Output Voltage High	V_{GLH}		V_{REG} – 0.2	–	–	V
GLx Output Voltage Low	V_{GLL}	–10 µA < I_{GL} < 10 µA	–	–	0.3	V
GHx Passive Pull-Down	R_{GHPD}	V_{BB} = 0 V, I_{GH} = 500 µA	–	5	–	kΩ
GLx Passive Pull-Down	R_{GLPD}	V_{BB} = 0 V, I_{GL} = 500 µA	–	5	–	kΩ
Bridge PWM Period	t_{PW}	Default power-up value, DS = 0, PMD = 0	47.9	50.5	53.0	µs
		Programmable range, DS = 0, PMD = 0	20.1	–	70.5	µs
Bridge PWM Dither Step Period	Δt_{PW}	Default power-up value	–0.21	–0.2	–0.19	µs
		Programmable range	–0.2	–	–1.6	µs
Bridge PWM Dither Dwell Time	t_{DIT}	Default power-up value	0.95	1	1.05	ms
		Programmable range	1	–	10	ms
Dead Time (Turn-Off to Turn-On Delay) [2][5]	t_{DEAD}	Default power-up value	1.52	1.6	1.68	µs
		Programmable range	0.1	–	3.15	µs

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS AND OUTPUTS						
Input Low Voltage (STRn, SCK, SDI, WDOG)	V_{IL}		–	–	0.3 × V_{LR}	V
Input High Voltage(STRn, SCK, SDI, WDOG)	V_{IH}		0.7 × V_{LR}	–	–	V
Input Hysteresis (STRn, SCK, SDI, WDOG)	V_{Ihys}		150	440	–	mV
Input Pull-Down Resistor (SCK, SDI, WDOG)	R_{PD}		30	50	70	kΩ
Input Pull-Up Resistor (STRn)	R_{PU}		30	50	70	kΩ
Input Low Voltage (IG)	V_{IL}		–	–	0.6	V
Input High Voltage (IG)	V_{IH}		3.0	–	–	V
Input Hysteresis (IG)	V_{Ihys}		300	–	–	mV
Input Current (IG)	I_G	$V_{IG} \geq 1$ V	–	–	20	µA
Input Pull-Down Resistor (IG)	R_{PD}	0 V < V_{IG} < 1 V	120	240	480	kΩ
Output Low Voltage (SDO, MRSTn)	V_{OL}	I_{OL} = 1 mA	–	–	0.4	V
Output High Voltage (SDO, MRSTn)	V_{OH}	I_{OL} = –1 mA [1]	V_{LR} – 0.4	–	–	V
Output Leakage [1] (SDO)	I_O	0 V < V_O < V_{IO}, STRn = 1	–1	–	1	µA
Output Low Voltage (DIAG)	V_{OLD}	I_{OD} = 4 mA, DIAG active	–	0.2	0.4	V
Output Current Limit (DIAG)	I_{ODLIM}	0 V < V_{OD} < 18 V, DIAG active	–	10	17	mA
		18 V ≤ V_{OD} < 50 V, DIAG active	–	–	2.5	mA
Output Leakage [1] (DIAG)	I_{OD}	0 V < V_{OD} < 6 V, DIAG inactive	–1	–	1	µA
		6 V ≤ V_{OD} < 50 V, DIAG inactive	–	–	2.5	mA

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE – TIMING PARAMETERS						
Clock High Time	t_{SCKH}	A in Figure 2	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 2	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 2	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 2	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 2	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 2	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 2	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 2	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	I in Figure 2	5	–	–	ns
Data In Set-Up Time To Clock Rising	t_{SDIS}	J in Figure 2	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	K in Figure 2	10	–	–	ns
Strn Delay From POR	t_{EN}	V_{BB} > V_{BBR} to STRn low	500	–	–	µs

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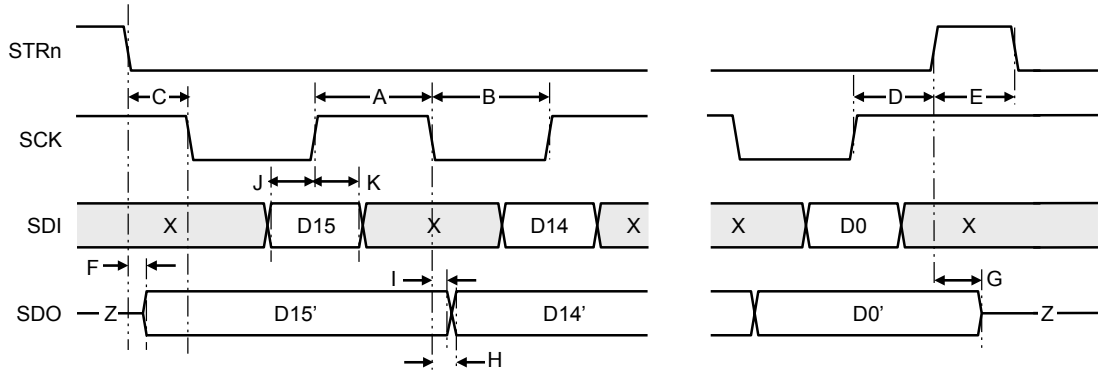

Figure 2: Serial Interface Timing
X = don't care, Z = high impedance (tri-state)

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LIN/PWM INTERFACE LOGIC I/O [10]						
Transmitter Input Low Voltage (LTX)	V_{IL}		–	–	0.3 × V_{LR}	V
Transmitter Input High Voltage (LTX)	V_{IH}		0.7 × V_{LR}	–	–	V
Transmitter Input Hysteresis (LTX)	V_{Ihys}		–	400	–	mV
Transmitter Input Pull-Up Resistor (LTX)	R_{PU}		30	50	70	kΩ
Receiver Output Low Voltage (LRX)	V_{OL}	I_{OL} = 1 mA, V_{BUS} = 0 V	–	–	0.4	V
Receiver Output High Voltage (LRX)	V_{OH}	I_{OL} = –1 mA [1], V_{BUS} = V_{BB}	V_{LR} – 0.4	–	–	V
LIN/PWM INTERFACE BUS TRANSMITTER [10]						
Bus Recessive Output Voltage	V_{BUSRO}	LTX High, Bus open load	0.8 × V_{BB}	–	–	V
Bus Dominant Output Voltage	V_{BUSDO}	LTX Low, R_{LIN} = 500 Ω, V_{BB} = 7 V	–	–	1.4	V
		LTX Low, R_{LIN} = 500 Ω, V_{BB} = 18 V	–	–	2.0	V
Bus Short Circuit Current	I_{BUSLIM}	V_{BUS} = 13.5 V	40	–	100	mA
Leakage Current – Dominant	$I_{BUS\_PAS\_dom}$	V_{BB} = 12 V, V_{BUS} = 0 V	–1	–	–	mA
Leakage Current – Recessive	$I_{BUS\_PAS\_rec}$	7 V < V_{BB} < 18 V, 7 V < V_{BUS} < 18 V V_{BUS} ≥ V_{BB}	–	–	20	µA
Leakage Current – Ground Disconnect	$I_{BUS\_NO\_GND}$	V_{BB} = 12 V, 0 V < V_{BUS} < 18 V	–1	–	1	mA
Leakage Current – Supply Disconnect	$I_{BUS\_NO\_BAT}$	V_{BB} = 0 V, 0 V < V_{BUS} < 18 V	–	–	100	µA
Bus Pull-Up Resistance	R_{SLAVE}	Normal operation	20	30	60	kΩ
		Sleep state	–	2	–	MΩ
Termination Diode Forward Voltage	$V_{SerDiode}$		0.4	0.7	1	V
LIN/PWM INTERFACE BUS RECEIVER [10]						
Receiver Center Voltage	V_{BUSCNT}		0.475 × V_{BB}	0.5 × V_{BB}	0.525 × V_{BB}	V
Receiver Dominant State	V_{BUSdom}		–	–	0.4 × V_{BB}	V
Receiver Recessive State	V_{BUSrec}		0.6 × V_{BB}	–	–	V
Receiver Hysteresis	V_{HYS}		0.05 × V_{BB}	–	0.175 × V_{BB}	V
Receiver Wake-Up Threshold Voltage	V_{BUSwk}		0.4 × V_{BB}	0.5 × V_{BB}	0.6 × V_{BB}	V
LIN/PWM INTERFACE – TIMING PARAMETERS [10]						
Receiver Propagation Delay H → L	t_{rx_pdf}	Bus dominant to LRX low	–	–	6	µs
Receiver Propagation Delay L → H	t_{rx_pdr}	Bus recessive to LRX high	–	–	6	µs
Receiver Delay Symmetry	t_{rx_sym}	t_{rx_pdf} – t_{rx_pdr}	–2	–	2	µs
Bus Dominant Time For Wake	t_{BUSWK}		22	–	150	µs
Wake Up Delay	t_{WL}	LIN Wake up to V_{REG} 90%	–	3	–	ms
PWM Input Timeout	t_{PTO}		209	220	231	ms
Transmit Dominant Time-Out	t_{TXTO}	LWK = 1, OPM = 0, LEN = 1	–	15	–	ms

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LIN/PWM INTERFACE – TIMING PARAMETERS (continued)						
Duty Cycle D1 (worst case at 20 kb/s) [7][9]	D1	7 V < V_{BB} < 18 V, t_{BIT} = 50 µs $TH_{Rec(max)}$ = 0.744 × V_{BB} $TH_{Dom(max)}$ = 0.581 × V_{BB} D1 = $t_{BUS\_rec(min)}$ / (2 × t_{BIT})	0.396	–	–	–
Duty Cycle D2 (worst case at 20 kb/s) [7][9]	D2	7 V < V_{BB} < 18 V, t_{BIT} = 50 µs $TH_{Rec(min)}$ = 0.422 × V_{BB} $TH_{Dom(min)}$ = 0.284 × V_{BB} D2 = $t_{BUS\_rec(max)}$ / (2 × t_{BIT})	–	–	0.581	–
Duty Cycle D3 (worst case at 10.4 kb/s) [7][9]	D3	7 V < V_{BB} < 18 V, t_{BIT} = 96 µs $TH_{Rec(max)}$ = 0.778 × V_{BB} $TH_{Dom(max)}$ = 0.616 × V_{BB} D3 = $t_{BUS\_rec(min)}$ / (2 × t_{BIT})	0.417	–	–	–
Duty Cycle D4 (worst case at 10.4 kb/s) [7][9]	D4	7 V < V_{BB} < 18 V, t_{BIT} = 96 µs $TH_{Rec(min)}$ = 0.389 × V_{BB} $TH_{Dom(min)}$ = 0.251 × V_{BB} D4 = $t_{BUS\_rec(max)}$ / (2 × t_{BIT})	–	–	0.590	–

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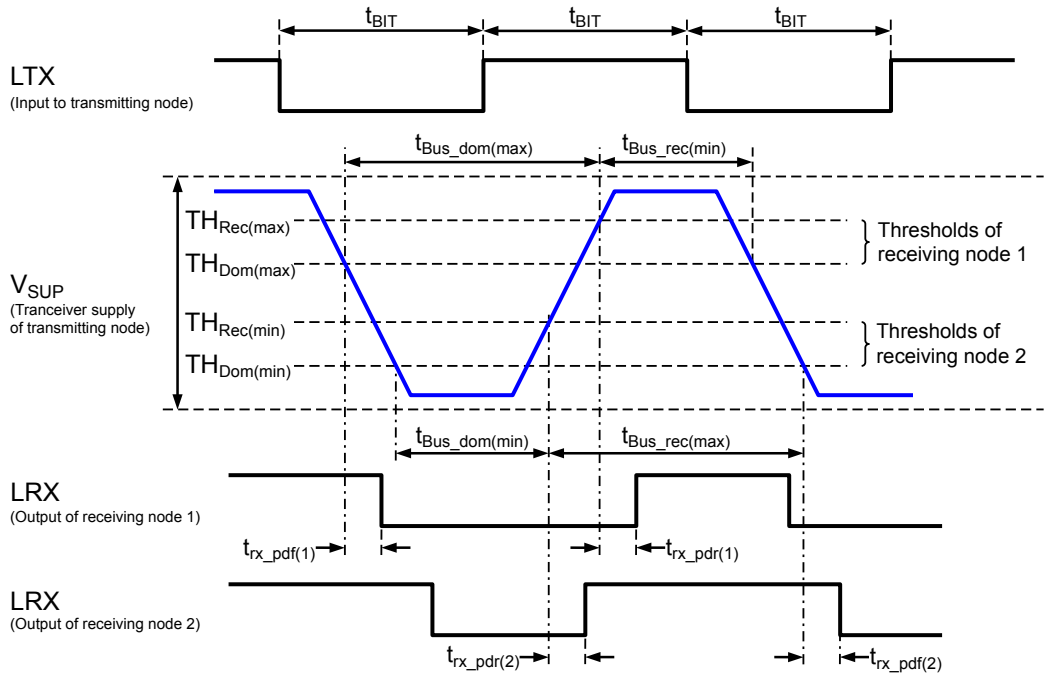

Figure 3: LIN Bus Timing

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT LIMITING						
Sense Amplifier Maximum Current Limit Threshold	V_{MIT}	Default power-up value; $V_{MIT} = V_{CSP} – V_{CSM}$	–	200	–	mV
		Programmable range; $V_{MIT} = V_{CSP} – V_{CSM}$	25	–	200	mV
Current Limit Threshold Error [6]	E_{ILIM}	VIL = 15, MIT = 0	–5%	–	+5%	%FS
Current Limit Blank Time	t_{OCB}	Default power-up value, OBT = 7	1.71	1.80	1.89	µs
		Programmable range	1	–	6.6	µs
DATA ACQUISITION SYSTEM						
Supply Voltage (VBRG): Measurement Range	V_{VM}		0	–	50.4	V
Supply Voltage (VBRG): Measurement Accuracy	E_{VM}	$V_{BRG} \leq 30$ V	–	±0.5	–	V
Average Supply Current Measurement: Sense Voltage Range	V_{VS}		0	–	200	mV
Average Supply Current Measurement: Sense Voltage Accuracy	E_{VS}		–	±1	–	%
Temperature Measurement Range	T_J		–50	–	190	°C
Temperature Measurement Accuracy	E_{TJ}		–	±5	–	°C

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MOTOR STARTUP PARAMETERS						
Hold Time	t_{HOLD}	Default power-up value	190	200	210	ms
		Programmable range	0	–	3	s
Hold Duty Cycle	D_H	Default power-up value	–	18.75	–	%
		Programmable range	3.125	–	100	%
Start Speed 1	f_{S1}	Default power-up value	3.8	4	4.2	Hz
		Programmable range	0.5	–	8	Hz
Start Speed 2	f_{S2}	Default power-up value	26.12	27.5	28.88	Hz
		Programmable range	10	–	47.5	Hz
Start Duty Cycle 1	D_{S1}	Default power-up value	–	50	–	%
		Programmable range	6.25	–	100	%
Start Duty Cycle 2	D_{S2}	Default power-up value	–	50	–	%
		Programmable range	6.25	–	100	%
Start Time Step	t_{SS}	Default power-up value	76	80	84	ms
		Programmable range	10	–	300	ms
Start Speed Step	f_{SS}	Default power-up value	0.95	1	1.05	Hz
		Programmable range	0.0125	–	15	Hz
Brake Duty Cycle	D_{WB}	Default power-up value	–	50	–	%
		Programmable range	6.25	–	100	%
Min. Windmill Frequency	f_{WM}	Default power-up value	6.46	6.8	7.14	Hz
		Programmable range	0.4	–	22.8	Hz
MOTOR RUN PARAMETERS						
BEMF Window	θ_{BW}	Default power-up value	–	7	–	°(elec.)
		Programmable range	1.4	–	60	°(elec.)
Windmill BEMF Filter Time	t_{BF}	Default power-up value	0.19	0.20	0.21	ms
		Programmable range	0	–	20	ms
Speed Control Resolution	f_{SR}	Default power-up value	0.095	0.1	0.105	Hz
		Programmable range	0.1	–	3.2	Hz
Phase Advance (in electrical degrees)	θ_{ADV}	Default power-up value	–	0	–	°(elec.)
		Programmable range	0	–	60	°(elec.)
Speed Error	E_{fE}		–5	–	+5	%
WATCHDOG –TIMING PARAMETERS						
Minimum Watchdog Time	t_{WM}	Default power-up value	0.95	1	1.05	ms
		Programmable range	1	–	63	ms
Watchdog Window Time	t_{WW}	Default power-up value	9.5	10.0	10.5	ms
		Programmable range	10	–	320	ms
Watchdog Detect To MRSTn Low	t_{WDET}		100	–	200	ns
MRSTn Low	t_{MRST}		9.5	10.0	10.5	ms

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NVM – PROGRAMMING PARAMETERS						
Programming Voltage	V_{PP}	Applied to VBB when programming	27	–	–	V
Programming Supply Setup Time	t_{PRS}	$V_{PP} > V_{PPMIN}$ to start of NVM write	10	–	–	ms
DIAGNOSTICS AND PROTECTION						
VBB Undervoltage Lockout	V_{BBON}	V_{BB} rising	4.0	4.3	4.5	V
	V_{BBOFF}	V_{BB} falling	3.8	4.0	4.2	V
VBB Undervoltage Lockout Hysteresis	V_{BBHys}		150	280	–	mV
VBB POR Voltage	V_{BBR}	V_{BB} falling	–	3.2	3.5	V
VPP Undervoltage	V_{PPUV}		21.6	–	26.6	V
VLR Undervoltage Reset 3.3 V	V_{LRON}	V_{LR} rising, VLR = 0	–	–	3.1	V
	V_{LROFF}	V_{LR} falling, VLR = 0	2.4	–	–	V
VLR Undervoltage Reset 5 V	V_{LRON}	V_{LR} rising, VLR = 1	–	–	4.8	V
	V_{LROFF}	V_{LR} falling, VLR = 1	4.2	–	–	V
VREG Undervoltage VRG = 0	V_{RON}	V_{REG} rising	6.2	6.5	6.8	V
	V_{ROFF}	V_{REG} falling	5.4	5.6	5.8	V
VREG Undervoltage VRG = 1	V_{RON}	V_{REG} rising	7.6	7.9	8.2	V
	V_{ROFF}	V_{REG} falling	6.9	7.15	7.4	V
Bootstrap Undervoltage	V_{BCUV}	V_{BOOT} falling, $V_{BOOT} = V_{Cx} – V_{Sx}$	60	–	71	$\%V_{REG}$
Bootstrap Undervoltage Hysteresis	$V_{BCUVHys}$		–	5	–	$\%V_{REG}$
VBRG Input Voltage	V_{BRG}		–1	V_{BB}	+1	V
VBRG Input Current	I_{VBRG}	V_{DST} = default, V_{BB} = 12 V 0 V < V_{BRG} < V_{BB}	–	–	500	µA
	I_{VBRGQ}	Sleep mode V_{BB} < 35 V	–	–	5	µA
VDS Threshold	V_{DST}	Default power-up level	1400	1550	1700	mV
		V_{BRG} ≥ 8 V [11]	–	–	3150	mV
		V_{BRG} < 8 V [11]	–	–	1550	mV
VDS Threshold Offset [3][4]	V_{DSTO}	V_{DST} > 1 V	–200	±100	+200	mV
		V_{DST} ≤ 1 V	–150	±50	+150	mV
VDS Qualifier Time [5]	t_{VDQ}	Default power-up value	2.99	3.15	3.31	µs
		Programmable range	0.6	–	3.15	µs
SDO Output: Clock Division Ratio	N_D	CKS = 1		280000		–
Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	ºC
Temperature Warning Hysteresis	T_{JWHhys}		–	15	–	ºC
Overtemperature Threshold	T_{JF}	Temperature increasing	170	175	180	ºC
Overtemperature Hysteresis	T_{JHyst}	Recovery = $T_{JF} – T_{JHyst}$	–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[2] See Figure 4 for gate drive output timing.
[3] As V_{SX} decreases, high-side fault occurs if $(V_{BAT} – V_{SX}) > (V_{DST} + V_{DSTO})$.
[4] As V_{SX} increases, low-side fault occurs if $V_{SX} > (V_{DST} + V_{DSTO})$.
[5] See Figure 4 and Figure 5 for V_{DS} monitor timing.
[6] Current limit threshold voltage error is the difference between the target threshold voltage and the actual threshold voltage, referred to maximum full scale (100%) current: $E_{ILIM} = 100 \times (V_{ILIMActual} – V_{ILIM}) / 200\%$. ($V_{ILIM}$ in mV).
[7] Slew rate is controlled during both transitions and will not exceed specified limits at any point between test limits.
[8] Ensured by design and characterization.
[9] LIN bus load conditions (C_{BUS}, R_{BUS}): 1 nF; 1 kΩ / 6.8 nF; 660 Ω / 10 nF; 500 Ω.
[10] Parameters are not guaranteed above or below the LIN 2.2 A operating limits V_{BB} = 7 to 18 V.
[11] Maximum value of VDS threshold that should be set in the configuration registers for correct operation when V_{BB} is within the stated range.

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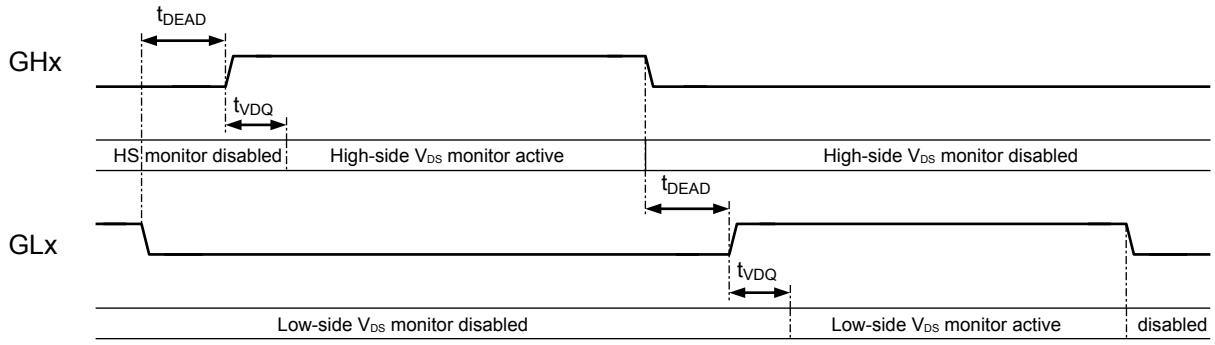

Figure 4: VDS Fault Monitor Activation – Blank Mode Timing (VDQ = 1)

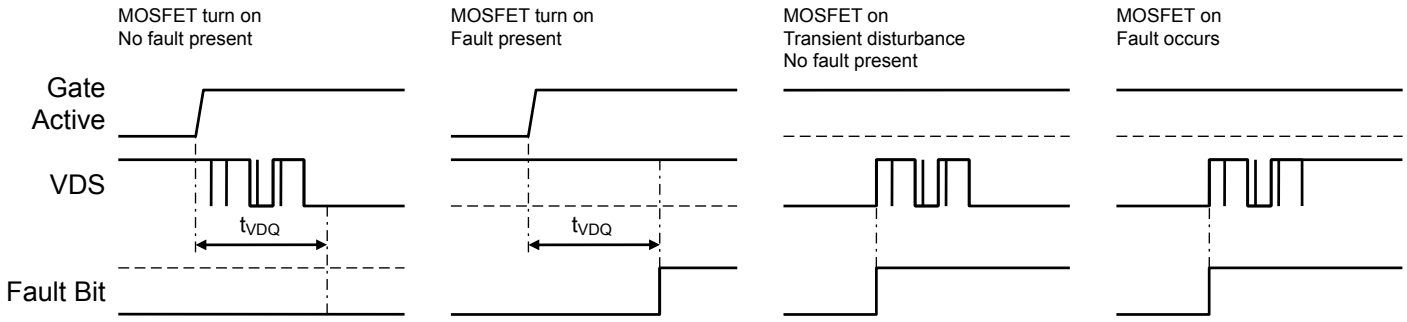

Figure 5a: VDS Fault Detection - Blank Mode Timing (VDQ = 1)

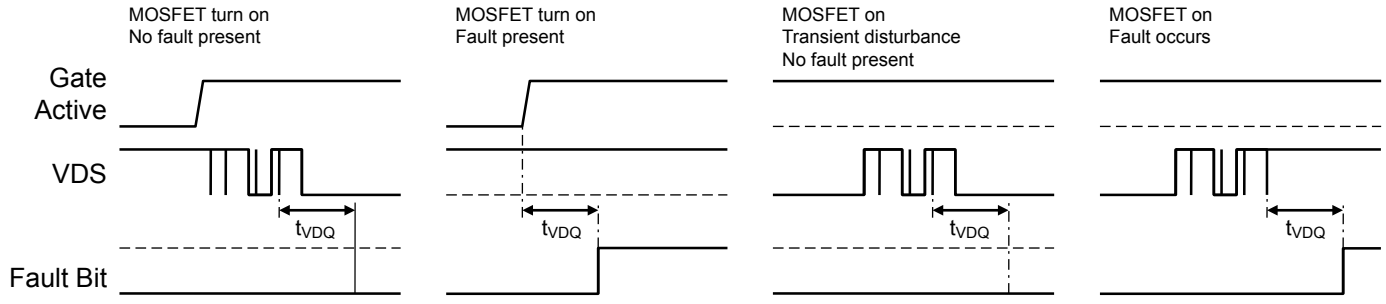

Figure 5b: VDS Fault Detection - Debounce Mode Timing (VDQ = 0)

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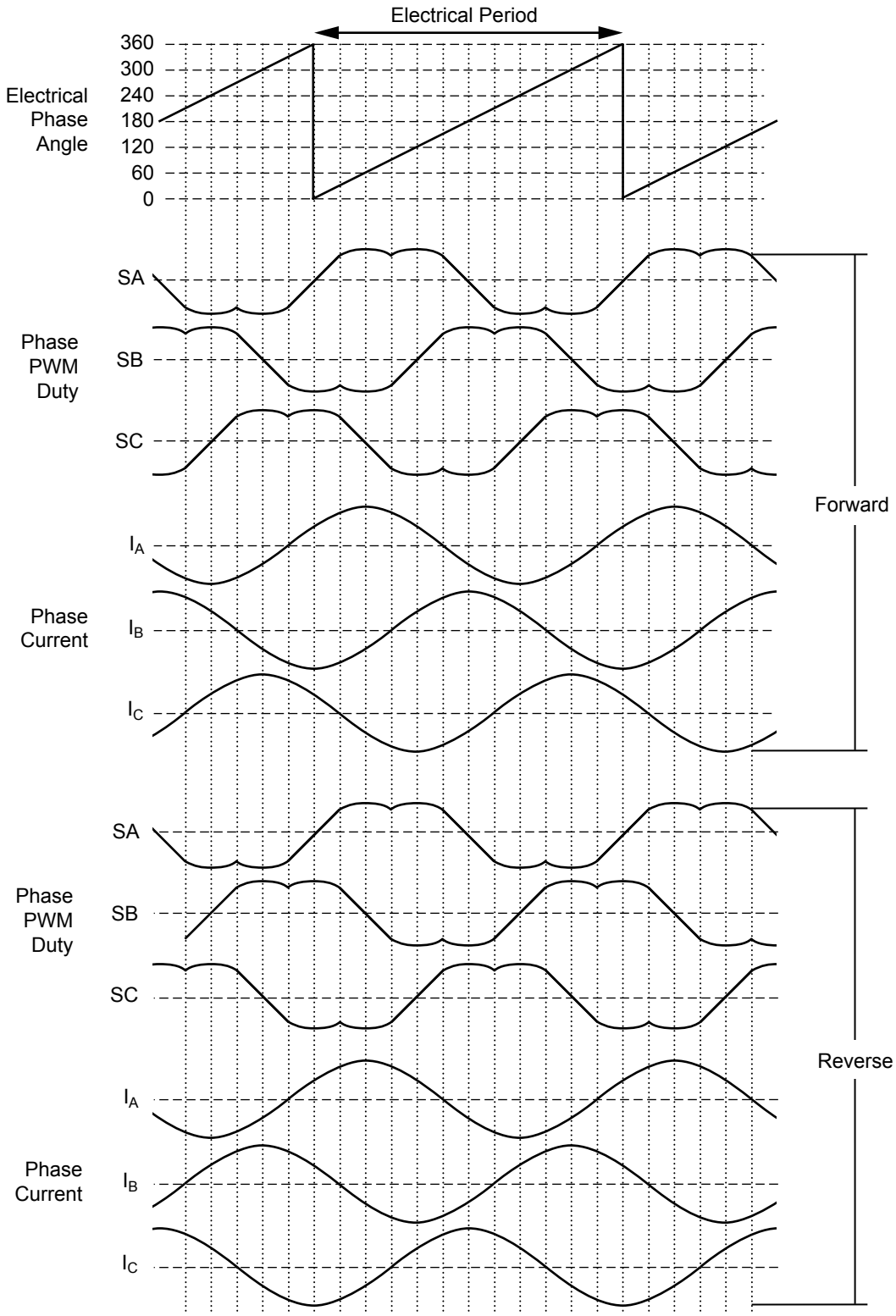

Figure 6: Phase Current Commutation Sequence for Sinusoidal Drive with 3-Phase Modulation

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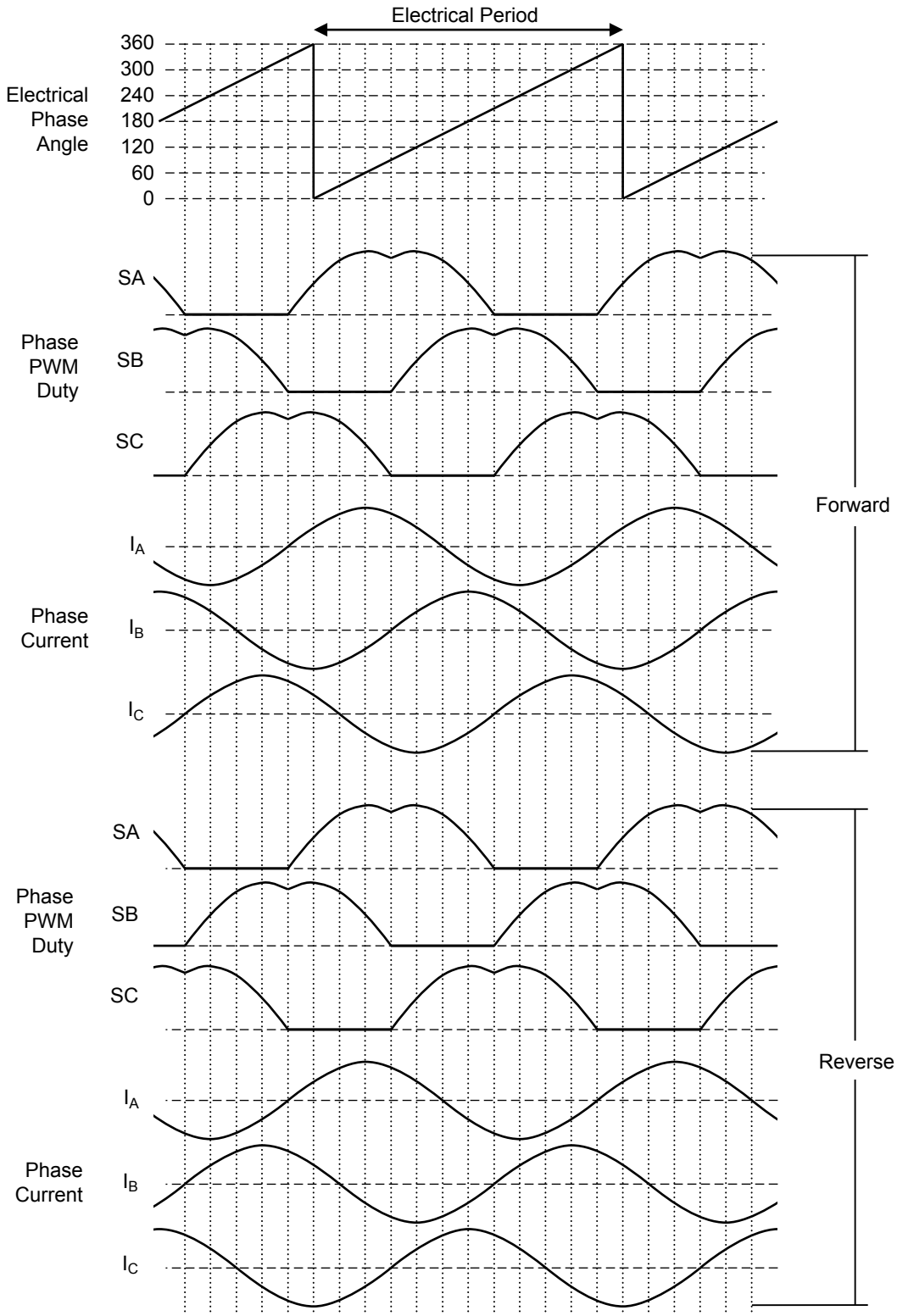

Figure 7: Phase Current Commutation Sequence for Sinusoidal Drive with 2-Phase Modulation

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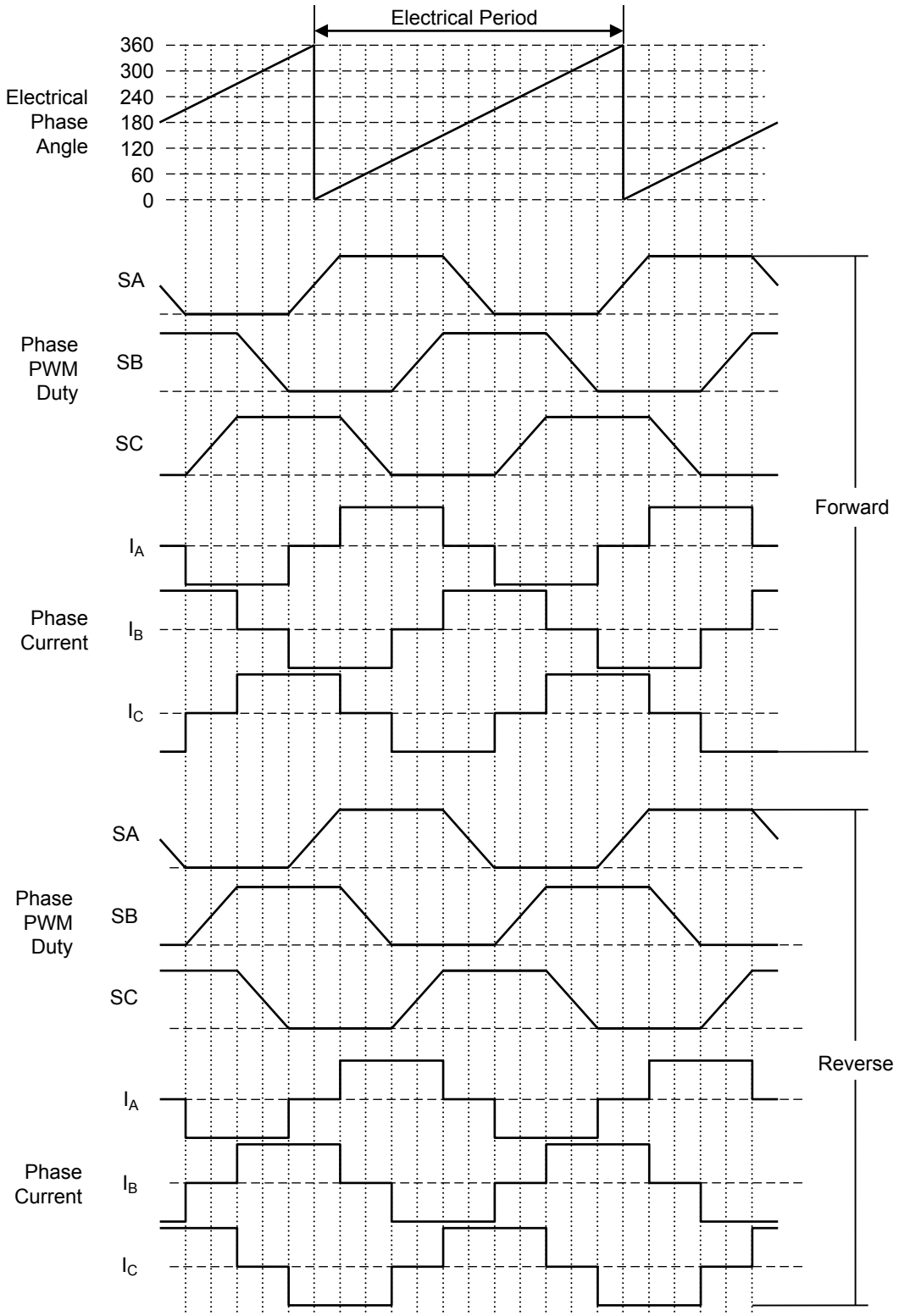

Figure 8: Phase Current Commutation Sequence for Trapezoidal Drive with 2-Phase Modulation

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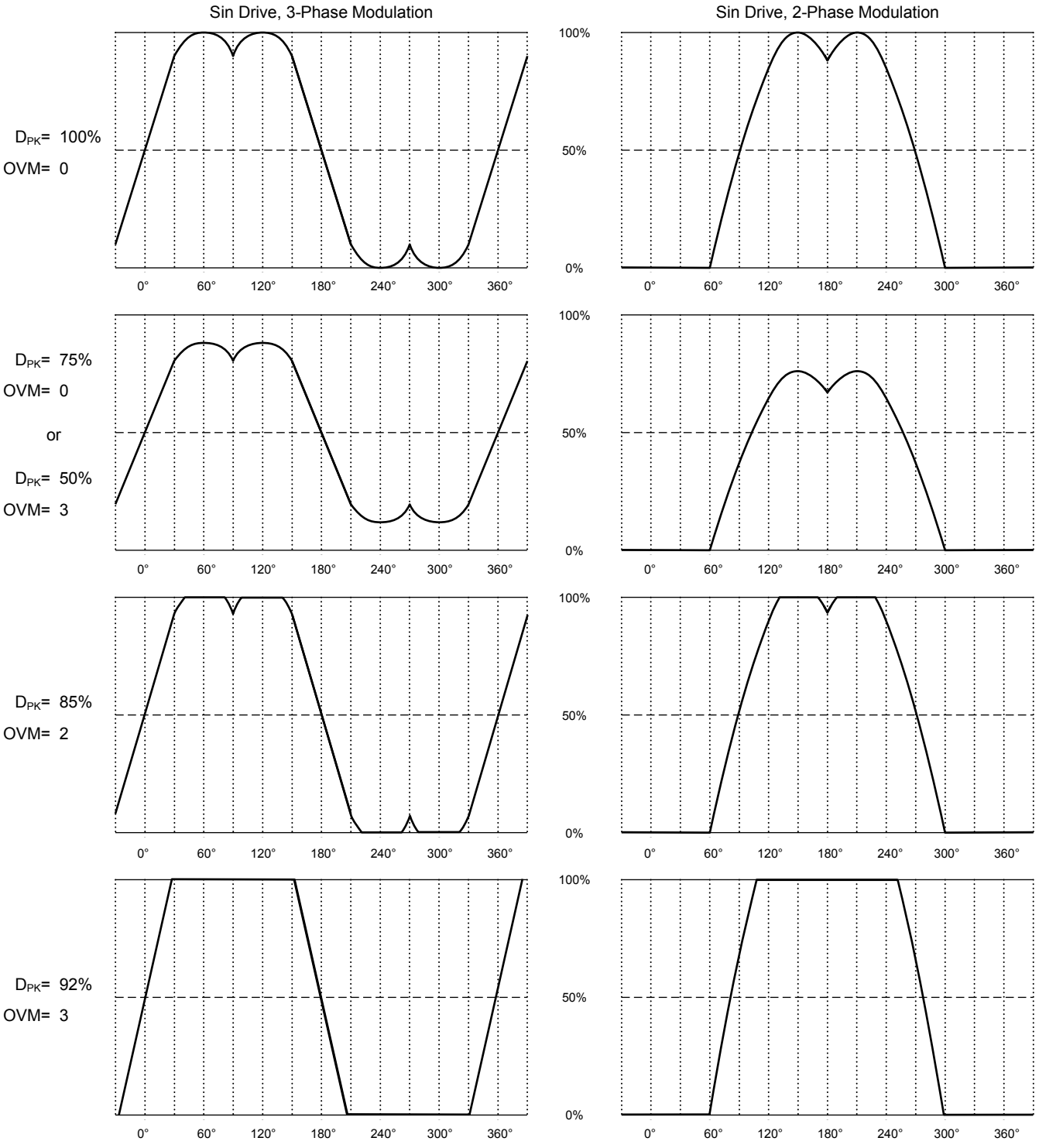

Figure 9: Modulation and Overmodulation Examples

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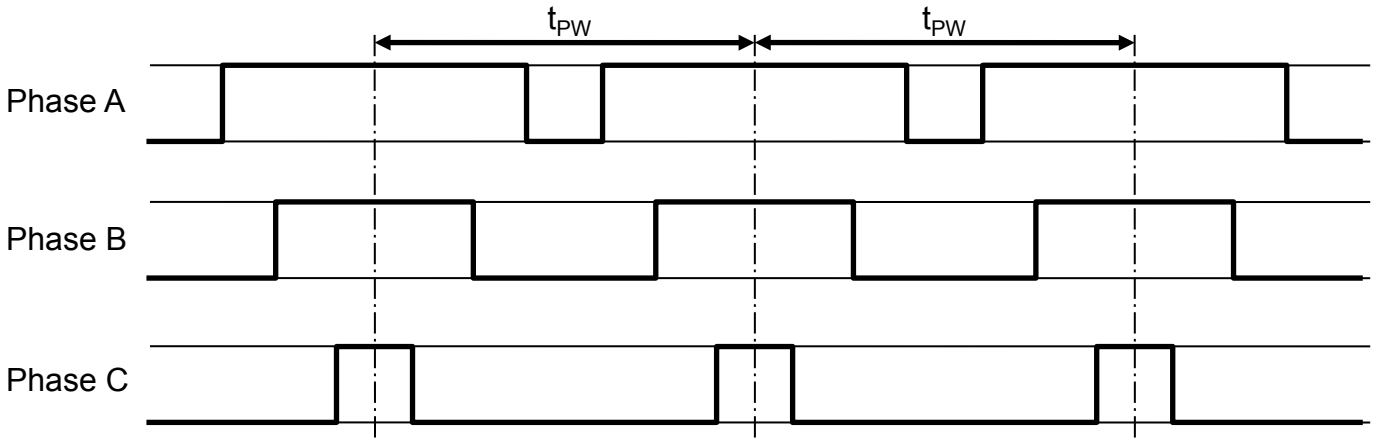

Figure 10a: Center-Aligned Bridge PWM Mode PMD = 0

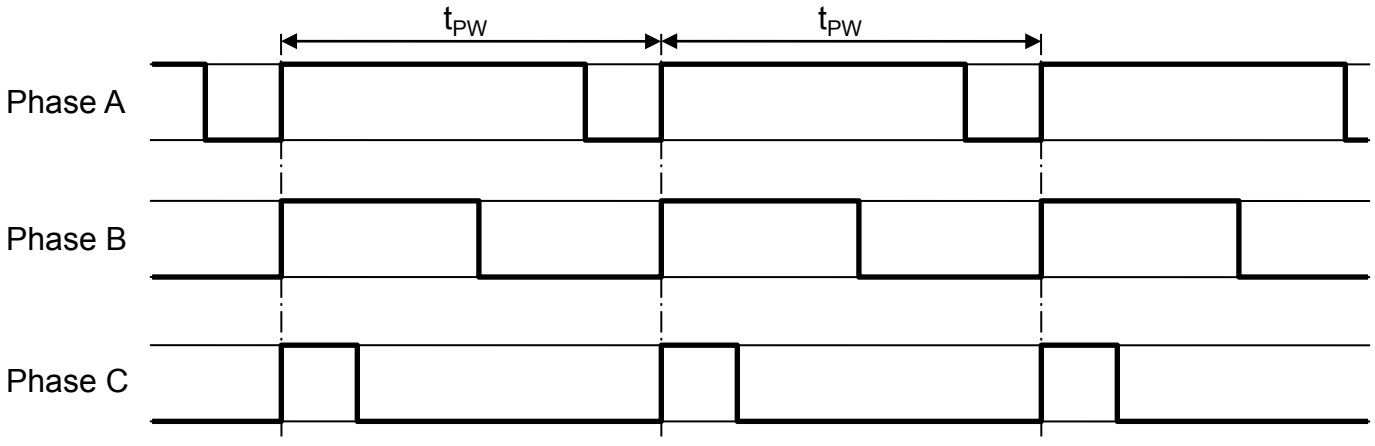

Figure 10b: Edge Aligned Bridge PWM Mode PMD = 1

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FUNCTIONAL DESCRIPTION

The A4964 is a three-phase, sensorless, brushless DC (BLDC) motor controller for use with external N-channel power MOSFETs and is specifically designed for automotive applications. The motor is driven using 3-phase sinusoidal current drive, where phase commutation is determined by a proprietary, motor back-emf (bemf) sensing technique. The motor bemf is sensed to determine the rotor position without the need for independent position sensors. An integrated sensorless startup scheme includes forwards and reverse pre-rotation (windmill) detection and syncronization and allows a wide range of motor and load combinations.

Motor current is provided by six external power N-channel MOSFETs arranged as a three-phase bridge. The A4964 provides six high current gate drives, three high-side and three low-side, capable of driving a wide range of MOSFETs. The maximum MOSFET drive voltage is internally limited under all supply conditions to protect the MOSFET from excessive gate-source voltage without the need for an external clamp circuit. The A4964 provides all the necessary circuits to ensure that the gate-source voltage of both high-side and low-side external MOSFETs are sufficiently high to achieve full correct conduction at low supply levels. A low-power sleep state allows the A4964, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

Three motor control modes are available: closed-loop speed control, open-loop speed (voltage) control, and current (torque) control. The motor control mode and the control and configuration parameters can be altered through an SPI-compatible serial interface and the user-defined power-up parameters can be stored in non-volatile memory. The A4964 can also operate in a stand-alone mode, without the need for an external microcontroller, where the duty cycle of a PWM signal applied to the LIN terminal is used to control the output of the motor.

Startup (inrush) current, and peak motor current is limited by an integrated fixed frequency PWM current limiter. The maximum current limit is set by a single external sense resistor and the active current limit can be modified through the serial interface.

An integrated data acquisition system provides measurement of the motor voltage, the chip temperature, the motor speed, and an estimate of the average supply current.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults, and can be configured to protect the power FETs under most short-circuit conditions. Detailed diagnostics are available through the serial interface.

Specific functions are described more fully in following sections.

Input and Output Terminal Functions

VBB. Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

VBRG. Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drain of the high-side MOSFETs in the bridge.

CP1, CP2. Pump capacitor connections for charge pump. Connect a 470 nF ceramic capacitor between CP1 and CP2.

VREG. Regulated voltage, nominally 11 V, used to supply the low-side gate drivers and to charge the bootstrap capacitors. A sufficiently large storage capacitor must be connected to this terminal to provide the transient charging current.

VLR. VLR regulator output. External logic can be powered by this node. The voltage can be selected as 3.3 or 5 V. A ceramic capacitor of at least 1 µF with an ESR of no more than 250 mΩ should be fitted between the VLR output and GND to ensure stability.

GND. Analog reference, digital and power ground. Connect to supply ground—see layout recommendations.

CA, CB, CC. High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

GHA, GHB, GHC. High-side gate-drive outputs for external N-channel MOSFETs.

SA, SB, SC. Motor phase connections. These terminals sense the voltages switched across the load. They are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers.

GLA, GLB, GLC. Low-side gate-drive outputs for external N-channel MOSFETs.

CSP, CSM. Differential current sense amplifier inputs. Connect directly to each end of the sense resistor using separate PCB traces.

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LIN. LIN bus connection compliant with LIN 2.2 A. This input can also be used as a PWM that can be passed to the LRX output or used directly as the demand input when operating in stand-alone mode.

LTX. LIN or FAULT transmit logic level input.

LRX. LIN or PWM receive logic level output.

IG. Ignition switch input, with resistor pull-down, to disable or wake-up the A4964 and enable the logic regulator for the microcontroller. When not used, IG should be tied to ground to minimize the effect on the supply current in the sleep state.

DIAG. Programmable diagnostic output. Can be shorted to ground or VBB without damage.

WDOG. Microcontroller watchdog logic input with resistor pull-down. Window watchdog with programmable minimum and maximum clock period.

MRSTn. Microcontroller reset control output. Holds the microcontroller in reset until supplies are available. Resets the microcontroller in case of watchdog failure.

SDI. Serial data input with resistor pull-down. 16-bit serial word input msb first.

SDO. Serial data output. High impedance when STRn is high. Outputs bit 15 of the Diagnostic register, the fault flag, as soon as STRn goes low.

SCK. Serial clock input with resistor pull-down. Data is latched in from SDI on the rising edge of CLK. There must be 16 rising edges per write and SCK must be held high when STRn changes.

STRn. Serial data strobe and serial access enable input with resistor pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

Supplies and Regulators

MAIN POWER SUPPLY

A single power supply voltage is required. The main power supply, V_{BB}, should be connected to VBB through a reverse voltage protection circuit. A 100 nF ceramic decoupling capacitor must be connected close to the supply and ground terminals of the A4964.

An internal regulator provides the supply to the internal logic. All logic is guaranteed to operate correctly to below the VBB POR level, ensuring that the A4964 will continue to operate safely until all logic is reset when a power-on-reset state is present.

The A4964 will operate within specified parameters with V_{BB} from 5.5 to 50 V. Below 5.5 V, the gate drive outputs may be inactive, but the A4964 will continue to respond through the serial interface with a supply down to 3.5 V. It will remain in a safe state between 0 and 50 V under all supply switching conditions. This provides a very rugged solution for use in the harsh automotive environment.

At power-up, the logic inputs and outputs will remain disabled until VLR rises above the rising undervoltage threshold, V_{LRON}. If the WD mask bit is saved as 0 in non-volatile EEPROM (NWM), the MRSTn output will remain low for 10 ms. If the WD mask bit is saved as 1 in NWM, the MRSTn output will remain low for 10 ms or until the first valid serial transfer (whichever occurs first). After the MRSTn output goes high, the gate drive outputs will be re-enabled as described in the Fault Action section.

VLR REGULATOR

An integrated, programmable, linear regulator is provided to supply the logic I/O and external logic-level circuits, such as a microcontroller or interface circuit. The output of the regulator on the VLR terminal is derived from V_{BB} and can be selected as 3.3 or 5 V using the VLR bit. The logic I/O threshold levels are also determined by the VLR bit, allowing the A4964 to match the logic I/O levels of external logic.

The regulator includes current limit, undervoltage, and short protection. The current limiting circuit will reduce the output voltage to ensure that the output current does not exceed the current limit, I_{LROC}. If the output voltage drops below the falling undervoltage threshold, V_{LROFF}, the MRSTn output will go low and can be used to reset an external microcontroller.

If the output voltage falls below the regulator shutdown threshold, V_{LROSD}, for a period exceeding the shutdown lockout period, t_{LRLO}, the regulator is turned off and all logic inputs and outputs are disabled. In this state a small pilot current, I_{LROP}, is driven through the regulator output to detect load resistance. If the resultant voltage rises above the regulator enable threshold, V_{LROE}, the regulator immediately attempts to restart.

At power-up, or when the regulator restarts, full output current is delivered for a period equal to the shutdown lockout period. During this time, the output voltage is not monitored for short-circuit conditions in order to ensure reliable regulator startup.

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If ESF = 1 and the A4964 internal junction temperature, T_J, rises above the overtemperature threshold, T_{JF}, the regulator is immediately shut down and MRSTn will go low. All A4964 functions other than the regulator remain active. When T_J drops by more than the overtemperature hysteresis below the overtemperature threshold ($T_J < T_{JF} – T_{JHyst}$), the regulator will remain shut down and MRSTn will remain low for 10 ms. After this timeout, MRSTn goes high and the regulator is re-enabled and attempts to restart. If an undervoltage shutdown and an overtemperature warning occur simultaneously, both must be cleared to allow the regulator to restart.

Internal A4964 logic circuitry is not powered from the VLR regulator and remains fully operational regardless of whether the VLR regulator is running normally or shut down.

A ceramic capacitor of at least 1 µF with an ESR of no more than 250 mΩ should be fitted between the VLR terminal and GND to guarantee stability and oscillation and voltage excursions beyond the specified output voltage range. In some applications, the use of redundant output capacitors may be advisable to avoid such a condition in the event of a single-point capacitor high-impedance failure.

PUMP REGULATOR

The gate drivers are powered by a programmable voltage internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. At low input supply voltage, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor, typically 470 nF, connected between the CP1 and CP2 terminals.

The regulated voltage, V_{REG}, can be programmed to 8 or 11 V and is available on the VREG terminal. The voltage level is selected by the value of the VRG bit. When VRG = 1, the voltage is set to 11 V; when VRG = 0, the voltage is set to 8 V. A sufficiently large storage capacitor (see applications section) must be connected to this terminal to provide the transient charging current to the low side drivers and the bootstrap capacitors.

Operating Modes

The A4964 has two operating modes: SPI mode and stand-alone mode. In SPI mode, it can be fully controlled by a small low-cost external microcontroller through the serial interface. In stand-alone mode, the LIN terminal becomes a PWM input that is used to set the input demand. All configuration settings and basic control functions, except for the demand input, can be programmed through the serial interface in both modes. The demand input can only be set through the serial interface in the SPI mode.

SPI MODE

When operating in SPI mode (OPM = 0) the demand input is determined by a 10-bit value, input from the external microcontroller. The LIN terminal is a simple LIN physical interface where the data on the LIN bus is interpreted, and the responses are provided by the external microcontroller. The only other function that the LIN input provides is to wake the A4964 when it is in the sleep state.

STAND-ALONE MODE

When operating in stand-alone mode (OPM = 1), the demand input is only determined by the duty cycle of a PWM signal applied to the LIN terminal. The 10-bit demand input through the serial interface is not available in this mode. However, all configuration settings and basic control functions, except for the demand input, can still be programmed through the serial interface. In this mode, the LIN input will also wake the A4964 when it is in the sleep state.

LOW-POWER SLEEP STATE

The A4964 provides a low-power sleep state where the consumption from the supply is reduced to a minimum by disabling all normal operation including the charge pump regulator, the internal logic regulator, the external regulator, and the internal clock. In the sleep state, the LIN terminal must be at the same voltage as the supply terminal, VBB, and the IG terminal should be tied to ground to achieve the minimum supply current.

There are two sleep states: the normal commanded sleep state and the permanent sleep state. The permanent sleep state is only entered following a watchdog cycle count failure. The state of the A4964 is the same in both cases, but it will only exit the permanent sleep state after a power off-on cycle as described in the Microcontroller Watchdog section.

When operating in SPI mode (OPM = 0), the A4964 can only be commanded to go into the normal sleep state using the serial interface to change the GTS bit from 0 to 1 when the LIN input is high (recessive). If the LIN input is low (dominant), any sleep command through the serial interface will be ignored, and the GTS bit must be changed to 0 followed by 1 to issue another go-to-sleep command when the LIN input is high (recessive).When operating in stand-alone mode (OPM = 1), the A4964 will go into the normal sleep state using the serial interface to change the GTS bit from 0 to 1, irrespective of the level on the LIN terminal. In stand-alone mode, it will also go to sleep when the IG input transitions from high to low.

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The sequence to wake the A4964 is determined by the LWK bit and is independent from the operating mode. When the LIN wake mode is selected (LWK = 1), the A4964 will wake up according to the LIN protocol. When the PWM wake mode is selected (LWK = 0), the A4964 will wake up on any valid transition of the signal at the LIN terminal. These sequences are fully described and defined in the LIN interface section below.

In either wake mode, the A4964 will also wake up on a low-to-high transition of the signal on the IG terminal.

In the sleep state, the MRSTn output is held low, latched faults are cleared, and the Diagnostic and Status registers are reset to zero.

When coming out of the sleep state, all registers are reset to the user-defined values held in the non-volatile memory, and the A4964 follows the same procedure as for a full power-on reset. MRSTn is held low until 10 ms after the external regulator output exceeds its undervoltage threshold. In addition, the charge pump output monitor ensures that the gate drive outputs are off until the charge pump reaches its correct operating condition. The charge pump will stabilize in approximately 2 ms under nominal conditions.

Table 1: Operating and Wake Mode Features

	Operating Mode	
	SPI	**Standalone**
OPM	0	1
Demand SPI	10-bit (DI[9:0])	No
Demand LIN	No	LIN(PWM) Duty
Sleep (SPI) Command	SPI (GTS 0→1) [Only when LIN is high]	SPI (GTS 0→1)
Sleep (IG) Command	No	IG high to low

	Wake Mode	
	PWM	**LIN**
LWK	0	1
Wake (IG)	IG L→H	IG L→H
Wake (LIN)	Any transition on LIN terminal present for > t_{BUSWK}	First L→H transition on LIN terminal after LIN terminal low for > t_{BUSWK}

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Microcontroller Reset and Watchdog

MICROCONTROLLER RESET

The microcontroller reset output, MRSTn, can be used to reset and re-initialize an external microcontroller if an undervoltage, watchdog fault, or power-on-reset (POR) occurs. The MRSTn output will be active low when the external regulator undervoltage or POR fault state is present and will remain low for 10 ms after all faults are removed. It will also go low for 10 ms when a watchdog fault is detected.

MICROCONTROLLER WATCHDOG

The A4964 includes a programmable window watchdog that can be used to determine if the external microcontroller is operating in an adverse state. After any transition (high-to-low or low-to-high) on the WDOG input, the WDOG input must be held at a DC level for the duration of the minimum watchdog time, t_{WM}, set by the WM variable. Following the end of the minimum watchdog time, a transition on the WDOG input must then be detected before the end of the watchdog window time, t_{WW}, set by the WW variable in order to reset the watchdog timer. This means that the time between each transition on the WDOG input must be longer than t_{WM} and shorter than $t_{WM} + t_{WW}$.

If a subsequent transition is detected before t_{WM} or if a transition is not detected within $t_{WM} + t_{WW}$, then the WD bit will be set in the Status register and the MRSTn output will go active low for 10 ms in order to reset the microcontroller.

In all fault cases (POR, undervoltage or watchdog) when MRSTn goes high after the 10 ms low period, the watchdog timer will be reset and remain reset for 100 ms. During this time, the WDOG input is ignored. The first transition must then be detected within $t_{WM} + t_{WW}$ or the micro-reset cycle will repeat. There is no minimum watchdog time, t_{WM}, following a micro-reset. The micro-reset and watchdog timing is shown in Figure 11. The WD bit will remain set in the Status register until cleared.

When a watchdog failure is detected, the motor drive is disabled and the motor will coast. The motor drive remains disabled until a valid watchdog transition is detected. Once a valid watchdog has been detected, the A4964 will attempt to restart the motor if the RUN and RSC bits are set to 1, and the demand input is at a level where starting the motor is permitted.

If the watchdog function is not required, it is possible to disable the function by setting the WD bit in the mask register to 1.

This will completely disable the watchdog monitor and any possible actions that it may take.

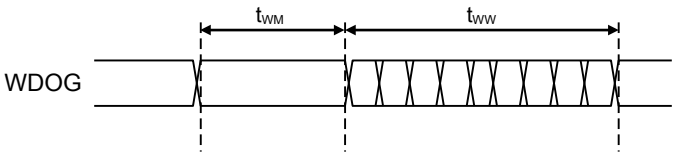

Figure 11a: Watchdog Timing Requirements

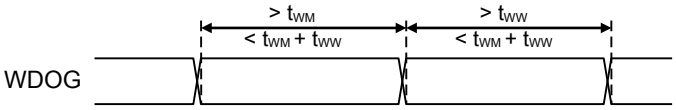

Figure 11b: Suitable Watchdog Signal

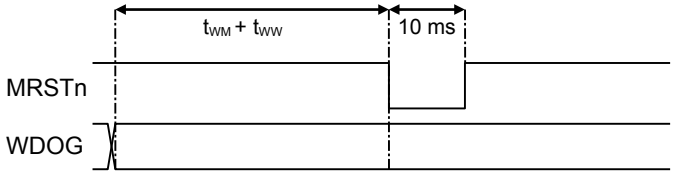

Figure 11c: Reset After Missing Watchdog Edge

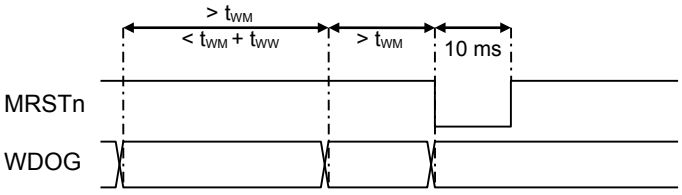

Figure 11d: Reset After Early Watchdog Edge

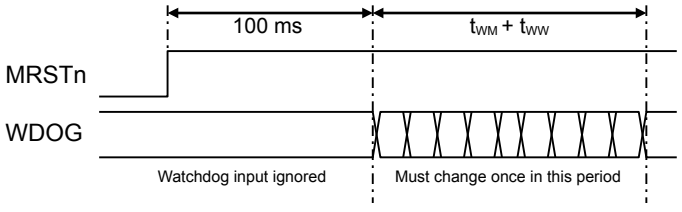

Figure 11e: Timing After Reset

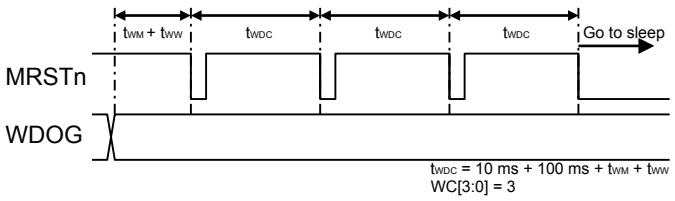

Figure 11f: Sleep After Fail Cycle Count

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If the microcontroller has completely stopped working it is possible to put the A4964 into the permanent sleep state, after a number of reset cycles using the watchdog fail cycle count variable, WC[3:0]. The value in WC[3:0] sets the number of watchdog fail-reset cycles that can occur before the A4964 goes into the permanent sleep state. A value of 1 will allow one fail-reset cycle and will go to sleep on the next watchdog failure if no valid transitions are detected on the WDOG input. A value of 8 will allow 8 fail-reset cycle and will go to sleep on the 9th watchdog failure if no transitions are detected on the WDOG input. The counter is reset if any valid transition is detected on the WDOG input. A valid transition is one that occurs after the initial 100 ms following a microcontroller reset and before the end of the initial watchdog window time, $t_{WM} + t_{WW}$. Figure 11f shows the fail-cycle operation when WC[3:0] is set to 3. A value of zero in WC[3:0] will disable this feature and permit unlimited fail-reset cycles. Once the A4964 goes into the permanent sleep state due to exceeding the fail-reset cycle limit, it will remain in this state until a power cycle occurs.

LIN Physical Interface

The A4964 includes a physical interface to drive and monitor a single wire LIN bus as a slave node that complies with the LIN 2.2 standard. The LIN terminal can withstand voltages from –14 V to +50 V with respect to the ground pin without adversely affecting LIN bus communications between other devices. LIN protocol handling is not included.

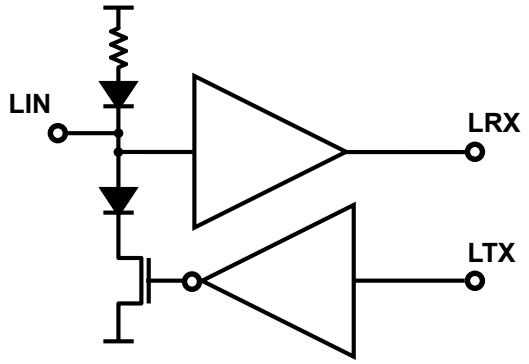

Figure 12: LIN Physical Interface

The LIN terminal meets all the voltage, timing, and slew limitation requirements of LIN 2.2 when actively transmitting and when receiving. When operating in SPI mode, a timer is included to ensure that the LIN output does not remain dominant when a fault occurs. If the LIN terminal is driven in the dominant state for longer than the transmit dominant timeout period, t_{TXTO}, then the output is disabled and allowed to return to the recessive state in order to avoid locking the LIN Bus for other messages. The dominant timeout function is disabled in standalone operating mode (OPM = 1), in PWM wake mode (LWK = 0), or when the LIN interface is in the standby state (LEN = 0).

The data to be transmitted is input to the LTX terminal and converted to LIN bus signals. A logic high on the LTX input produces a recessive bus (high) state while a logic low produces a dominant bus (low) state. The LTX input has an internal pull-up resistor to ensure a recessive state if the pin is not connected or becomes disconnected.

The logic state of the LIN Bus is determined by the receiver and output as a logic level on the LRX terminal. LRX will be low when the LIN Bus is in the dominant (low) state and high when the LIN Bus is in the recessive (high) state. In the sleep state, LRX is not active and will be low.

In SPI mode, the LIN interface can also be used as a PWM interface to the external microcontroller. The level of the PWM signal applied to the LIN terminal will be output as a logic level on the LRX terminal. When used as a PWM input in SPI mode (OPM = 0), the LTX input can be used to pull the PWM signal low in order to indicate a fault to the external ECU. In standalone mode, the DIAG output can be connected directly to the LIN terminal to indicate a fault to the external ECU. See Diagnostics section for additional detail.

When the A4964 is in the sleep state, the LIN terminal changes to a passive input and the resistance of the pull-up resistor on the LIN terminal increases to approximately 2 MΩ. This ensures that the LIN terminal is unable to affect the LIN bus signal. The LIN terminal continues to be monitored in the normal sleep state in order to detect a wake request.

Two wake sequence modes are possible, selected by the LWK bit. The selected wake sequence mode is independent of the operating mode.

When LWK = 1, the A4964 will wake up according to the LIN protocol. In this mode, the wake request is valid on the first low-to-high transition on the LIN terminal after the LIN terminal is in a dominant (low) state for longer than the wake time, t_{BUSWK}, as shown in Figure 13a. If the LIN terminal changes to recessive (high) within t_{BUSWK} then the A4964 returns to the sleep state.

When LWK = 0, the A4964 will wake up on any valid transition of the signal at the LIN terminal. In this mode, the wake signal is valid when the signal on the LIN terminal changes state, high-to-low or low-to high, and remains in the changed state for longer than the wake time, t_{BUSWK}, as shown in Figure 13b. This mode

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is usually used when the LIN terminal is used as a PWM input, either in SPI mode or in standalone mode. If the LIN terminal does not remain in the changed state for longer than the wake time, t_{BUSWK}, then the A4964 returns to the sleep state.

When a valid wake request is detected on the LIN terminal or the IG terminal transitions from low to high, the A4964 will exit normal the sleep state, turn on all regulators and control circuits, and commence operation.

At this time, if the LEN bit is 0, the LIN interface will remain in the standby state where the LIN terminal is a passive input. The LRX output will indicate the state of the LIN terminal but the signal on the LTX terminal is ignored. The LIN interface becomes fully active when LEN is set to 1. If the default value of LEN is 1, then the standby state is bypassed and the LIN interface is fully active as soon as the internal regulators are fully active.

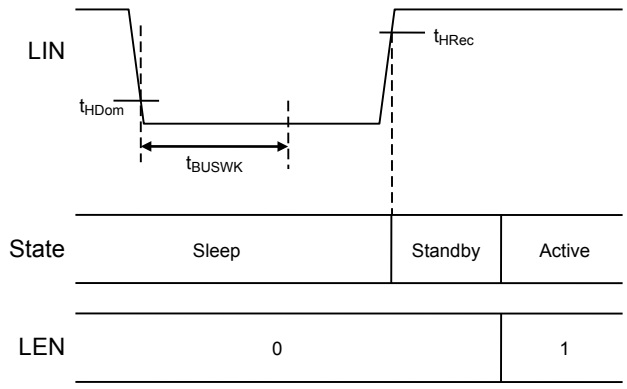

Figure 13a: LIN Wake Sequence and Timing

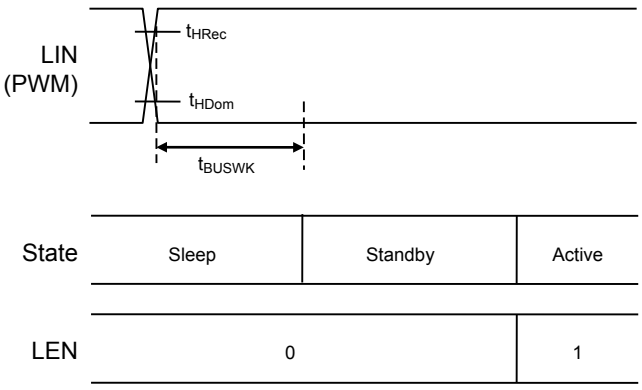

Figure 13b: PWM Wake Sequence and Timing

Motor Drive

The motor drive consists of three half-bridge gate drive outputs, each driving one leg of an external three-phase MOSFET power bridge. The state of the gate drive outputs is determined by a three-phase PWM generator that determines the necessary PWM duty cycle required at each of the three-phase connections to the motor.

GATE DRIVE

The A4964 is designed to drive external, low on-resistance, power n-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drives and the recharge current for the bootstrap capacitors is provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitors connected between the Cx and Sx terminal, one for each phase. The MOSFET gate charge and discharge rate can be controlled using an external resistor in series with the connection to the gate of the MOSFET or by selecting the gate drive current and timing using a group of parameters set via the serial interface.

GATE DRIVE VOLTAGE REGULATION

The gate drivers are powered by a programmable voltage internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. At low supply voltage, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor, typically 470 nF, connected between the CP1 and CP2 terminals.

The regulated voltage, V_{REG}, can be programmed to 8 or 11 V and is available on the VREG terminal. The voltage level is selected by the value of the VRG bit. When VRG = 1, the voltage is set to 11 V; when VRG = 0, the voltage is set to 8 V. A sufficiently large storage capacitor (see applications section) must be connected to this terminal to provide the transient charging current to the low side drivers and the bootstrap capacitors.

LOW-SIDE GATE DRIVE

The low-side, gate-drive outputs on GLA, GLB, and GLC are referenced to the GND terminal. These outputs are designed to drive external N-channel power MOSFETs. GLx = ON (or "high") means that the upper half of the driver is turned on and it will source current to the gate of the low-side external MOSFET, turning it on. GLx = OFF (or "low") means that the lower half of

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the driver is turned on and it will sink current from the gate of the external MOSFET, turning it off.

MOSFET gate charge and discharge rates may be controlled by external resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) or by programming the gate drive via the serial interface as detailed in the Gate Drive Control section below.

HIGH-SIDE GATE DRIVE

The high-side gate-drive outputs on GHA, GHB, and GHC are referenced to the SA, SB, and SC respectively. These outputs are designed to drive external N-channel power MOSFETs. GHx = ON (or "high") means that the upper half of the driver is turned on and its drain will source current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. GHx = OFF (or "low") means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET's gate circuit to the respective Sx terminal, turning it off.

The SA, SB, and SC terminals are connected directly to the motor phase connections. These terminals sense the voltages switched across the load. They are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drives. These inputs are referred to elsewhere as the Sx inputs where x is replaced by A, B, or C depending on the phase. The discharge current from the high-side MOSFET gate capacitance flows through these connections which should have low-impedance traces to the MOSFET bridge. These terminals also provide the phase voltage feedback used to determine the rotor position.

The CA, CB, and CC terminals are the positive supply for the floating high-side gate drives. These inputs are referred to elsewhere as the Cx inputs where x is replaced by A, B, or C, depending on the phase. The bootstrap capacitors are connected between corresponding Cx and Sx terminals. The bootstrap capacitors are charged to approximately V_{REG} when the associated output Sx terminal is low. When the Sx output swings high, the charge on the bootstrap capacitor causes the voltage at the corresponding Cx terminal to rise with the output to provide the boosted gate voltage needed for the high-side FETs.

BOOTSTRAP SUPPLY

When a high-side driver is active, the reference voltage, Sx, will rise to close to the bridge supply voltage. The supply to the driver will then have to be above the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by bootstrap capacitors, one for each high-side driver.

These three bootstrap capacitors are connected between the bootstrap supply terminals, CA, CB, and CC, and the corresponding high-side reference terminal, SA, SB, and SC.

The bootstrap capacitors are independently charged to approximately V_{REG} when the associated reference terminal, Sx, is low. When the output swings high, the voltage on the bootstrap supply terminal, Cx, rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

BOOTSTRAP CHARGE MANAGEMENT

The A4964 monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. Before a high-side drive can be turned on, the bootstrap capacitor voltage must be higher than the turn-on voltage limit. If this is not the case, then the A4964 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances, this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active, and if the voltage drops below the turn-off voltage, a charge cycle is also initiated.

The bootstrap charge management circuit may actively charge the bootstrap capacitor regularly when the PWM duty cycle is very high, particularly when the PWM off-time is too short to permit the bootstrap capacitor to become sufficiently charged.

If, for any reason, the bootstrap capacitor cannot be sufficiently charged, a bootstrap fault will occur—see Diagnostics section for further details.

GATE DRIVE PASSIVE PULL-DOWN

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as 950 kΩ between the gate drive and the source connections for each MOSFET. It is only active when the A4964 is not driving the output to ensure that any charge accumulated on the MOSFET gate has a discharge path even when the power is not connected.

GATE DRIVE CONTROL

In some applications, it may be necessary to limit the rate of change of the voltage at the motor phase connections to help comply with EMC emission requirements. This is usually achieved by controlling the MOSFET gate charge and discharge rates.

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The conventional approach is to add an external resistor between the gate drive output and the gate connection to each MOSFET, and possibly an additional small value capacitor between the gate and source of the external MOSFET.

In addition to operating in this basic switch mode drive, the A4964 gate drive output can be programmed to provide control of the slew rate of the drain-source voltage of the external power MOSFET. This is achieved by controlling the gate sink or source current during the time when the drain-source voltage is changing. This occurs during the Miller region when the gate-drain capacitance of the external MOSFET is being charged or discharged. This capacitance is referred to as the Miller capacitor and the period of time as the Miller time.

MOSFET gate drives are controlled according to the values set in the slew control variables IR1, IR2, IF1, IF2, TRS, and TFS. The off-to-on transition is controlled by IR1, IR2, and TRS. The on-to-off transition is controlled by IF1, IF2, and TFS.

There are two gate drive control modes, switched and slew control. All gate drives operate in the same mode.

In switched mode, the gates are driven at the full capability of the pull-up or pull-down switches in the gate drive, as shown in Figure 14b. If both IR1 and IR2 are set to zero, the gate drive operates in full switched mode for the off-to-on transition. If both IF1 and IF2 are set to zero, the gate drive operates in full switched mode for the on-to-off transition.

In slew-control mode, the gates are driven using programmable currents to provide some control over the slew rate of the motor phase connection as shown in Figure 14a. To operate in slew-control mode for the off-to-on transition, both IR1 and IR2 must be non-zero. To operate in slew-control mode for the on-to-off transition, both IF1 and IF2 must be non-zero. If any of the drive currents are set to zero, then the output will operate in switched mode for the period of time when that current is active.

The basic principle of the slew rate mode is to drive the gate with a controlled current for a fixed time to quickly get the MOSFET to the Miller region where the drain-source voltage, V_{DS}, starts to change, then to follow this with a second usually lower current to control the VDS slew rate. Finally, the gate drive changes to switch mode once VDS has completed its transition.

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In slew control mode, when a gate drive is commanded to turn on, a current, I_{R1} (defined by IR1[3:0]), is sourced from the relevant gate drive output for a duration, t_R (defined by TR[3:0]). These parameters should typically be set to quickly charge the MOSFET input capacitance such that the gate-source voltage rises close to the Miller voltage of the MOSFET. The drain-source voltage of the MOSFET will not start to change until the gate-source voltage reaches this level. After this time, the current sourced on the gate drive output is set to a value of I_{R2} (as defined by IR2[3:0]) and remains at this value while the MOSFET transitions through the Miller region. I_{R2} should be selected to achieve the required slew rate of the drain-source voltage by setting the charge time of the drain-gate (Miller) capacitor.

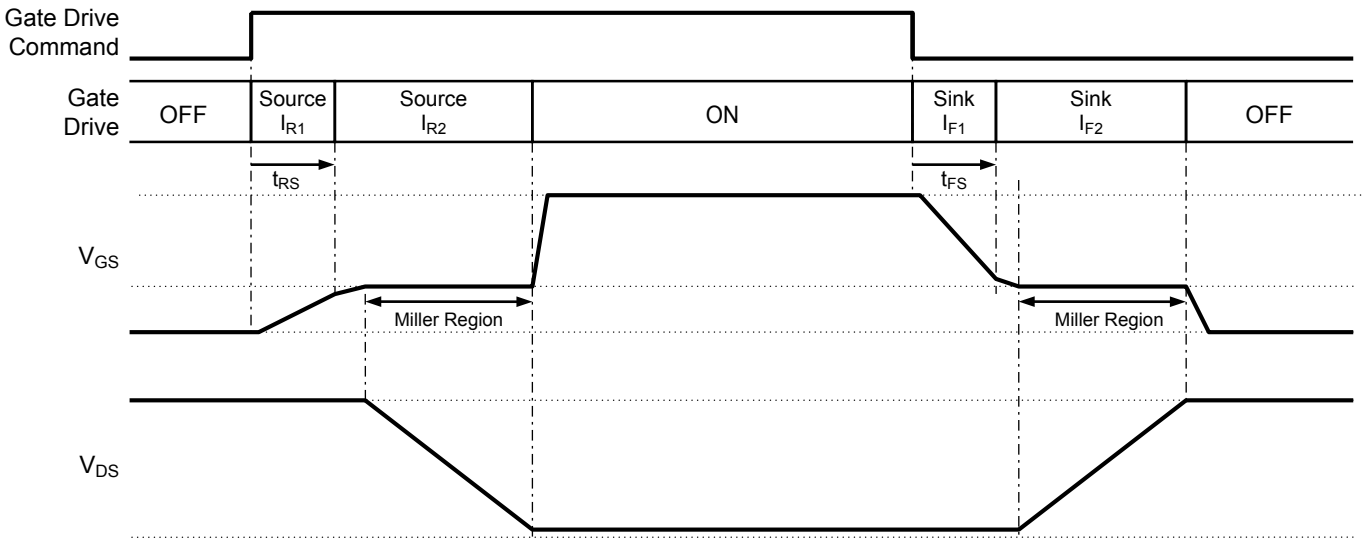

Figure 14a: Off-to-On and On-to-Off Transitions with Gate Drive Control Enabled

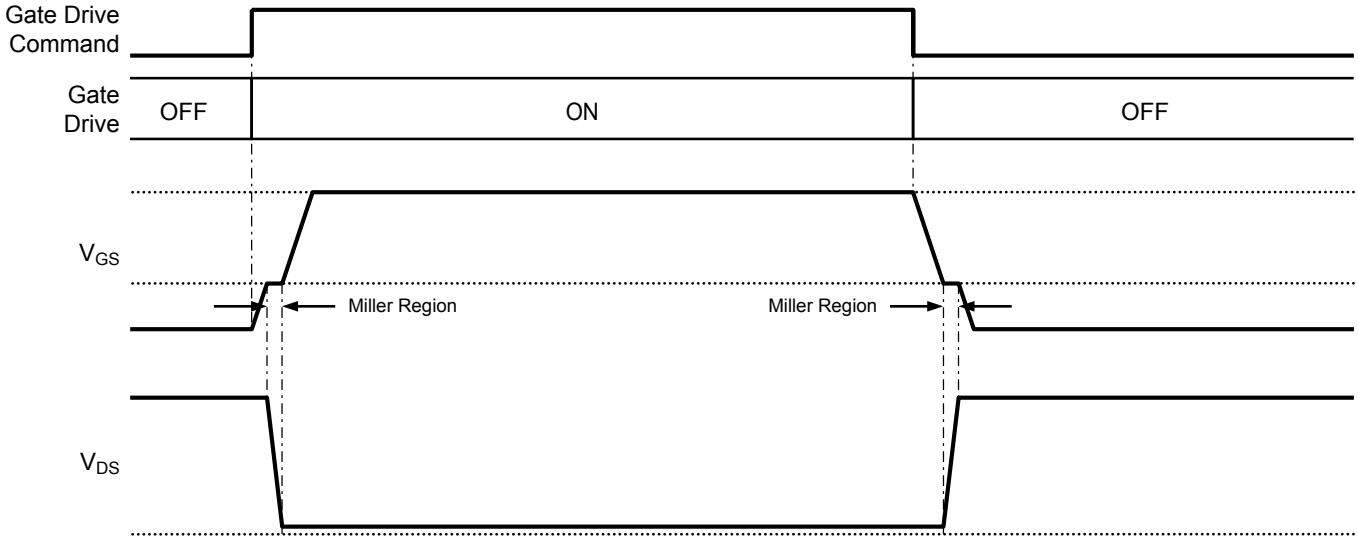

Figure 14b: Off-to-On and On-to-Off Transitions with Gate Drive Control Disabled

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When the MOSFET reaches the fully on state, the gate drive output changes from current drive to voltage drive to hold the MOSFET in the on state.

A high-side MOSFET is considered to be in the fully on state when the drain-source voltage, V_{DS} (= V_{BB} – V_{Sx}), drops below the programmed V_{DS} threshold voltage, V_{DST}.

A low-side MOSFET is considered to be in the fully on state when the drain-source voltage, V_{DS} (= V_{Sx} – V_{GND}), drops below the programmed V_{DS} threshold voltage, V_{DST}.

When a gate drive is commanded to turn off in slew control mode, a current, I_{F1} (defined by IF1[3:0]) is sunk to the relevant gate drive output for a duration, t_{FS} (defined by TFS[3:0]). These parameters should typically be set to quickly discharge the MOSFET input capacitance such that the gate-source voltage drops to close to the Miller voltage of the MOSFET. The drain-source voltage of the MOSFET will not start to change until the gate-source voltage reaches this level. After this time, the current sourced on the gate drive output is set to a value of I_{F2} (as defined by IF2[3:0]) and remains at this value while the MOSFET transitions through the Miller region. I_{F2} should be selected to achieve the required slew rate of the drain-source voltage by setting the discharge time of the drain-gate (Miller) capacitor.

When the MOSFET reaches the fully off state the gate drive output changes from current drive to voltage drive to hold the MOSFET in the off state.

A high-side MOSFET is considered to be in the fully off state when the drain-source voltage of its complementary low-side MOSFET, V_{DS} (= V_{Sx} – V_{GND}), drops below the programmed V_{DS} threshold voltage, V_{DST}.

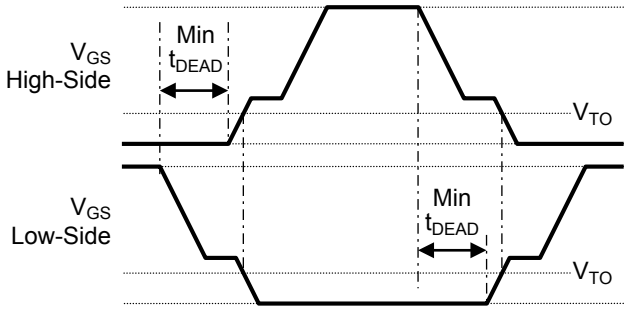

Figure 15: Minimum Dead Time

A low-side MOSFET is considered to be in the fully off state when the drain-source voltage of its complementary high-side MOSFET, V_{DS} (= V_{BB} – V_{Sx}), drops below the programmed V_{DS} threshold voltage, V_{DST}.

DEAD TIME

To prevent shoot-through (transient cross-conduction) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs is switched at the same time, for example, at the PWM switch point. In the A4964, the dead time for all three phases is set by the contents of the DT[5:0] bits. These six bits contain a positive integer that determines the dead time by division from the system clock.

The dead time is defined as:

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0] and t_{DEAD} has a minimum value of 100 ns.

For example, when DT[5:0] contains [01 1000] (= 24 in decimal), then t_{DEAD} = 1.2 µs, typically.

The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the electrical characteristics table. A value of 0, 1, or 2 in DT[5:0] will set the minimum dead time of 100 ns.

The value of the dead time should be selected such that the gate-source voltage of any pair of complementary MOSFETs is never above the threshold voltage for both MOSFET at the same time as shown in Figure 15. This applies in either the slew control mode or the switch mode. In the slew control mode, the dead time must be increased to accommodate the extended switching times.

PWM FREQUENCY

In all control modes, the base frequency of the bridge PWM signal is fixed by the value of the base PWM period, t_{PW}. This base frequency can be altered by the frequency dither function described below.

The PWM waveforms applied to each phase of the bridge can be aligned in two ways selected by the PMD bit. When PMD is set to 0, the bridge is in center-aligned mode and the three-phase PWM waveforms are centered about a common point in time, as shown in Figure 10a. When PMD is set to 1, the bridge is in edge-aligned mode and the three-phase PWM waveforms all change from low to high at the same time as shown in Figure 10b.

In both modes, the period of the PWM frequency is set by the PW[5:0] variable. The six bits of PW contain a positive integer that determines the PWM period derived by division from the system clock.

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The PWM period is defined as:

$$t_{PW} = 20.10\ \mu s + (n \times 0.8)\ \mu s \quad (when\ PMD = 0)$$

$$t_{PW} = 20.05\ \mu s + (n \times 0.8)\ \mu s \quad (when\ PMD = 1)$$

where *n* is a positive integer defined by PW[5:0].

For example, when PW[5:0] = [10 0110] and PMD = 0, then t_{PW} = 50.5 µs and the PWM frequency is 19.8 kHz.

PWM FREQUENCY DITHER

The A4964 includes an optional PWM frequency dither scheme that can be used to reduce the peak radiated and conducted electromagnetic (EM) emissions. This is accomplished by stepping the PWM period in a triangular pattern in order to spread the EM energy created by the PWM switching. There are three programmable variables that can be used to adjust the frequency spreading for different applications: dither step period, $t_{\Delta PW}$, dwell time, t_{DD}, and the number of steps in the pattern, N_{DS}. These are identified in Figure 16.

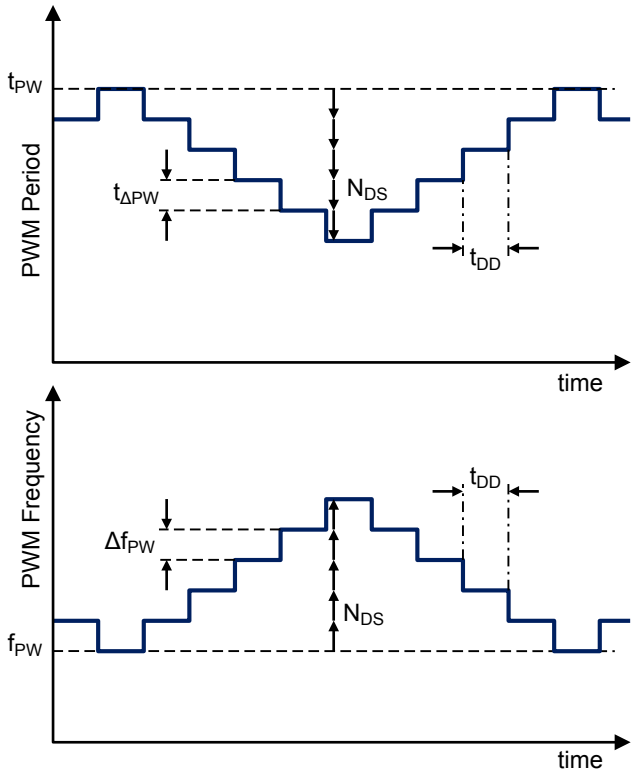

Figure 16: PWM Frequency Dither

Figure 16 shows the dithered period on top and the corresponding frequency below. The PWM frequency at any time is defined by the PWM period. The base PWM period, t_{PW}, is indicated as is the resulting base frequency, f_{PW}.

The dither step period, $t_{\Delta PW}$, is the incremental change in PWM period at each dither step and is defined by:

$$t_{\Delta PW} = -0.2 - (n \times 0.2)\ \mu s$$

where *n* is a positive integer defined by DP[2:0].

Following each change, the PWM period will remain at the new value for the duration of the dither dwell time, selected as 1 ms, 2 ms, 5 ms, or 10 ms by the contents of the DD[1:0] variable.

The number of dither steps, N_{DS}, is the value in the DS[3:0] variable. Starting at the base PWM period, the PWM period will decrease by the dither step period N_{DS} times, then increase by the same amount and number of steps before restarting the cycle. N_{DS} can have a value between 0 and 15. A value of 0 will disable PWM frequency dither. The minimum PWM period in any case is 18 µs. If the frequency dither settings attempt to reduce the PWM period below 18 µs, then it will be held at 18 µs until the dither sequence brings the required value above 18 µs again.

As the frequency shift is defined by a fixed period change, the change in frequency will be slightly different for each step, but the frequency spreading effect will still be effective.

Current Limit

An integrated fixed-frequency PWM current control circuit is provided to limit the motor current during periods where the torque demand exceeds the normal operating range, and to provide a variable current limit in the closed-loop current control mode. The frequency of the current control circuit is set to be the same as the programmed bridge PWM defined by the value of PW[5:0].

The current limit can be disabled in either of the speed control modes by setting the disable current limit bit, DIL, to 1. When the closed-loop current control mode is selected, DIL must be set to 0.

The state of the current control circuit is reported by the current limit bit, CLI, in the Status register. In either of the speed control modes, the CLI bit is set to 1 when the motor current exceeds the current limit and reset to 0 when the motor current falls below the current limit. In the closed-loop current control mode, the CLI bit is set to 1 when the motor current does not reach the variable current limit and reset to 0 when the motor current reaches the variable current limit.

The ground return current is measured as a voltage, V_{SENSE}, across a sense resistor, R_{SENSE}, placed between the supply ground and the common connection to the sources of the low-side MOSFETs in the three-phase power bridge. A sense amplifier with high common-mode rejection and a fast response time is provided

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to convert the differential current sense voltage, directly across the sense resistor, to a ground-referenced voltage and remove any common-mode noise. The gain of the sense amplifier is programmable to provide four levels of threshold sensitivity. The maximum threshold voltage is set by the contents of the MIT[1:0] variable as follows:

MIT1	MIT0	Maximum Threshold (mV)
0	0	200
0	1	100
1	0	50
1	1	25

The output of the sense amplifier is compared to a current limit threshold voltage, V_{ILIM}, to indicate to the PWM control circuit when the bridge current is greater than the current limit threshold.

The value of V_{ILIM} can be set in two ways depending on the motor control method selected.

When either of the speed control modes are selected, the value of V_{ILIM} is determined by:

$$V_{ILIM} = V_{MIT} \times V_{ISC}$$

where V_{MIT} is the maximum threshold of the sense amplifier as defined by the MIT variable, and V_{ISC} is the current limit scale as defined by the VIL variable.

When the closed-loop current control mode is selected, V_{ILIM} is determined by demand input. This sets the required value of V_{ILIM} as a ratio of the maximum threshold of V_{MIT}. For example, when the demand input is 256 and V_{MIT} is 200 mV then V_{ILIM} will be 50 mV. In this mode, only the 5 most significant bits of the 10-bit demand input are used to set the value of V_{ILIM}. For example if DI[9:0] = 0100000000, then the demand input is 287, and if DI[9:0] = 0100011111, then the demand input is also 287.

The relationship between the threshold voltage and the threshold current is defined as:

$$I_{LIM} = V_{ILIM} / R_{SENSE}$$

where R_{SENSE} is the value of the sense resistor.

At the start of a PWM cycle, the MOSFETs in the bridge are always turned on at the appropriate time to generate the required phase currents.

During the PWM switching, the sum of the currents, in the phases where the low-side MOSFET for the phase is active, will pass through the sense resistor. If the current through the sense resistor increases such that the voltage across it, V_{SENSE}, rises above V_{ILIM}, the bridge will switch off all high-side MOSFETs and allow the phase currents to recirculate round the low-side MOSFETs.

The MOSFETs in the bridge will remain in this state until the high-side MOSFETs are switched on again after the start of the next PWM period.

CURRENT COMPARATOR BLANKING

When the bridge is switching, the voltage across the sense resistor will be subject to various transient voltage spikes. To prevent these spikes from being detected as a current-limit trip, the output from the current comparator is qualified using a blanking timer to ensure that any current-limit trip that is detected is valid.

The blank timer is started each time any gate drive output changes. At the end of the blank time, if the comparator is indicating that the current is higher than the trip level, then the current-limit trip is considered valid and the bridge MOSFETs will be switched as above.

The length of the blank time, t_{OCB}, is set by the contents of the OBT[4:0] variable. These four bits contain a positive integer that determines the time derived by division from the system clock.

The blank time is defined as:

$$t_{OCB} = (n + 2) \times 200\ ns$$

where n is a positive integer defined by OBT[4:0].

For example, when OBT[4:0] contains [1 0110] (= 22 in decimal), then t_{OCB} = 4.8 µs, typically.

Setting a value of OBT = 0, 1, 2, and 3 will set the blank time to 1 µs.

The user must ensure that the blank time is long enough to mask any current transients seen by the internal sense amplifier.

Motor Commutation Control

The A4964 can drive a 3-phase BLDC motor using sinusoidal drive or trapezoidal drive (block commutation). Depending on the motor design, sinusoidal drive can be used to reduce audible motor noise by driving the motor with low output torque ripple. Trapezoidal drive provides the highest motor output but with an increased torque ripple at the commutation points.

PWM GENERATOR

A three-phase PWM generator is used to create the required waveform at each phase. When the drive mode bit, DRM, is set to 0, the PWM generator modulates (multiplies) the peak PWM duty cycle with an envelope that will create three sinusoidal

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waveforms between the phases. When DRM is set to 1, the PWM generator drives each phase in sequence with the peak PWM duty cycle and ramps the duty cycle up and down at the beginning and end of the peak PWM duty cycle period to produce a trapezoidal drive waveform at each phase.

In addition, the PWM generator can be set, using the PWM modulation bit, MOD, to drive the bridge with two-phase or three-phase modulation. When MOD is set to 0, the bridge will be driven with three-phase modulation, where all three phases will always be driven with a PWM signal. When MOD is set to 1, the bridge will be driven with two-phase modulation, where, at any instant, one phase will be held low and the other two phases driven with a PWM signal. Three-phase modulation must be enabled in order to use automatic phase advance. Two-phase modulation will reduce the switching losses in the bridge and the power dissipation in the A4964.

Table 2: Trapezoidal Drive Phase Sequence

Reverse	Forward	State	Motor Phase		
DIR = 1	DIR = 0		SA	SB	SC
↑	↓	1	Z	LO	HI
		2	HI	LO	Z
		3	HI	Z	LO
		4	Z	HI	LO
		5	LO	HI	Z
		6	LO	Z	HI

HI ≡ high-side FET active, LO ≡ low-side FET active
Z ≡ high impedance, both FETs off

The modulation for each phase and each option is shown in Figure 6, Figure 7, and Figure 8. Figure 6 shows sinusoidal drive with three-phase modulation and Figure 7 with two-phase modulation. In both cases, although the resulting individual phase signals are not sinusoidal, they will produce sinusoidal signals between the three phases.

In trapezoidal drive mode, the A4964 will ramp the phase duty cycle between the minimum and maximum duty cycles. This will produce a “soft switching” effect where the torque transitions smoothly between commutation points. If a classical trapezoidal drive is required as shown in Table 2, then set DRM to 1 for trapezoidal drive and set BW to 31 to set the bemf window to 60°.

OVERMODULATION

The A4964 also provides an overmodulation function, which may be used to increase the drive to the motor beyond the drive available using the pure sinusoidal drive. This function is enabled by setting a non-zero value in the overmodulation variable, OVM[1:0]. A value of 1, 2, or 3 in OVM will set the overmodulation factor to 112.5%, 125%, and 150% respectively. This overmodulation factor is applied to each setting of the PWM duty cycle sent to the bridge. For example, when OVM is set to 2, the overmodulation factor is set to 125%, and each modulation level is multiplied by 1.25, up to the 100% maximum duty cycle. The effect of this is to distort the sinusoidal waveform such that the 100% duty cycle is present for longer. This provides a similar effect to switching to trapezoidal drive but maintains the sinusoidal waveform when the product of the overmodulation factor and the PWM level sent to the bridge is less than 100%. Overmodulation examples are shown in Figure 9.

ROTOR POSITION SENSING USING MOTOR BEMF

The phase sequences create a rotating magnetic field around the rotor against which the permanent magnets in the rotor can react to produce torque at the motor output shaft causing the motor to rotate. For the motor to run with low torque ripple the three-phase drive has to be synchronized to the motor phase position. That is the position of the magnetic poles of the rotor in relation to the poles of the stator. This phase angle is determined by a closed-loop commutation controller consisting of a position estimator and commutation timer. This controller uses the output of a complete self-contained bemf sensing scheme to determine the actual position of the motor, and adjusts the estimated position and commutation frequency to synchronize with the rotor poles in the motor.

A key element of the controller is the back-emf (bemf) zero-crossing detector. This is a dedicated analog system that continuously monitors all three motor phases. It is capable of operating at high and low supply voltage with a very low bemf voltage in the presence of switching noise. This results in the ability to run a suitable motor from very low speeds to extremely high speeds. The internally generated center-tap (zero crossing reference) voltage follows the bridge drive voltage levels to allow bemf crossing detection during both PWM-on and PWM-off states.

In trapezoidal drive mode, the rotor position is determined by comparing the voltage on the undriven (tri-state) motor phase (indicated by Z in Table 2) to the voltage at the center tap of the motor, approximated using an internally generated reference voltage. The voltage on the undriven phase with reference to the center tap voltage is the bemf of the motor. The bemf zero crossing, the point where the voltage of the undriven motor winding crosses the reference voltage, occurs when a pole of the rotor is in alignment with a pole of the stator and is used as a positional reference for the commutation controller. In this case, the bemf

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for each phase is monitored for the complete commutation period where the phase is not driven.

In sinusoidal drive, all three phases are being continuously driven. This does not allow for the bemf to be monitored independently of the drive signals, so the A4964 stops applying the driving signal for a brief duration close to the expected bemf crossing point. The size of this window and the number of times the window is opened per electrical cycle is programmable through the serial interface using the BW (bemf window) and BS (bemf samples) variables. The window can be programmed in 1.4° steps from 1.4° to 43.4° and to 60° when BW = 31. All angles are with respect to the electrical cycle. The window is opened just before the time at which the bemf is expected to be at the zero crossing point.

In both cases the commutation controller compares the expected zero crossing point to the detected zero crossing point and adjusts the phase and frequency of the position estimator and commutation timer to minimize the difference between the expected and actual crossing points over a number of commutation periods.

PHASE ADVANCE

The controller also allows programmable phase advance, where the magnetic field of the stator can be driven ahead of the rotor. This can be used to produce an effect known as field weakening, which effectively reduces the bemf of the motor and allows the motor to run at a higher speed for the same applied voltage. It can also be used to optimize the efficiency of the drive by aligning the phase of the current with the phase of the applied voltage. There are two phase advance modes available: manual and automatic, selected by the phase advance mode bit, PAM.

In manual phase advance mode, when PAM = 0, the angular position of the estimated bemf zero crossing point is simply adjusted to be later in the commutation period. The controller modifies the commutation timing to minimize the difference between the estimated and measured bemf zero-crossing points. This results in a phase advance of the stator field from the rotor position.

In automatic phase advance mode, when PAM = 1, the angular position of the estimated bemf zero crossing point is adjusted based on the phase angle between the applied voltage waveform and the motor current. In this mode, when the programmed phase angle is set to zero, the A4964 will adjust the estimated bemf zero crossing point such that the angle between the motor phase current and applied phase voltage is zero. The programmed phase advance angle will then be the angle between the motor phase current and applied phase voltage. The automatic phase advance mode will adjust the estimated bemf zero crossing point to achieve the optimum performance across a wide range of speeds, loads and supply voltages and temperatures without having to update the phase angle as would be required in the manual mode. The gain of the control loop for the automatic phase advance can be adjusted by the KIP[1:0] variable to 1, 2, 4, or 8. A higher value will result in a faster change but less stability. A lower value will result in greater stability but a slower response to speed, voltage, and load variations.

COMMUTATION CONTROLLER TUNING

The commutation controller uses proportional and integral feedback (PI control) to provide a fast response with good long-term accuracy. The proportional and the integral gains can be adjusted independently for operation in the steady state and in the transient state. The commutation control loop is defined to be in steady state when the difference between the estimated motor speed and the target motor speed is less than 10 Hz. When the difference increases to greater than 10 Hz, the control loop is defined to be in the transient state. Once in the transient state, the speed difference must reduce below 5 Hz before the control loop returns to the steady state.

In the steady state, the proportional and integral control loop gains are set by the CP[3:0] and CI[3:0] variables respectively, through the serial interface. In the transient state, the proportional and integral control loop gains are set by the CPT[3:0] and CIT[3:0] variables respectively. This allows the dynamic response of the commutation controller to be tuned to different system conditions if required.

The control method used is tolerant to missing bemf zero crossing detection and will simply change the speed of the applied commutation sequence by an amount determined by the proportional gain of the control loop. This results in a much more stable system that does not lose synchronization due to impulse perturbations in the motor load torque. It also means that real loss of synchronization cannot be determined by missing bemf zero crossing detection and has to be determined in a different way.

In the extreme case when a motor stalls due to excessive load on the output, there will be no bemf zero crossing detection and the frequency of the commutation sequence will be reduced at each commutation point to try and regain synchronization. If the resulting speed reduces below the low-speed threshold, set by the SL[3:0] variable, then the controller will enter the loss of synchronization state and either stop or attempt to restart the motor.

In some cases, rather than a complete stall, it is also possible for the motor to vibrate at a whole fraction (subharmonic) of the commutation frequency produced by the controller. In this case,

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the controller will still detect the bemf zero crossing but at a rate much higher than the motor is capable of running. If the resulting speed increases above the overspeed threshold, set by the SH[3:0] variable, then the controller will enter the loss of synchronization state and either stop or attempt to restart the motor.

MOTOR STARTUP

The sensorless commutation method used in the A4964 relies on the motor bemf voltage. This voltage must be high enough to allow detection of the zero crossing point. When the motor is stationary, or moving at very low speed, the bemf is either zero or at a level lower than can be detected by the bemf zero crossing detector, so the motor position cannot be determined.

This means that a startup sequence must be used that will start the motor rotating and accelerate the motor to a sufficiently high speed for bemf zero crossings to be detected. This must be done without reference to the actual motor position. To achieve reliable startup over a wide range of motors, loads, supply and environmental conditions, the A4964 provides multiple programmable startup features. The basic sequence starts by checking the motor bemf to determine if the motor is already rotating. If so, special pre-rotation functions are implemented as described below. If no rotation is detected, then the normal startup sequence consists of an alignment time followed by open-loop commutation with increasing speed, then a short coast period before switching into the closed-loop commutation control system and the closed-loop speed control, if selected.

Each of the startup features has several programmable variables, and the alignment and coast features can be completely disabled. The complete sequence is shown in Figure 17.

ALIGNMENT

The alignment feature can be used to move the motor into a known position. This helps to achieve a consistent startup pattern and helps avoid noise in the initial stages of the startup sequence. The duration of the alignment time (also known as hold time) is determined by the value of the HT[3:0] variable. If the alignment feature is not required, then it can be disabled by setting HT[3:0] to zero. During the alignment, the peak duty cycle is set to the value defined by the HD[4:0] variable. The peak value is then modified by the PWM generator to produce the duty cycles at each phase for the 0° position shown in Figure 6 and Figure 7.

For two-phase modulation, the peak duty cycle for each phase is defined as:

$$Phase\ A = (D_H \div 2)\%$$

$$Phase\ B = 0$$

$$Phase\ C = D_H\%$$

For three-phase modulation, the peak duty cycle for each phase is defined as:

$$Phase\ A = 50\%$$

$$Phase\ B = 50\% - (D_H \div 2)\%$$

$$Phase\ C = 50\% + (D_H \div 2)\%$$

where D_H is the peak PWM duty during alignment defined by HD[4:0].

The time to rise from zero to the programmed value can be selected as a percentage of the alignment time by the HR[1:0] variable. This can be 0%, 25%, 50%, or 100%. At 0%, the programmed value will be present for the full alignment time. For example, at 25%, it will ramp from zero to the programmed value for the first 25% of the alignment time, then hold at the programmed value for the remainder of the alignment time. At 100%, it will ramp from zero to the programmed value over the full alignment time.

The integrated current limit remains active, if enabled, during the hold time in order to limit the inrush current and to limit the effects of increased supply voltage or low operating temperature.

RAMP

Following the alignment time, sinusoidal (DRM = 0) or trapezoidal (DRM = 1) waveforms are applied to the three phases to create a rotating magnetic field in the motor and start the motor running in the required direction. During this time, the motor position is ignored and the motor phases are driven in open-loop commutation mode. The starting speed of the rotating field is defined by the SF1[3:0] variable and the speed is ramped up linearly until it reaches the ramp end speed defined by SF2[3:0]. The slope of the speed ramp and the duration are defined by the speed increment, f_{SS}, defined by the SFS[3:0] variable, and the step time, t_{SS}, defined by the STS[3:0] variable. All speed variables define the electrical frequency as defined by the electrical period shown in Figure 6, and are set in hertz. When the ramp starts, the peak duty cycle applied to the bridge is defined by the contents of the SD1[3:0] variable. The peak duty cycle is then increased linearly up to the peak duty cycle applied to the bridge, defined by the contents of the SD2[3:0] variable at the end of the ramp.

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COAST

At the end of the ramp period, if the STM bit is set to 1, the outputs will be disabled and the motor will coast for a short time. During this time, the motor bemf is sensed and the zero-crossing point detected in order to correctly synchronize the motor phase angle counter to the motor position and the drive frequency to the motor speed. Once three correct synchronization events have been detected, the motor phase drive is re-enabled and the motor runs with closed-loop commutation.

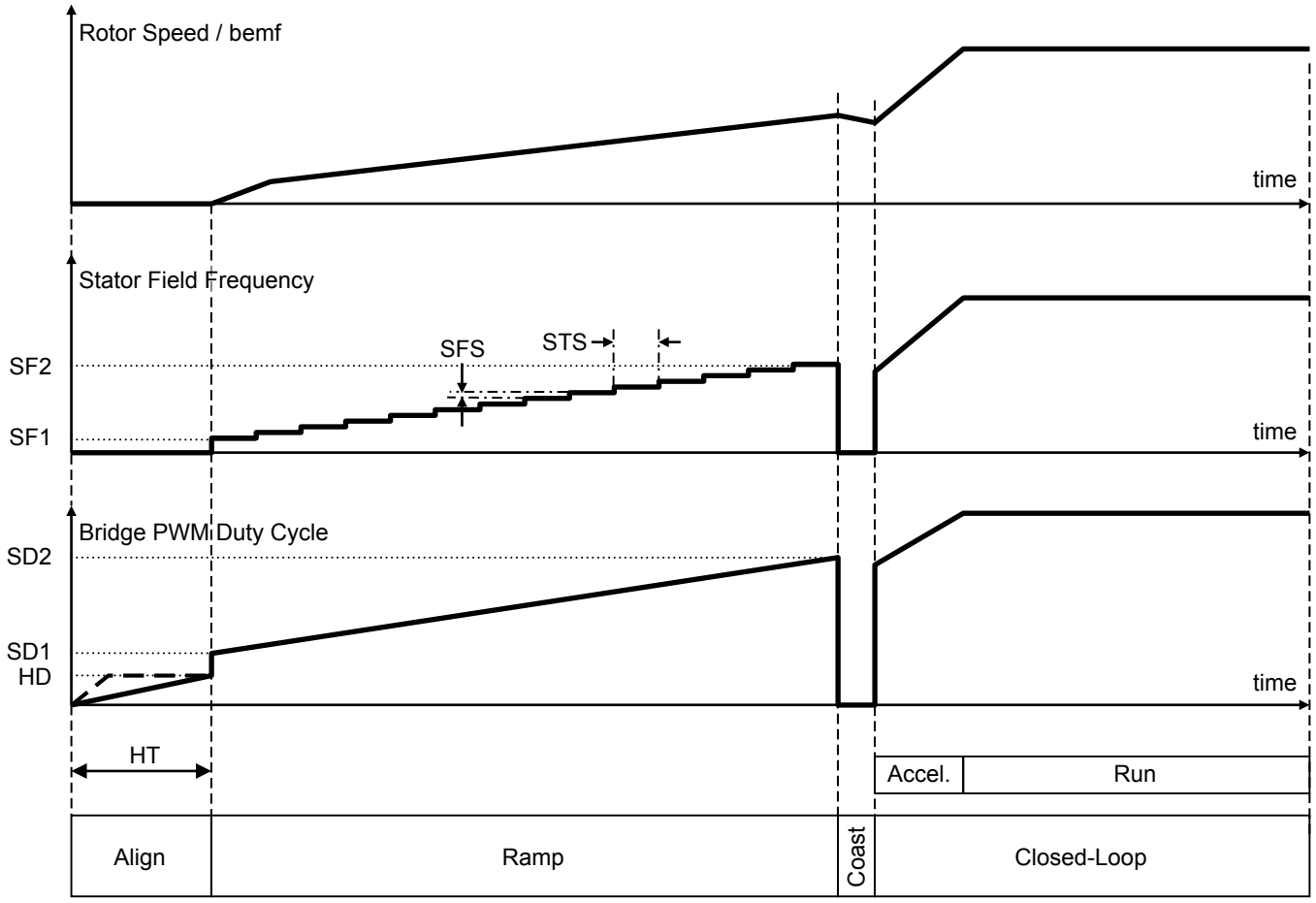

Figure 17: Sensorless Start Sequence

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To ensure a smooth transition into the full commutation closed-loop operation, the peak duty cycle applied to the power bridge should be close to the duty cycle required for the present motor speed. This avoids large inrush or braking currents as the drive is re-enabled. The required duty cycle is determined using the measured motor speed, the speed resolution and the motor constant, K_M, as:

$$D_{PK} = \frac{\left(\frac{f_E}{0.1} \times K_M\right)}{1023} \times 100\ (\%)$$

where D_{PK} is the peak duty cycle applied to the bridge, f_E is the motor electrical cycle frequency and K_M is the motor constant set by the value in the KM[3:0] variable and can be between 0.3 and 1.05 in steps of 0.05.

The actual motor electrical cycle frequency, f_E, is defined by:

$$f_E = n \times SR\ (Hz)$$

where *SR* is the speed resolution defined by the SR[2:0] variable and *n* is a positive integer defined by DO[9:0] when RBS[2:0] = [001].

Calculation of the correct duty cycle is also used during the windmill detection phase if enabled.

In many systems where the motor and load inertia is low and the friction load is high, it is more effective to go directly from ramp to closed-loop commutation without the coast period. In this case, STM can be set to zero to disable the coast function during start-up. The coast function during startup is beneficial for high inertia loads such as fans and blowers and helps provide a low audible noise startup.

Once in commutation closed-loop mode, the A4964 will synchronize the applied field, created by the motor phase angle counter and the sinusoidal PWM generator, to the motor position and ramp the speed to match the demand input.

START WITH PRE-ROTATION (WINDMILLING)

In some cases when motor start is required, the motor may still be coasting from a previously running state or it may be rotating by the action of the load on the motor. Setting the WIN bit to 1 will modify the startup sequence by initially monitoring the motor bemf for windmill bemf zero-crossing events in order to detect any pre-rotation. A windmill bemf zero-crossing event must be present for longer than the windmill bemf filter time, t_{bf}, for the motor speed and direction to be determined. The windmill bemf filter time is set through the serial interface using the BF variable. The motor speed is available from the readback register during this time.

If no windmill bemf zero-crossing events are detected within 300 ms or the motor speed is less than the minimum windmill detection frequency, f_{WMF}, defined by the WMF[3:0] variable, then the motor is assumed to be stationary and the normal start sequence is followed. If WIN is set to 0, then any pre-rotation will be ignored and the normal start sequence followed.

If the bemf indicates that the motor is running in the opposite direction to that programmed, then a brake torque is applied by applying a PWM signal to all low-side MOSFETs until the bemf indicates that the motor is stationary. The low-side MOSFETs are switched at the programmed PWM frequency with the window brake duty cycle, D_{WB}, defined by the contents of the WBD[3:0] variable. Once the motor speed is less than f_{WMF}, then the motor is assumed to be stationary and the normal start sequence is followed.

If the bemf indicates that the motor is running in the same direction to that programmed, then the alignment and ramp functions are not used and the startup sequence goes directly to coast and synchronization before switching directly to full commutation closed-loop operation.

Motor Control Modes

There are three motor control methods included in the A4964. These are:

1. open-loop speed (voltage) control
2. closed-loop torque (current) control
3. closed-loop speed control

The control mode and all associated parameters are determined by the contents of the configuration and control registers. These registers can be changed on-the-fly through the SPI. The user-defined values in these registers are held in programmable non-volatile memory, allowing the A4964 to be pre-programmed with default values for a specific application and avoid the need to program the register contents at each power on. The motor movement can be controlled directly through the SPI or, in standalone mode, by a PWM applied to the LIN terminal.

In SPI operating mode, selected by setting the OPM variable to 0, the running state, direction, and output of the motor are controlled by a combination of commands through the serial interface. These are a demand input variable, DI[9:0], plus three control bits, RUN, DIR, and BRK.

In stand-alone operating mode, selected by setting the OPM variable to 1, the output of the motor is controlled by the duty cycle of a PWM input, which sets the value in the DI[9:0] demand input variable. The three control bits, RUN, DIR, and BRK can still control the running state of the motor through the serial inter-

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face but the demand input is only accepted from the PWM signal applied to the LIN terminal. All configuration parameters can be modified in either mode.

When RUN = 1, the A4964 is allowed to run the motor or to commence the startup sequence. When RUN = 0, all gate drive outputs go low, no commutation takes place, and the motor is allowed to coast. RUN = 0 overrides all other control inputs.

The DIR bit determines the direction of rotation. Forward is defined as DIR = 0, reverse is when DIR = 1. The forward and reverse waveforms are defined in Figure 6, Figure 7, Figure 8, and Table 2.

In SPI operating mode, the BRK bit can be set to apply an electrodynamic brake which will decelerate a rotating motor. It will also provide some holding torque for a stationary motor. When RUN = 1 and BRK = 1, all low-side MOSFETs will be turned on and all high-side MOSFETs turned off, effectively applying a short between the motor windings. This allows the reverse voltage generated by the rotation of the motor (motor bemf) to set up a current in the motor phase windings that will produce a braking torque. This braking torque will always oppose the direction of rotation of the motor. The strength of the braking or holding torque will depend on the motor parameters. No commutation takes place during braking and no current control is available. Care must be taken to ensure that the braking current does not exceed the capability of the low-side MOSFETs.

In stand-alone operating mode, the BRK bit does not directly control braking, but can be set to enable braking when the PWM input is held low as described below.

The 10-bit demand input variable, DI[9:0], sets the bridge PWM duty cycle for the open-loop speed control mode, the torque (current) reference for the current control mode, or the speed reference for the closed-loop speed control mode. For the speed control modes, the resolution is better than 0.1%. For the current control mode, only the most significant 8 bits are used and the demand input resolution is 0.5%. In standalone operating mode, DI[9:0] cannot be changed through the serial interface.

PWM CONTROL INPUT

In the stand-alone operating mode, selected by setting OPM to 1, the function of the LIN input terminal changes to a PWM input, the duty cycle of which provides a proportional demand input for the selected control mode and replaces the contents of DI[9:0]. It can be driven between ground and VBB and has hysteresis and a noise filter to improve noise performance. The sense of the PWM input can be selected as active high or active low using the IPI bit. When IPI is 0, the LIN input is active high. When IPI is 1, then the LIN input is inverted and active low.

The PWM input, applied to the LIN terminal, is a low frequency signal, between 5 Hz and 1 kHz. The duty cycle of this signal is measured with a 10-bit counter system, giving better than 0.1% resolution in duty cycle. When IPI is 0, the duty cycle is the ratio of the PWM (active) high duration to the PWM period measured between rising edges of the PWM input signal. When IPI is 1, the duty cycle is the ratio of the PWM (active) low duration to the PWM period measured between falling edges of the PWM input signal. The measured duty cycle is written to the DI[9:0] variable at the end of each PWM measurement period when the PWM signal changes back to the active state.

The A4964 can accept slight variation in the PWM frequency from cycle to cycle. However, any variation will be translated to a demand input variation.

In standalone operating mode, the DIR and RUN bits still control the motor direction and activity. RUN must be set to 1 to permit the PWM input to control the motor output. The function of the BRK bit function changes to be a PWM brake enable as described below.

When the PWM input changes from the inactive state, with DI = 0 and the motor in the brake or coast mode, the first write to DI will occur at the end of the first PWM cycle if the duty cycle is less than 100%. If the duty cycle is 100%, i.e. the PWM input goes from inactive to active, the first write to DI will occur at the end of the PWM timeout period, t_{PTO}.

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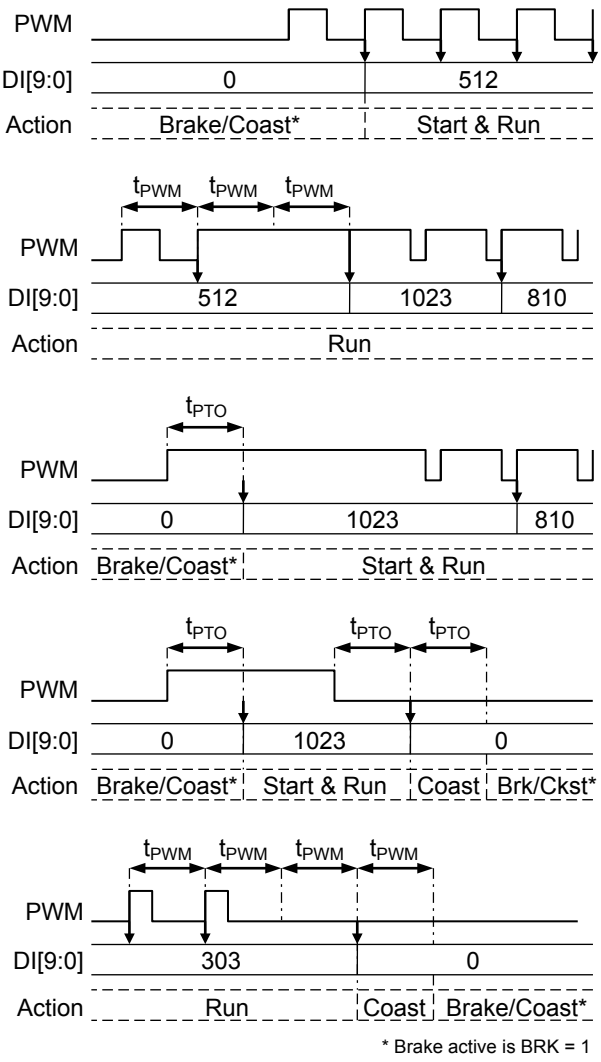

Figure 18: PWM Timing (IPI = 0; PWM active high)

When the duty cycle changes from a value less than 100% to 100%, the write of the maximum value 1023 to DI will occur after two t_{PWM} periods from the previous inactive to active transition. When the PWM duty cycle changes back to a value less than 100%, the maximum value will remain in DI until the end of the first full PWM period at the second inactive to active transition after the 100% input.

If the PWM signal remains in the inactive state for more than twice the length of time of the last measured period, then the A4964 will put the bridge into the PWM-off state permanently and allow the motor current to decay. Holding the PWM signal inactive for a further PWM period, as shown in Figure 18, will force a brake condition if BRK is set to 1. The brake condition can only be active when RUN = 1 and BRK = 1.

Once enabled, the brake condition will be held until the PWM terminal is changed to its active state. If the motor operation is enabled, with RUN = 1, then the A4964 will initiate a start sequence once the PWM duty cycle is in the correct range to permit the start. During the start sequence, if the PWM signal is held inactive as described above, then the start sequence will be terminated and, if enabled, the brake condition will be forced.

For single-wire control systems, the DIAG output can be connected directly to the LIN terminal or to the LTX input to force the PWM signal, applied to the LIN terminal, into a low state in order to inform the remote ECU controlling the A4964 that a fault condition exists. As the PWM signal is always pulled low, the active high PWM input mode (IPI = 0) should be selected for this configuration.

For the simple (active-low fault flag) DIAG mode, selected when DGS[1:0] is 0, a fault will pull the PWM signal low. This will simply stop the motor until the fault clears or is reset.

For the mode where DIAG is high for no fault and pulsed low when a fault is present (DGS[1:0] = [10]), the PWM duty cycle detector will ignore the PWM input signal when DIAG is low and maintain the value in DI at the previously detected level. DI will be updated at the end of the first full PWM period after DIAG goes high. The PWM period time is maintained from the previous duty cycle detection and is available when DIAG goes high to permit detection of an intended low level on the PWM signal, indicating a zero demand input.

For the other two DIAG modes, the DIAG output should not be used to pull the LIN terminal low, as the FG signal will interfere with the PWM signal causing unpredictable results. See Diagnostics section for additional detail.

OPEN-LOOP SPEED (VOLTAGE) CONTROL

In motor control systems where application specific speed control is required the A4964 provides a simple variable duty PWM control mode. In this mode the demand input is directly converted to the duty cycle of the PWM applied to the motor bridge as shown in figure 19. The frequency of the PWM signal applied to the power bridge is determined by the value of the PW[5:0] variable. The resulting bridge PWM duty cycle is used as the peak duty cycle and is further modulated by the 3-phase sine or trapezoidal generator.

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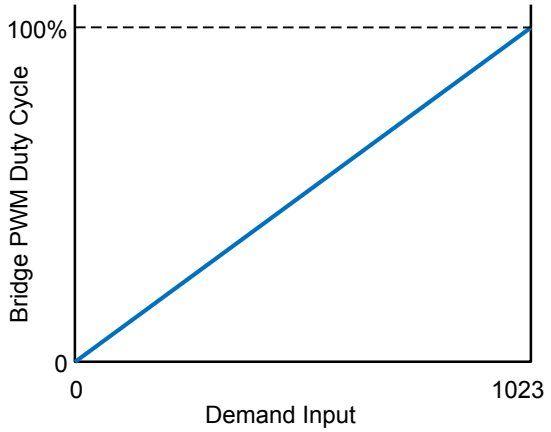

Figure 19: Bridge PWM versus Demand Input

This control mode is equivalent to voltage mode or open-loop speed control. In this mode, the speed is not regulated and will vary with load and supply voltage. Current limiting will remain active if enabled.

The A4964 does not limit the minimum or maximum peak duty cycle applied to the bridge. At 100% demand input, the motor will be running at full speed as determined by the load and the applied voltage. At very low duty cycles, there may not be sufficient current flowing in the motor to maintain sufficient speed for sensorless operation. However, the A4964 will not limit the minimum applied duty cycle in order to provide full flexibility for the speed control ECU to manage the motor operation. If the motor speed drops below the underspeed threshold, f_{SL}, then the A4964 will indicate the loss of synchronization condition.

If a loss of synchronization occurs when the RUN and RSC bits are set to 1, and the demand input is not 0%, then the start sequencer is reset and the start sequence immediately initiated. This cycle will continue until stopped by setting the demand input to 0 or setting either the RUN bit or the RSC bit to 0.

If a loss of synchronization occurs and RSC = 0, the A4964 will remain in the loss of synchronization state until the demand input is set to 0%, the RUN bit is set to 0, or a serial read of the Status register with DSR = 0 occurs.

CLOSED-LOOP TORQUE (CURRENT) CONTROL

The fixed-frequency current limiting feature described above can be used to provide a closed-loop torque control by varying the current reference threshold voltage. Current control can be used in any of the drive modes, but the most accurate phase current control will only be achievable when the motor is driven in two-phase trapezoidal mode with a 60° bemf window.

When operating in the current control mode, the demand input linearly adjusts the current limit threshold voltage, between 0 and V_{MIT} as defined by the MIT variable. Although the demand input is 10 bits, only the 5 most significant bits will be effective.

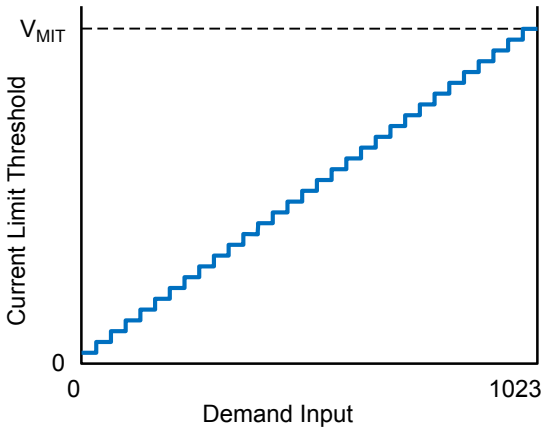

Figure 20: Current Limit versus Demand Input

If the motor load exceeds the available torque for the demanded current limit, then the motor speed will drop until the motor load matches the available torque. If the motor speed drops below the underspeed threshold, then the A4964 will indicate the loss of synchronization condition. If this condition occurs when the RUN and RSC bits are set to 1, and the demand input is not 0%, then the start sequencer is reset and the start sequence is immediately initiated. This cycle will continue until stopped by setting the demand input to 0 or setting either the RUN bit or the RSC bit to 0.

If a loss of synchronization occurs and RSC = 0, the A4964 will remain in the loss of synchronization state until the demand input is set to 0%, the RUN bit is set to 0 or a serial read of the Status register with DSR = 0 occurs.

CLOSED-LOOP SPEED CONTROL

The A4964 includes a speed control loop to provide constant speed under varying supply, load, and temperature conditions. The required motor speed, f_{REF}, is the product of the demand input and the speed control resolution defined by the SR[2:0] variable as defined by:

$$f_{REF} = DI \times SR \ (Hz)$$

where f_{REF} is the required reference speed in Hz, *DI* is the 10-bit demand input, and *SR* is the speed resolution in Hz.

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The reference frequency defines the motor speed as the electrical cycle frequency. The motor speed in rpm can be calculated from:

$$\omega_M = \frac{f_E \times 60}{N_{PP}}$$

where ω_M is the motor speed in rpm, f_E is the electrical cycle frequency, and N_{PP} is the number of magnetic pole pairs in the motor.

The maximum value of f_{REF} for each value of SR is listed in table 3, which also shows the equivalent motor speed (in rpm) for several motor pole-pair options.

The closed-loop speed controller compares the required reference speed to the motor speed. It then adjusts the duty cycle of the PWM signal applied to the bridge in a controlled manner until the motor speed matches the reference speed.

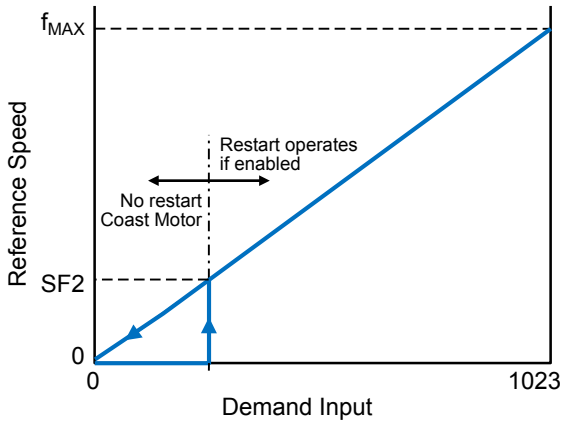

Figure 21: Reference Speed versus Demand Input

The relationship between the demand input and the motor reference speed is shown in Figure 21. As the demand input increases from 0 the bridge drive will be disabled allowing the motor to coast. This output state will remain until the reference speed is greater than the start ramp end speed set by SF2, at which point the start-up sequence is initiated and the motor is allowed to run. Once sensorless operation is achieved the motor speed will change to match the reference speed determined by the demand input. The speed then continues to match the demand without being affected by varying the steady-state supply voltage or load up to the torque limit. The torque limit is imposed by either the peak current limiter or effective applied voltage limited by the motor bemf.

Table 3: Speed Range and Resolution

SR	f_{RES} (Hz)	f_{MAX} (Hz)	Motor Pole-Pairs (Speed in rpm)				
			1	2	3	4	6
0	0.1	102.3	6138	3069	2046	1535	1023
1	0.2	204.6	12276	6138	4092	3069	2046
2	0.4	409.2	24552	12276	8184	6138	4092
3	0.8	819.4	49104	24552	16368	12276	8184
4	1.6	1636.8	98208	49104	32736	24552	16368
5	3.2	3273.6	–	98208	65472	49104	32736

As the reference speed reduces, the motor speed will follow until it is too low to maintain sensorless operation and the motor speed drops below the underspeed threshold set by the SL[3:0] variable. At this point, the A4964 will turn off all bridge MOSFETs, allowing the motor to coast. The LOS bit will be set to 1, indicating a loss of synchronization.

If a loss of synchronization occurs and RSC = 0, the bridge MOSFETs will remain in this state until demand input is set to 0 or the RUN bit is set to 0.

If a loss of synchronization occurs when the RUN = 1 and RSC = 1 and when the demand input sets the reference speed to greater than SF2, then the start sequencer resets and the start sequence is initiated. This cycle will continue until stopped by setting the demand input to zero or setting either the RUN bit or the RSC bit to 0.

When using closed-loop speed control, the A4964 will continue to provide current limiting using the internal fixed-frequency current limiter.

SPEED CONTROL DYNAMIC RESPONSE

The dynamic response of the speed controller can be tuned to the motor and load dynamics using three variables: SG[3:0], SGL[4:0], and DF.

The speed control loop operates as a sampled system where the sampling rate is the bridge PWM frequency. The bridge peak duty cycle is altered based on the value of the speed error and both are updated each bridge PWM period.

When the motor speed is close to the reference speed, the control loop response is determined by the gain factor set by the SG[3:0] variable. This gain multiplies the speed error—the difference between the motor speed and the reference speed—to increase

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or decrease the peak PWM duty cycle applied to the bridge. This causes the motor to accelerate or decelerate to minimize the speed error. The amount of acceleration or deceleration is therefore determined by the product of the speed error and the gain determined by SG. In general, the gain setting can be higher for low-inertia motor/load combinations with a high dynamic response and will be lower for high-inertia motor/load combinations with a low dynamic response.

When there is a large difference between the motor speed and the reference speed—for example, when a large step change in speed is required—the error will be large and this will cause a large change to the peak duty cycle applied to the bridge. If the speed change is from a low speed to a high speed, then the step change in the bridge PWM duty cycle will cause a large increase in current to provide the high acceleration torque to increase the speed of the motor. This sudden large increase in acceleration torque may cause an increase in audible noise or even some instability and speed overshoot. To avoid these undesirable outcomes, the maximum acceleration is limited by limiting the maximum speed error using the SGL[4:0] variable and SG[3:0] variable. This will limit the speed error value that used to determine the peak value of the bridge PWM and will in turn limit any step increase in the peak duty cycle and the resulting torque and acceleration. As for the gain setting variable, the error limit value can be higher for low-inertia motor/load combinations with a high dynamic response and will be lower for high-inertia motor/load combinations with a low dynamic response.

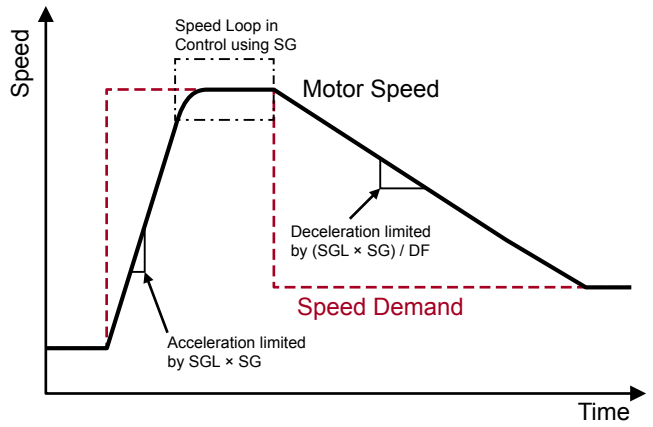

Figure 22: Speed Control Dynamic Response Limits

If the speed change is from a high speed to a low speed, then the resulting step change in the bridge PWM duty cycle will attempt to apply a large reverse current to provide the high deceleration torque to reduce the speed of the motor. As for the acceleration case, this sudden large increase in deceleration torque may cause an increase in audible noise, some instability and possibly speed undershoot. To avoid this, the maximum deceleration is also limited by limiting the maximum speed error using the SGL[4:0] variable and SG[3:0] variable. However, in addition to these common effects of speed change, deceleration produces an additional undesirable outcome. During deceleration, the current will flow in the reverse direction back to the bridge supply. This reverse current may cause an increase in the bridge voltage depending on the ability of the bridge supply to absorb the energy delivered by the current. If the energy cannot be absorbed either by the supply or by any capacitors connected to the supply then the voltage may reach dangerous levels. To limit this effect, the deceleration factor variable, DF[1:0], can be used to enforce a lower deceleration limit in proportion to the acceleration limit. The acceleration limit is determined by the value of SGL × SG, and the deceleration limit by (SGL × SG)/DF. In general, the deceleration factor setting can be set to 1 for low-inertia motor/load combinations and to a higher value for high-inertia motor/load combinations. In cases where the supply is capable of absorbing the motor energy from the reverse current, for example high performance battery powered systems or systems with large low impedance supply capacitors, the value of DF[1:0] can also be set to 1.

The effect of the acceleration and deceleration limits and dynamic limits are shown in Figure 22.

SUPPLY VOLTAGE COMPENSATION

Any change in the bridge supply voltage will change the relationship between applied duty cycle and resulting drive output.

The two closed-loop control modes of the A4964 will automatically compensate for these changes if the rate of change is less than the response time of the control loop. However, the rate of change is faster than the control loop response time, then there will be a transient disturbance in the motor speed or torque output.

To overcome these effects, the A4964 includes a duty cycle voltage compensation function for two nominal voltage levels, 12 V and 24 V. The nominal voltage is the bridge supply voltage at which the bridge duty cycle is unaltered. When the bridge supply voltage rises above the nominal voltage, then the bridge duty cycle is reduced in proportion. When the bridge supply voltage falls below the nominal voltage, then the bridge duty cycle is increased in proportion.

Supply voltage compensation is only applied to the open-loop and closed-loop speed modes, and operates continuously when enabled. For the closed-loop speed mode, this means that any transient disturbance in the motor speed, caused by the change

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in supply voltage, will be minimized. For the open-loop speed mode, it means that the duty cycle applied to the bridge will be continuously modulated to maintain the same effective voltage applied to the motor.

Supply voltage compensation is not required for the closed-loop current control mode. In this mode, the current is controlled on a PWM cycle-by-cycle basis and is therefore unaffected by any change in supply voltage.

The range of bridge supply voltage over which the duty cycle compensation is effective is limited in each case. For the 12 V nominal selection, the range is 7 V to 19 V. For the 24 V nominal selection, the range is 14 V to 38 V.

The function is enabled and the nominal voltage selected by the contents of the DV[1:0] variable. When DV[1:0] = [0,0], the duty cycle compensation feature is disabled.

When DV[1:0] = [0,1] or [1,1], the nominal voltage is 12 V.

When DV[1:0] = [1,0], the nominal voltage is 24 V.

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Diagnostics

Multiple diagnostic features provide fault monitoring for the basic chip status, for the state of the external bridge and for the motor control function. Most of the non-critical diagnostics can be masked by setting the appropriate bit in the mask register. The detectable faults are listed in table 5. The fault status is available through the serial interface or through the DIAG output. The serial output, SDO, can also be programmed to provide a divided version of the system clock that can be used for clock frequency verification or system calibration.

SERIAL STATUS REGISTER

The serial interface allows detailed diagnostic information to be read from the Status register at any time.

The first bit (bit 15) of the Status register contains a common fault flag, FF, which will be high if any of the fault bits in the registers have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low, the first bit in the Status register can be read to determine if a fault has been detected at any time since the last Status or Diagnostic register reset. In all cases, the fault bits in the diagnostic registers are latched and only cleared after the associated fault bit is read through the serial interface with DSR = 0.

DIAGNOSTIC REGISTER

The diagnostic register provides additional details of any VDS overvoltage or bootstrap undervoltage faults. It also provides an indication when the reported motor speed is above the maximum programmable level.

The status and diagnostic registers are described further in the serial interface section description below.

DIAG OUTPUT

DIAG is a battery-compliant open-drain pull-down output that provides the following four optional signals selected by the DGS[1:0] variable:

DGS = 0: An active-low fault flag which will be low when a fault is present or a fault state is latched.

DGS = 1: An FG speed signal providing a square wave at the electrical cycle frequency.

DGS = 2: Time-based pulses to differentiate the fault groups as described in table 5 below. DIAG will be inactive when no fault is present.

DGS = 3: Time-based pulses to differentiate the fault groups as described in table 5 below. DIAG will output the FG signal when no fault is present.

When operating in stand-alone mode and DGS = 0 or 2, DIAG can be externally connected directly to the LIN terminal or to the LTX input to superimpose the fault information onto the PWM input. When DGS = 2, the PWM input duty cycle detection will ignore the state of the PWM signal when DIAG is low and maintain the last detected demand input.

Further details on using the DIAG output for error reporting are provided in the applications section in this datasheet.

Table 4: DIAG Pulse Definition and Fault Allocation

		DGS[1:0]				
		00	01	10	11	
Fault Description	**Fault Group**	**DIAG Output**				**Priority**
No Fault	No Fault	H	FG	H	FG	–
Serial Error						
VBB POR						
Temperature Warning						
System Error	System	L	FG	L	L	5
VBB Undervoltage	Undervoltage	L	FG	L: 2.5 s / H: 1 s	L: 2.5 s / H: 1 s	4
VLR Undervoltage						
VREG Undervoltage						
Bootstrap Undervoltage						
Over Temperature	Temperature	L	FG	L: 2 s / H: 1 s	L: 2 s / H: 1 s	3
VDS Overvoltage	Short Detect	L	FG	L: 1 s / H: 1 s	L: 1 s / H: 1 s	2
Loss of Synchronization	Motor lock	L	FG	L: 1.5 s / H: 1 s	L: 1.5 s / H: 1 s	1

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DIAG FAULT WAVEFORMS

Table 5 lists the output signal on the DIAG terminal for each fault and each setting of DGS. The faults are grouped into six groups. When DGS = 0, the DIAG output will be low when any fault is present. When DGS = 1, the FG speed signal will be present on DIAG. The FG signal will remain high when the motor is stationary. When DGS = 2 or 3, the faults are reported in six groups. Each group has a unique timing combination of low (active pull-down) and high (passive pull-up). If a fault is present when DGS = 2 or 3, the fault groups will be identified by the length of time that the DIAG output will be low. Except in the case of a system error, the DIAG output will be high for 1 second between each identifying time, ranging from 1 second to 2.5 seconds. The fault groups are each assigned a priority from 1 (low) to 5 (high); when more than one fault is present, the highest priority fault is reported. If system error is present, the DIAG output will be held low.

FAULT ACTION

The action taken for each fault is listed in Table 5a, Table 5b, and appendix A. When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (stored) until reset. The faults that are latched are indicated in Table 5. Some latched fault states are reset with specific actions, but all fault states are always reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface with DSR = 0. Any fault bits that have been set in the diagnostic registers are only reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface with DSR = 0.

The fault conditions VBB POR (power-on-reset) and VREG undervoltage are considered critical to the safe operation of the A4964 and the system. If these faults are detected, then the gate drive outputs are automatically driven low and all MOSFETs in the bridge held in the off state. This state will remain until the fault is removed.

Table 5a: Fault Response Actions (ESF = 0, no faults masked)

Fault Description	Disable Outputs	RSC[7]	Fault State Latched	Other Action	Fault State Reset	Re-enable Outputs
No Fault	No	n/a	n/a	None	n/a	
System Error	Yes [1]	n/a	Yes	RUN = 0	POR, RUN = 1	
Serial Error	No	n/a	No	None	POR or SPI [3]	n/a
VBB POR	Yes [1]	n/a	No	Internal logic shutdown and reset	Condition removed	RUN = 1
VBB Undervoltage	No	0	Yes	None	Demand input = 0, RUN = 0 or SPI [3][4]	n/a
		1	No		Condition removed	
VLR Undervoltage	Yes [1]	0	Yes	MCU reset	First watchdog transition after 100 ms from MRSTn going high	Demand input reset [5], RUN reset [6], or SPI [3][4]
		1	Yes		First watchdog transition after 100 ms from MRSTn going high	
Watchdog Fault	Yes [1]	0	Yes	MCU reset	First watchdog transition after 100 ms from MRSTn going high	Demand input reset [5], RUN reset [6], or SPI [3][4]
		1	Yes		First watchdog transition after 100 ms from MRSTn going high	
VREG Undervoltage	Yes [1]	n/a	No	None	Condition removed	
Bootstrap Undervoltage	Yes [2]	n/a	No	None	PWM on	
Temperature Warning	No	n/a	No	None	Condition removed	n/a
Overtemperature	No	n/a	No	None	Condition removed	n/a
Loss of Synchronization	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No	Stop and restart	Condition removed	
VDS Overvoltage	Yes [2]	n/a	No	None	PWM on	

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only when DSR = 0.
[4] Serial read of Status or Diagnostic register.
[5] Set demand input = 0 then set demand input to a new operating value.
[6] Set RUN bit = 0 then set RUN bit = 1.
[7] Restart control bit.

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Table 5b: Fault Response Actions (ESF = 1, no faults masked)

Fault Description	Disable Outputs	RSC[7]	Fault State Latched	Other Action	Fault State Reset	Re-enable Outputs
No Fault	No	n/a	n/a	None	n/a	
System Error	Yes [1]	n/a	Yes	RUN = 0	POR, RUN = 1	
Serial Error	No	n/a	No	None	POR or SPI [3]	n/a
VBB POR	Yes [1]	n/a	No	Internal logic shutdown and reset	Condition removed	RUN = 1
VBB Undervoltage	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No		Condition removed	
VLR Undervoltage	Yes [1]	0	Yes	MCU reset	First watchdog transition after 100 ms from MRSTn going high	Demand input reset [5], RUN reset [6], or SPI [3][4]
		1	Yes		First watchdog transition after 100 ms from MRSTn going high	
Watchdog Fault	Yes [1]	0	Yes	MCU reset	First watchdog transition after 100 ms from MRSTn going high	Demand input reset [5], RUN reset [6] or SPI [3][4]
		1	Yes		First watchdog transition after 100 ms from MRSTn going high	
VREG Undervoltage	Yes [1]	n/a	No	None	Condition removed	
Bootstrap Undervoltage	Yes [1]	n/a	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
Temperature Warning	No	n/a	No	None	Condition removed	n/a
Overtemperature	Yes [1]	0	Yes	VLR regulator shutdown and MCU reset	First watchdog transition after 100 ms from MRSTn going high	Demand input reset [5], RUN reset [6], or SPI [3][4]
		1	Yes		First watchdog transition after 100 ms from MRSTn going high	
Loss of Synchronization	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No	Stop and restart	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
VDS Overvoltage	Yes [1]	n/a	Yes	None	SPI [3][4]	

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only when DSR = 0.
[4] Serial read of Status or Diagnostic register.
[5] Set demand input = 0 then set demand input to a new operating value.
[6] Set RUN bit = 0 then set RUN bit = 1.
[7] Restart control bit.

VBB undervoltage is not considered critical and the action taken depends on the state of the enable stop on fault bit, ESF. If a VBB undervoltage condition exists and ESF = 1, the gate drive outputs will be disabled and the motor will coast until the condition is removed. If the restart bit, RSC, is set to 1, then the motor will restart when the VBB undervoltage condition is removed. If RSC = 0, the motor will remain stationary until:

- Demand input is set to 0 and then set to a new operating value (demand input reset),
- RUN bit is set to 0 then RUN bit is set to 1 (RUN reset),
- Status register is read through the serial interface with DSR = 0, or
- Power-on-reset occurs.

The action taken when a short fault, bootstrap undervoltage, or overtemperature condition is detected is also determined by the state of ESF. When ESF = 1, any short fault condition, bootstrap undervoltage, or overtemperature condition will disable all the gate drive outputs and coast the motor. For short faults and bootstrap undervoltage, this fault state is latched and all gate drive outputs remain disabled until a demand input reset, a RUN bit reset, a serial read of the Diagnostic register with DSR = 0, or a power-on-reset occurs. For overtemperature fault conditions, the outputs will remain disabled until 10 ms after the condition is removed.

When ESF = 0, no action will be taken for an overtemperature condition. For any short fault or bootstrap undervoltage condition, only the MOSFET associated with the detected fault will be

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disabled. This fault state will be latched until the next PWM-on state for the associated phase. In some cases, this will allow the A4964 to continue to operate the motor in a reduced functional mode depending on the specific fault condition.

When a loss of synchronization is detected, all the gate drive outputs are disabled and the motor coasts. If the restart bit, RSC, is set to 1, the A4964 immediately goes into a startup sequence. If RSC = 0, the loss of synchronization fault state is latched and all gate drive outputs remain disabled until a demand input reset, a RUN bit reset, a serial read of the Status register with DSR = 0, or a power-on-reset occurs.

In all cases, any fault bits that have been set in the diagnostic registers are latched and only reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface with DSR = 0.

FAULT MASKS

Individual diagnostics, except POR and system error, can be disabled by setting the corresponding bit in the mask register. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, no fault flags or diagnostic bits will be set, and no fault actions will be taken. See the mask register definition for bit allocation.

Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

CHIP-LEVEL DIAGNOSTICS

Parameters, which are critical for safe operation of the A4964 and the external MOSFETs, are monitored. These include serial interface, chip temperature, minimum internal logic supply voltage, and the minimum motor supply voltage. Faults are latched in the Status or Diagnostic register when they occur and the register is only reset by a Status or Diagnostic register reset.

CHIP FAULT STATE: POWER-ON RESET

The supply to the logic sections of the A4964 is generated by an internal regulator from VBB and is monitored to ensure correct logical operation. The internal logic is guaranteed to operate with the voltage at the VBB terminal, V_{BB}, down to V_{BBR}. When V_{BB} drops below the V_{BBR} threshold, then the logical function of the A4964 cannot be guaranteed, all outputs will be immediately disabled and all the logic reset. The A4964 will enter a power-down state and all internal activity, other than the logic supply voltage monitor will be suspended.

When V_{BB} rises above the V_{BBR} threshold, the A4964 will exit the power down state, all serial control registers will be reset to their power-on state, and all fault states will be reset. The FF bit and the POR bit in the Status register will be set to one to indicate that a power-on-reset has taken place. In general, the VSU, VRU, and VLU bits may also be set following a power-on-reset as the regulators may not have reached their respective rising undervoltage thresholds until after the register reset is completed.

At power-up, the logic inputs and outputs will remain disabled until VLR rises above the rising undervoltage threshold, V_{LRON}. If the WD mask bit is saved as 0 in non-volatile EEPROM (NWM), the MRSTn output will remain low for 10 ms. If the WD mask bit is saved as 1 in NWM, the MRSTn output will remain low for 10 ms or until the first valid serial transfer (whichever occurs first). After the MRSTn output goes high, the gate drive outputs will be re-enabled as described in the Fault Action section.

The same power-on-reset sequence occurs for initial power-on or for a VBB “brown-out” where V_{BB} only drops below V_{BBR} momentarily.

CHIP FAULT STATE: OVERTEMPERATURE

Two temperature thresholds are provided. A hot warning and an overtemperature shutdown.

- If the chip temperature rises above the temperature warning threshold, T_{JW}, the thermal warning bit, TW, will be set in the Status register. No action will be taken by the A4964 when a thermal warning fault condition is present. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHys}, the fault condition is removed. The thermal warning bit, TW, remains latched in the Status register until reset.
- If the chip temperature rises above the over temperature threshold, T_{JF}, the over temperature bit, OT, will be set in the Status register.

If ESF = 1, all gate drive outputs will be disabled, the VLR regulator is shut down and MRSTn will go low. All A4964 functions other than the regulator remain active. When T_J drops by more than the overtemperature threshold ($T_J < T_{JF} - T_{JHyst}$), the regulator will remain shut down and MRSTn will remain low for 10 ms. After this timeout, MRSTn goes high and the regulator is re-enabled and attempts to restart. The overtemperature bit, OT, remains latched in the Status register until reset.

If ESF = 0, no circuitry will be disabled and action must be taken by the user to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more

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than the hysteresis value, T_{JFHys}, the fault condition is removed. The overtemperature bit, OT, remains latched in the Status register until reset.

CHIP FAULT STATE: VBB UNDERVOLTAGE

The VBB undervoltage monitor provides an indication that the main power supply has dropped below the desirable operating level. This monitor is provided as a system level function to indicate that the supply voltage has dropped to a voltage level where the motor may not be capable of providing full performance. When a VBB undervoltage state is present, the VSU bit in the Status register will be set, but the A4964 will still be capable of operating to the full specification.

A VBB undervoltage condition will be present when the voltage at the VBB terminal, V_{BB}, drops below the VBB undervoltage lockout threshold, V_{BBOFF}. The VBB undervoltage condition is removed when V_{BB} rises above the VBB undervoltage lockout threshold, V_{BBON}.

During a VBB undervoltage fault condition, if ESF = 1 all gate drive outputs will be disabled. When the fault condition is removed, the A4964 will enter the startup sequence if RSC = 1. If RSC = 0, the fault state will be latched and remain until the demand input is set to 0, the RUN bit is set to 0, the Status register is read with DSR = 0 or a power-on-reset occurs. If ESF = 0, no action will be taken. In all cases, the VSU bit remains set in the Status register until cleared.

The VBB undervoltage monitor and fault action can be disabled by setting the VSU bit in the mask register.

CHIP FAULT STATE: VREG UNDERVOLTAGE

The internal charge-pump regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the regulated voltage at the VREG terminal, V_{REG}, is sufficiently high before enabling any of the outputs.

If V_{REG} goes below the VREG undervoltage threshold, V_{ROFF}, the VREG undervoltage bit, VRU, will be set in the Status register, all gate drive outputs will go low, and the motor drive will coast. When V_{REG} rises above V_{RON}, the gate drive outputs are re-enabled. The VRU fault bit remains in the Status register until cleared.

The VREG undervoltage monitor circuit is active during power up. All gate drives will remain low until V_{REG} is greater than approximately 8 V. Note that this is sufficient to turn on standard threshold external power MOSFETs at a battery voltage as low as 5.5 V, but the on-resistance of the MOSFET may be higher than its specified maximum.

CHIP FAULT STATE: VLR UNDERVOLTAGE

The voltage at the VLR terminal, V_{LR}, is monitored to ensure that the supply for any external controller is high enough to permit correct operation of the controller. If V_{LR} drops below the falling undervoltage threshold, V_{LROFF}, the regulator undervoltage bit, VLU, will be set in the Status register, the MRSTn output will go low to reset the external microcontroller and all gate drive outputs will be disabled. When V_{LR} rises above the rising undervoltage threshold, V_{LRON}, the MRSTn output will remain low. After 10 ms the MRSTn output will go high and the watchdog timer will be reset. The watchdog timer will remain reset for 100 ms and during this time the WDOG input will be ignored. The A4964 will then attempt to restart the motor on the first watchdog transition if the RUN and RSC bits are set to 1, and the demand input is at a level where starting the motor is permitted. If the RSC bit is set to 0, the gate drive outputs will remain disabled until the first watchdog transition and a demand input reset, a RUN bit reset, a serial read of the Status register with DSR = 0, or a power-on-reset occurs. The VLU fault bit remains in the Status register until cleared.

CHIP FAULT STATE: VPP UNDERVOLTAGE

During a NVM write operation, the voltage at the VPP terminal, V_{PP}, is monitored to ensure that the programming supply remains high enough to ensure correct programming of the EEPROM memory cells. If V_{PP} drops below the programming undervoltage level, V_{PPUV}, during the save sequence, then the sequence will be terminated immediately and the FF and VPU bits will be set in the Status register. The SAV[1:0] bits will also indicate that the write was not successful. The VPU bit can only be set during a write sequence. For normal operation, the VPP undervoltage comparator is disabled.

CHIP FAULT STATE: SERIAL ERROR

The data transfer into the A4964 through the serial interface is monitored for two fault conditions: transfer length and parity. A transfer length fault is detected if there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK. A parity fault is detected if the total number of logic 1 states in the 16-bit transfer is an even number. In both cases, the write will be cancelled without writing data to the registers. In addition, the Status register will not be reset and the FF bit and SE bit will be set to indicate a data transfer error. No further action will be taken. The SE bit will remain in the Status register until the next successful serial write with DSR = 0 or a power-on reset occurs.

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CHIP FAULT STATE: SYSTEM ERROR

If the SE bit is 1 at the same time as the POR bit is 1, then this indicates that a fault was detected when reading the NVM and the user-defined states have not been loaded into the control and configuration registers. In this case, the control and configuration registers will contain the default states and the RUN bit will be set to 0 to prevent any attempt to activate the outputs. The SE bit will remain in the Status register until the next successful SPI write or a power-on reset occurs. This gives an external microcontroller the opportunity to write the user-defined bits to the registers and activate the drive.

If the A4964 is operating without an external microcontroller when system error is indicated, then it will be held in this state until the power is cycled off then on and another attempt is made to transfer the NVM contents into the registers.

MOTOR FAULT: LOSS OF SYNCHRONIZATION

The motor operation is controlled by a closed-loop position estimator system, so it does not have any direct, immediate means of determining whether the motor is synchronized to the rotating field generated by the A4964. A loss of synchronization can only be detected if the commutation controller attempts to drive the motor too fast (overspeed) or too slow (underspeed).

The underspeed (low-speed) threshold, f_{SL}, is defined as:

$$f_{SL} = 8 \times n \times f_{RES}\ (Hz)$$

where n is a positive integer defined by SL[3:0], f_{SL} is the underspeed threshold, and f_{RES} is the speed resolution defined by SR[2:0].

The overspeed (high speed) threshold, f_{SH}, is defined as:

$$f_{SH} = [127 + (n \times 128)] \times f_{RES}\ (Hz)$$

where n is a positive integer defined by SH[3:0], f_{SH} is the overspeed threshold, and f_{RES} is the speed resolution defined by SR[2:0].

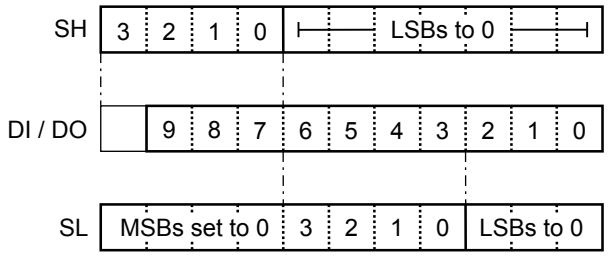

Figure 23: Over- and Underspeed versus Reference Speed

These thresholds must be set to a suitable level to provide appropriate overspeed and underspeed limits for all motor control modes.

The overspeed and underspeed thresholds are shown, in Figure 23, relative to the reference speed set by DI[9:0] and the actual speed reported by DO[9:0].

The four bits of the underspeed threhold variable, SL[3:0], have the same weighting as bits 6:3 of the reference speed variable DI.

The least significant 3 bits of the overspeed threhold variable, SH[3:0], have the same weighting as the most significant 3 bits of the reference speed variable DI. The most significant bit of SH has twice the weighting of the most significant bit of DI. Relative to the reference speed, the overspeed threshold variable can be considered as an 11-bit value where the most significant bits are set by SH[3:0] and the least significant 7 bits are set to 1.

The overspeed threshold can therefore be programmed between approximately 12% and 200% of the maximum reference speed and the underspeed threshold between 0% and 12.4% of the maximum reference speed.

If the commutation controller attempts to drive the motor at less than the underspeed threshold or greater than the overspeed threhold, then the A4964 will indicate loss of synchronization.

Note that the underspeed threshold, SL, should always be set to be lower than the minimum windmill frequency, f_{WMF}, defined by WMF[3:0]. If it is set higher, then any use of windmill start below the underspeed threshold but above the minimum windmill frequency will immediately indicate loss of synchronization.

In the extreme case when a motor stalls due to excessive load on the output, there will be no bemf zero crossing detection and the frequency of the commutation sequence will be reduced at each expected commutation point to try and regain synchronization. The resulting speed will eventually reduce below the underspeed threshold after a number of commutation cycles and the A4964 will set the LOS bit in the Status register to 1 and coast the motor.

In some cases, rather than a complete stall, it is also possible for the motor to vibrate at a whole fraction (subharmonic) of the commutation frequency produced by the controller. In this case, the controller will still detect the bemf zero crossing, but at a rate much higher than the motor is capable of running. The commutation controller will increase the commutation rate to compensate and the resulting speed will increase above the overspeed threshold and the A4964 will set the LOS bit in the Status register to 1 and coast the motor.

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When loss of synchronization is detected, the controller will either stop or attempt to restart the motor depending on the state of the RUN bit, the restart control bit, RSC, and the demand input.

If the RUN and RSC bits are set to 1, and the demand input is greater than the minimum limit for the motor to run in the selected motor control mode (see mode descriptions for details), then the start sequencer will reset and retry. This cycle will continue until stopped by taking the demand input to zero or setting either the RUN bit or the RSC bit to 0.

If the RSC bit is set to 0, the motor will continue to coast until a demand input reset, a RUN bit reset, a serial read of the Status register with DSR = 0, or a power-on-reset occurs.

The LOS bit will remain in the Status register until reset.

MOSFET FAULT DETECTION

Faults on any external MOSFETs are determined by measuring the drain-source voltage of the MOSFET and comparing it to the drain-source overvoltage threshold, V_{DST}, defined by the VT[5:0] variable. These bits provide the input to a 6-bit DAC with a least significant bit value of typically 50 mV. The output of the DAC produces V_{DST}, approximately defined as:

$$V_{DST} = n \times 50\ mV$$

where n is a positive integer defined by VT[5:0].

The drain-source voltage for any low-side MOSFET is measured between the GND terminal and the appropriate Sx terminal. Any low-side current sense voltage should be taken into account when setting the V_{DST} level.

The drain-source voltage for any high-side MOSFET is measured between the VBRG terminal and the appropriate Sx terminal. Using the VBRG terminal rather than VBB avoids adding any reverse diode voltage or high-side current sense voltage to the real high-side drain-source voltage and avoids false VDS fault detection.

The VBRG terminal is an independent low-current sense input to the top of the MOSFET bridge. It should be connected independently and directly to the common connection point for the drains of the power bridge MOSFETs at the positive supply connection point in the bridge. The input current to the VBRG terminal is proportional to the drain-source threshold voltage, V_{DST}, and is approximately:

$$I_{VBRG} = 72 \times V_{DST} + 52$$

where I_{VBRG} is the current into the VBRG terminal in µA and V_{DST} is the drain-source threshold voltage described above.

Note that the VBRG terminal can withstand a negative voltage up to –5 V. This allows the terminal to remain connected directly to the top of the power bridge during negative transients where the body diodes of the power MOSFETs are used to clamp the negative transient. The same applies to the more extreme case where the MOSFET body diodes are used to clamp a reverse battery connection.

MOSFET FAULT QUALIFICATION

The output from each VDS overvoltage comparator is filtered by a VDS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VDS fault. The duration of the VDS fault qualifying timer, t_{VDQ}, is determined by the contents of the VQT[5:0] variable as:

$$t_{VDQ} = n \times 50\ ns$$

where n is a positive integer defined by VQT[5:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In the default, debounce mode, a timer is started each time the comparator output indicates a VDS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the VDS fault is considered valid and the corresponding VDS fault bit, AH, AL, BH, BL, CH, or CL will be set in the Diagnostic register.

In the optional, blanking mode, a timer is started when a gate drive is turned on. All VDS overvoltage comparator outputs are ignored (blanked) for the duration of the timeout period, set by t_{VDQ}. If the comparator output indicates an overcurrent event when the MOSFET is switched on and the blanking timer is not active, then the VDS fault is considered valid and the corresponding VDS fault bit, AH, AL, BH, BL, CH, or CL will be set to 1 in the Diagnostic register.

If a valid VDS fault is detected when ESF = 1, then this fault condition will be latched and all external MOSFETs will be immediately switched off and disabled until the fault is reset.

If a valid VDS fault is detected when ESF = 0, then the external MOSFET where the fault is detected is immediately switched off by the A4964 but the remaining MOSFETs continue to operate. The MOSFET where the fault is detected will be switched on again the next time the internal bridge control switches it from off to on.

To limit any damage to the external MOSFETs, when ESF = 0,

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the A4964 should either be fully disabled by setting the demand input to 0 or by setting RUN to 0 through a serial write. Alternatively, setting the ESF bit to 1 will allow the A4964 to completely disable the MOSFETs as soon as a fault is detected. Any fault bits set to 1 in the Diagnostic register remain set until cleared.

BOOTSTRAP UNDERVOLTAGE FAULT

In addition to a monitor on VREG, the A4964 also monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. Before a high-side drive can be turned on, the bootstrap capacitor voltage must be higher than the turn-on voltage limit. If this is not the case, then the A4964 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances, this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active and if the voltage drops below the turn-off voltage, a charge cycle is also initiated. In either case, if there is a fault that prevents the bootstrap capacitor charging within typically 200 µs, then the charge cycle will timeout, a bootstrap undervoltage condition is detected, and the corresponding bootstrap undervoltage fault bit, BA, BB, or BC is set to 1 in the Diagnostic register.

If a bootstrap undervoltage condition is detected and ESF = 1, then all gate drive output will be disabled. In this case, the gate drive outputs will remain disabled and the bootstrap undervoltage fault state will be held until a demand input reset, a RUN bit reset, a serial read of the Diagnostic register with DSR = 0, or a power-on-reset occurs. When ESF = 0, only the high-side gate drive for the affected phase will be switched off and only for the remainder of the PWM period. At each PWM-on time, an attempt will be made to again turn on the high-side MOSFET.

Any fault bits set to 1 in the Diagnostic register remain set until cleared.

SYSTEM CLOCK VERIFICATION

The SDO output can be set to provide a logic-level square wave output at a ratio of the internal clock frequency to allow verification of the system clock frequency and more precise calibration of the timing settings if required.

When the CKS bit is set to 0, the SDO terminal operates as described in the serial interface description. When the CKS bit is set to 1, the SDO terminal will output the divided clock signal when STRn is held high. The division ratio, N_D, is defined in the electrical characteristics table.

When CKS = 1 and STRn is low, the serial interface will continue to accept data on SDI and output the normal serial data on SDO.

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SERIAL INTERFACE

Serial Registers Definition (default values shown below each input register bit)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: PWM config	0	0	0	0	0	WR	MOD		PMD	PW5	PW4	PW3	PW2	PW1	PW0	P
							0	0	0	1	0	0	1	1	0	
1: PWM config	0	0	0	0	1	WR	DP2	DP1	DP0	DD1	DD0	DS3	DS2	DS1	DS0	P
							0	0	0	0	0	0	0	0	0	
2: Bridge config	0	0	0	1	0	WR		SA1	SA0	DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	0	0	0	0	0	
3: Gate drive config	0	0	0	1	1	WR		IR13	IR12	IR11	IR10	IR23	IR22	IR21	IR20	P
							0	0	0	0	0	0	0	0	0	
4: Gate drive config	0	0	1	0	0	WR		IF13	IF12	IF11	IF10	IF23	IF22	IF21	IF20	P
							0	0	0	0	0	0	0	0	0	
5: Gate drive config	0	0	1	0	1	WR		TRS3	TRS2	TRS1	TRS0	TFS3	TFS2	TFS1	TFS0	P
							0	0	0	0	0	0	0	0	0	
6: Current limit	0	0	1	1	0	WR	OBT4	OBT3	OBT2	OBT1	OBT0	VIL3	VIL2	VIL1	VIL0	P
							0	0	1	1	1	1	1	1	1	
7: VDS monitor	0	0	1	1	1	WR	MIT1	MIT0		VT5	VT4	VT3	VT2	VT1	VT0	P
							0	0	0	0	1	1	1	1	1	
8: VDS monitor	0	1	0	0	0	WR		VDQ		VQT5	VQT4	VQT3	VQT2	VQT1	VQT0	P
							0	0	0	1	1	1	1	1	1	
9: Watchdog config	0	1	0	0	1	WR					WM4	WM3	WM2	WM1	WM0	P
							0	0	0	0	0	0	0	0	0	
10: Watchdog config	0	1	0	1	0	WR	WC3	WC2	WC1	WC0	WW4	WW3	WW2	WW1	WW0	P
							0	0	0	0	0	0	0	0	0	
11: Commutation	0	1	0	1	1	WR		CP3	CP2	CP1	CP0	CI3	CI2	CI1	CI0	P
							0	0	1	1	1	0	1	1	1	
12: Commutation	0	1	1	0	0	WR		CPT3	CPT2	CPT1	CPT0	CIT3	CIT2	CIT1	CIT0	P
							0	0	0	0	0	0	0	0	0	
13: BEMF config	0	1	1	0	1	WR					BW4	BW3	BW2	BW1	BW0	P
							0	0	0	0	0	0	1	0	0	
14: BEMF config	0	1	1	1	0	WR				BS1	BS0	BF3	BF2	BF1	BF0	P
							0	0	0	0	0	0	0	0	1	
15: Startup config	0	1	1	1	1	WR	HT3	HT2	HT1	HT0	HD4	HD3	HD2	HD1	HD0	P
							0	0	0	1	0	0	1	0	1	
16: Startup config	1	0	0	0	0	WR	STM	RSC		KM3	KM2	KM1	KM0	HR1	HR0	P
							0	0	0	0	1	1	1	0	0	

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Serial Registers Definition (default values shown below each input register bit)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
17: Startup config	1	0	0	0	1	WR		WIN	WMF2	WMF1	WMF0	WBD3	WBD2	WBD1	WBD0	P
							0	0	0	1	0	0	1	1	1	
18: Startup config	1	0	0	1	0	WR		SF23	SF22	SF21	SF20	SF13	SF12	SF11	SF10	P
							0	0	1	1	1	0	1	1	1	
19: Startup config	1	0	0	1	1	WR		SD23	SD22	SD21	SD20	SD13	SD12	SD11	SD10	P
							0	0	1	1	1	0	1	1	1	
20: Startup config	1	0	1	0	0	WR		STS3	STS2	STS1	STS0	SFS3	SFS2	SFS1	SFS0	P
							0	0	1	0	0	0	1	1	1	
21: Speed loop	1	0	1	0	1	WR	SGL4	SGL3	SGL2	SGL1	SGL0	SG3	SG2	SG1	SG0	P
							0	0	1	0	1	0	1	0	1	
22: Speed loop	1	0	1	1	0	WR	DV1	DV0	DF1	DF0			SR2	SR1	SR0	P
							0	1	0	0	0	0	0	0	0	
23: Speed loop	1	0	1	1	1	WR		SL3	SL2	SL1	SL0	SH3	SH2	SH1	SH0	P
							0	0	1	1	1	0	1	1	1	
24: NVM Write	1	1	0	0	0	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	
25: System	1	1	0	0	1	WR	ESF	VLR	VRG	OPM	LWK	IPI	DIL	CM1	CM0	P
							1	0	1	0	0	0	0	0	0	
26: Phase advance	1	1	0	1	0	WR	PAM	KIP1	KIP0	PA5	PA4	PA3	PA2	PA1	PA0	P
							0	0	0	0	0	0	0	0	0	
27: Motor function	1	1	0	1	1	WR		LEN	GTS	OVM1	OVM0	DRM	BRK	DIR	RUN	P
							0	0	0	0	0	0	0	0	0	
28: Mask	1	1	1	0	0	WR	WD	LOS	OT	TW	VSU	VRU	VLU	BU	VO	P
							1	0	0	0	0	0	0	0	0	
29: Readback Select	1	1	1	0	1	WR	DGS1	DGS0	DSR		LBR	CKS	RBS2	RBS1	RBS0	P
							0	0	0	0	0	0	0	0	0	
30: Write Only	1	1	1	1	0	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	P
						0	0	0	0	0	0	0	0	0	0	
31: Read Only	1	1	1	1	1	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	P
						0	0	0	0	0	0	0	0	0	0	
Status	FF	POR	SE	VPU	CLI		WD	LOS	OT	TW	VSU	VRU	VLU	BU	VO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

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A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the A4964. A fourth wire can be used to provide diagnostic feedback and readback of the register contents. The fourth wire can also be set to provide a logic-level square wave output at a ratio of the internal clock frequency as described in the Diagnostics section.

The serial interface provides full access to all the features of the A4964. In addition to full control of the motor activity and output demand, it also provides access to all control options and programmable parameters.

The serial interface timing requirements are specified in the electrical characteristics table and illustrated in Figure 2. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. The STRn terminal is normally held high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI, SCK, and SDO connections. Each slave then requires an independent STRn connection.

After 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the Status or Diagnostic registers are reset depending on the transfer.

Diagnostic information or the contents of the registers is output on the SDO terminal msb first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the Status register, is output as soon as STRn goes low.

The first five bits, D[15:11], in a serial word are the register address bits providing 32 addressable registers. In addition to these, there is a read-only Status register. Two of the addressable registers have special functions. Register address 30 is the write-only demand input register and accepts a 10-bit demand input. Register address 31 is the read-only measurement output register and provides a 10-bit integer output from the internal data acquisition system.

The remaining 30 registers provide configuration and control for the A4964. Each of these registers has a write bit, WR (bit 10), as the first bit after the register address. This bit must be set to one to write the subsequent bits into the selected register. If WR is zero, then the remaining data bits (bits 9 to 0) are ignored. For these registers, the state of the WR bit also determines the data output on SDO. If WR is set to one, then the Status register is output. If WR is set to zero, then the contents of the register selected by the first five bits on SDI is output.

In all cases, the first five bits output on SDO will always include the FF bit, the POR bit, the SE bit, and the VPU bit from the Status register.

The last bit in any serial transfer, D[0], is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. A parity fault is detected if the total number of logic 1 states in the 16-bit transfer is an even number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

If a parity fault is detected, or there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without latching data to the registers. In addition, the Status register will not be reset and the FF bit and SE bits will be set to indicate a data transfer error.

CONFIGURATION AND CONTROL REGISTERS

The serial data word is 16 bits, input msb first, the first five bits are defined as the register address. This provides 32 addressable registers, 30 of which are read/write, 1 is read only, and 1 write only. The registers are grouped as follows:

- PWM frequency and dither configuration
- Bridge dead time and MOSFET drive configuration
- Current limit configuration
- VDS monitor configuration
- Watchdog configuration
- Commutation and bemf configuration
- Start-up configuration
- Speed loop configuration
- System function configuration
- Motor function control
- Fault mask
- Readback select and readback
- Demand input

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Register 0: PWM:

- MOD, Selects 2-phase or 3-phase modulation.
- PMD, Selects the bridge PWM mode.
- PW[5:0], a 6-bit integer to set the PWM period.

Register 1: PWM dither:

- DP[2:0], 3 bits to select the dither step period.
- DD[1:0], 2 bits to select the dither dwell time.
- DS[3:0], 3-bit integer to select the dither steps.

Register 2: Bridge dead time:

- SA[1:0], 2-bit integer to set sense amp gain.
- DT[5:0], a 6-bit integer to set the dead time.

Register 3: Gate drive:

- IR1[3:0], 4 bits to set turn-on current 1.
- IR2[3:0], 4 bits to set turn-on current 2.

Register 4: Gate drive:

- IF1[3:0], 4 bits to set turn-off current 1.
- IRF2[3:0], 4 bits to set turn-off current 2.

Register 5: Gate drive:

- TRS[3:0], 4-bit integer to set turn-on time.
- TFS[3:0], 4-bit integer to set turn-off time.

Register 6: Current limit:

- OBT[4:0], 5-bit integer to set the current limit blank time.
- VIL[3:0], 4-bit integer to set the current limit scale.

Register 7: VDS & Current Sense:

- MIT[1:0], 2-bit integer to set sense amp maximum threshold.
- VT[5:0], 6-bit integer to set the VDS limit.

Register 8: VDS:

- VDQ, selects VDS qualifier mode.
- VQT[5:0], 6-bit integer to set the VDS qualifier time.

Register 9: Watchdog:

- WM[4:0], 5-bit integer to set the minimum watchdog time.

Register 10: Watchdog:

- WC[3:0], 4-bit integer to set watchdog cycle count.
- WW[4:0], 5-bit integer to set the watchdog window time.

Register 11: Commutation:

- CP[3:0], 4-bits to set the steady-state phase control proportional gain.
- CI[3:0], 4-bits to set the steady-state phase controller integral gain.

Register 12: Commutation:

- CPT[3:0], 4-bits to set the transient phase control proportional gain.
- CIT[3:0], 4-bits to set the transient phase controller integral gain.

Register 13: BEMF:

- BW[4:0], 5-bit integer to set the BEMF detect window.

Register 14: BEMF:

- BS[1:0], 2 bits to select the number of BEMF samples.
- BF[3:0], 4 bits to select the windmill BEMF filter time.

Register 15: Startup:

- HT[3:0], a 4-bit integer to set the time of the initial alignment.
- HD[3:0], a 4-bit integer to set the PWM duty cycle applied during the alignment time.

Register 16: Startup:

- STM, enables the coast function during startup.
- RSC, enables restart after loss of synchronization.
- KM[3:0], 4-bit integer to set the motor constant.
- HR[1:0], 2 bits to select the alignment duty cycle ramp time.

Register 17: Startup:

- WIN, enables windmill detection at start-up
- WMF[2:0], 3-bit integer to select the minimum windmill detection frequency.
- WBD[3:0], 4-bit integer to select windmill brake duty cycle.

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Register 18: Startup:

- SF2[3:0], a 4-bit integer to set final start frequency.
- SF1[3:0], a 4-bit integer to set initial start frequency.

Register 19: Startup:

- SD2[3:0], a 4-bit integer to set initial start PWM duty.
- SD1[3:0], a 4-bit integer to set final start PWM duty.

Register 20: Startup:

- STS[3:0], a 4-bit integer to set the start time step.
- SFS[3:0], a 4-bit integer to set the start frequency step.

Register 21: Speed control loop:

- SGL[5:0], a 5-bit integer to set the speed control loop acceleration limit.
- SG[3:0], a 4-bit integer to set the speed control loop proportional gain.

Register 22: Speed control loop:

- DV[1:0], 2 bits to select the voltage compensation level.
- DF[1:0], 2 bits to select the deceleration factor.
- SR[2:0], 3 bits to select the speed control resolution.

Register 23: Speed control loop:

- SL[3:0], 4 bits to select the underspeed threshold.
- SH[3:0], 4 bits to select the overspeed threshold.

Register 24: NVM:

- SAV[1:0], controls and reports saving the register contents to the NVM.

Register 25: System Functions:

- ESF, the enable stop on fault bit that defines the action taken when a fault is detected.
- VLR, selects logic regulator voltage.
- VRG, selects gate drive regulator voltage.
- OPM, selects the stand-alone operating mode.
- LWK, selects the wake-up mode.
- IPI, selects the sense of the PWM input.
- DIL, disables current limit for speed modes.
- CM[1:0], 2 bits to select the required control mode.

Register 26: Phase advance:

- PAM, selects the phase advance mode.
- KIP[1:0], sets the auto phase advance control gain.
- PA[5:0], a 6-bit integer to set the phase advance.

Register 27: Motor function:

- LEN, controls LIN standby/active state.
- GTS, initiates go-to-sleep function.
- OVM[1:0], selects overmodulation level.
- DRM, selects drive mode.
- BRK, brake control.
- DIR, direction control.
- RUN, enables the motor to start and run.

Register 28: Fault mask:

The Fault Mask Register contains a fault mask bit for each fault bit in the Status register other than FF, POR, and SE. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or diagnostic bits will be set.

Register 29: Readback select:

- DGS[1:0], 2 bits to select output on the DIAG terminal.
- DSR, disables reset on serial transfer.
- LBR, selects select LIN baud rate.
- CKS, selects divided system clock on SDO terminal.
- RBS[2:0], 3 bits to select the data that will be read from register 31.

Register 30 (Write only): Demand input:

- DI[9:0], 10-bit integer providing the demand input for the selected control mode.

Register 31 (Read only): Data acquisition:

- DO[9:0], 10 bits providing the internal monitor data selected by RBS[2:0].

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STATUS AND DIAGNOSTIC REGISTERS

There is one read-only Status register in addition to the 32 addressable registers. When any register transfer takes place, the first five bits output on SDO are always the most significant five bits of the Status register regardless of whether the addressed register is being read or written.

When register 31 is addressed, the remaining eleven bits on SDO are always the ten bits of the selected output plus a parity bit. For all other registers, the sixth bit will be zero and the content of the remaining ten bits will depend on the state of the WR bit input on SDI. When WR is 1, the addressed register will be written and the remaining ten bits output on SDO will be the least significant nine bits of the Status register followed by a parity bit. When WR is 0, the addressed register will be read and the remaining ten bits will be the contents of the addressed register followed by a parity bit.

The read-only Status register provides a summary of the chip, bridge, and motor status. The most significant three bits of the Status register indicate critical system faults. Bit 11 reports the state of the current control circuit. Bits 9 through 3 provide fault flags for specific individual diagnostic monitors, and bits 2 and 1 provide indicators for the contents of the Diagnostic register.

The Diagnostic register is an additional register that can be selected for readback through register 31. This register contains detailed information on bootstrap undervoltage faults and VDS overvoltage faults for each MOSFET in the bridge. If a bootstrap undervoltage is detected, then bit 2 of the Status register, BU, will be set and the specific phase can be determined by reading bits BA, BB, and BC in the Diagnostic register. If a VDS overvoltage is detected, then bit 1 of the Status register, VO, will be set and the specific MOSFET can be determined by reading bits AH, AL, BH, BL, CH, and CL in the Diagnostic register.

When selected for readback, the Diagnostic register contains an additional bit, OSR, in position DO9, which indicates if the actual motor speed is above the maximum speed reference level. OSR can be used as an additional most significant bit with the speed readback to double the range of the speed that can be reported. OSR will not set any bits in the status register and will be updated continuously by the speed monitor.

Whenever a fault occurs, the corresponding flag bit in the Status or Diagnostic register will be set to 1 and latched until reset. Resetting the Status or Diagnostic register only affects latched faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the register reset.

Except for the BU and VO bits, bits 2 and 1 respectively, the fault flags in the Status register are only reset to 0 on the completion of a serial read of the Status register or when a power-on-reset occurs. The BU and VO bits are reset to 0 when the corresponding fault flags in the Diagnostic register are reset. The fault flags in the Diagnostic register are only reset to 0 on the completion of a serial read of the Diagnostic register or when a power-on-reset occurs.

In some systems, it is preferable to be able to read the Status or Diagnostic register without causing a reset and allowing the A4964 to re-enable the outputs. The DSR (Disable Serial Reset) bit provides this functionality. When DSR is set to one, any valid read of any of the read-only registers will not result in that register being reset. When DSR = 0, any valid read of any of the read-only registers will reset the content of that register. This provides a way for the external controller to access the diagnostic information without automatically re-enabling any outputs, but retains a way to reset the faults under control of the controller.

The first most significant bit in the Status register, bit 15, is the status register flag, FF. This is high if any fault bits in the Status register are set. When STRn goes low to start a serial write, SDO comes out of its high-impedance state and outputs the serial register fault flag. This allows the main controller to poll the A4964 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state.

The second most significant bit in the Status register, bit 14, is the POR bit. At power-up or after a power-on-reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on-reset has taken place. All other diagnostic bits are reset and all other registers are returned to their default state. Note that a power-on-reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on-reset is not affected by the state of the V_{BB} supply voltage or V_{REG} regulator output voltage. In general, the VSU, VRU, and VLU bits may also be set following a power-on-reset as the regulators may not have reached their respective rising undervoltage thresholds until after the register reset is completed.

Bit 13 in the Status register is the SE bit. If the POR bit is 0, then the SE bit indicates if the previous serial transfer was not completed successfully. If SE is 1 when POR is 1, then this indicates that a fault was detected in the EEPROM and the user-defined values have not been loaded into the registers.

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READBACK REGISTER

The read-only readback register, register 31, provides access to six additional measurements plus the Diagnostic register described above. The measurement to be output on SDO when register 31 is addressed is selected by the RBS[2:0] variable as shown in Table 6:

Table 6: Read-Back Output Select

RBS	Register 31 Output
0	Diagnostic register
1	Motor speed
2	Average supply current
3	Supply voltage
4	Chip temperature
5	Demand input
6	Applied bridge peak duty cycle
7	Applied phase advance

The first five bits of the readback register are always the most significant five bits of the Status register. The 10-bit readback value is the next ten bits followed by a parity bit.

The motor speed measurement is relative to the speed resolution defined by SR[2:0] and therefore has the same range and resolution as the speed demand input through register 30. The motor speed is also available during windmill detection in the forward direction.

The motor speed, f_E,is defined as:

$$f_E = n \times f_{RES}\ (Hz)$$

where n is a positive integer defined by DO[9:0], f_{RES} is the speed resolution defined by SR[2:0], and f_E is the electrical cycle frequency of the controller.

The motor speed, ω_M, can be calculated from :

$$\omega_M = \frac{f_E \times 60}{N_{PP}}\ (rpm)$$

where ω_M is the motor speed in rpm, f_E is the electrical cycle frequency, and N_{PP} is the number of pole-pairs in the rotor.

This range can be extended by a factor of two by using the most significant bit of the diagnostic register, OSR, as bit 11 of the speed measurement. That is, when OSR = 1, the speed is defined as:

$$f_E = (n + 1024) \times f_{RES}\ (Hz)$$

The update period for the motor speed measurement can be calculated from:

$$t_{DO} = \frac{1}{S_{EMF} \times f_E}\ (ms)$$

where f_E is the electrical cycle frequency and S_{EMF} is the number of bemf samples per cycle.

The average supply current measurement is derived from the average output of the sense amplifier and represents the average supply current into the motor. The average current value, I_{SAVG}, is defined as:

$$I_{SAVG} = \frac{1.76 \times n}{A_V \times R_{SENSE}}\ (A)$$

where n is a positive integer defined by DO[9:0], R_{SENSE} is the sense resistor value in mΩ, A_V is the gain of the sense amplifier as defined by the SA variable.

The supply voltage measurement is a direct measurement of the V_{BRG} voltage with a resolution of 53 mV and a range of 54 V. The supply voltage, V_S, is defined as:

$$V_S = n \times 0.0528\ (V)$$

where n is a positive integer defined by DO[9:0].

Used together, the average supply current and the supply voltage measurements can provide a measurement of the average electrical power into the motor.

The chip junction temperature measurement is determined by the voltage of the internal temperature measurement diodes. The chip junction temperature, T_J, is defined as:

$$T_J = 367.7 - (n \times 0.451)\ (°C)$$

where n is a positive integer defined by DO[9:0].

The temperature measurement result range is –93°C to 367°C, but the useable measurement range is –50°C to 190°C.

The average supply current, supply voltage, and chip temperature measurements are updated every 2 ms.

The remaining three selections provide a readback capability for the variables that can be modified internally by the A4964.

The demand input can be written directly or can be derived from an input PWM duty cycle. The demand input readback simply provides the contents of DI[9:0] at the time of readback.

The applied bridge peak duty cycle output provides the peak value of the duty cycle as determined by the motor control algorithm. The bridge duty cycle, D_{BR}, is defined by:

$$D_{BR} = \frac{n}{1023}\ (\%)$$

where n is a positive integer defined by DO[9:0].

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The applied phase advance, θ_{ADV}, when PAM = 0 (manual) is defined by:

$$\theta_{ADV} = n \times 0.7^{\circ(elec)} \quad | n = 0..62$$

$$\theta_{ADV} = 60^{\circ(elec)} \quad | n = 63$$

where *n* is a positive integer defined by DO[9:0].

The applied phase advance, θ_{ADV}, when PAM = 1 (automatic) is defined by:

$$\theta_{ADV} = n \times 0.7^{\circ(elec)}$$

where *n* is a positive integer defined by DO[9:0].

The applied bridge peak duty cycle and applied phase advance measurements are updated each bridge PWM period, t_{PW}.

Non-Volatile Memory

The values in the configuration and control registers are held in non-volatile EEPROM (NVM), allowing the A4964 to be pre-programmed with different user-defined register values for each application, thus avoiding the need to program the register contents at each power on.

The A4964 provides a simple method to write the contents of the registers into the NVM using the serial interface. When the SAV[1:0] bits in register 24 are changed from [01] to [10], in a single serial write, the present contents of registers 0 to 23, 25 to 29, except register 27 bit 7, and bits [10:3] of register 30 (DI[9:2]) are saved (written to NVM) as a single operation. The save sequence takes typically 400 ms to complete. It is not possible to save single register values. Although the motor may be operating during the save sequence, it is recommended that the motor drive is disabled before starting a save sequence to avoid any corruption caused by the electrical noise or any faults from the motor.

Note that the GTS bit (register 27[7]) is not saved. This is to avoid a lockout condition where the A4964 is commanded to go to sleep as soon as the wake-up sequence is complete.

The register save sequence requires a programming voltage, V_{PP}, to be applied to the VBB terminal. V_{PP} must be present on the VBB terminal for a period of time, t_{PRS}, before the save sequence is started. V_{PP} must remain on VBB until the save sequence is completed.

During the save sequence, the SPI remains active for read only. Any attempt to write to the registers during the save sequence will cause the FF and SE bits to be set in the Status register.

During the save sequence, the A4964 will automatically complete all the necessary steps to ensure that the NVM is correctly programmed and will complete the sequence by verifying that the contents of the NVM have been securely programmed. On successful completion of a save sequence, the SAV[1:0] bits will be set to 01. Register 24 should be read to determine if the save has completed successfully. If SAV[1:0] is reset to 00, then the save sequence has been terminated and has not completed successfully.

If V_{PP} drops below the programming undervoltage level, V_{PPUV}, during the save sequence, then the sequence will be terminated immediately, the FF and VPU bits set in the Status register, and SAV[1:0] will be reset to 00.

To externally verify the data saved in the NVM, the V_{BB} supply must be cycled off then on to cause a power-on reset. Following a power-on reset, the contents of the NVM are copied to the serial registers which can then be read through the serial interface and verified.

For guaranteed data retention reliability, the NVM in the A4964 should be written no more than 1000 times.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: PWM config	0	0	0	0	0	WR	MOD		PMD	PW5	PW4	PW3	PW2	PW1	PW0	P
							0	0	0	1	0	0	1	1	0	
1: PWM config	0	0	0	0	1	WR	DP2	DP1	DP0	DD1	DD0	DS3	DS2	DS1	DS0	P
							0	0	0	0	0	0	0	0	0	
2: Bridge config	0	0	0	1	0	WR		SA1	SA0	DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	0	0	0	0	0	

Register 0: PWM Configuration

MOD Modulation Mode Select

MOD	Modulation Mode	Default
0	3-phase	D
1	2-phase	

PMD Bridge PWM Mode Select

PMD	PWM Mode	Default
0	Center aligned	D
1	Edge aligned	

PW[5:0] Bridge PWM Fixed Period

$$t_{PW} = 20.10\ \mu s + (n \times 0.8\ \mu s) \text{ when PMD} = 0$$
$$t_{PW} = 20.05\ \mu s + (n \times 0.8\ \mu s) \text{ when PMD} = 1$$

where n is a positive integer defined by PW[5:0],
e.g. when PW[5:0] = [10 0110] and PMD = 0
then t_{PW} = 50.5 µs.

The range of t_{PW} is 20.1 µs to 70.5 µs when PMD = 0 and 20.05 µs to 70.45 µs when PMD = 1.

This is equivalent to 50 kHz to 14.2 kHz.

Register 1: PWM Configuration

DP[2:0] PWM Dither Step Period

$$t_{\Delta PW} = -0.2\ \mu s - (n \times 0.2\ \mu s)$$

where n is a positive integer defined by DP[2:0],
e.g. when DP[2:0] = [101] then $t_{\Delta PW}$ = –1.2 µs.

The range of $t_{\Delta PW}$ is –0.2 µs to –1.6 µs.

Register 1: PWM Configuration (continued)

DD[1:0] PWM Dither Dwell Time

DD1	DD0	Dwell Time	Default
0	0	1 ms	D
0	1	2 ms	
1	0	5 ms	
1	1	10 ms	

DS[3:0] PWM Dither Step Count

The number of dither steps is directly defined by the integer value of DS[3:0],
e.g. when DS[3:0] = [0111] then there will be 7 frequency steps.

The maximum number of steps is 15.

Setting DS[3:0] to 0 will disable PWM dither.

Register 2: Bridge and Sense Amp Configuration

SA[1:0] Sense Amp Gain

SA1	SA0	Gain	Default
0	0	2.5	D
0	1	5	
1	0	10	
1	1	20	

DT[5:0] Dead Time

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0],
e.g. when DT[5:0] = [01 0100] then t_{DEAD} = 1 µs.

The range of t_{DEAD} is 100 ns to 3.15 µs. Selecting a value of 0, 1, or 2 will set the dead time to 100 ns.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3: Gate drive config	0	0	0	1	1	WR		IR13	IR12	IR11	IR10	IR23	IR22	IR21	IR20	P
							0	0	0	0	0	0	0	0	0	
4: Gate drive config	0	0	1	0	0	WR		IF13	IF12	IF11	IF10	IF23	IF22	IF21	IF20	P
							0	0	0	0	0	0	0	0	0	

Register 3: Gate Drive Configuration

IR1[3:0] Turn-On Current 1

$$I_{R1} = n \times -5\ mA$$

where n is a positive integer defined by IR1[3:0], e.g. when IR1[3:0] = [1000] then I_{R1} = –40 mA.

The range of I_{R1} is –5 mA to –75 mA.

Selecting a value of 0 will set the gate drive to switch mode to turn on the MOSFET as quickly as possible.

IR2[3:0] Turn-On Current 2

$$I_{R2} = n \times -5\ mA$$

where n is a positive integer defined by IR2[3:0], e.g. when IR2[3:0] = [0010] then I_{R2} = –10 mA.

The range of I_{R2} is –5 mA to –75 mA.

Selecting a value of 0 will set the gate drive to switch mode to turn on the MOSFET as quickly as possible.

Register 4: Gate Drive Configuration

IF1[3:0] Turn-Off Current 1

$$I_{F1} = n \times 5\ mA$$

where n is a positive integer defined by IF1[3:0], e.g. when IF1[3:0] = [1100] then I_{F1} = 60 mA.

The range of I_{F1} is 5 mA to 75 mA.

Selecting a value of 0 will set the gate drive to switch mode to turn off the MOSFET as quickly as possible.

IF2[3:0] Turn-Off Current 2

$$I_{F2} = n \times 5\ mA$$

where n is a positive integer defined by IF2[3:0], e.g. when IF2[3:0] = [0011] then I_{F2} = 15 mA.

The range of I_{F2} is 5 mA to 75 mA.

Selecting a value of 0 will set the gate drive to switch mode to turn off the MOSFET as quickly as possible.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5: Gate drive config	0	0	1	0	1	WR		TRS3	TRS2	TRS1	TRS0	TFS3	TFS2	TFS1	TFS0	P
							0	0	0	0	0	0	0	0	0	
6: Current limit config	0	0	1	1	0	WR	OBT4	OBT3	OBT2	OBT1	OBT0	VIL3	VIL2	VIL1	VIL0	P
							0	0	1	1	1	1	1	1	1	

Register 5: Gate Drive Configuration

TRS[3:0] Slew Control Turn-On Time

$$t_{RS} = n \times 50\ ns$$

where n is a positive integer defined by TRS[3:0], e.g. when TRS[3:0] = [0110] then t_{RS} = 300 ns.

The range of t_{RS} is 0 ns to 750 ns.

TFS[3:0] Slew Control Turn-Off Time

$$t_{FS} = n \times 50\ ns$$

where n is a positive integer defined by TFS[3:0], e.g. when TFS[3:0] = [1100] then t_{FS} = 600 ns.

The range of t_{FS} is 0 ns to 750 ns.

Register 6: Current Limit Configuration

OBT[4:0] Current Limit Blank Time

$$t_{OCB} = (n + 2) \times 200\ ns$$

where n is a positive integer defined by OBT[4:0], e.g. when OBT[4:0] = [1 0000] then t_{OCB} = 3.6 µs.

The range of t_{OCB} is 1 µs to 6.6 µs.

Setting a value of OBT = 0, 1, 2, and 3 will set the blank time to 1 µs.

VIL[3:0] Current Limit Scale

V_{ILIM} defined by Scale × Maximum Threshold:

VIL3	VIL2	VIL1	VIL0	Scale	Default
0	0	0	0	1/16	
0	0	0	1	2/16	
0	0	1	0	3/16	
0	0	1	1	4/16	
0	1	0	0	5/16	
0	1	0	1	6/16	
0	1	1	0	7/16	
0	1	1	1	8/16	
1	0	0	0	9/16	
1	0	0	1	10/16	
1	0	1	0	11/16	
1	0	1	1	12/16	
1	1	0	0	13/16	
1	1	0	1	14/16	
1	1	1	0	15/16	
1	1	1	1	16/16	D

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7: VDS monitor	0	0	1	1	1	WR	MIT1	MIT0		VT5	VT4	VT3	VT2	VT1	VT0	P
							0	0	0	0	1	1	1	1	1	
8: VDS monitor	0	1	0	0	0	WR		VDQ		VQT5	VQT4	VQT3	VQT2	VQT1	VQT0	P
							0	0	0	1	1	1	1	1	1	
9: Watchdog config	0	1	0	0	1	WR					WM4	WM3	WM2	WM1	WM0	P
							0	0	0	0	0	0	0	0	0	
10: Watchdog config	0	1	0	1	0	WR	WC3	WC2	WC1	WC0	WW4	WW3	WW2	WW1	WW0	P
							0	0	0	0	0	0	0	0	0	

Register 7: VDS Monitor and Sense Amp Configuration

MIT[1:0] Sense Amp Maximum Threshold

MIT1	MIT0	Maximum Threshold	Default
0	0	200 mV	D
0	1	100 mV	
1	0	50 mV	
1	1	25 mV	

VT[5:0] VDS Overvoltage Threshold

$$V_{DST} = n \times 50\ mV$$

where n is a positive integer defined by VT[5:0],
e.g. when VT[5:0] = [01 1000] then V_{DST} = 1.2 V

The range of V_{DST} is 0 to 3.15 V.

Register 8: VDS Monitor Configuration

VDQ VDS Fault Qualifier Mode

VDQ	VDS Fault Qualifier	Default
0	Debounce	D
1	Blank	

VQT[5:0] VDS Qualify Time

$$t_{VDQ} = n \times 50\ ns$$

where n is a positive integer defined by VQT[5:0],
e.g. when VQT[5:0] = [01 1000] then t_{VDQ} = 1.2 µs.

The useable range of t_{VDQ} is 600 ns to 3.15 µs.

Setting a value of VQT = 0 may result in false VDS under-voltage fault detection.

Register 9: Watchdog Configuration

WM[4:0] Watchdog Minimum Time

$$t_{WM} = 1 + (n \times 2)\ ms$$

where n is a positive integer defined by WM[4:0],
e.g. when WM[4:0] = [0 1010] then t_{WM} = 21 ms.

The range of t_{WM} is 1 ms to 63 ms.

Register 10: Watchdog Configuration

WC[3:0] Watchdog Fail Cycle Count Before Sleep

$$C_{WC} = n \quad | \ n > 0$$

where n is a positive integer defined by WC[4:0],
e.g. when WC[3:0] = [1010] then C_{WC} = 10.

The range of C_{WC} is 1 to 15.

Setting WC[3:0] to [0000] disables the watchdog cycle counter.

WW[4:0] Watchdog Window Time

$$t_{WW} = 10 + (n \times 10)\ ms$$

where n is a positive integer defined by WW[4:0],
e.g. when WW[4:0] = [0 1010] then t_{WW} = 110 ms.

The range of t_{WW} is 10 ms to 320 ms.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11: Commutation	0	1	0	1	1	WR		CP3	CP2	CP1	CP0	CI3	CI2	CI1	CI0	P
							0	0	1	1	1	0	1	1	1	
12: Commutation	0	1	1	0	0	WR		CPT3	CPT2	CPT1	CPT0	CIT3	CIT2	CIT1	CIT0	P
							0	0	0	0	0	0	0	0	0	

Register 11: Commutation Configuration

CP[3:0] Steady-State Commutation Controller Proportional Gain

Position control proportional gain is K_{CP} defined as:

$$K_{CP} = 2^{(n-7)}$$

where *n* is a positive integer defined by CP[3:0], e.g., when CP[3:0] = [1000] then $K_{CP} = 2$.

The range of K_{CP} is 1/128 to 256.

CI[3:0] Steady-State Commutation Controller Integral Gain

Position control proportional gain is K_{CI} defined as:

$$K_{CI} = 2^{(n-7)}$$

where *n* is a positive integer defined by CI[3:0], e.g., when CI[3:0] = [1000] then $K_{CI} = 2$.

The range of K_{CI} is 1/128 to 256.

Register 12: Commutation Configuration

CPT[3:0] Transient Commutation Controller Proportional Gain

Position control proportional gain is K_{CP} defined as:

$$K_{CP} = 2^{(n-7)}$$

where *n* is a positive integer defined by CP[3:0], e.g., when CP[3:0] = [1000] then $K_{CP} = 2$.

The range of K_{CP} is 1/128 to 256.

CIT[3:0] Transient Commutation Controller Integral Gain

Position control proportional gain is K_{CI} defined as:

$$K_{CI} = 2^{(n-7)}$$

where *n* is a positive integer defined by CI[3:0], e.g., when CI[3:0] = [1000] then $K_{CI} = 2$.

The range of K_{CI} is 1/128 to 256.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
13: BEMF config	0	1	1	0	1	WR					BW4	BW3	BW2	BW1	BW0	P
							0	0	0	0	0	0	1	0	0	
14: BEMF config	0	1	1	1	0	WR				BS1	BS0	BF3	BF2	BF1	BF0	P
							0	0	0	0	0	0	0	0	1	

Register 13: BEMF Configuration

BW[4:0] BEMF Detection Window

For values up to 30, the window is defined as:

$$\theta_{BW} = (n + 1) \times 1.4^{\circ(elec)} \quad |n=0..30$$

$$\theta_{BW} = 60^{\circ(elec)} \quad |n=31$$

where n is a positive integer defined by BW[4:0], e.g. when BW[4:0] = [0 1010] then $\theta_{BW} = 15.4^{\circ(elec)}$.

The range of θ_{BW} is 1.4° to 43.4° and 60°.

Note: all angles refer to the electrical cycle.

Register 14: BEMF Configuration

BS[1:0] BEMF Sampling

BS1	BS0	Samples per Cycle	Default
0	0	1	D
0	1	2	
1	0	3	
1	1	6	

BF[3:0] Windmill BEMF Filter Time

t_{BF} defined by:

BF3	BF2	BF1	BF0	Filter Time	Default
0	0	0	0	0	
0	0	0	1	200 µs	D
0	0	1	0	400 µs	
0	0	1	1	600 µs	
0	1	0	0	800 µs	
0	1	0	1	1 ms	
0	1	1	0	2 ms	
0	1	1	1	4 ms	
1	0	0	0	5 ms	
1	0	0	1	6 ms	
1	0	1	0	10 ms	
1	0	1	1	12 ms	
1	1	0	0	14 ms	
1	1	0	1	16 ms	
1	1	1	0	18 ms	
1	1	1	1	20 ms	

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15: Startup config	0	1	1	1	1	WR	HT3	HT2	HT1	HT0	HD4	HD3	HD2	HD1	HD0	P
							0	0	0	1	0	0	1	0	1	
16: Startup config	1	0	0	0	0	WR	STM	RSC		KM3	KM2	KM1	KM0	HR1	HR0	P
							0	0	0	0	1	1	1	0	0	

Register 15: Startup Configuration

HT[3:0] Alignment (Hold) Time

$$t_{HOLD} = n \times 200\ ms$$

where n is a positive integer defined by HT[3:0], e.g. when HT[3:0] = [0010] then t_{HOLD} = 400 ms.

The range of t_{HOLD} is 0 to 3 s.

HD[4:0] Peak PWM Duty During Alignment

$$D_H = (n + 1) \times 3.125\%$$

where n is a positive integer defined by HD[3:0], e.g. when HQ[3:0] = [0101] then D_H = 18.75%.

The range of D_H is 3.125% to 100%.

Register 16: Startup Configuration

STM Start Coast Mode Select

STM	Start Coast Mode	Default
0	Coast disabled	D
1	Coast enabled	

RSC Restart Control

RSC	Restart Mode	Default
0	No restart	D
1	Allow restart after loss of sync	

KM[3:0] Motor Constant (Ratio Between Speed and BEMF)

$$K_M = 0.3 + (n \times 0.05)$$

where n is a positive integer defined by KM[3:0], e.g. when KM[3:0] = [0110] then K_M = 0.6.

The range of K_M is 0.3 to 1.05.

HR[1:0] Alignment Duty Cycle Ramp Time

HR1	HR0	Time to reach peak D	Default
0	0	0	D
0	1	25% t_{HOLD}	
1	0	50% t_{HOLD}	
1	1	100% t_{HOLD}	

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
17: Startup config	1	0	0	0	1	WR		WIN	WMF2	WMF1	WMF0	WBD3	WBD2	WBD1	WBD0	P
							0	0	0	1	0	0	1	1	1	
18: Startup config	1	0	0	1	0	WR		SF23	SF22	SF21	SF20	SF13	SF12	SF11	SF10	P
							0	0	1	1	1	0	1	1	1	

Register 17: Startup Configuration

WIN Windmill Mode Select

WIN	Windmill Mode	Default
0	Windmilling disabled	D
1	Windmilling enabled	

WMF[2:0] Minimum Windmill Detection Frequency

$$f_{WM} = 0.4 + (n \times 3.2)\ Hz$$

where *n* is a positive integer defined by WMF[3:0], e.g. when WMF[2:0] = [010] then f_{WM} = 6.8 Hz.

The range of f_{WM} is 0.4 Hz to 22.8 Hz.

WBD[3:0] Duty Cycle During Windmill Braking

$$D_{WB} = (n + 1) \times 6.25\%$$

where *n* is a positive integer defined by WBD[3:0], e.g. when WBD[3:0] = [0111] then D_{WB} = 50%

The range of D_{WB} is 6.25% to 100%.

Register 18: Startup Configuration

SF2[3:0] Start Ramp Final Frequency

$$f_{S2} = 10 + (n \times 2.5)\ Hz$$

where *n* is a positive integer defined by SF2[3:0], e.g. when SF2[3:0] = [0111] then f_{S2} = 27.5 Hz.

The range of f_{S2} is 10 Hz to 47.5 Hz.

SF1[3:0] Start Ramp Initial Frequency

$$f_{S1} = 0.5 + (n \times 0.5)\ Hz$$

where *n* is a positive integer defined by SF1[3:0], e.g. when SF1[3:0] = [0111] then f_{S1} = 4 Hz.

The range of f_{S1} is 0.5 Hz to 8 Hz.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
19: Startup config	1	0	0	1	1	WR		SD23	SD22	SD21	SD20	SD13	SD12	SD11	SD10	P
							0	0	1	1	1	0	1	1	1	
20: Startup config	1	0	1	0	0	WR		STS3	STS2	STS1	STS0	SFS3	SFS2	SFS1	SFS0	P
							0	0	1	0	0	0	1	1	1	

Register 19: Startup Configuration

SD2[3:0] Start Ramp Final Duty Cycle

$$D_{S2} = (n + 1) \times 6.25\%$$

where n is a positive integer defined by SD2[3:0], e.g. when SD2[3:0] = [0111] then D_{S2} = 50%.

The range of D_{S2} is 6.25% to 100%.

SD1[3:0] Start Ramp Initial Duty Cycle

$$D_{S1} = (n + 1) \times 6.25\%$$

where n is a positive integer defined by SD1[3:0], e.g. when SD1[3:0] = [0100] then D_{S1} = 31.25%

The range of D_{S1} is 6.25% to 100%.

Register 20: Startup Configuration

STS[3:0] Start Ramp Step Time

$$t_{SS} = 10\ ms \quad |n=0$$

$$t_{SS} = n \times 20\ ms \quad |n=1..15$$

where n is a positive integer defined by STS[3:0], e.g. when STS[3:0] = [0100] then t_{STS} = 80 ms.

The range of t_{STS} is 10 ms to 300 ms.

SFS[3:0] Start Ramp Frequency Step

f_{SS} defined by:

SFS3	SFS 2	SFS 1	SFS 0	Frequency Step	Default
0	0	0	0	0.0125 Hz	
0	0	0	1	0.025 Hz	
0	0	1	0	0.05 Hz	
0	0	1	1	0.1 Hz	
0	1	0	0	0.2 Hz	
0	1	0	1	0.4 Hz	
0	1	1	0	0.8 Hz	
0	1	1	1	1 Hz	D
1	0	0	0	1.5 Hz	
1	0	0	1	2 Hz	
1	0	1	0	2.5 Hz	
1	0	1	1	3 Hz	
1	1	0	0	5 Hz	
1	1	0	1	8 Hz	
1	1	1	0	10 Hz	
1	1	1	1	15 Hz	

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
21: Speed loop	1	0	1	0	1	WR	SGL4	SGL3	SGL2	SGL1	SGL0	SG3	SG2	SG1	SG0	P
							0	0	1	0	1	0	1	0	1	
22: Speed loop	1	0	1	1	0	WR	DV1	DV0	DF1	DF0			SR2	SR1	SR0	P
							0	1	0	0	0	0	0	0	0	
23: Speed loop	1	0	1	1	1	WR		SL3	SL2	SL1	SL0	SH3	SH2	SH1	SH0	P
							0	0	1	1	1	0	1	1	1	

Register 21: Speed Control Loop Configuration

SGL[4:0] Speed Control Acceleration Limit

$$K_{SL} = 6.3 + (n \times 6.4)\ Hz$$

where n is a positive integer defined by SGL[4:0], e.g. when SGL[4:0] = [0 0111] then K_{SL} = 51.5 Hz.

The range of K_{SL} is 6.3 Hz to 204.7 Hz.

SG[3:0] Speed Control Gain

$$K_S = 1 + (n \times 2)$$

where n is a positive integer defined by SG[3:0], e.g., when SG[3:0] = [1000] then K_S = 9.

The range of K_S is 1 to 31.

Register 22: Speed Control Loop Configuration

DV[1:0] Duty Cycle Compensation

DV1	DV0	Nominal supply voltage	Default
0	0	Disabled	
0	1	12 V	D
1	0	24 V	
1	1	12 V	

DF[1:0] Deceleration Factor

DF1	DF0	Deceleration factor	Default
0	0	1	D
0	1	2	
1	0	5	
1	1	10	

Register 22: Speed Control Loop Configuration (continued)

SR[2:0] Speed Control Resolution

SR2	SR1	SR0	Speed Resolution	Default
0	0	0	0.1 Hz	D
0	0	1	0.2 Hz	
0	1	0	0.4 Hz	
0	1	1	0.8 Hz	
1	0	0	1.6 Hz	
1	0	1	3.2 Hz	
1	1	0	3.2 Hz	
1	1	1	3.2 Hz	

Register 23: Speed Control Loop Configuration

SL[3:0] Underspeed (Low-Speed) Threshold

$$f_{SL} = 8 \times n \times f_{RES}\ (Hz)$$

where n is a positive integer defined by SL[3:0],
f_{SL} is the underspeed threshold, and
f_{RES} is the speed resolution defined by SR[2:0].

SH[3:0] Underspeed (High-Speed) Threshold

$$f_{SH} = [127 + (n \times 128)] \times f_{RES}\ (Hz)$$

where n is a positive integer defined by SH[3:0],
f_{SH} is the underspeed threshold, and
f_{RES} is the speed resolution defined by SR[2:0].

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24: NVM Write	1	1	0	0	0	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	
25: System	1	1	0	0	1	WR	ESF	VLR	VRG	OPM	LWK	IPI	DIL	CM1	CM0	P
							1	0	1	0	0	0	0	0	0	

Register 24: Write NVM Control

SAV[1:0] Save Parameters to Non-Volatile Memory (NVM)

When SAV[1:0] is changed from 01 to 10, the present contents of registers 0 to 23, 25 to 29, and bits [10:3] of register 30 (DI[9:2]) will be written to NVM.

When the NVM save has completed successfully, SAV[1:0] will be set to 01 and can be read to verify completion of the write. If SAV[1:0] is reset to 00, the save has not completed successfully.

Register 25: System Configuration

ESF Enable Stop On Fail Select

ESF	Stop on Fail	Default
0	No stop on fail	
1	Stop on fail	D

VLR Logic Regulator Voltage

VLR	Logic Regulator Voltage	Default
0	3.3 V	D
1	5 V	

VRG Gate Drive Regulator Voltage

VRG	Gate Drive Regulator Voltage	Default
0	8 V	
1	11 V	D

Register 25: System Configuration (continued)

OPM Operating Mode Select

OPM	Operating Mode	Default
0	SPI only	D
1	Stand-alone with SPI	

LWK Wake Mode Select

LWK	Wake Mode	Default
0	PWM Wake Mode	D
1	LIN Wake Mode	

IPI PWM Input Sense (when OPM = 1)

IPI	PWM Sense	Default
0	True, Active high	D
1	Inverted, Active low	

DIL Disable Current Limit (Speed Modes)

DIL	Current Limit	Default
0	Enabled	D
1	Disabled	

CM[1:0] Selects Motor Control Mode

CM1	CM0	Motor Control Mode	Default
0	0	Closed-loop speed	D
0	1	Closed-loop speed	
1	0	Closed-loop current	
1	1	Open-loop speed	

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
26: Phase advance	1	1	0	1	0	WR	PAM	KIP1	KIP0	PA5	PA4	PA3	PA2	PA1	PA0	P
							0	0	0	0	0	0	0	0	0	
27: Motor function	1	1	0	1	1	WR		LEN	GTS	OVM1	OVM0	DRM	BRK	DIR	RUN	P
							0	0	0	0	0	0	0	0	0	

Register 26: Phase Advance Select

PAM Phase Advance Mode

PAM	Phase Advance Mode	Default
0	Manual	D
1	Automatic	

KIP[1:0] Auto Phase Advance Control Gain

KIP1	KIP0	Gain	Default
0	0	1	D
0	1	2	
1	0	4	
1	1	8	

PA[5:0] Phase Advance

$$\theta_{ADV} = n \times 0.7^{\circ(elec)} \quad |n=0..62$$

$$\theta_{ADV} = 60^{\circ(elec)} \quad |n=63$$

where n is a positive integer defined by PA[5:0], e.g. when PA[5:0] = [00 1000] then $\theta_{ADV} = 5.6°$.

The range of θ_{ADV} is 0 to 43.4° and 60°.

Note: All angles refer to the electrical cycle.

Register 27: Motor Function Control

LEN Lin Enable

LEN	LIN State	Default
0	Standby	D
1	Active	

Register 27: Motor Function Control (continued)

GTS Go to Sleep Command

GTS	Sleep transition	Default
0	No change in state	D
1	No change in state	
1 → 0	No change in state	
0 → 1	Enter sleep state if enabled	

OVM[1:0] Overmodulation Select

OVM1	OVM0	Overmodulation	Default
0	0	None (100%)	D
0	1	112.5%	
1	0	125%	
1	1	150%	

DRM Drive Mode Select

DRM	Drive mode	Default
0	Sinusoidal	D
1	Trapezoidal	

BRK Brake Function Select

BRK	Brake Mode	Default
0	Brake disabled	D
1	Brake enabled	

DIR Rotation Direction Select

DIR	Direction	Default
0	Forward (Figure 6, Figure 7, and Table 1)	D
1	Reverse (Figure 6, Figure 7, and Table 1)	

RUN Run enable

RUN	Motor running status	Default
0	Disable outputs, coast motor	D
1	Start and run motor	

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
28: Mask	1	1	1	0	0	WR	WD	LOS	OT	TW	VSU	VRU	VLU	BU	VO	P
							1	0	0	0	0	0	0	0	0	
Status	FF	POR	SE	VPU	CLI		WD	LOS	OT	TW	VSU	VRU	VLU	BU	VO	P
							0	0	0	0	0	0	0	0	0	

Register 28: Mask Register

WD Watchdog
LOS Loss of bemf synchronization
OT Overtemperature
TW Temperature warning
VSU VBB undervoltage
VRU VREG undervoltage
VLU VLR undervoltage
BU Bootstrap undervoltage
VO VDS overvoltage

xx	Fault Mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

Status Register

FF Status register flag (not including CLI)
POR Power-on-reset
SE Serial transfer error
VPU VPP undervoltage
CLI Current limit*
WD Watchdog
LOS Loss of bemf synchronization
OT Overtemperature
TW Temperature warning
VSU VBB undervoltage
VRU VREG undervoltage
VLU VLR undervoltage
BU Bootstrap undervoltage
VO VDS fault

xx	Fault
0	No fault detected
1	Fault detected

*The state of the CLI bit is not reported by the Status register flag. CLI reporting is described in the Current Limit section

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
29: Readback Select	1	1	1	0	1	WR	DGS1	DGS0	DSR		LBR	CKS	RBS2	RBS1	RBS0	P
							0	0	0	0	0	0	0	0	0	

Register 29: Readback Select

DGS[1:0] Selects output DIAG terminal.

DGS1	DGS0	DIAG Output	Default
0	0	Active low fault flag	D
0	1	FG; high when motor is stationary	
1	0	Pulse output; high when no fault present	
1	1	Pulse output; FG when no fault present	

DSR Serial reset of fault state and fault bit

DSR	Reset on serial read	Default
0	Enabled	D
1	Disabled	

LBR Selects LIN baud rate

LBR	LIN Baud Rate	Default
0	10 kHz	D
1	20 kHz	

CKS Selects output on SDO when STRn = 1

CKS	SDO Output (STRn = 1)	Default
0	High impedance	D
1	Divided system clock	

Register 29: Readback Select (continued)

RBS[2:0] Selects data output on register 31

RBS2	RBS1	RBS0	Register 31 contents	Default
0	0	0	Diagnostic register	D
0	0	1	Motor speed	
0	1	0	Average supply current	
0	1	1	Supply voltage	
1	0	0	Chip temperature	
1	0	1	Demand input	
1	1	0	Applied bridge peak duty cycle	
1	1	1	Applied phase advance	

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
30: Write Only	1	1	1	1	0	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	P
						0	0	0	0	0	0	0	0	0	0	

Register 30: Demand input (Write Only)

DI[9:0] (CM=0,1) Speed Reference

$$f_{REF} = n \times f_{RES}\ (Hz)$$

where n is a positive integer defined by DI[9:0],
f_{REF} is the reference speed for the control loop,
f_{RES} is the speed resolution defined by SR[2:0].

DI[9:0] (CM=2) Current Limit

$$V_{LIM} = \frac{n \text{ OR } 0h01F}{1023} \cdot V_{MIT}$$

where n is a positive integer defined by DI[9:0],
(note: n is logically OR'd with 0h01F to restrict selection to the most significant 5 bits), and
V_{MIT} is the maximum threshold voltage of the sense amplifier as defined by the MIT variable.

DI[9:0] (CM=3) Bridge PWM Duty Cycle

$$D_{PK} = \frac{n}{1023}\%$$

where n is a positive integer defined by DI[9:0], and
D_{PK} is the bridge peak duty cycle.

In sinusoidal drive mode, D_{PK} is modulated by the sine generator to produce the actual bridge PWM duty cycle for each PWM period.

In trapezoidal drive mode, D_{PK} is the duty cycle applied to the bridge.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31: Read Only	1	1	1	1	1	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	P
						0	0	0	0	0	0	0	0	0	0	

Register 31: Readback Register (Read Only)

Bits 15 - 13

FF Status register flag

POR Power-on-reset

SE Serial transfer error

The contents of DO[9:0] are selected by the RBS[2:0] variable as follows:

DO[9:0] (RBS=0) Diagnostic register

DO9	OSR	Over speed range
DO8	BA	Bootstrap fault detected on Phase A high-side
DO7	BB	Bootstrap fault detected on Phase B high-side
DO6	BC	Bootstrap fault detected on Phase C high-side
DO5	AH	VDS fault detected on Phase A high-side
DO4	AL	VDS fault detected on Phase A low-side
DO3	BH	VDS fault detected on Phase B high-side
DO2	BL	VDS fault detected on Phase B low-side
DO1	CH	VDS fault detected on Phase C high-side
DO0	CL	VDS fault detected on Phase C low-side

xx	Fault
0	No fault detected
1	Fault detected

D0[9:0] (RBS=1) Motor Speed

$$f_E = n \times f_{RES}\ (Hz)$$

where n is a positive integer defined by DO[9:0],
f_{RES} is the speed resolution defined by SR[2:0], and
f_E is the electrical cycle frequency of the controller.

The motor speed can be calculated from:

$$\omega_M = \frac{f_E \times 60}{N_{PP}}\ (rpm)$$

where ω_M is the motor speed in rpm,
f_E is the electrical cycle frequency, and
N_{PP} is the number of pole-pairs in the rotor.

Register 31: Readback Register (Read Only) (continued)

DO[9:0] (RBS=1) Motor Speed (continued)

The OSR bit can be used as an additional 11th bit with twice the significance of bit DO9.

The motor speed is also available during windmill detection in the forward direction.

DO[9:0] (RBS=2) Average Supply Current

$$I_{SAVG} = 1.76 \times \frac{n}{A_V \times R_{SENSE}}\ (A)$$

where n is a positive integer defined by DO[9:0],
R_{SENSE} is the sense resistor value in mΩ, and
A_V is the gain of the sense amplifier as defined by the SA variable.

DO[9:0] (RBS=3) Supply Voltage

$$V_S = n \times 0.0528\ (V)$$

where n is a positive integer defined by by DO[9:0].

The measurement range is 0 to 50.4 V.

DO[9:0] (RBS=4) Chip Temperature

$$T_J = 367.7 - (n \times 0.451)\ (°C)$$

where n is a positive integer defined by by DO[9:0].

The result range is –93°C to 367°C, but the useable measurement range is –50°C to 190°C.

DO[9:0] (RBS=5) Demand Input

Readback contents of DI[9:0].

DO[9:0] (RBS=6) Applied Bridge Peak Duty Cycle

$$D_{BR} = \frac{n}{1023}\ (\%)$$

where n is a positive integer defined by DO[9:0].

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Register 31: Readback Register (Read Only) (continued)

DO[9:0] Applied Phase Advance
(RBS=7)

The applied phase advance, θ_{ADV}, when PAM = 0 (manual) is defined by:

$$\theta_{ADV} = n \times 0.7^{\circ(elec)} \quad | n = 0..62$$

$$\theta_{ADV} = 60^{\circ(elec)} \quad | n = 63$$

where n is a positive integer defined by DO[9:0].

The applied phase advance, θ_{ADV}, when PAM = 1 (automatic) is defined by:

$$\theta_{ADV} = n \times 0.7^{\circ(elec)}$$

where n is a positive integer defined by DO[9:0].

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APPLICATIONS INFORMATION

Dead Time Selection

The choice of power MOSFET and external series gate resistance determines the selection of the dead time. The dead time, t_{DEAD}, should be made long enough to ensure that one MOSFET has stopped conducting before the complementary MOSFET starts conducting. This should also account for the tolerance and variation of the MOSFET gate capacitance, the series gate resistance and the on-resistance of the driver in the A4964.

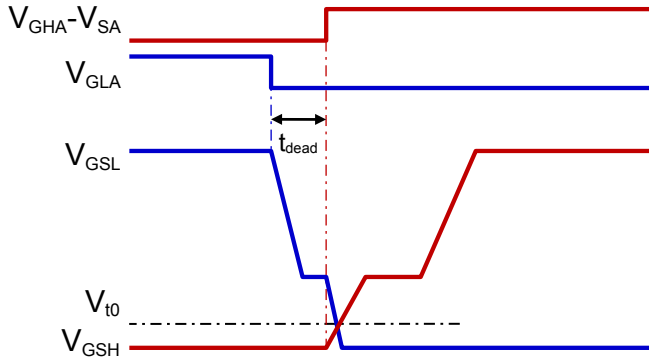

Figure 24: Minimum Dead Time

Figure 24 shows the typical switching characteristics of a pair of complementary MOSFETs. Ideally, one MOSFET should start to turn on just after the other has completely turned off. The point at which a MOSFET starts to conduct is the threshold voltage V_{t0}. The dead time should be long enough to ensure that the gate-source voltage of the MOSFET that is switching off is just below V_{t0} before the gate-source voltage of the MOSFET that is switching on rises to V_{t0}. This will be the minimum theoretical dead time, but in practice the dead time will have to be longer than this to accommodate variations in MOSFET and driver parameters for process variations and over temperature.

Bootstrap Capacitor Selection

The A4964 requires three bootstrap capacitors: CA, CB, and CC. To simplify this description of the bootstrap capacitor selection criteria, generic naming is used here. So, for example, C_{BOOT}, Q_{BOOT}, and V_{BOOT} refer to any of the three capacitors, and Q_{GATE} refers to any of the six associated MOSFETs. C_{BOOT} must be correctly selected to ensure proper operation of the device: too large and time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and PWM frequency; too small and there can be a large voltage drop at the time the charge is transferred from C_{BOOT} to the MOSFET gate.

To keep the voltage drop due to charge sharing small, the charge in the bootstrap capacitor, Q_{BOOT}, should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} \gg Q_{GATE}$$

A factor of 20 is a reasonable value.

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

$$C_{BOOT} = (Q_{GATE} \times 20) / V_{BOOT}$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET is being turned on can be approximated by:

$$\Delta V = Q_{GATE} / C_{BOOT}$$

so for a factor of 20, ΔV will be 5% of V_{BOOT}.

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG} max. However, in some circumstances the voltage may transiently reach a maximum of 18 V, which is the clamp voltage of the Zener diode between the Cx terminal and the Sx terminal. In most applications, with a good ceramic capacitor the working voltage can be limited to 16 V.

Bootstrap Charging

It is good practice to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE}, in µs, is approximated by:

$$t_{CHARGE} = (C_{BOOT} \times \Delta V) / I_{DBOOT}$$

where C_{BOOT} is the value of the bootstrap capacitor in nF, ΔV is the required voltage of the bootstrap capacitor, and I_{DBOOT} is the bootstrap diode current limit, typically 500 mA.

At power up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, ΔV can be considered to be the full high-side drive voltage. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the Sx terminal is pulled low and current flows from C_{REG}, the capacitor connected to the VREG terminal through the internal bootstrap diode circuit to C_{BOOT}.

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VREG Capacitor Selection

The internal reference, V_{REG}, supplies current for the low-side gate-drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate-drive circuit will provide the high transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator but must be supplied by an external capacitor, C_{REG}, connected between the VREG terminal and GND.

The turn-on current for the high-side MOSFET is similar in value but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from C_{REG} through the VREG terminal. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn-on occurs. This means that the value of C_{REG} between VREG and GND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge. For block commutation control (trapezoidal drive),where only one high-side and one low-side are switching during each PWM period, a minimum value of 20 × C_{BOOT} is reasonable. For sinusoidal control schemes, a minimum value of 40 × C_{BOOT} is recommended.

As the maximum working voltage of C_{REG} will never exceed V_{REG}, the part's voltage rating can be as low as 15 V. However, it is recommended that a capacitor rated to at least twice the maximum working voltage should be used to reduce any impact operating voltage may have on capacitance value. For best performance, C_{REG} should be ceramic rather than electrolytic. If the required value of C_{REG} is too large for a single ceramic capacitor, then a low ESR electrolytic capacitor may be used, with a ceramic capacitor greater than 100 nF in parallel to provide the initial current peak. C_{REG} should be mounted as close to the VREG terminal as possible.

Braking

In the A4964, setting the BRK bit to 1 when RUN = 1 will enable dynamic braking by forcing all low-side MOSFETs on and all high-side MOSFETs off. This will effectively short-circuit the back-emf of the motor, creating a braking torque. During braking, the load current, I_{BRAKE}, can be approximated by:

$$I_{BRAKE} = V_{BEMF} / R_L$$

where V_{BEMF} is the voltage generated by the motor and R_L is the resistance of the phase winding. Care must be taken during braking to ensure that the power MOSFETs' maximum ratings are not exceeded. Dynamic braking is equivalent to slow decay with synchronous rectification and all phases enabled.

The A4964 can also be used to perform regenerative braking. This is equivalent to using fast decay with synchronous rectification. Note that the supply must be capable of managing the reverse current, for example, by connecting a resistive load or dumping the current to a battery or capacitor.

Current Sense Amplifier

The output of the sense amplifier takes two paths. One path is to a comparator to set the current limit, and the other is to a filter an analog-to-digital converter (ADC) to provide a digital average current measurement.

The current limit comparator operates on the output of the sense amplifier. This output is compared to current limit threshold voltage, V_{ILIM}, to indicate to the PWM control circuit when the bridge current is greater than the current limit threshold.

The value of V_{ILIM} can be set in two ways, depending on the motor control method selected.

When either of the speed control modes are selected, the value of V_{ILIM} is determined by:

$$V_{ILIM} = V_{MIT} \times V_{ISC}$$

where V_{MIT} is the maximum threshold of the sense amplifier as defined by the MIT variable, and V_{ISC} is the current limit scale as defined by the VIL variable.

When the closed-loop current control mode is selected, V_{ILIM} is determined by demand input. This sets the required value of V_{ILIM} as a ratio of the maximum threshold (V_{MIT}). For example, when the demand input is 256 and V_{MIT} is 200 mV, then V_{ILIM} will be 50 mV. In this mode, only the 5 most significant bits of the 10-bit demand input are used to set the value of V_{ILIM}.

The relationship between the threshold voltage and the threshold current is defined as:

$$I_{LIM} = V_{ILIM} / R_{SENSE}$$

where R_{SENSE} is the value of the sense resistor.

As the average current filter and ADC also operates on the output of the sense amplifier, the average current value calculation is also dependent on the sense resistor value, and the amplifier gain

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and is defined as:

$$I_{SAVG} = 1.76 \times \frac{n}{A_V \times R_{SENSE}} \text{ (A)}$$

where n is a positive integer defined by DO[9:0], R_{SENSE} is the sense resistor value in mΩ, and A_V is the gain of the sense amplifier as defined by the SA variable.

Single-Wire PWM Diagnostic Feedback

When operating in LIN mode, the diagnostic information will usually be transmitted to the ECU (central electronic control unit) through the LIN protocol message. When operating in single-wire PWM mode, any diagnostic or error information can be transmitted to the ECU by pulling the incoming PWM signal line to a low level. The PWM source at the ECU must be a passive (resistor) pull-up with active pull-down for this to be possible. The specific method employed for this function will depend on the source of the error information and the requirements of the PWM interface to the ECU.

Systems with Negative Voltage Requirements

In systems where the PWM input must be able to withstand a significant negative voltage with respect to ground, then the circuit used to pull down the PWM signal must include reverse voltage protection. In these cases, the pull-down output of the LIN terminal on the A4964 can be used to pull the PWM input down to the LIN dominant output voltage level. The PWM source in the ECU must be able to recognize this level (max 2 V) as a valid low level on the PWM signal, indicating and error feedback signal is present.

The pull-down output of the LIN terminal on the A4964 is controlled by the LTX input. When the LTX input is low, the LIN output pull-down will be active. When LTX is high, the LIN output pull-down will be off.

The LTX input can be driven directly by the DIAG output when the A4964 is used without an external MCU, as shown in Figure 25c. In this case, the internal pull-up in the LTX input will provide the logic high level input. If a faster response is required, this pull-up resistor can be supplemented by an external pull-up resistor connected to the logic regulator output, VLR.

Alternatively, when an external MCU is used to manage the interface to the ECU, a logic output from the MCU can be used to drive the LTX input directly, as shown in Figure 25a.

Systems with Low-Level Input Requirements

In systems where the PWM input does not require negative voltage protection and the ECU requires a lower voltage level on the PWM signal before an error feedback is recognized, then the pull-down on the PWM signal can be driven directly by the DIAG output, as shown in Figure 25d, or by an additional pull-down transistor, as shown in Figure 25b.

The DIAG output is capable of sinking 4 mA at an output voltage of 0.4 V. To ensure the output low level on the DIAG output does not exceed the maximum voltage, the total pull-up resistance connected to the PSM signal node must have a high enough value to ensure that the current into the DIAG output does not exceed 4 mA during normal operation. For example, if the maximum bus voltage during operation is 16 V, then the resistance must be greater than 3.9 kΩ. If the bus must operate at 28 V, then then the resistance must be greater than 6.9 kΩ. The DIAG output is also capable of surviving a voltage up to 50 V without damage and so will not be damaged should the PWM signal reach these levels during a load-dump event.

As described above, for the case where the DIAG output is used, any additional external pull-down transistor must also be capable of pulling the PWM signal to the required level and may also have to survive any load-dump voltage on the PWM signal.

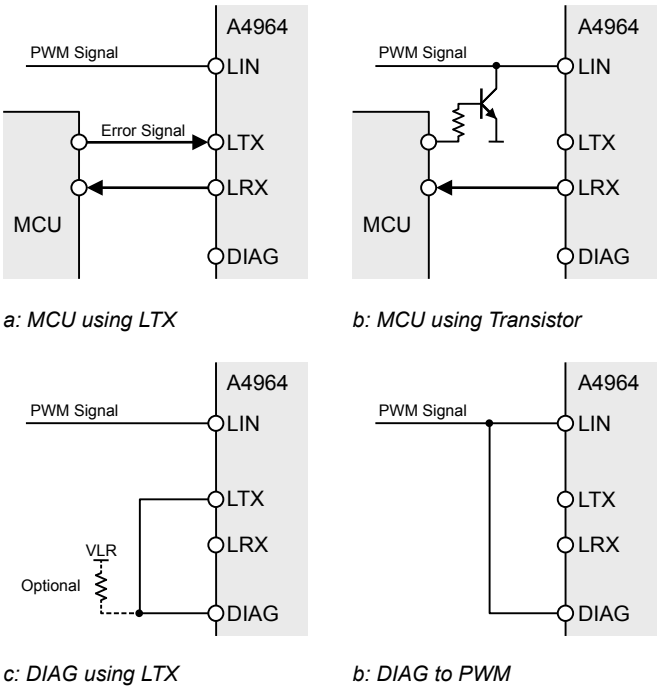

Figure 25: Error Signal Feedback Options

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LAYOUT RECOMMENDATIONS

Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits:

- The two ground terminals of the QFN (EV) package, both designated GND, are internally connected, but must also be connected together on the PCB close to the device for correct operation. This common point should return separately to the negative side of the motor supply filtering capacitor. This will minimize the effect of switching noise on the device logic and analog reference.
- The ground terminal of the QFP (JP) package should return separately to the negative side of the motor supply filtering capacitor.
- The exposed thermal pad should be connected to the GND terminals.
- Minimize stray inductance by using short, wide copper tracks at the drain and source terminals of all power MOSFETs and the input power bus. Particular care should be taken around the common source of the low-side power MOSFETs and the sense resistor. This will minimize voltages induced by fast switching of large load currents.
- Consider the addition of small (100 nF) ceramic decoupling capacitors across the source and drain of the power MOSFETs to limit fast transient voltage spikes caused by track inductance.
- Keep the gate discharge return connections Sx as short as possible. Any inductance on these tracks will cause negative transitions on the corresponding A4964 terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to the GND terminals.
- Decoupling for the supply should be provided by typically a 10 µF low ESR electrolytic capacitor and 100 nF ceramic capacitor in parallel. These should be connected between VBB and GND. The ceramic capacitor in particular should be mounted as close to the A4964 terminals as possible.
- The VREG capacitor should be connected between VREG and GND as close to the A4964 terminals as possible. For larger values of capacitance, a low ESR electrolytic capacitor may be used with a ceramic capacitor greater than 100 nF in parallel. In this case, the ceramic capacitor in particular should be mounted as close to the A4964 terminals as possible.
- The bootstrap capacitors should be mounted close to the associated terminals of the A4964.
- Gate charge drive paths and gate discharge return paths may carry a large transient current pulse. Therefore, the traces from GHx, GLx, and Sx (x = A, B or C) should be as short and wide as possible to reduce the track inductance.
- The inputs to the sense amplifier, CSP and CSM, should take the form of independent tracks directly to the terminals of the sense resistor, and for best results should be matched in length and route.
- A low-cost diode can be placed in the connection to VBB to provide reverse battery protection. In reverse battery conditions, it is possible to use the body diodes of the power MOSFETs to clamp the reverse voltage to approximately 4 V. In this case, the additional diode in the VBB connection will prevent damage to the A4964 and the VBRG input will survive the reverse voltage.

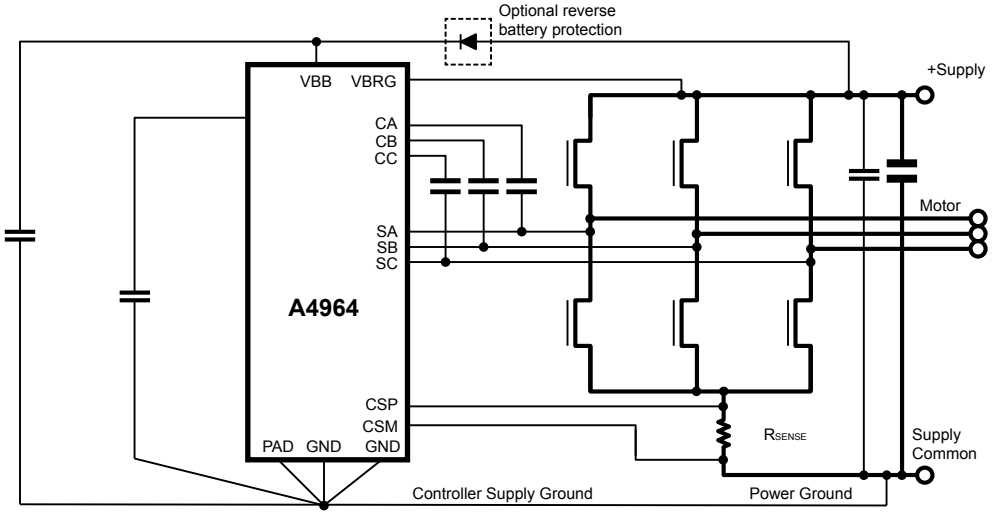

Figure 26: Supply Routing Suggestions

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INPUT / OUTPUT STRUCTURES

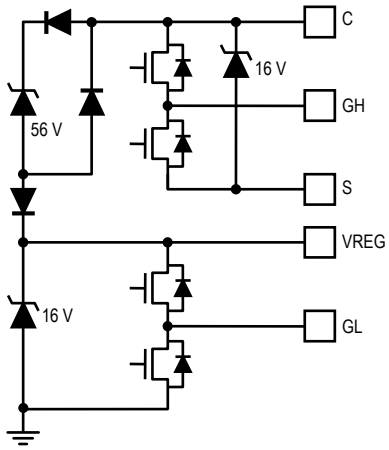

Figure 27a: Gate Drive Outputs

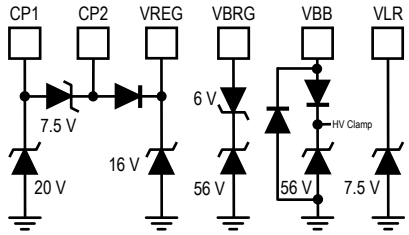

Figure 27b: Supplies

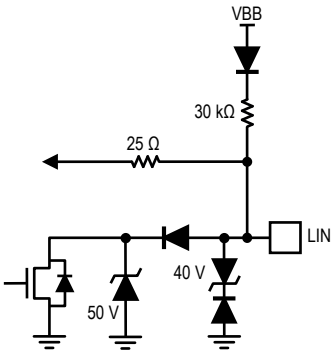

Figure 27c: LIN Bus I/O

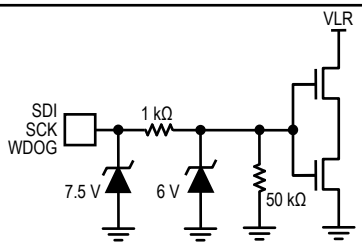

Figure 27d: Logic Inputs with Pull-Down

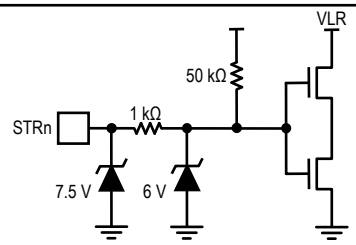

Figure 27e: Logic Inputs with Pull-Up

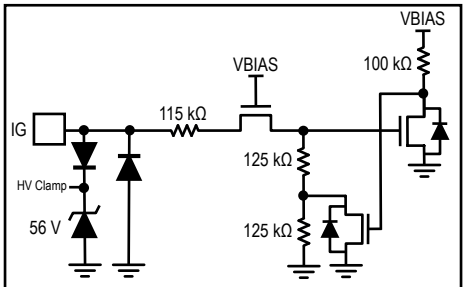

Figure 27f: HV Compliant Logic Inputs

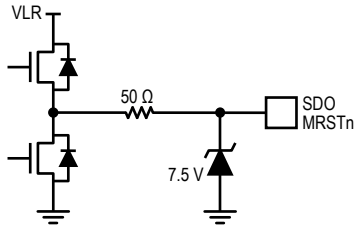

Figure 27g: Logic Output

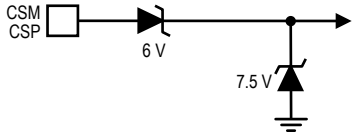

Figure 27h: Current Sense Amp Inputs

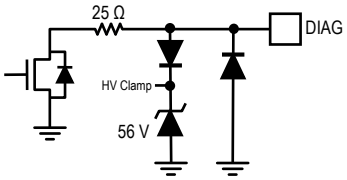

Figure 27i: HV Compliant Output

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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBAHD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

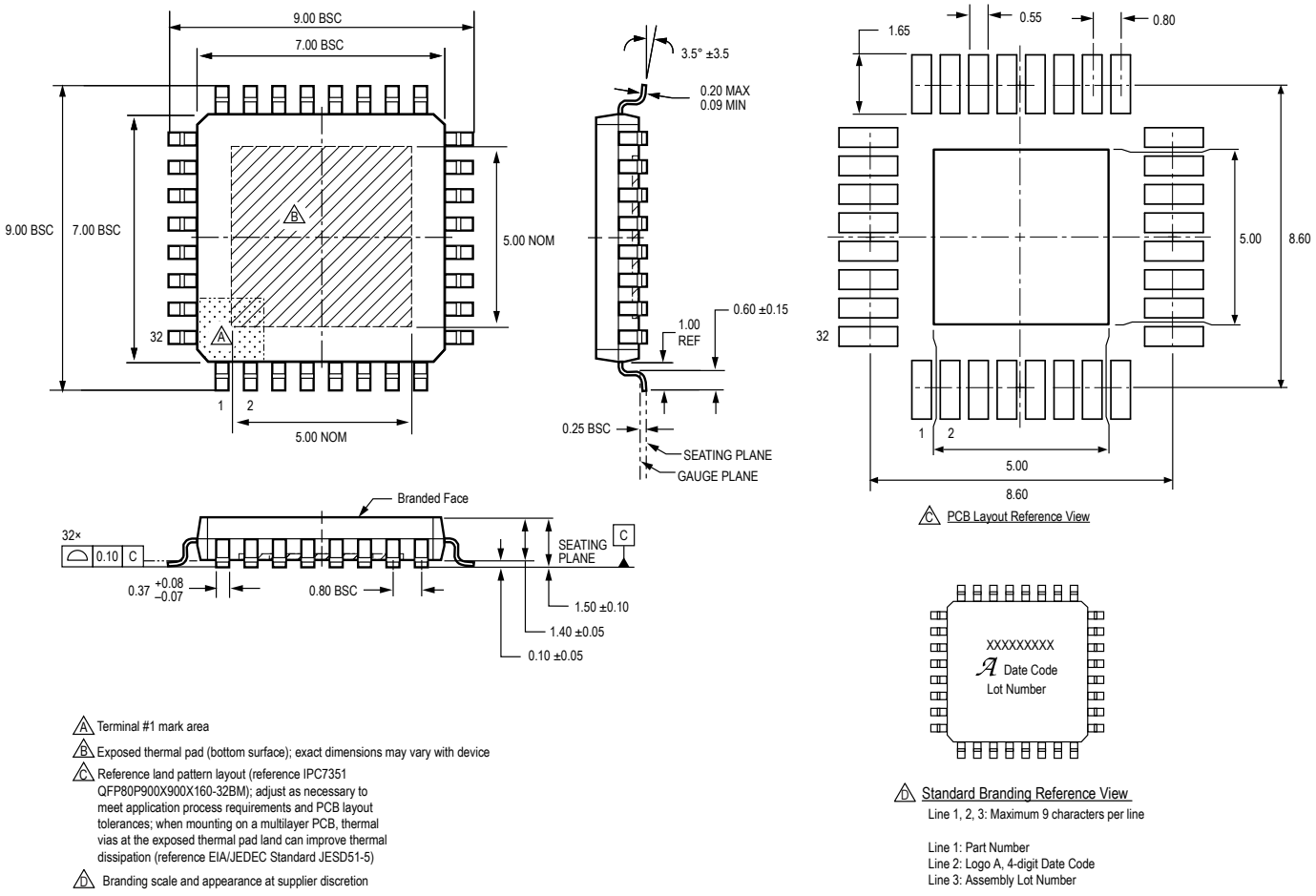

Figure 28: JP Package, 32-Pin QFP with Exposed Thermal Pad

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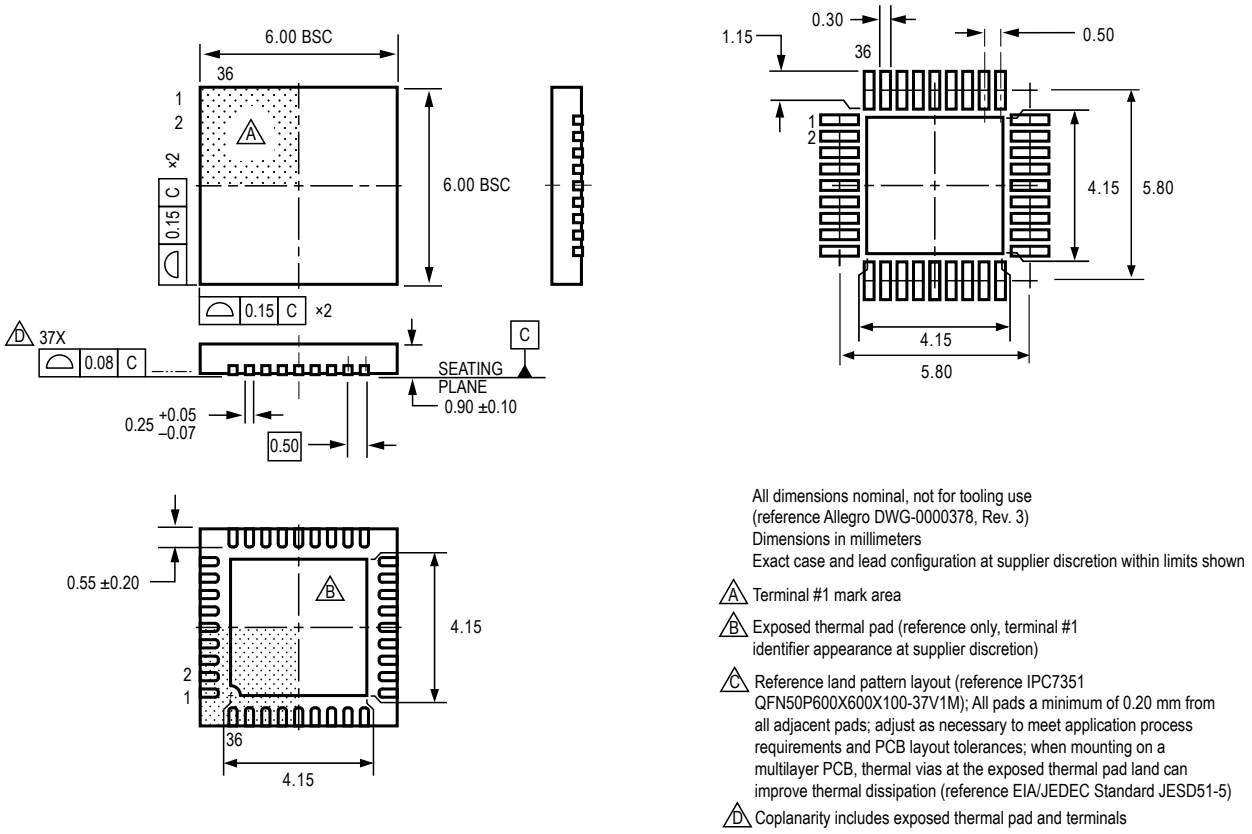

Figure 29: EV Package, 36-Pin QFN with Exposed Thermal Pad

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APPENDIX A: FAULT RESPONSE ACTIONS

Table A1a: Fault Response Actions (ESF = 0, VLU masked)

Fault Description	Disable Outputs	RSC [7]	Fault State Latched	Other Action	Fault State Reset	Re-Enable Outputs
No Fault	No	n/a	n/a	None	n/a	
System Error	Yes [1]	n/a	Yes	RUN = 0	POR, RUN = 1	
Serial Error	No	n/a	No	None	POR or SPI [3]	n/a
VBB POR	Yes [1]	n/a	No	Internal logic shutdown & reset	Condition removed	RUN = 1
VBB Undervoltage	No	0	Yes	None	Demand input = 0, RUN = 0, or SPI [3][4]	n/a
		1	No		Condition removed	
Watchdog Fault	Yes [1]	0	Yes	MCU reset	First watchdog transition after 100 ms from MRSTn going high	Demand input reset [5], RUN reset [6], or SPI [3][4]
		1	Yes		First watchdog transition after 100 ms from MRSTn going high	
VREG Undervoltage	Yes [1]	n/a	No	None	Condition removed	
Bootstrap Undervoltage	Yes [2]	n/a	No	None	PWM on	
Temperature Warning	No	n/a	No	None	Condition removed	n/a
Overtemperature	No	n/a	No	None	Condition removed	n/a
Loss of Synchronization	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No	Stop and restart	Condition removed	
VDS Overvoltage	Yes [2]	n/a	No	None	PWM on	

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only when DSR = 0.
[4] Serial read of Status or Diagnostic register.
[5] Set demand input = 0 then set demand input to a new operating value.
[6] Set RUN bit = 0 then set RUN bit = 1.
[7] Restart control bit.

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Table A1b: Fault Response Actions (ESF = 1, VLU masked)

Fault Description	Disable Outputs	RSC [7]	Fault State Latched	Other Action	Fault State Reset	Re-Enable Outputs
No Fault	No	n/a	n/a	None	n/a	
System Error	Yes [1]	n/a	Yes	RUN = 0	POR, RUN = 1	
Serial Error	No	n/a	No	None	POR or SPI [3]	n/a
VBB POR	Yes [1]	n/a	No	Internal logic shutdown & reset	Condition removed	RUN = 1
VBB Undervoltage	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No		Condition removed	
Watchdog Fault	Yes [1]	0	Yes	MCU reset	First watchdog transition after 100 ms from MRSTn going high	Demand input reset [5], RUN reset [6], or SPI [3][4]
		1	Yes		First watchdog transition after 100 ms from MRSTn going high	
VREG Undervoltage	Yes [1]	n/a	No	None	Condition removed	
Bootstrap Undervoltage	Yes [1]	n/a	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
Temperature Warning	No	n/a	No	None	Condition removed	n/a
Overtemperature	Yes [1]	n/a	Yes	VLR regulator shutdown & MCU reset	First watchdog transition after 100 ms from MRSTn going high	
Loss of Synchronization	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No	Stop and restart	Condition removed	
VDS Overvoltage	Yes [1]	n/a	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only when DSR = 0.
[4] Serial read of Status or Diagnostic register.
[5] Set demand input = 0 then set demand input to a new operating value.
[6] Set RUN bit = 0 then set RUN bit = 1.
[7] Restart control bit.

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Table A2a: Fault Response Actions (ESF = 0, WD masked)

Fault Description	Disable Outputs	RSC [7]	Fault State Latched	Other Action	Fault State Reset	Re-Enable Outputs
No Fault	No	n/a	n/a	None	n/a	
System Error	Yes [1]	n/a	Yes	RUN = 0	POR, RUN = 1	
Serial Error	No	n/a	No	None	POR or SPI [3]	n/a
VBB POR	Yes [1]	n/a	No	Internal logic shutdown & reset	Condition removed	RUN = 1
VBB Undervoltage	No	0	Yes	None	Demand input = 0, RUN = 0, or SPI [3][4]	n/a
		1	No		Condition removed	
VLR Undervoltage	Yes [1]	0	Yes	MCU reset	10 ms after condition removed when MRSTn goes high	Demand input reset [5], RUN reset [6], or SPI [3][4]
		1	Yes		10 ms after condition removed when MRSTn goes high	
VREG Undervoltage	Yes [1]	n/a	No	None	Condition removed	
Bootstrap Undervoltage	Yes [2]	n/a	No	None	PWM on	
Temperature Warning	No	n/a	No	None	Condition removed	n/a
Overtemperature	No	n/a	No	None	Condition removed	n/a
Loss of Synchronization	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No	Stop and restart	Condition removed	
VDS Overvoltage	Yes [2]	n/a	No	None	PWM on	

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only when DSR = 0.
[4] Serial read of Status or Diagnostic register.
[5] Set demand input = 0 then set demand input to a new operating value.
[6] Set RUN bit = 0 then set RUN bit = 1.
[7] Restart control bit.

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Table A2b: Fault Response Actions (ESF = 1, WD masked)

Fault Description	Disable Outputs	RSC [7]	Fault State Latched	Other Action	Fault State Reset	Re-Enable Outputs
No Fault	No	n/a	n/a	None	n/a	
System Error	Yes [1]	n/a	Yes	RUN = 0	POR, RUN = 1	
Serial Error	No	n/a	No	None	POR or SPI [3]	n/a
VBB POR	Yes [1]	n/a	No	Internal logic shutdown & reset	Condition removed	RUN = 1
VBB Undervoltage	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No		Condition removed	
VLR Undervoltage	Yes [1]	0	Yes	MCU reset	10 ms after condition removed when MRSTn goes high	Demand input reset [5], RUN reset [6], or SPI [3][4]
		1	Yes		10 ms after condition removed when MRSTn goes high	
VREG Undervoltage	Yes [1]	n/a	No	None	Condition removed	
Bootstrap Undervoltage	Yes [1]	n/a	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
Temperature Warning	No	n/a	No	None	Condition removed	n/a
Overtemperature	Yes [1]	n/a	Yes	VLR regulator shutdown & MCU reset	10 ms after condition removed when MRSTn goes high	Demand input reset [5], RUN reset [6], or SPI [3][4]
					10 ms after condition removed when MRSTn goes high	
Loss of Synchronization	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No	Stop and restart	Condition removed	
VDS Overvoltage	Yes [1]	n/a	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only when DSR = 0.
[4] Serial read of Status or Diagnostic register.
[5] Set demand input = 0 then set demand input to a new operating value.
[6] Set RUN bit = 0 then set RUN bit = 1.
[7] Restart control bit.

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Table A3a: Fault Response Actions (ESF = 0, VLR and WD masked)

Fault Description	Disable Outputs	RSC [7]	Fault State Latched	Other Action	Fault State Reset	Re-Enable Outputs
No Fault	No	n/a	n/a	None	n/a	
System Error	Yes [1]	n/a	Yes	RUN = 0	POR, RUN = 1	
Serial Error	No	n/a	No	None	POR or SPI [3]	n/a
VBB POR	Yes [1]	n/a	No	Internal logic shutdown & reset	Condition removed	RUN = 1
VBB Undervoltage	No	0	Yes	None	Demand input = 0, RUN = 0, or SPI [3][4]	n/a
		1	No		Condition removed	
VREG Undervoltage	Yes [1]	n/a	No	None	Condition removed	
Bootstrap Undervoltage	Yes [2]	n/a	No	None	PWM on	
Temperature Warning	No	n/a	No	None	Condition removed	n/a
Overtemperature	No	n/a	No	None	Condition removed	n/a
Loss of Synchronization	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No	Stop and restart	Condition removed	
VDS Overvoltage	Yes [2]	n/a	No	None	PWM on	

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only when DSR = 0.
[4] Serial read of Status or Diagnostic register.
[5] Set demand input = 0 then set demand input to a new operating value.
[6] Set RUN bit = 0 then set RUN bit = 1.
[7] Restart control bit.

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Table A3b: Fault Response Actions (ESF = 1, VLR and WD masked)

Fault Description	Disable Outputs	RSC [7]	Fault State Latched	Other Action	Fault State Reset	Re-Enable Outputs
No Fault	No	n/a	n/a	None	n/a	
System Error	Yes [1]	n/a	Yes	RUN = 0	POR, RUN = 1	
Serial Error	No	n/a	No	None	POR or SPI [3]	n/a
VBB POR	Yes [1]	n/a	No	Internal logic shutdown & reset	Condition removed	RUN = 1
VBB Undervoltage	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No		Condition removed	
VREG Undervoltage	Yes [1]	n/a	No	None	Condition removed	
Bootstrap Undervoltage	Yes [1]	n/a	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
Temperature Warning	No	n/a	No	None	Condition removed	n/a
Overtemperature	Yes [1]	n/a	Yes	VLR regulator shutdown & MCU reset	10 ms after condition removed when MRSTn goes high	
Loss of Synchronization	Yes [1]	0	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	
		1	No	Stop and restart	Condition removed	
VDS Overvoltage	Yes [1]	n/a	Yes	None	Demand input = 0 or RUN = 0	Demand input reset [5] or RUN reset [6]
					SPI [3][4]	

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only when DSR = 0.
[4] Serial read of Status or Diagnostic register.
[5] Set demand input = 0 then set demand input to a new operating value.
[6] Set RUN bit = 0 then set RUN bit = 1.
[7] Restart control bit.

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Revision History

Number	Date	Description
–	June 8, 2017	Initial release
1	September 15, 2017	Updated Speed Error values (p. 14), Figure 12 (p. 27), Peak Duty Cycle equation (p. 39), and Chip Fault State: VLR Undervoltage description (p. 50).
2	December 4, 2017	Updated VLR Regulator section (p. 23), Current Limit section (p. 34), Figure 20 (p. 42), and Readback Register section (p. 60).
3	December 20, 2018	Minor editorial updates
4	January 8, 2020	Minor editorial updates
5	February 8, 2022	Updated package drawings (pages 84-85)

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