THE DATASHEET OF

9EPRS475BGLF

Integrated Circuit Systems, Inc.

ICS9EPRS475 Datasheet

System Clock for Embedded AMD™ based Systems

Recommended Application:

AMD M690T/780E systems

Output Features:

- 2 - Greyhound compatible K8 CPU pair
- 4 - low-power differential SRC pairs
- 2 - low-power differential SouthBridge SRC pairs
- 3 - low-power differential ATIG pairs
- 1 - Selectable 100MHz low-power differential/ 66 MHz single-ended HTT clock
- 2 - 48MHz USB clock
- 3 - 14.318MHz Reference clock

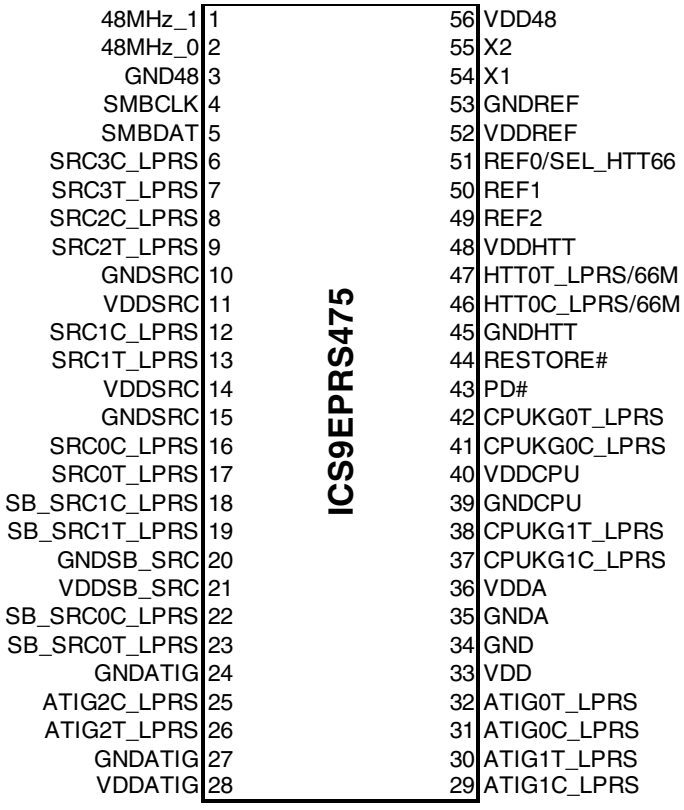
Key Specifications:

- CPU outputs cycle-to-cycle jitter < 150ps
- SRC outputs cycle-to-cycle jitter < 125ps
- ATIG outputs cycle-to-cycle jitter < 125ps
- +/- 300ppm frequency accuracy on CPU, SRC & ATIG clocks

Features/Benefits:

- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- External crystal load capacitors for maximum frequency accuracy
- PCI Express Generation 2.0 compliant

Pin Configuration



56-Pin TSSOP

*Other names and brands may be claimed as the property of others.

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	48MHz_1	OUT	48MHz clock output.
2	48MHz_0	OUT	48MHz clock output.
3	GND48	GND	Ground pin for the 48MHz outputs
4	SMBCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
5	SMBDAT	I/O	Data pin for SMBus circuitry, 5V tolerant.
6	SRC3C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
7	SRC3T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
8	SRC2C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
9	SRC2T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
10	GNDSRC	GND	Ground pin for the SRC outputs
11	VDDSRC	PWR	Supply for SRC core, 3.3V nominal
12	SRC1C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
13	SRC1T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
14	VDDSRC	PWR	Supply for SRC core, 3.3V nominal
15	GNDSRC	GND	Ground pin for the SRC outputs
16	SRC0C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
17	SRC0T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
18	SB_SRC1C_LPRS	OUT	Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
19	SB_SRC1T_LPRS	OUT	True clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
20	GNDSB_SRC	GND	Ground pin for the SB_SRC outputs
21	VDDSB_SRC	PWR	Supply for SRC core, 3.3V nominal
22	SB_SRC0C_LPRS	OUT	Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
23	SB_SRC0T_LPRS	OUT	True clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed
24	GNDATIG	GND	Ground pin for the ATIG outputs
25	ATIG2C_LPRS	OUT	Complementary clock of low-power differential push-pull ATIG pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
26	ATIG2T_LPRS	OUT	True clock of low-power differential push-pull ATIG pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
27	GNDATIG	GND	Ground pin for the ATIG outputs
28	VDDATIG	PWR	Power supply for ATIG core, nominal 3.3V
29	ATIG1C_LPRS	OUT	Complementary clock of low-power differential push-pull ATIG pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
30	ATIG1T_LPRS	OUT	True clock of low-power differential push-pull ATIG pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)

Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
31	ATIG0C_LPRS	OUT	Complementary clock of low-power differential push-pull ATIG pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
32	ATIG0T_LPRS	OUT	True clock of low-power differential push-pull ATIG pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed)
33	VDD	PWR	Power supply, nominal 3.3V
34	GND	GND	Ground pin
35	GNDA	GND	Ground for the Analog Core
36	VDDA	PWR	3.3V Power for the Analog Core
37	CPUKG1C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor.(no 33 ohm series resistor needed)
38	CPUKG1T_LPRS	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed)
39	GNDCPU	GND	Ground pin for the CPU outputs
40	VDDCPU	PWR	Supply for CPU core, 3.3V nominal
41	CPUKG0C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed)
42	CPUKG0T_LPRS	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor.(no 33 ohm series resistor needed)
43	PD#	IN	Enter /Exit Power Down. 0 = Power Down, 1 = normal operation.
44	RESTORE#	I/O	Open Drain I/O. As an input it restores the PLL's to power up default state. As an output, this signal is driven low when the internal watchdog hardware timer expires. It is cleared when the internal watchdog hardware timer is reset or disabled. The input is falling edge triggered. 0 = Restore Settings, 1 = normal operation.
45	GNDHTT	PWR	Ground pin for the HTT outputs
46	HTT0C_LPRS/66M	OUT	Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 3.3V single ended 66MHz hyper transport clock
47	HTT0T_LPRS/66M	OUT	True signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 3.3V single ended 66MHz hyper transport clock
48	VDDHTT	PWR	Supply for HTT clocks, nominal 3.3V.
49	REF2	OUT	14.318 MHz reference clock, 3.3V
50	REF1	OUT	14.318 MHz 3.3V reference clock
51	REF0/SEL_HTT66	I/O	14.318 MHz 3.3V reference clock./ 3.3V tolerant latched input to select Hyper Transport Clock Frequency. 0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock
52	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
53	GNDREF	GND	Ground pin for the REF outputs.
54	X1	IN	Crystal input, nominally 14.318MHz
55	X2	OUT	Crystal output, nominally 14.318MHz
56	VDD48	PWR	Power pin for the 48MHz outputs and core. 3.3V

General Description

The **ICS9EPRS475** is a main clock synthesizer chip that provides all clocks required for AMD embedded systems. An SMBus interface allows full control of the device.

Block Diagram

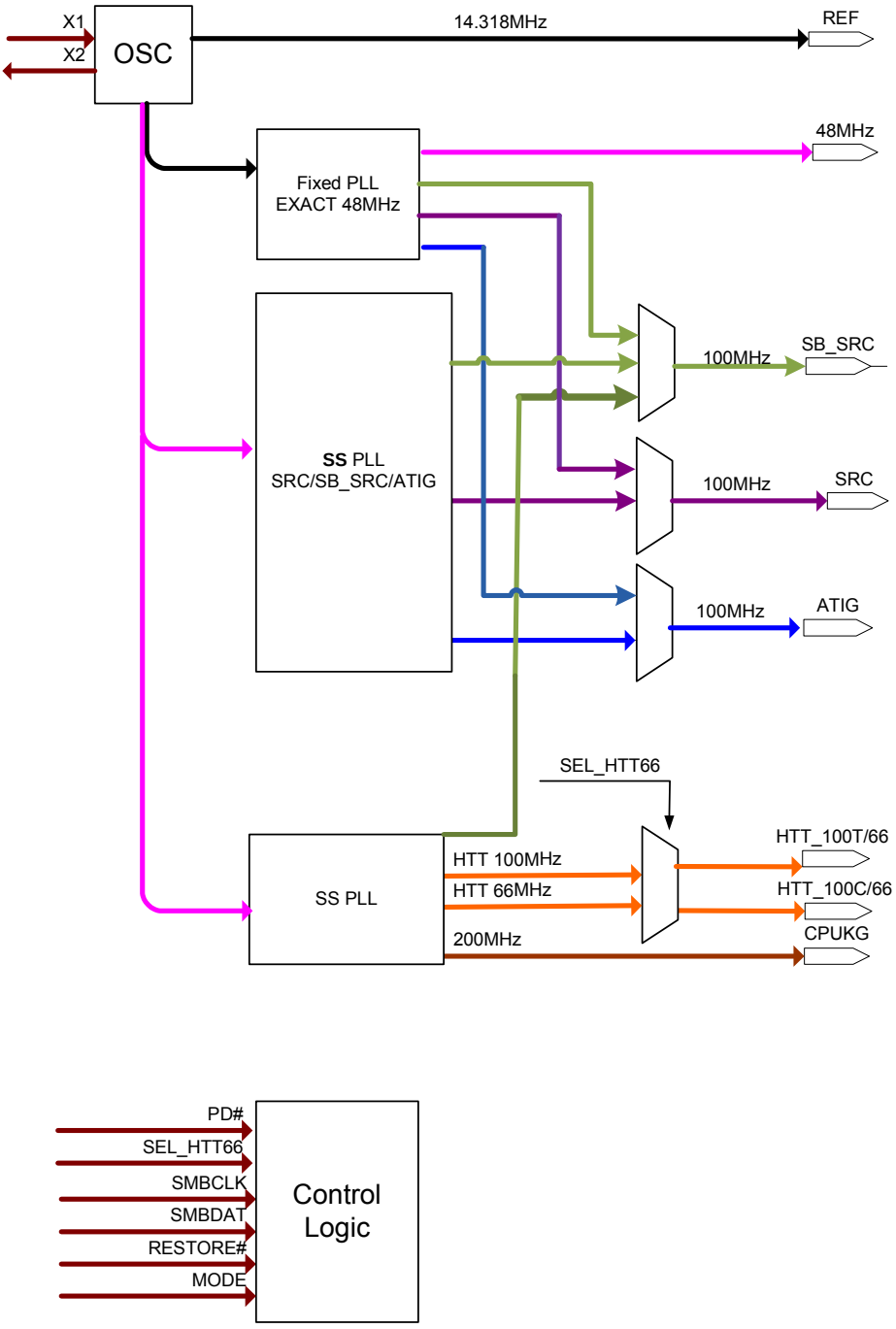


Table1: CPU and HTT Frequency Selection Table

Byte 3					CPU (MHz)	HTT Single-ended	HTT or SB_SRC Differential	SB_SRC (MHz)	Spread %	CPU OverClock %	CPU Output Divider	VCO
Bit5	Bit4	Bit3	Bit1	Bit0								
CPU FS4	CPU FS3	CPU FS2	CPU FS1	CPU FS0		SEL_HTT66 = 1	SEL_HTT66 = 0					(MHz)
0	0	0	0	0	133.33	44.44	66.67	66.67	-0.5%	-33%	3	400.00
0	0	0	0	1	137.78	45.93	68.89	68.89		-31%	3	413.33
0	0	0	1	0	142.22	47.41	71.11	71.11		-29%	3	426.67
0	0	0	1	1	146.67	48.89	73.33	73.33		-27%	3	440.00
0	0	1	0	0	151.11	50.37	75.56	75.56		-24%	3	453.33
0	0	1	0	1	155.56	51.85	77.78	77.78		-22%	3	466.67
0	0	1	1	0	160.00	53.33	80.00	80.00		-20%	3	480.00
0	0	1	1	1	164.44	54.81	82.22	82.22		-18%	3	493.33
0	1	0	0	0	168.89	56.30	84.44	84.44		-16%	3	506.67
0	1	0	0	1	173.33	57.78	86.67	86.67		-13%	3	520.00
0	1	0	1	0	177.78	59.26	88.89	88.89		-11%	3	533.33
0	1	0	1	1	182.22	60.74	91.11	91.11		-9%	3	546.67
0	1	1	0	0	186.67	62.22	93.33	93.33		-7%	3	560.00
0	1	1	0	1	191.11	63.70	95.56	95.56		-4%	3	573.33
0	1	1	1	0	195.56	65.19	97.78	97.78		-2%	3	586.67
0	**1**	**1**	**1**	**1**	**200.00**	**66.67**	**100.00**	100.00	**Off**	**0%**	**3**	**600.00**
1	0	0	0	0	200.00	66.67	100.00	100.00	-0.50%	0%	3	600.00
1	0	0	0	1	206.25	68.75	103.13	103.13	-0.50%	3%	3	618.75
1	0	0	1	0	212.50	70.83	106.25	106.25		6%	3	637.50
1	0	0	1	1	218.75	72.92	109.38	109.38		9%	3	656.25
1	0	1	0	0	225.00	75.00	112.50	112.50		13%	3	675.00
1	0	1	0	1	231.25	77.08	115.63	115.63		16%	3	693.75
1	0	1	1	0	237.50	79.17	118.75	118.75		19%	3	712.50
1	0	1	1	1	243.75	81.25	121.88	121.88		22%	3	731.25
1	1	0	0	0	250.00	83.33	125.00	125.00		25%	3	750.00
1	1	0	0	1	256.25	85.42	128.13	128.13		28%	3	768.75
1	1	0	1	0	262.50	87.50	131.25	131.25		31%	3	787.50
1	1	0	1	1	268.75	89.58	134.38	134.38		34%	3	806.25
1	1	1	0	0	275.00	91.67	137.50	137.50		38%	3	825.00
1	1	1	0	1	281.25	93.75	140.63	140.63		41%	3	843.75
1	1	1	1	0	287.50	95.83	143.75	143.75		44%	3	862.50
1	1	1	1	1	293.75	97.92	146.88	146.88		47%	3	881.25

Table 2: SRC Frequency Selection Table

Byte 4					SRC (MHz)	ATIG(3:0) (MHz)	SB_SRC (1:0) (MHz)	Spread %	OverClock %	SRC Output Divider	VCO (MHz)
Bit4	Bit3	Bit2	Bit1	Bit0							
SB FS4	SB FS3	SB FS2	SB FS1	SB FS0							
0	0	0	0	0	87.00	87.00	87.00	-0.48 max	-13%	10	870.00
0	0	0	0	1	87.87	87.87	87.87		-12%	10	878.70
0	0	0	1	0	88.73	88.73	88.73		-11%	10	887.30
0	0	0	1	1	89.60	89.60	89.60		-10%	10	896.00
0	0	1	0	0	90.47	90.47	90.47		-10%	10	904.70
0	0	1	0	1	91.33	91.33	91.33		-9%	10	913.30
0	0	1	1	0	92.20	92.20	92.20		-8%	10	922.00
0	0	1	1	1	93.07	93.07	93.07		-7%	10	930.70
0	1	0	0	0	93.93	93.93	93.93		-6%	10	939.30
0	1	0	0	1	94.80	94.80	94.80		-5%	10	948.00
0	1	0	1	0	95.67	95.67	95.67		-4%	10	956.70
0	1	0	1	1	95.67	95.67	95.67		-4%	10	956.70
0	1	1	0	0	97.40	97.40	97.40		-3%	10	974.00
0	1	1	0	1	98.27	98.27	98.27		-2%	10	982.70
0	1	1	1	0	99.13	99.13	99.13		-1%	10	991.30
0	**1**	**1**	**1**	**1**	**100.00**	**100.00**	**100.00**	**Off**	**0%**	**10**	**1000.00**
1	0	0	0	0	100.00	100.00	100.00	-0.48 max	0%	10	1000.00
1	0	0	0	1	100.87	100.87	100.87		1%	10	1008.70
1	0	0	1	0	101.73	101.73	101.73		2%	10	1017.30
1	0	0	1	1	102.60	102.60	102.60		3%	10	1026.00
1	0	1	0	0	103.47	103.47	103.47		3%	10	1034.70
1	0	1	0	1	104.33	104.33	104.33		4%	10	1043.30
1	0	1	1	0	105.20	105.20	105.20		5%	10	1052.00
1	0	1	1	1	106.07	106.07	106.07		6%	10	1060.70
1	1	0	0	0	106.93	106.93	106.93		7%	10	1069.30
1	1	0	0	1	107.80	107.80	107.80		8%	10	1078.00
1	1	0	1	0	108.67	108.67	108.67		9%	10	1086.70
1	1	0	1	1	109.53	109.53	109.53		10%	10	1095.30
1	1	1	0	0	110.40	110.40	110.40		10%	10	1104.00
1	1	1	0	1	111.27	111.27	111.27		11%	10	1112.70
1	1	1	1	0	112.13	112.13	112.13		12%	10	1121.30
1	1	1	1	1	113.00	113.00	113.00		13%	10	1130.00

NOTE: All frequencies assume that the SRC / SB_SRC / ATIG are at 0% Overclocking.

General SMBus serial interface information for the ICS9EPRS475

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Latched Input Readback Output Enable Control Register

Byte 0	Name	Description	X.3	0	1	Default
Bit 7	SEL_HTT66 readback	Hypertransport Select	R	100MHz Differential HTT clock	66 MHz 3.3V Single-ended HTT clock	Latch
Bit 6	Reserved					0
Bit 5	REF0_OE	Output Enable	RW	Low	Enabled	1
Bit 4	REF1_OE	Output Enable	RW	Low	Enabled	1
Bit 3	REF2_OE	Output Enable	RW	Low	Enabled	1
Bit 2	48MHz_1_OE	Output Enable	RW	Low	Enabled	1
Bit 1	48MHz_0_OE	Output Enable	RW	Low	Enabled	1
Bit 0	SS_Enable	Spread Spectrum Enable (CPU, HTT)	RW	Spread Off	Spread On	0

SMBus Table:Output Enable Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	CPU1_OE	Output enable	RW	Low/Low	Enable	1
Bit 6	CPU0_OE	Output enable	RW	Low/Low	Enable	1
Bit 5	SRC3_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 4	SRC2_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 3	HTT100_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 2	SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 1	Reserved					1
Bit 0	SRC0_OE	Output Enable	RW	Low/Low	Enabled	1

SMBus Table: Output Enable and 48MHz Strength Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SB_SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 6	SB_SRC0_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 5	SRC_PLL_SS_Enable	Spread Spectrum Enable (SRC, SB_SRC, ATIG)	RW	Spread Off	Spread On	0
Bit 4	ATIG2_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 3	ATIG1_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 2	ATIG0_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 1	48MHz_1_Strength	48MHz_1 Drive Strength Sel.	RW	1 Load	2 Load	1
Bit 0	48MHz_0_Strength	48MHz_0 Drive Strength Sel.	RW	1 Load	2 Load	1

SMBus Table: CPU/HTT Frequency Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	CPU_FS4	CPU Frequency Select MSB	RW	See CPU Frequency Select Table Default value corresponds to 200MHz. Note that Selected HTT frequency tracks the CPU frequency.		0
Bit 3	CPU_FS3	CPU Frequency Select	RW			1
Bit 2	CPU_FS2	CPU Frequency Select	RW			1
Bit 1	CPU_FS1	CPU Frequency Select	RW			1
Bit 0	CPU_FS0	CPU Frequency Select LSB	RW			1

SMBus Table: SRC Frequency Control Register

Byte 4	Name	Control Function	Type	0	1	Default
Bit 7	REF0_Strength	REF0_Drive Strength Sel	RW	1 Load	2 Load	1
Bit 6	REF1_Strength	REF1_Drive Strength Sel	RW	1 Load	2 Load	1
Bit 5	REF2_Strength	REF2_Drive Strength Sel	RW	1 Load	2 Load	1
Bit 4	SRC_FS4	SRC Frequency Select MSB	RW	See SRC Frequency Select Table Note: SB_SRC and ATIG Clocks are synchronous to these outputs. Changing this frequency will alter the SB_SRC and ATIG frequency by the same percentage.		0
Bit 3	SRC_FS3	SRC Frequency Select	RW			1
Bit 2	SRC_FS2	SRC Frequency Select	RW			1
Bit 1	SRC_FS1	SRC Frequency Select	RW			1
Bit 0	SRC_FS0	SRC Frequency Select LSB	RW			1

SMBus Table: Reserved

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					1
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	Reserved					1

SMBus Table: Reserved

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					1
Bit 2	Reserved					1
Bit 1	HTT66M_OE_1	Output Enable	RW	Low/Low	Enable	1
Bit 0	HTT66M_OE_0	Output Enable	RW	Low/Low	Enable	1

SMBus Table: Device ID register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Device ID7	Device ID	R	70 hex		0
Bit 6	Device ID6		R			1
Bit 5	Device ID5		R			1
Bit 4	Device ID4		R			1
Bit 3	Device ID3		R			0
Bit 2	Device ID2		R			0
Bit 1	Device ID1		R			0
Bit 0	Device ID0		R			0

SMBus Table: Vendor & Revision ID Register

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7	RID3	REVISION ID	R	-	-	0
Bit 6	RID2		R	-	-	0
Bit 5	RID1		R	-	-	1
Bit 4	RID0		R	-	-	0
Bit 3	VID3	VENDOR ID	R	-	-	0
Bit 2	VID2		R	-	-	0
Bit 1	VID1		R	-	-	0
Bit 0	VID0		R	-	-	1

SMBus Table: WatchDog Timer Control Register

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable and Reload Hard Alarm Timer, Clear	Enable Timer	0
Bit 6	Reserved					0
Bit 5	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
Bit 3	HWD3	WD Hard Alarm Timer Bit 3	RW	These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 x 290 ms = 2s		0
Bit 2	HWD2	WD Hard Alarm Timer Bit 2	RW			1
Bit 1	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 0	HWD0	WD Hard Alarm Timer Bit 0	RW			1

SMBus Table: Reserved

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					1
Bit 4	Reserved					0
Bit 3	Reserved					1
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	Reserved					1

SMBus Table: Byte Count Register

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	BC5	Byte Count bit 5 (MSB)	RW	Determines the number of bytes that are read back from the device. Default is 0F hex.		0
Bit 4	BC4	Byte Count bit 4	RW			0
Bit 3	BC3	Byte Count bit 3	RW			1
Bit 2	BC2	Byte Count bit 2	RW			1
Bit 1	BC1	Byte Count bit 1	RW			1
Bit 0	BC0	Byte Count bit 0 (LSB)	RW			1

SMBus Table: M/N Programming Enable and I/O Vout Control Register

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	CPU M/N En	CPU PLL M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 6	SRC M/N En	SRC M/N Prog.Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 5	SKIP_N_INC	Skip N Incrementing during CPU PLL M/N Programming	RW	N-Increment	Bypass N-Increment	0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	See Table 5: V_IO Selection (Default is 0.8V)		1
Bit 1	IO_VOUT1	IO Output Voltage Select	RW			0
Bit 0	IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1

SMBus Table: Reserved Register

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: Reserved Register

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	CPU NDiv0	LSB N Divider Programming	RW	Byte 27 has the N Divider LSB (bit 0) for CPU		X
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	SB_SRCDiv3	SB_SRC Divider Ratio Programming Bits from CPU PLL	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
Bit 2	SB_SRCDiv2		RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	X
Bit 1	SB_SRCDiv1		RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	X
Bit 0	SB_SRCDiv0		RW	0011:/9 ; 0111:/18	1011:/36 ; 1111:/72	X

SMBus Table:Test Mode Register

Byte	15	Name	Control Function	Type	0	1	Default
	Bit 7	Test_Md_Sel	Selects Test Mode	RW	Normal mode	All ouputs are REF/N	0
	Bit 6	Reserved					0
	Bit 5	Reserved					0
	Bit 4	Reserved					0
	Bit 3	Reserved					0
	Bit 2	Reserved					0
	Bit 1	Reserved					0
	Bit 0	Reserved					0

SMBus Table: CPU PLL Frequency Control Register

Byte	16	Name	Control Function	Type	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 16 and 17 will configure the VCO frequency. Default at power up = Byte 0 Rom table. See M/N Caculation Tables for VCO frequency formulas.		X
	Bit 6	N Div1	N Divider Prog bit 1	RW			X
	Bit 5	M Div5	M Divider Programming bits	RW			X
	Bit 4	M Div4		RW			X
	Bit 3	M Div3		RW			X
	Bit 2	M Div2		RW			X
	Bit 1	M Div1		RW			X
	Bit 0	M Div0		RW			X

SMBus Table: CPU PLL Frequency Control Register

Byte	17	Name	Control Function	Type	0	1	Default
	Bit 7	N Div10	N Divider Programming b(10:3)	RW	The decimal representation of M and N Divider in Byte 16 and 17 will configure the VCO frequency. Default at power up = Byte 0 Rom table. See M/N Caculation Tables for VCO frequency formulas.		X
	Bit 6	N Div9		RW			X
	Bit 5	N Div8		RW			X
	Bit 4	N Div7		RW			X
	Bit 3	N Div6		RW			X
	Bit 2	N Div5		RW			X
	Bit 1	N Div4		RW			X
	Bit 0	N Div3		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	18	Name	Control Function	Type	0	1	Default
	Bit 7	Reserved					1
	Bit 6	Reserved					0
	Bit 5	Reserved					0
	Bit 4	Reserved					0
	Bit 3	SB_SRC_Ssel	SB_SRC PLL Source Selection (MSB)	RW	10 - N/A	11 - CPU PLL	0
	Bit 2	ATIG_Ssel	ATIGCLK PLL Source Selection	RW	SRC PLL	FIX PLL	0
	Bit 1	SRC_Ssel	SRC PLL Source Selection	RW	SRC PLL	FIX PLL	0
	Bit 0	SB_SRC_Ssel	SB_SRC PLL Source Selection (LSB)	RW	00 - SRC PLL	01 - FIX PLL	0

SMBus Table: Reserved

Byte	19	Name	Control Function	Type	0	1	Default
	Bit 7	Reserved					0
	Bit 6	Reserved					0
	Bit 5	Reserved					0
	Bit 4	Reserved					0
	Bit 3	Reserved					0
	Bit 2	Reserved					0
	Bit 1	Reserved					0
	Bit 0	Reserved					0

SMBUS Table: SRC spread enable

Byte	20	Name	Control Function	Type	0	1	Default
	Bit 7	SRC_PLL_SS_Enable	Spread Spectrum Enable (SRC, SB_SRC, ATIG)	RW	Spread Off	Spread On	0
	Bit 6	Reserved					0
	Bit 5	Reserved					0
	Bit 4	Reserved					0
	Bit 3	Reserved					0
	Bit 2	Reserved					0
	Bit 1	Reserved					0
	Bit 0	Reserved					0

SMBUS Table: Reserved

Byte	21	Name	Control Function	Type	0	1	Default
	Bit 7	Reserved					0
	Bit 6	Reserved					0
	Bit 5	Reserved					0
	Bit 4	Reserved					0
	Bit 3	Reserved					0
	Bit 2	Reserved					0
	Bit 1	Reserved					0
	Bit 0	Reserved					0

SMBUS Table: Reserved

Byte	22	Name	Control Function	Type	0	1	Default
	Bit 7	ATIGDiv3	ATIG Divider Ratio Programming Bits	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
	Bit 6	ATIGDiv2		RW	N/A ; 0101:/6	1001:/12 ; 1101:/24	X
	Bit 5	ATIGDiv1		RW	N/A ; 0110:/10	1010:/20 ; 1110:/40	X
	Bit 4	ATIGDiv0		RW	N/A ; 0111:/14	1011:/28 ; 1111:/56	X
	Bit 3	SB_SRCDiv3	SB_SRC Divider Ratio Programming Bits from SRC Fixed / PLL	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
	Bit 2	SB_SRCDiv2		RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	X
	Bit 1	SB_SRCDiv1		RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	X
	Bit 0	SB_SRCDiv0		RW	0011:/7 ; 0111:/14	1011:/28 ; 1111:/56	X

SMBUS Table: SRC Spread Spectrum Control Register

Byte	23	Name	Control Function	Type	0	1	Default
	Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These bits set the SRC, the ATIG and SB_SRC spread pecentages.Please contact ICS for the appropriate values.		X
	Bit 6	SSP6		RW			X
	Bit 5	SSP5		RW			X
	Bit 4	SSP4		RW			X
	Bit 3	SSP3		RW			X
	Bit 2	SSP2		RW			X
	Bit 1	SSP1		RW			X
	Bit 0	SSP0		RW			X

SMBUS Table: SRC Spread Spectrum Control Register

Byte	24	Name	Control Function	Type	0	1	Default
	Bit 7	SSP15	Spread Spectrum Programming bit(15:8)	RW	These bits set the SRC, the ATIG and SB_SRC spread pecentages.Please contact ICS for the appropriate values.		X
	Bit 6	SSP14		RW			X
	Bit 5	SSP13		RW			X
	Bit 4	SSP12		RW			X
	Bit 3	SSP11		RW			X
	Bit 2	SSP10		RW			X
	Bit 1	SSP9		RW			X
	Bit 0	SSP8		RW			X

SMBUS Table: SRC Frequency Control Register

Byte	25	Name	Control Function	Type	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 20 and 21 configure the SRC VCO frequency. See M/N Caculation Tables for VCO frequency formulas. NOTE: Changing this frequency will also alter the ATIG and SB_SRC frequencies by a similar amount.		X
	Bit 6	N Div1	N Divider Prog bit 1	RW			X
	Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
	Bit 4	M Div4		RW			X
	Bit 3	M Div3		RW			X
	Bit 2	M Div2		RW			X
	Bit 1	M Div1		RW			X
	Bit 0	M Div0		RW			X

SMBUS Table: SRC Frequency Control Register

Byte	26	Name	Control Function	Type	0	1	Default
	Bit 7	N Div10	N Divider Programming Byte16 bit(7:0) and Byte15 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 20 and 21 configure the SRC VCO frequency. See M/N Caculation Tables for VCO frequency formulas. NOTE: Changing this frequency will also alter the ATIG and SB_SRC frequencies by a similar amount.		X
	Bit 6	N Div9		RW			X
	Bit 5	N Div8		RW			X
	Bit 4	N Div7		RW			X
	Bit 3	N Div6		RW			X
	Bit 2	N Div5		RW			X
	Bit 1	N Div4		RW			X
	Bit 0	N Div3		RW			X

SMBUS Table: CPU Output Divider Control Register

Byte	27	Name	Control Function	Type	0	1	Default
	Bit 7	HTTDiv3	HTT Divider Ratio Programming Bits	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
	Bit 6	HTTDiv2		RW	N/A ; 0101:/6	1001:/12 ; 1101:/24	X
	Bit 5	HTTDiv1		RW	N/A ; 0110:/10	1010:/20 ; 1110:/40	X
	Bit 4	HTTDiv0		RW	N/A ; 0111:/18	1011:/36 ; 1111:/72	X
	Bit 3	CPUDiv3	CPU Divider Ratio Programming Bits	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
	Bit 2	CPUDiv2		RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	X
	Bit 1	CPUDiv1		RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	X
	Bit 0	CPUDiv0		RW	0011:/9 ; 0111:/18	1011:/36 ; 1111:/72	X

SMBUS Table: CPU PLL Spread Spectrum Control Register

Byte	28	Name	Control Function	Type	0	1	Default
	Bit 7	SSP7	Spread Spectrum Programming b(7:0)	RW	These bits set the CPU/HTT spread pecentage.Please contact ICS for the appropriate values.		X
	Bit 6	SSP6		RW			X
	Bit 5	SSP5		RW			X
	Bit 4	SSP4		RW			X
	Bit 3	SSP3		RW			X
	Bit 2	SSP2		RW			X
	Bit 1	SSP1		RW			X
	Bit 0	SSP0		RW			X

SMBUS Table: CPU PLL Spread Spectrum Control Register

Byte	29	Name	Control Function	Type	0	1	Default
	Bit 7	SSP15	Spread Spectrum Programming b(15:8)	RW	These bits set the CPU/HTT spread pecentage.Please contact ICS for the appropriate values.		X
	Bit 6	SSP14		RW			X
	Bit 5	SSP13		RW			X
	Bit 4	SSP12		RW			X
	Bit 3	SSP11		RW			X
	Bit 2	SSP10		RW			X
	Bit 1	SSP9		RW			X
	Bit 0	SSP8		RW			X

SMBUS Table: SRC Output Divider Control Register

Byte	30	Name	Control Function	Type	0	1	Default
	Bit 7	SRC NDiv0	LSB N Divider Programming	RW	Byte 30 has the N Divider LSB (bit 0) for SRC		X
	Bit 6	Reserved					X
	Bit 5	Reserved					X
	Bit 4	Reserved					X
	Bit 3	SRCDiv3	SRC Divider Ratio Programming Bits	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
	Bit 2	SRCDiv2		RW	N/A ; 0101:/6	1001:/12 ; 1101:/24	X
	Bit 1	SRCDiv1		RW	N/A; 0110:/10	1010:/20 ; 1110:/40	X
	Bit 0	SRCDiv0		RW	N/A; 0111:/14	1011:/28 ; 1111:/56	X

SMBUS Table: Reserved Register

Byte	31	Name	Control Function	Type	0	1	Default
	Bit 7	Reserved					X
	Bit 6	Reserved					X
	Bit 5	Reserved					X
	Bit 4	Reserved					X
	Bit 3	Reserved					X
	Bit 2	Reserved					X
	Bit 1	Reserved					X
	Bit 0	Reserved					X

Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDDxxx	-		3.3	GND + 3.9V	V	1
Storage Temperature	Ts	-	-65		150	˚C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDDxxx	-	3.135	3.3	3.465	V	1
Input High Voltage	V_{IH}	VDD = 3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	VDD = 3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	VDD = 3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	VDD = 3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	3.3V VDD current, all outputs driven			115	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs low/low			12	mA	1
Input Frequency	F_i	VDD = 3.3 V +/-5%		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DDSMB}		2.7		5.5	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	$I_{PULLUPSMB}$		4	6		mA	1
SMBCLK/SMBDAT Clock/Data Rise Time	T_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SMBCLK/SMBDAT Clock/Data Fall Time	T_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

AC Electrical Characteristics - Low-Power DIF Outputs: CPUKG and HTT

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement			140	mV	1,2,5
Frequency	f	Spread Specturm On	198.8		200	MHz	1,3
Long Term Accuracy	ppm	Spread Specturm Off	-300		+300	ppm	1,11
Rising Edge Slew Rate	S_{RISE}	Differential Measurement	0.5		10	V/ns	1,4
Falling Edge Slew Rate	S_{FALL}	Differential Measurement	0.5		10	V/ns	1,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
CPU, DIF HTT Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement			150	ps	1,6
Accumulated Jitter	t_{JACC}	See Notes			1	ns	1,7
Peak to Peak Differential Voltage	$V_{D(PK-PK)}$	Differential Measurement	400		2400	mV	1,8
Differential Voltage	V_D	Differential Measurement	200		1200	mV	1,9
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
Amplitude Variation	ΔV_D	Change in V_D DC cycle to cycle	-75		75	mV	1,10
CPU[1:0] Skew	CPU_{SKEW10}	Differential Measurement			100	ps	1

Notes on Electrical Characteristics:

Guaranteed by design and characterization, not 100% tested in production.

Single-ended measurement at crossing point. Value is maximum – minimum over all time. DC value of common mode is not important due to the blocking cap.

Minimum Frequency is a result of 0.5% down spread spectrum

Differential measurement through the range of ±100 mV, differential signal must remain monotonic and within slew rate spec when crossing through this region.

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

[6] Max difference of t_{CYCLE} between any two adjacent cycles.

[7] Accumulated tjc.over a 10 µs time period, measured with JIT2 TIE at 50ps interval.

[8] VD(PK-PK) is the overall magnitude of the differential signal.

[9] VD(min) is the amplitude of the ring-back differential measurement, guaranteed by design, that ring-back will not cross 0V VD. VD(max) is the largest amplitude allowed.

[10] The difference in magnitude of two adjacent VD_DC measurements. VD_DC is the stable post overshoot and ring-back part of the signal.

[11] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

AC Electrical Characteristics - Low-Power DIF Outputs: SRC, SB_SRC, ATIG

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	0.6		4	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	0.6		4	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot			1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300			mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	300			mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300		550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement			140	mV	1,3,5
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
SRC Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement			125	ps	1
SRC[3:0] Skew	SRC_{SKEW}	Differential Measurement			100	ps	1
SB_SRC[1:0] Skew	SRC_{SKEW}	Differential Measurement			100	ps	1

Notes on Electrical Characteristics:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics - Single-ended HTT 66MHz Clock

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
PCI33 Clock period	T_{period}	33.33MHz output nominal	29.9910		30.0090	ns	2
		33.33MHz output spread	29.9910		30.1598	ns	2
HTT66 Clock period	T_{period}	66.67MHz output nominal	14.9955		15.0045	ns	2
		66.67MHz output spread	14.9955		15.0799	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@ MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	δV/δt	Rising edge rate (VOL = 0.4 V, VOH = 2.4 V)	1		4	V/ns	1
Edge Rate	δV/δt	Falling edge rate (VOL = 0.4 V, VOH = 2.4 V)	1		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			180	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

Electrical Characteristics - USB - 48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8229		20.8344	ns	2
Clock Low Time	T_{low}	Measure from < 0.6V	9.3750		11.4580	ns	2
Clock High Time	T_{high}	Measure from > 2.0V	9.3750		11.4580	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	δV/δt	Rising edge rate (VOL = 0.4 V, VOH = 2.4 V)	1.3		4	V/ns	1
Edge Rate	δV/δt	Falling edge rate (VOL = 0.4 V, VOH = 2.4 V)	1.3		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			130	ps	1,2

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]ICS recommended and/or chipset vendor layout guidelines must be followed to meet this specification

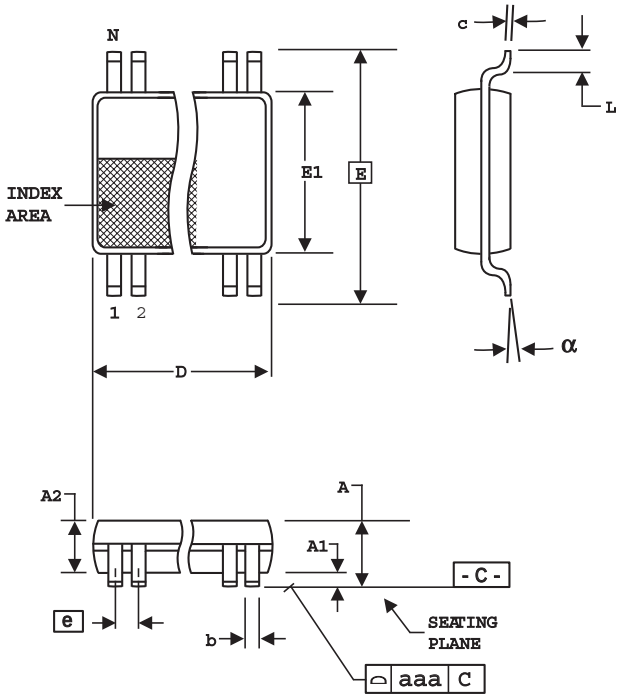
Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Clock Low Time	T_{low}	Measure from < 0.6V	30.9290		37.9130	ns	2
Clock High Time	T_{high}	Measure from > 2.0V	30.9290		37.9130	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Edge Rate	δV/δt	Rising edge rate (VOL = 0.4 V, VOH = 2.4 V)	1.3		2	V/ns	1
Edge Rate	δV/δt	Falling edge rate (VOL = 0.4 V, VOH = 2.4 V)	1.3		2	V/ns	1
Skew	t_{sk1}	V_T = 1.5 V			250	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			300	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz



56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part/Order Number	Shipping Packaging	Package	Temperature
9EPRS475BGLF	Tubes	56-pin TSSOP	0 to 70° C
9EPRS475BGLFT	Tape and Reel	56-pin TSSOP	0 to 70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
Due to package size constraints, actual top-side marking may differ from the full orderable part number.

Revision History

Rev.	Issue Date	Description	Page #
0.1	7/31/2009	Initial Release	-
A	8/19/2009	Released to final.	

Looking for pricing, stock, or lifecycle information?

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