



**THE DATASHEET OF
9DBL0941BKILFT**



Description

The 9DBL09x1 devices are 3.3V members of IDT's Full-Featured PCIe clock family. The 9DBL09x1 devices support PCIe Gen1–4 Common Clocked (CC) and PCIe Separate Reference Independent Spread (SRIS) systems. They offer a choice of integrated output terminations providing direct connection to 85Ω or 100Ω transmission lines. The 9DBL09P1 can be factory programmed with a user-defined power up default SMBus configuration.

Recommended Application

PCIe Gen1–4 clock distribution for Riser Cards, Storage, Networking, JBOD, Communications, Access Points

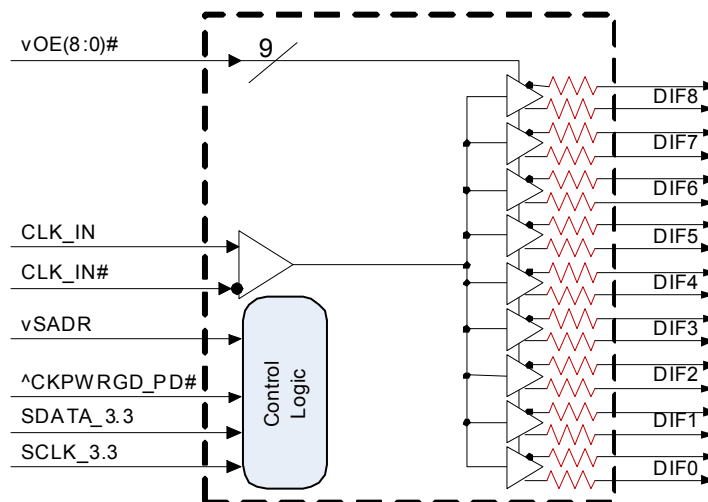
Output Features

- 9 – 1-200 MHz Low-Power (LP) HCSL DIF pairs
 - 9DBL0941 default Zout = 100Ω
 - 9DBL0951 default Zout = 85Ω
 - 9DBL09P1 factory programmable defaults
- Easy AC-coupling to other logic families, see IDT application note [AN-891](#).

Key Specifications

- DIF *additive* cycle-to-cycle jitter < 5ps
- DIF output-to-output skew < 50ps
- *Additive* phase jitter is 0ps (typical rms) for PCIe Gen1–4 CC, SRIS
- *Additive* phase jitter 111fs rms typical at 156.25M (1.5M to 10M)

Block Diagram

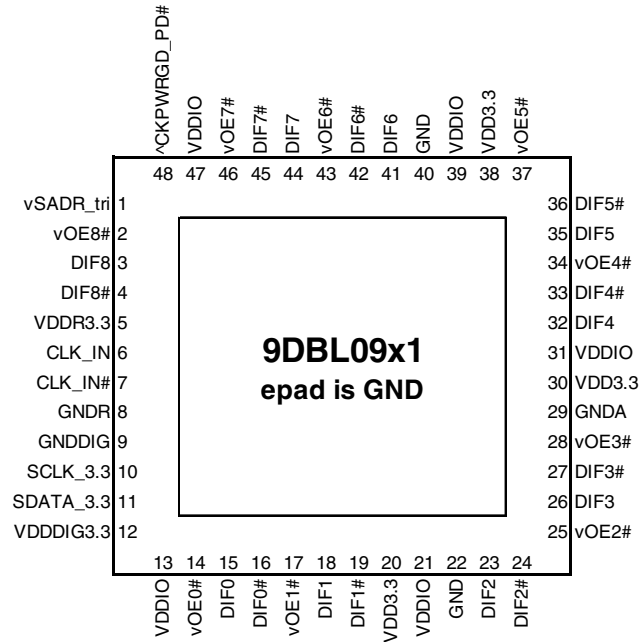


Note: Resistors default to internal on 41/51 devices. P1 devices have programmable default impedances on an output-by-output basis.

Features/Benefits

- Direct connection to 100Ω (xx41) or 85Ω (xx51) transmission lines; saves 36 resistors compared to standard PCIe devices
- 165mW typical power consumption (at 3.3V); eliminates thermal concerns
- VDDIO allows 50% power savings at optional 1.05V; maximum power savings
- SMBus-selectable features allows optimization to customer requirements:
 - control input polarity
 - control input pull up/downs
 - slew rate for each output
 - differential output amplitude
 - output impedance for each output
- Customer defined SMBus power up default can be programmed into P1 device; allows exact optimization to customer requirements
- OE# pins; support DIF power management
- HCSL differential input; can be driven by common clock sources
- Spread spectrum tolerant; allows reduction of EMI
- Device contains default configuration; SMBus interface not required for device operation
- Three selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 48-pin 6 x 6mm VFQFPN; minimal board space

Pin Configuration



48-pin VFQFPN, 6x6 mm, 0.4mm pitch

^v prefix indicates internal 120KOhm pull up *AND* pull down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

^ prefix indicates internal 120KOhm pull up resistor

SMBus Address Selection Table

| | SADR | Address | + Read/Write bit |
|---|------|---------|------------------|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101011 | x |
| | M | 1101100 | x |
| | 1 | 1101101 | x |

Note: If not using CKPWRGD (i.e., CKPWRGD tied to VDD3.3), all 3.3V VDD need to transition from 2.1V to 3.135V in <300usec.

Power Management Table

| CKPWRGD_PD# | CLK_IN | SMBus OEx bit | OEx# Pin | DIFx | |
|-------------|---------|---------------|----------|------------------|------------------|
| | | | | True O/P | Comp. O/P |
| 0 | X | X | X | Low ¹ | Low ¹ |
| 1 | Running | 0 | X | Low ¹ | Low ¹ |
| 1 | Running | 1 | 0 | Running | Running |
| 1 | Running | 1 | 1 | Low ¹ | Low ¹ |

1. The output state is set by B11[1:0] (Low/Low default)

Power Connections

| Pin Number | | | Description |
|-------------|----------------|-------------|-----------------------|
| VDD | VDDIO | GND | |
| 5 | | 8 | Input receiver analog |
| 12 | | 9 | Digital Power |
| 20,30,31,38 | 13,21,31,39,47 | 22,29,40,49 | DIF outputs |

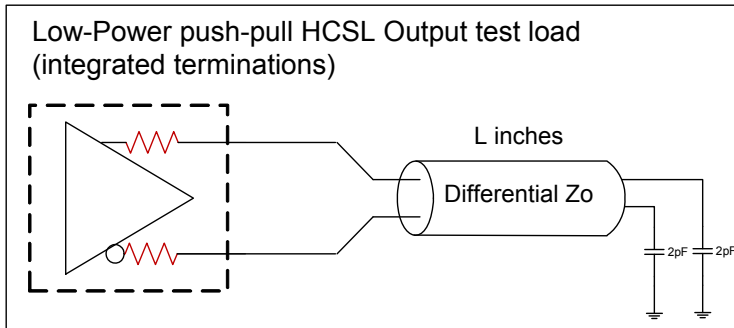
Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------|------------|--|
| 1 | vSADR_tri | LATCHED IN | Tri-level latch to select SMBus Address. See SMBus Address Selection Table. |
| 2 | vOE8# | IN | Active low input for enabling DIF pair 8. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 3 | DIF8 | OUT | Differential true clock output |
| 4 | DIF8# | OUT | Differential Complementary clock output |
| 5 | VDDR3.3 | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 6 | CLK_IN | IN | True Input for differential reference clock. |
| 7 | CLK_IN# | IN | Complementary Input for differential reference clock. |
| 8 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 9 | GNDDIG | GND | Ground pin for digital circuitry |
| 10 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 11 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 12 | VDDDIG3.3 | PWR | 3.3V digital power (dirty power) |
| 13 | VDDIO | PWR | Power supply for differential outputs |
| 14 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 15 | DIF0 | OUT | Differential true clock output |
| 16 | DIF0# | OUT | Differential Complementary clock output |
| 17 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 18 | DIF1 | OUT | Differential true clock output |
| 19 | DIF1# | OUT | Differential Complementary clock output |
| 20 | VDD3.3 | PWR | Power supply, nominal 3.3V |
| 21 | VDDIO | PWR | Power supply for differential outputs |
| 22 | GND | GND | Ground pin. |
| 23 | DIF2 | OUT | Differential true clock output |
| 24 | DIF2# | OUT | Differential Complementary clock output |
| 25 | vOE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 26 | DIF3 | OUT | Differential true clock output |
| 27 | DIF3# | OUT | Differential Complementary clock output |
| 28 | vOE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 29 | GNDA | GND | Ground pin for the PLL core. |
| 30 | VDD3.3 | PWR | Power supply, nominal 3.3V |
| 31 | VDDIO | PWR | Power supply for differential outputs |
| 32 | DIF4 | OUT | Differential true clock output |
| 33 | DIF4# | OUT | Differential Complementary clock output |
| 34 | vOE4# | IN | Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 35 | DIF5 | OUT | Differential true clock output |
| 36 | DIF5# | OUT | Differential Complementary clock output |
| 37 | vOE5# | IN | Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 38 | VDD3.3 | PWR | Power supply, nominal 3.3V |
| 39 | VDDIO | PWR | Power supply for differential outputs |
| 40 | GND | GND | Ground pin. |

Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------|------|---|
| 41 | DIF6 | OUT | Differential true clock output |
| 42 | DIF6# | OUT | Differential Complementary clock output |
| 43 | vOE6# | IN | Active low input for enabling DIF pair 6. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 44 | DIF7 | OUT | Differential true clock output |
| 45 | DIF7# | OUT | Differential Complementary clock output |
| 46 | vOE7# | IN | Active low input for enabling DIF pair 7. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 47 | VDDIO | PWR | Power supply for differential outputs |
| 48 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 49 | EPAD | GND | Connect to Ground. |

Test Loads



L = 5 inches

Alternate Terminations

The 9DBL family can easily drive LVPECL, LVDS, and CML logic. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs”](#) for details.

Terminations

| Device | Zo (Ω) | Rs (Ω) |
|----------|-----------------|-----------------|
| 9DBL0941 | 100 | None needed |
| 9DBL0951 | 100 | 7.5 |
| 9DBL09P1 | 100 | Prog. |
| 9DBL0941 | 85 | N/A |
| 9DBL0951 | 85 | None needed |
| 9DBL09P1 | 85 | Prog. |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBL09x1. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|---------------------------|------|-----|----------------------|-------|-------|
| Supply Voltage | VDDx | | | | 4.6 | V | 1,2 |
| Input Voltage | V _{IN} | | -0.5 | | V _{DD} +0.5 | V | 1,3 |
| Input High Voltage, SMBus | V _{IHSMB} | SMBus clock and data pins | | | 3.9 | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2500 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

³Not to exceed 4.6V.

Electrical Characteristics–SMBus Parameters

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|---------------------|--------------------------------------|-----|-----|------|-------|-------|
| SMBus Input Low Voltage | V _{ILSMB} | V _{DD} SMB = 3.3V | | | 0.8 | V | |
| SMBus Input High Voltage | V _{IHSMB} | V _{DD} SMB = 3.3V | 2.1 | | 3.6 | V | |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | |
| Nominal Bus Voltage | V _{DD} SMB | | 2.7 | | 3.6 | V | |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{SMB} | SMBus operating frequency | | | 500 | kHz | 2,3 |

¹Guaranteed by design and characterization, not 100% tested in production.

²The device must be powered up for the SMBus to function.

³The differential input clock must be running for the SMBus to be active

Electrical Characteristics–Clock Input Parameters

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|--------------------|---|-----|-----|-----|-------|-------|
| Input Crossover Voltage - DIF_IN | V _{CROSS} | Cross Over Voltage | 150 | | 900 | mV | 1 |
| Input Swing - DIF_IN | V _{SWING} | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | |
| Input Duty Cycle | d _{tin} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFIn} | Differential Measurement | 0 | | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--|------------------------|---|-----------------------|----------------------|------------------------|--------|-------|
| Supply Voltage | V _{DDx} | Supply voltage for core and analog | 3.135 | 3.3 | 3.465 | V | |
| Output Supply Voltage | V _{DDIO} | Supply voltage for Low Power HCSL Outputs | 0.95 | 1.05-3.3 | 3.465 | V | |
| Ambient Operating Temperature | T _{AMB} | Industrial range | -40 | 25 | 85 | °C | |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus | 0.75 V _{DDx} | | V _{DDx} + 0.3 | V | |
| Input Low Voltage | V _{IL} | | -0.3 | | 0.25 V _{DDx} | V | |
| Input High Voltage | V _{IHtri} | Single-ended tri-level inputs ('_tri' suffix) | 0.75 V _{DDx} | | V _{DD} + 0.3 | V | |
| Input Mid Voltage | V _{IMtri} | | 0.4 V _{DDx} | 0.5 V _{DDx} | 0.6 V _{DDx} | V | |
| Input Low Voltage | V _{ILtri} | | -0.3 | | 0.25 V _{DDx} | V | |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -50 | | 50 | uA | |
| Input Frequency | F _{IN} | | 1 | | 200 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | f _{MODINPCIe} | Allowable Frequency for PCIe Applications (Triangular Modulation) | 30 | | 33 | kHz | |
| Input SS Modulation Frequency non-PCIe | f _{MODIN} | Allowable Frequency for non-PCIe Applications (Triangular Modulation) | 0 | | 66 | kHz | |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t _F | Fall time of single-ended control inputs | | | 5 | ns | 2 |
| Trise | t _R | Rise time of single-ended control inputs | | | 5 | ns | 2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------------|---|------|-----|------|-------|-------|
| Slew rate | dV/dt | Scope averaging on, fast setting | 1.7 | 2.7 | 4 | V/ns | 1,2,3 |
| | dV/dt | Scope averaging on, slow setting | 0.8 | 1.9 | 2.8 | V/ns | 1,2,3 |
| Slew rate matching | Δ dV/dt | Slew rate matching | | 6 | 20 | % | 1,4 |
| Voltage High | V _{HIGH} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 783 | 850 | mV | 7 |
| Voltage Low | V _{LOW} | | -150 | -17 | 150 | | 7 |
| Max Voltage | V _{max} | Measurement on single ended signal using absolute value. (Scope averaging off) | | 818 | 1150 | mV | 7 |
| Min Voltage | V _{min} | | -300 | -54 | | | 7 |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off | 250 | 377 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ -V _{cross} | Scope averaging off | | 18 | 140 | mV | 1,6 |

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting Δ -V_{cross} to be smaller than V_{cross} absolute.

⁷ At default SMBus settings.

Electrical Characteristics–Current Consumption

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|----------------------|---|-----|------|-----|-------|-------|
| Operating Supply Current | I _{DD} | VDD + VDDR All outputs active @100MHz, 100 Loads | | 13 | 20 | mA | |
| | I _{DDDIG} | VDDDIG All outputs active @100MHz, 100 Loads | | 0.4 | 0.8 | mA | |
| | I _{DDIO} | VDDIO All outputs active @100MHz, 100 Loads | | 36 | 40 | mA | |
| Powerdown Current | I _{DDPD} | VDD + VDDR, CKPWRGD_PD#=0 | | 1 | 2 | mA | 2 |
| | I _{DDDIGPD} | VDDDIG, CKPWRGD_PD#=0 | | 0.4 | 0.8 | mA | 2 |
| | I _{DDIOPD} | VDDIO, CKPWRGD_PD#=0 | | 0.04 | 0.1 | mA | 2 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, and Skew Characteristics

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|---------------------------------|------|------|------|-------|-------|
| Duty Cycle Distortion | t _{DCD} | Measured differentially, 100MHz | -1 | -0.1 | 1 | % | 3 |
| Skew, Input to Output | t _{pd} | V _T = 50% | 2200 | 2982 | 4000 | ps | 2 |
| Skew, Output to Output | t _{sk3} | V _T = 50% | | 43 | 50 | ps | 2,4 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | Additive Jitter | | 0.1 | 1 | ps | 2 |

¹ Applies to all differential outputs, guaranteed by design and characterization.

² Measured from differential waveform

³ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

⁴ All outputs at same slew rate

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures^{1,5}

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|-----------------------|---------------------------|---|-----|------|------|----------------|----------|-------|
| Additive Phase Jitter | t _{jphPCIeG1-CC} | PCIe Gen 1 | | 0.4 | 2 | n/a | ps (p-p) | 2,3 |
| | t _{jphPCIeG2-CC} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz) | | 0.0 | 0.1 | | ps (rms) | 2,4 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz) | | 0.24 | 0.5 | | ps (rms) | 2,4 |
| | t _{jphPCIeG3-CC} | PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) | | 0.07 | 0.15 | | ps (rms) | 2,4 |
| | t _{jphPCIeG4-CC} | PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) | | 0.07 | 0.15 | | ps (rms) | 2,4 |

¹ Applies to all differential outputs, guaranteed by design and characterization.

² Based on PCIe Base Specification Rev4.0 version 0.7draft. See <http://www.pcisig.com> for latest specifications.

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ For RMS values additive jitter is calculated by solving the following equation for b [$a^2 + b^2 = c^2$] where a is rms input jitter and c is rms total jitter.

⁵ Driven by 9FGL0841 or equivalent

Electrical Characteristics—Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures¹

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|-----------------------|-----------------------------|---|-----|------|------|----------------|------------|-------|
| Additive Phase Jitter | t _{jphPCIeG1-SRIS} | PCIe Gen 1 | TBD | | | Note 5 | ps (pk-pk) | 2,3 |
| | t _{jphPCIeG2-SRIS} | PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz) | | 0.3 | 0.4 | | ps (rms) | 2 |
| | t _{jphPCIeG3-SRIS} | PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) | | 0.03 | 0.13 | | ps (rms) | 2 |
| | t _{jphPCIeG4-SRIS} | PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz) | TBD | | | | ps (rms) | 2 |

¹ Applies to all differential outputs, guaranteed by design and characterization.

² Based PCIe Base Specification Rev3.1a filters. These filters are different than Common Clock filters. See <http://www.pcisig.com> for latest specifications and are not defined for Gen1 or Gen4

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ For RMS values, additive jitter is calculated by solving the following equation for b [$a^2 + b^2 = c^2$] where a is rms input jitter and c is rms total jitter.

⁵ As of PCIe Base Specification Rev4.0 draft 0.7, SRIS limits are defined as implementation dependent.

Electrical Characteristics—Unfiltered Phase Jitter Parameters¹

T_A = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|-----------------------|----------------------------|--|-----|-----|-----|----------------|----------|-------|
| Additive Phase Jitter | t _{jph156M} | 156.25MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 111 | | N/A | fs (rms) | 2,3 |
| | t _{jph156M12k-20} | 156.25MHz, 12kHz to 20MHz, -20dB/decade rollover < 12kHz, -40db/decade rolloff > 20MHz | | 272 | | N/A | fs (rms) | 2,3 |

¹ Applies to all differential outputs, guaranteed by design and characterization.

² Driven by Rohde & Schartz SMA100

³ For RMS values, additive jitter is calculated by solving the following equation for b [$a^2 + b^2 = c^2$] where a is rms input jitter and c is rms total jitter.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|-----------------------------|-----------|--------|----------------------|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | O |
| O | | | O |
| O | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|----------------------------|-----------------|--------|----------------------|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | Data Byte Count=X |
| ACK | | X Byte | |
| ACK | | | Beginning Byte N |
| | | | O |
| | | | O |
| | | | O |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

Note: SMBus Address is Latched on SADR pin. Unless otherwise indicated, default values are for the xx41 and xx51. P1 devices are fully factory programmable.

SMBus Table: Output Enable Register ¹

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|--------|---------|------------------|------|---------|---------|---------|
| Bit 7 | DIF OE7 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 6 | DIF OE6 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 5 | DIF OE5 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 4 | DIF OE4 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 3 | DIF OE3 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 2 | DIF OE2 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 1 | DIF OE1 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 0 | DIF OE0 | Output Enable | RW | Low/Low | Enabled | 1 |

1. A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

SMBus Table: Output Enable and Output Amplitude Control Register

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------|---------------------------|------|------------|------------|---------|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | DIF OE8 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 1 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.6V | 01 = 0.68V | 1 |
| Bit 0 | AMPLITUDE 0 | | RW | 10 = 0.75V | 11 = 0.85V | 0 |

1. A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

SMBus Table: DIF Slew Rate Control Register

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|--------------------------|------|--------------|--------------|---------|
| Bit 7 | SLEWRATESEL DIF7 | Adjust Slew Rate of DIF7 | RW | Slow Setting | Fast Setting | 1 |
| Bit 6 | SLEWRATESEL DIF6 | Adjust Slew Rate of DIF6 | RW | Slow Setting | Fast Setting | 1 |
| Bit 5 | SLEWRATESEL DIF5 | Adjust Slew Rate of DIF5 | RW | Slow Setting | Fast Setting | 1 |
| Bit 4 | SLEWRATESEL DIF4 | Adjust Slew Rate of DIF4 | RW | Slow Setting | Fast Setting | 1 |
| Bit 3 | SLEWRATESEL DIF3 | Adjust Slew Rate of DIF3 | RW | Slow Setting | Fast Setting | 1 |
| Bit 2 | SLEWRATESEL DIF2 | Adjust Slew Rate of DIF2 | RW | Slow Setting | Fast Setting | 1 |
| Bit 1 | SLEWRATESEL DIF1 | Adjust Slew Rate of DIF1 | RW | Slow Setting | Fast Setting | 1 |
| Bit 0 | SLEWRATESEL DIF0 | Adjust Slew Rate of DIF0 | RW | Slow Setting | Fast Setting | 1 |

Note: See "Low-Power HCSSL Outputs" table for slew rates.

SMBus Table: DIF Slew Rate Control Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|--------------------------|------|--------------|--------------|---------|
| Bit 7 | Reserved | | | | | 1 |
| Bit 6 | Reserved | | | | | 1 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | Reserved | | | | | 1 |
| Bit 0 | SLEWRATESEL DIF8 | Adjust Slew Rate of DIF8 | RW | Slow Setting | Fast Setting | 1 |

Note: See "Low-Power HCSSL Outputs" table for slew rates.

Byte 4 is Reserved and reads back 'hFF'

SMBus Table: Revision and Vendor ID Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|--------------|---|---------|
| Bit 7 | RID3 | Revision ID | R | B rev = 0001 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 1 |
| Bit 3 | VID3 | VENDOR ID | R | 0001 = IDT | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

SMBus Table: Device Type/Device ID

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|--------|--------------|------------------|------|---|---|---------|
| Bit 7 | Device Type1 | Device Type | R | 00 = FGx, 01 = DBx, 10 = DMx, 11= DBx w/oPLL | | 1 |
| Bit 6 | Device Type0 | | R | | | 1 |
| Bit 5 | Device ID5 | Device ID | R | 001001binary or 09 hex | | 0 |
| Bit 4 | Device ID4 | | R | | | 0 |
| Bit 3 | Device ID3 | | R | | | 1 |
| Bit 2 | Device ID2 | | R | | | 0 |
| Bit 1 | Device ID1 | | R | | | 0 |
| Bit 0 | Device ID0 | | R | | | 1 |

SMBus Table: Byte Count Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------------|------|---|---|---------|
| Bit 7 | | Reserved | | | | 0 |
| Bit 6 | | Reserved | | | | 0 |
| Bit 5 | | Reserved | | | | 0 |
| Bit 4 | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

Bytes 8 and 9 are Reserved

SMBus Table: PLL MN Enable, PD_Restore

| Byte 10 | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------------------------|-------------------------------|------|--------------------|-------------------|---------|
| Bit 7 | | Reserved | | | | 1 |
| Bit 6 | Power-Down (PD) Restore | Restore Default Config. In PD | RW | Clear Config in PD | Keep Config in PD | 1 |
| Bit 5 | | Reserved | | | | 0 |
| Bit 4 | | Reserved | | | | 0 |
| Bit 3 | | Reserved | | | | 0 |
| Bit 2 | | Reserved | | | | 0 |
| Bit 1 | | Reserved | | | | 0 |
| Bit 0 | | Reserved | | | | 0 |

SMBus Table: Impedance Control

| Byte 11 | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------------|--|------|-----------------|------------------|----------|
| Bit 7 | DIF8_imp[1] | DIF8 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | see Note |
| Bit 6 | DIF8_imp[0] | | RW | 01=85Ω DIF Zout | 11 = Reserved | |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | STP[1] | True/Complement DIF Output Disable State | RW | 00 = Low/Low | 10 = High/Low | 0 |
| Bit 0 | STP[0] | | RW | 01 = HiZ/HiZ | 11 = Low/High | 0 |

Note: xx41 = 10, xx51 = 01, P1 = factory programmable.

SMBus Table: Impedance Control

| Byte 12 | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------------|------------------|------|-----------------|------------------|----------|
| Bit 7 | DIF3_imp[1] | DIF3 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | see Note |
| Bit 6 | DIF3_imp[0] | DIF3 Zout | RW | 01=85Ω DIF Zout | 11 = Reserved | |
| Bit 5 | DIF2_imp[1] | DIF2 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | |
| Bit 4 | DIF2_imp[0] | DIF2 Zout | RW | 01=85Ω DIF Zout | 11 = Reserved | |
| Bit 3 | DIF1_imp[1] | DIF1 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | |
| Bit 2 | DIF1_imp[0] | DIF1 Zout | RW | 01=85Ω DIF Zout | 11 = Reserved | |
| Bit 1 | DIF0_imp[1] | DIF0 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | |
| Bit 0 | DIF0_imp[0] | DIF0 Zout | RW | 01=85Ω DIF Zout | 11 = Reserved | |

Note: xx41 = 10, xx51 = 01, P1 = factory programmable.

SMBus Table: Impedance Control

| Byte 13 | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------------|------------------|------|-----------------|------------------|----------|
| Bit 7 | DIF7_imp[1] | DIF7 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | see Note |
| Bit 6 | DIF7_imp[0] | DIF7 Zout | RW | 01=85Ω DIF Zout | 11 = Reserved | |
| Bit 5 | DIF6_imp[1] | DIF6 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | |
| Bit 4 | DIF6_imp[0] | DIF6 Zout | RW | 01=85Ω DIF Zout | 11 = Reserved | |
| Bit 3 | DIF5_imp[1] | DIF5 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | |
| Bit 2 | DIF5_imp[0] | DIF5 Zout | RW | 01=85Ω DIF Zout | 11 = Reserved | |
| Bit 1 | DIF4_imp[1] | DIF4 Zout | RW | 00=33Ω DIF Zout | 10=100Ω DIF Zout | |
| Bit 0 | DIF4_imp[0] | DIF4 Zout | RW | 01=85Ω DIF Zout | 11 = Reserved | |

Note: xx41 = 10, xx51 = 01, P1 = factory programmable.

SMBus Table: Pull-up Pull-down Control

| Byte 14 | Name | Control Function | Type | 0 | 1 | Default |
|---------|--------------|---|------|---------|---------------|---------|
| Bit 7 | OE3_pu/pd[1] | OE3 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 6 | OE3_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |
| Bit 5 | OE2_pu/pd[1] | OE2 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 4 | OE2_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |
| Bit 3 | OE1_pu/pd[1] | OE1 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 2 | OE1_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |
| Bit 1 | OE0_pu/pd[1] | OE0 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 0 | OE0_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |

Note: These values are for xx41 and xx51. P1 is factory programmable.

SMBus Table: Pull-up Pull-down Control

| Byte 15 | Name | Control Function | Type | 0 | 1 | Default |
|---------|--------------|--|------|---------|---------------|---------|
| Bit 7 | OE7_pu/pd[1] | OE7 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 6 | OE7_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |
| Bit 5 | OE6_pu/pd[1] | OE6 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 4 | OE6_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |
| Bit 3 | OE5_pu/pd[1] | OE5 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 2 | OE5_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |
| Bit 1 | OE4_pu/pd[1] | OE4 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 0 | OE4_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |

Note: These values are for xx41 and xx51. P1 is factory programmable.

SMBus Table: Pull-up Pull-down Control

| Byte 16 | Name | Control Function | Type | 0 | 1 | Default |
|---------|---------------------|---|------|---------|---------------|---------|
| Bit 7 | | Reserved | | | | 0 |
| Bit 6 | | Reserved | | | | 0 |
| Bit 5 | | Reserved | | | | 1 |
| Bit 4 | | Reserved | | | | 0 |
| Bit 3 | OE8_pu/pd[1] | OE8 Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 0 |
| Bit 2 | OE8_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 1 |
| Bit 1 | CKPWRGD_PD_pu/pd[1] | CKPWRGD_PD Pull-up(PuP)/ Pull-down(Pdwn) control | RW | 00=None | 10=Pup | 1 |
| Bit 0 | CKPWRGD_PD_pu/pd[0] | | RW | 01=Pdwn | 11 = Pup+Pdwn | 0 |

Note: These values are for xx41 and xx51. P1 is factory programmable.

Bytes 17 is Reserved and reads back 0h00.

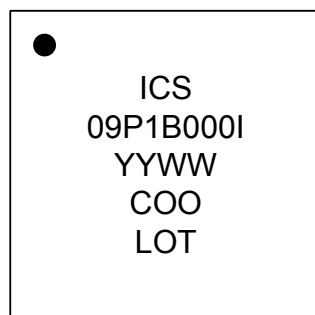
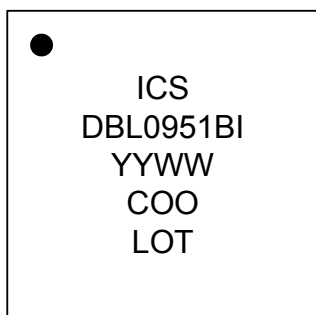
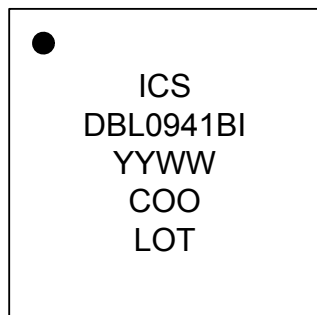
SMBus Table: Polarity Control

| Byte 18 | Name | Control Function | Type | 0 | 1 | Default |
|---------|--------------|-------------------|------|------------------|-------------------|---------|
| Bit 7 | OE7_polarity | Sets OE7 polarity | RW | Enabled when Low | Enabled when High | 0 |
| Bit 6 | OE6_polarity | Sets OE6 polarity | RW | Enabled when Low | Enabled when High | 0 |
| Bit 5 | OE5_polarity | Sets OE5 polarity | RW | Enabled when Low | Enabled when High | 0 |
| Bit 4 | OE4_polarity | Sets OE4 polarity | RW | Enabled when Low | Enabled when High | 0 |
| Bit 3 | OE3_polarity | Sets OE3 polarity | RW | Enabled when Low | Enabled when High | 0 |
| Bit 2 | OE2_polarity | Sets OE2 polarity | RW | Enabled when Low | Enabled when High | 0 |
| Bit 1 | OE1_polarity | Sets OE1 polarity | RW | Enabled when Low | Enabled when High | 0 |
| Bit 0 | OE0_polarity | Sets OE0 polarity | RW | Enabled when Low | Enabled when High | 0 |

SMBus Table: Polarity Control

| Byte 19 | Name | Control Function | Type | 0 | 1 | Default |
|---------|--------------|-----------------------------------|------|------------------------|-------------------------|---------|
| Bit 7 | | Reserved | | | | 0 |
| Bit 6 | | Reserved | | | | 0 |
| Bit 5 | | Reserved | | | | 0 |
| Bit 4 | | Reserved | | | | 0 |
| Bit 3 | | Reserved | | | | 0 |
| Bit 2 | | Reserved | | | | 0 |
| Bit 1 | OE8_polarity | Determines OE9 polarity | RW | Enabled when Low | Enabled when High | 0 |
| Bit 0 | CKPWRGD_PD | Determines CKPWRGD_PD polarity | RW | Power Down when Low | Power Down when High | 0 |

Marking Diagrams



Notes:

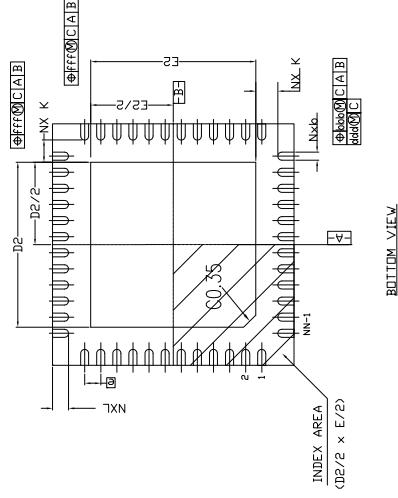
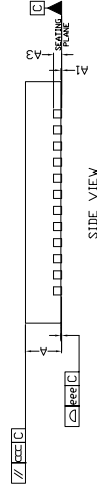
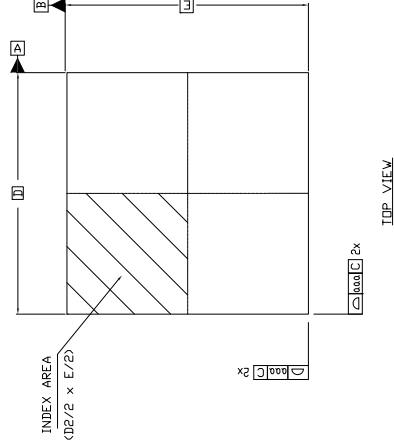
1. "LOT" is the lot sequence number.
2. "COO" denotes country of origin.
3. "YYWW" is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. "I" denotes industrial temperature range device.

Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|--------------------|----------------------|---------------------------------|-------|-----------|-------|-------|
| Thermal Resistance | θ_{JC} | Junction to Case | NDG48 | 33 | °C/W | 1 |
| | θ_{Jb} | Junction to Base | | 2.1 | °C/W | 1 |
| | $\theta_{JA0\theta}$ | Junction to Air, still air | | 37 | °C/W | 1 |
| | θ_{JA1} | Junction to Air, 1 m/s air flow | | 30 | °C/W | 1 |
| | θ_{JA3} | Junction to Air, 3 m/s air flow | | 27 | °C/W | 1 |
| | θ_{JA5} | Junction to Air, 5 m/s air flow | | 26 | °C/W | 1 |

¹ePad soldered to board

| REVISIONS | |
|-----------|-----------------|
| REV | DESCRIPTION |
| 00 | INITIAL RELEASE |




NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N REFERS TO THE NUMBER OF LEADS.
4. ND AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

| SYMBOL | DIMENSION | |
|------------------------------|-----------|----------|
| | MIN | MAX |
| D2 | 3.95 | 4.10 |
| E2 | 3.95 | 4.10 |
| L | 0.30 | 0.40 |
| K | 0.55 REF | |
| D | 6.00 BSC | |
| E | 6.00 BSC | |
| e | 0.40 BSC | |
| A | 0.80 | 0.90 |
| A1 | 0.00 | 0.02 |
| A3 | --- | 0.20 REF |
| N | 48 | |
| ND | 12 | |
| NE | 12 | |
| b | 0.15 | 0.20 |
| TOLERANCE of FORM & POSITION | | |
| aaa | 0.10 | |
| bbb | 0.07 | |
| ccc | 0.10 | |
| ddd | 0.05 | |
| eee | 0.08 | |
| fff | 0.10 | |

| | | |
|---|-------------|----------------------|
| TOLERANCES UNLESS SPECIFIED IN DECIMAL XXX± ANGULAR ±1° APPROVALS DRAWN CHECKED | TITLE | ND/NDG 48 |
| | DATE | 01/11/08 |
| | SIZE | 6.0 x 6.0 mm |
| | DRAWING No. | 0.40 mm PL |
| | C | PS |
| | | DO NOT SCALE DRAWING |


 www.IDT.com

Ordering Information

| Part / Order Number | Output Impedance | Shipping Packaging | Package | Temperature |
|---------------------|--|--------------------|---------------|---------------|
| 9DBL0941BKILF | 100Ω | Trays | 48-pin VFQFPN | -40 to +85° C |
| 9DBL0941BKILFT | | Tape and Reel | 48-pin VFQFPN | -40 to +85° C |
| 9DBL0951BKILF | 85Ω | Trays | 48-pin VFQFPN | -40 to +85° C |
| 9DBL0951BKILFT | | Tape and Reel | 48-pin VFQFPN | -40 to +85° C |
| 9DBL09P1BxxxKILF | Factory configurable. Contact IDT for additional information. | Trays | 48-pin VFQFPN | -40 to +85° C |
| 9DBL09P1BxxxKILFT | | Tape and Reel | 48-pin VFQFPN | -40 to +85° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“B” is the device revision designator (will not correlate with the datasheet revision).

“xxx” is a unique factory assigned number to identify a particular default configuration.

Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|------|-----------|------------|--|---------|
| A | RDW | 9/16/2016 | <ol style="list-style-type: none"> Updated front page text Changed VDDA3.3 pin to VDD3.3, since this part has no PLL Removed references to PLL mode, since this part has no PLL Regrouped IDD values to simplify the table Updated Electrical tables to latest version, including PCIe Gen4 Updated ordering information to B rev Corrected readback of Smbus B1[1:0], B3[7], B5[4], B10[7], B16[5] - most of these are reserved bits Updated footnote text under block diagram. Updated block diagram for stylistic consistency. Updated electrical tables with char data, move to final. | Various |
| B | RDW | 9/26/2016 | <ol style="list-style-type: none"> Corrected Byte 11[1:0] bit definitions. | 13 |
| C | RDW | 8/1/2017 | Removed reference to differential waveform in slew rate matching spec | 7 |

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