



**THE DATASHEET OF  
840004AG-11LFT**



## General Description

The 840004-11 is a 4 output LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the family of high performance clock solutions from IDT. Using a 25MHz, 18pF parallel resonant crystal, 125MHz and 62.5MHz can be generated based on one frequency select pin (F\_SEL). The 840004-11 uses IDT's 3<sup>rd</sup> generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Ethernet jitter requirements. The 840004-11 is packaged in a small 20-pin TSSOP package.

## Features

- Four single-ended LVCMOS/LVTTL outputs  
17Ω typical output impedance
- Crystal oscillator interface
- Input frequency range: 22.4MHz to 28MHz
- Output frequency range: 56MHz - 140MHz
- VCO range: 560MHz - 700MHz
- RMS phase jitter at 125MHz (1.875MHz – 20MHz):  
0.70ps (typical)

Phase Noise:

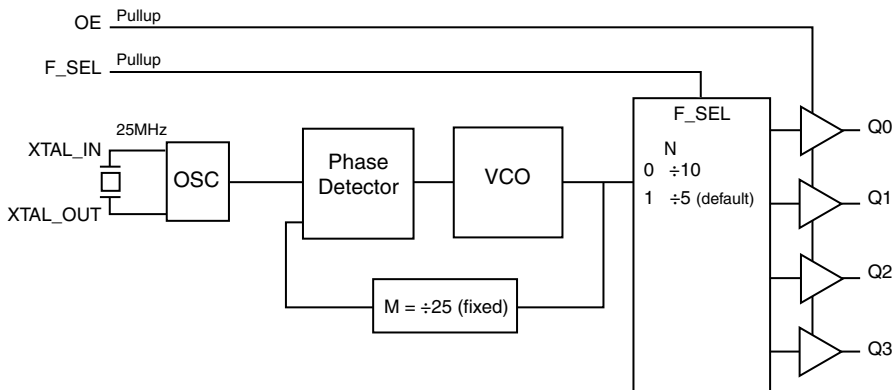
Offset	Noise Power
100Hz	-95.5 dBc/Hz
1kHz	-123.6 dBc/Hz
10kHz	-132.8 dBc/Hz
100kHz	-133.4 dBc/Hz

- Full 3.3V output supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Frequency Select Function Table for Ethernet Frequencies

Inputs			Output Frequency (MHz), 25MHz Reference
F_SEL	M Divider Value	N Divider Value	
0	25	10	62.5
1	25	5	125 (default)

## Block Diagram



## Pin Assignment

F_SEL	1	20	nc
nc	2	19	GND
nc	3	18	Q0
nc	4	17	Q1
OE	5	16	VDDO
nc	6	15	Q2
nc	7	14	Q3
VDDA	8	13	GND
nc	9	12	XTAL_IN
VDD	10	11	XTAL_OUT

**ICS840004-01**

20-Lead TSSOP

6.5mm x 4.4mm x 0.925mm

package body

G Package

Top View

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	F_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
2, 3, 4, 6, 7, 9, 20	nc	Unused		No connect.
5	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
8	V <sub>DDA</sub>	Power		Analog supply pin.
10	V <sub>DD</sub>	Power		Core supply pin.
11, 12	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
13, 19	GND	Power		Power supply ground.
14, 15, 17, 18	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. 17Ω typical output impedance. LVCMOS/ LVTTL interface levels.
16	V <sub>DDO</sub>	Power		Output supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>DD</sub> = V <sub>DDO</sub> = 3.465V		8		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance			17		Ω

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				100	mA
$I_{DDA}$	Analog Supply Current				12	mA
$I_{DDO}$	Output Supply Current	No Load			10	mA

**Table 3B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	OE, F_SEL $V_{DD} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current	OE, F_SEL $V_{DD} = 3.465V, V_{IN} = 0V$	-150			$\mu A$
$V_{OH}$	Output High Voltage; NOTE 1	$V_{DDO} = 3.3V \pm 5\%$	2.6			V
$V_{OL}$	Output Low Voltage; NOTE 1	$V_{DDO} = 3.3V \pm 5\%$			0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section. *Load Test Circuit diagram*.

**Table 4. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{out}$	Output Frequency	F_SEL = 1	112		140	MHz
		F_SEL = 0	56		70	MHz
$t_{sk(o)}$	Output Skew: NOTE 1, 2				80	ps
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 3	125MHz, Integration Range: 1.875MHz – 20MHz		0.70		ps
		62.5MHz, Integration Range: 1.875MHz – 20MHz		0.54		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	F_SEL = 0	48		52	%
		F_SEL = 1	46		54	%

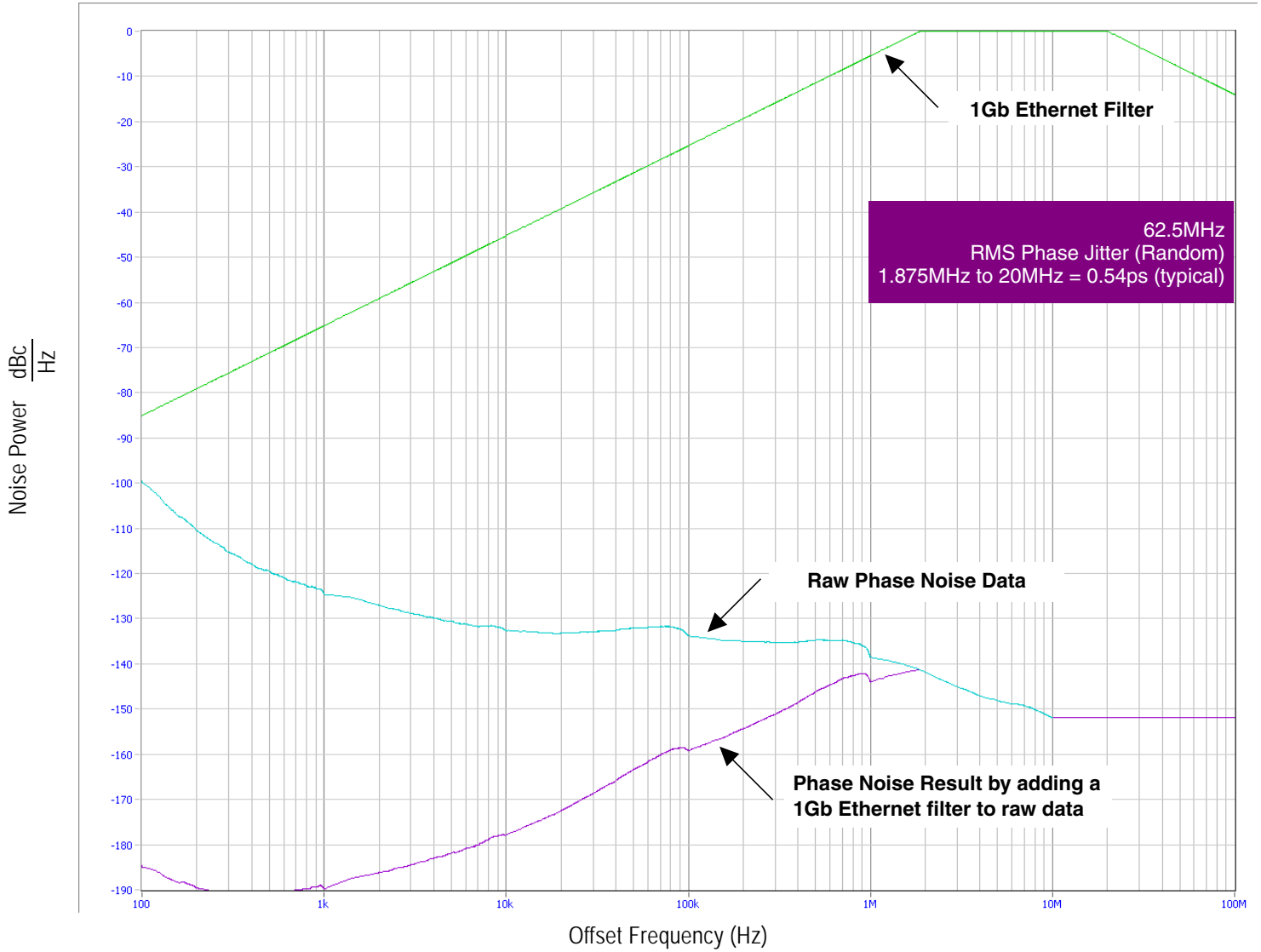
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

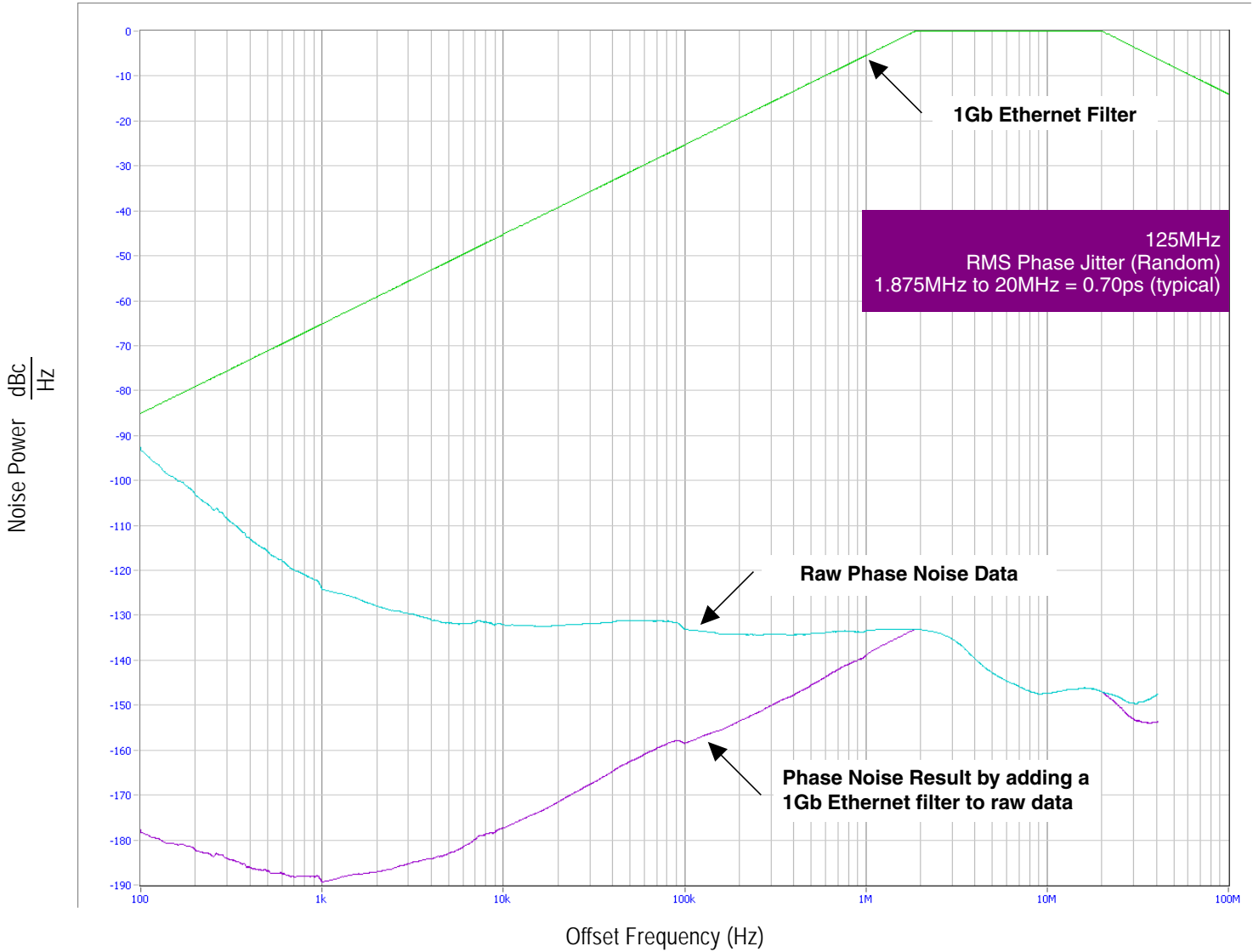
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plots.

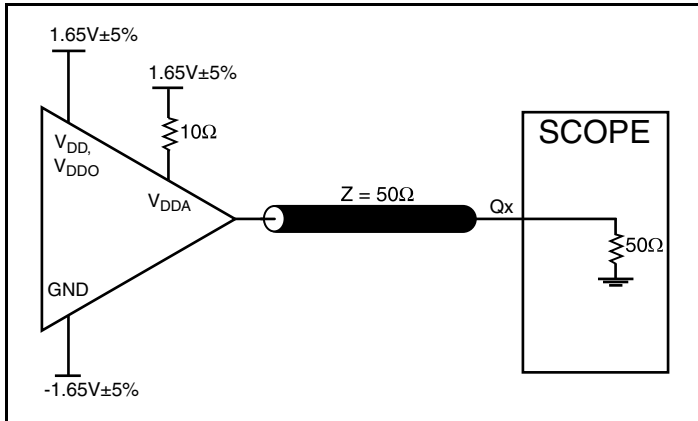
## Typical Phase Noise at 62.5MHz



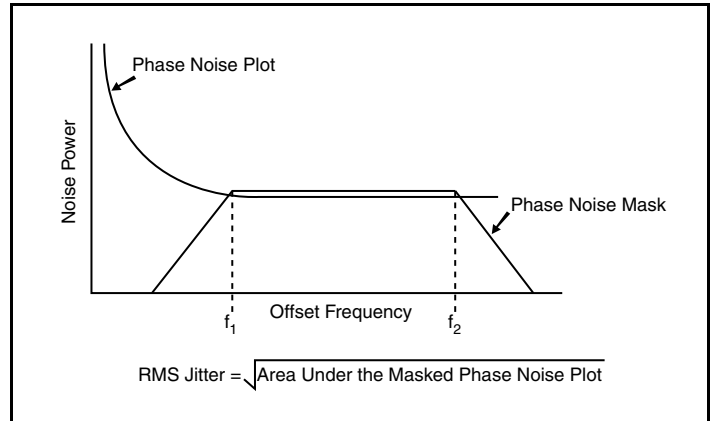
## Typical Phase Noise at 125MHz



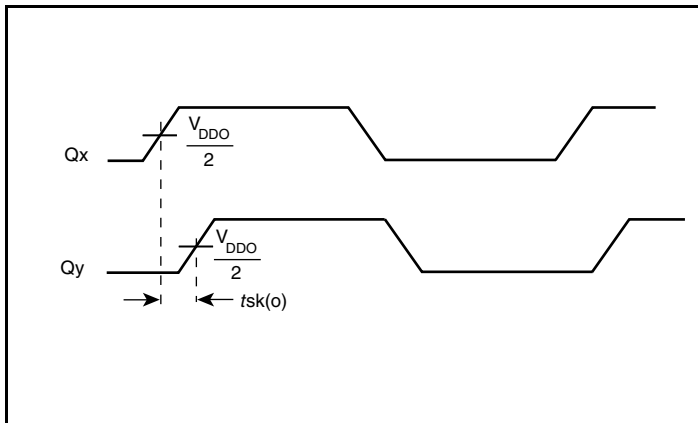
## Parameter Measurement Information



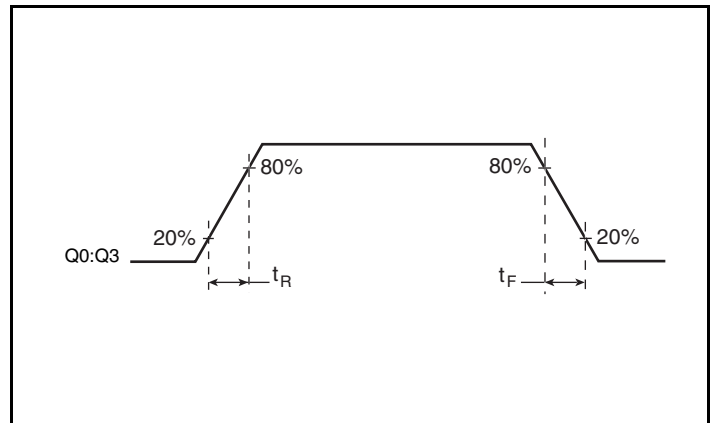
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



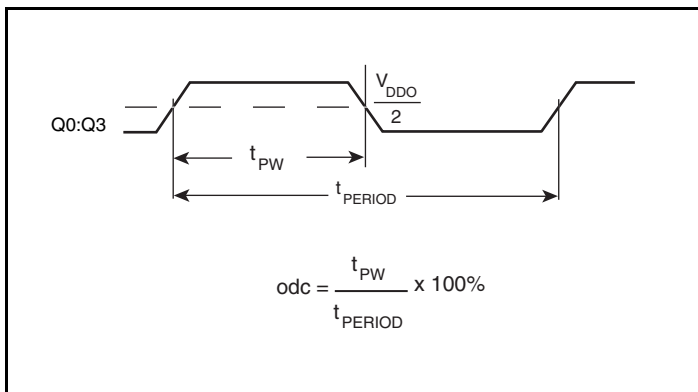
RMS Phase Jitter



Output Skew



Output Rise/Fall Time



Output Duty Cycle Pulse Width/Period

## Application Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Outputs:

##### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. We recommend that there is no trace attached.

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 840004-11 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and 0.01μF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional 10Ω resistor along with a 10μF bypass capacitor be connected to the  $V_{DDA}$  pin.

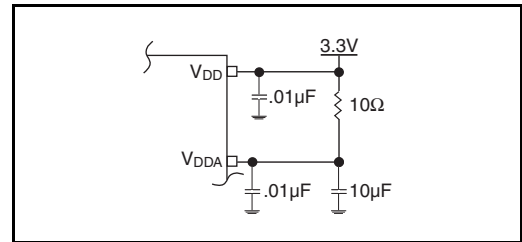


Figure 1. Power Supply Filtering

## Crystal Input Interface

The 840004-11 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

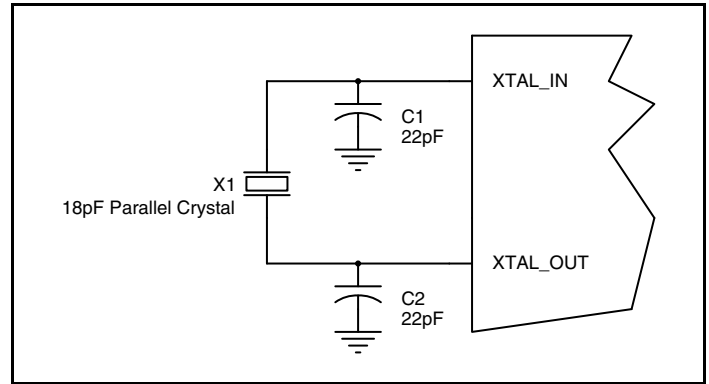


Figure 2. Crystal Input Interface

## LVC MOS to XTAL Interface

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals

the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

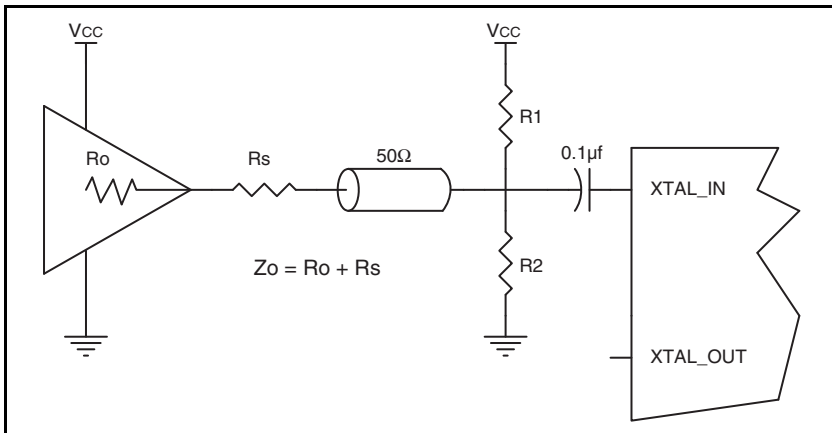


Figure 3. General Diagram for LVC MOS Driver to XTAL Input Interface

## Reliability Information

Table 6.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

Linear Feet per Minute	$\theta_{JA}$ by Velocity		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## Transistor Count

The transistor count for 840004-11: 1795

## Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

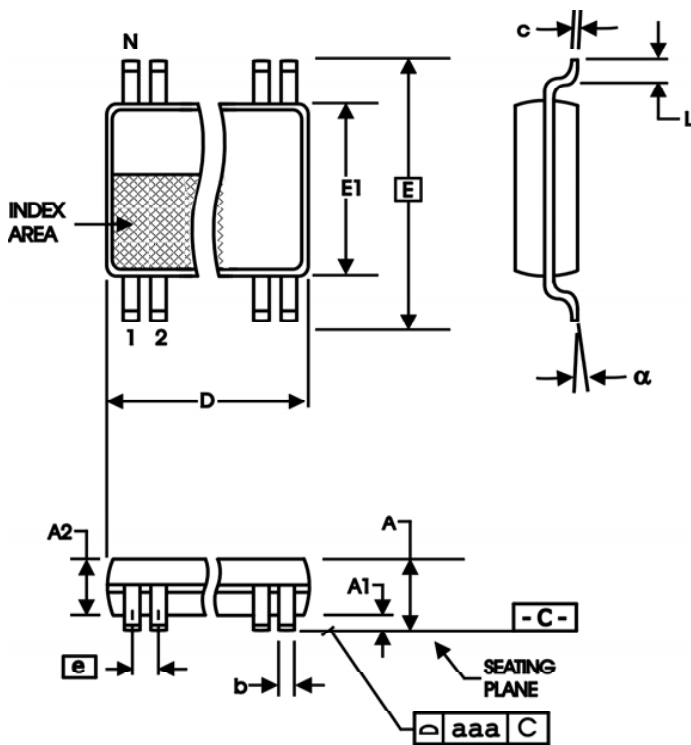


Table 7. Package Dimensions for 20 Lead TSSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

**Table 8. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840004AG-11LF	ICS40004A11L	20 Lead "Lead-Free" TSSOP	Tube	0°C to 70°C
840004AG-11LFT	ICS40004A11L	20 Lead "Lead-Free" TSSOP	Tape & Reel	0°C to 70°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T5	4	AC Characteristics Tables - added Thermal note.	9/16/09
		9	Added LVCMOS to XTAL Interface section.	
	T8	11	Ordering Information Table - deleted "ICS" prefix from Part/Order Number column. Converted datasheet format.	
A	T8	11	Ordering Information - removed leaded devices, quantity for tape and reel and the LF note below the table. Updated datasheet format.	12/7/15



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