



**THE DATASHEET OF
74CBTLV3861PW,118**



74CBTLV3861

10-bit bus switch with output enable

Rev. 5 — 16 February 2021

Product data sheet

1. General description

The 74CBTLV3861 is a 10-bit bus switch with one output enable (\overline{OE}) input. When \overline{OE} is LOW, the switch is closed and port A is connected to the B port. When \overline{OE} is HIGH, the switch is disabled.

To ensure the high-impedance OFF-state during power-up or power-down, \overline{OE} should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

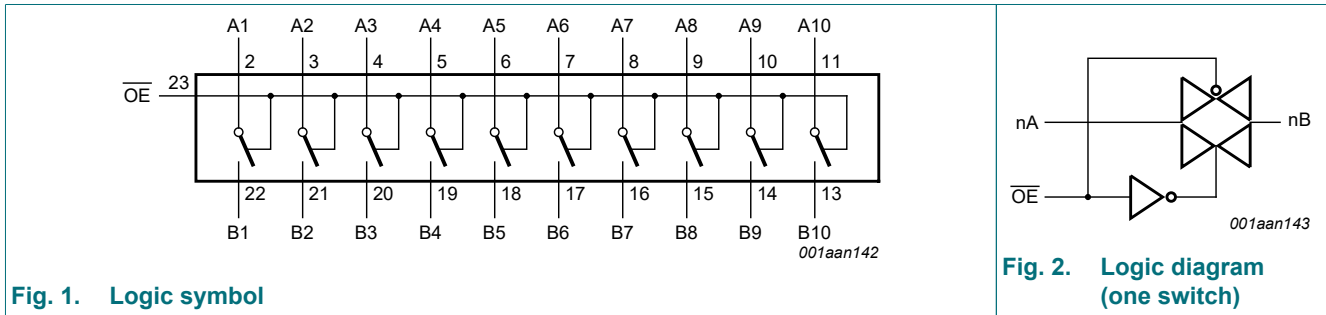
- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

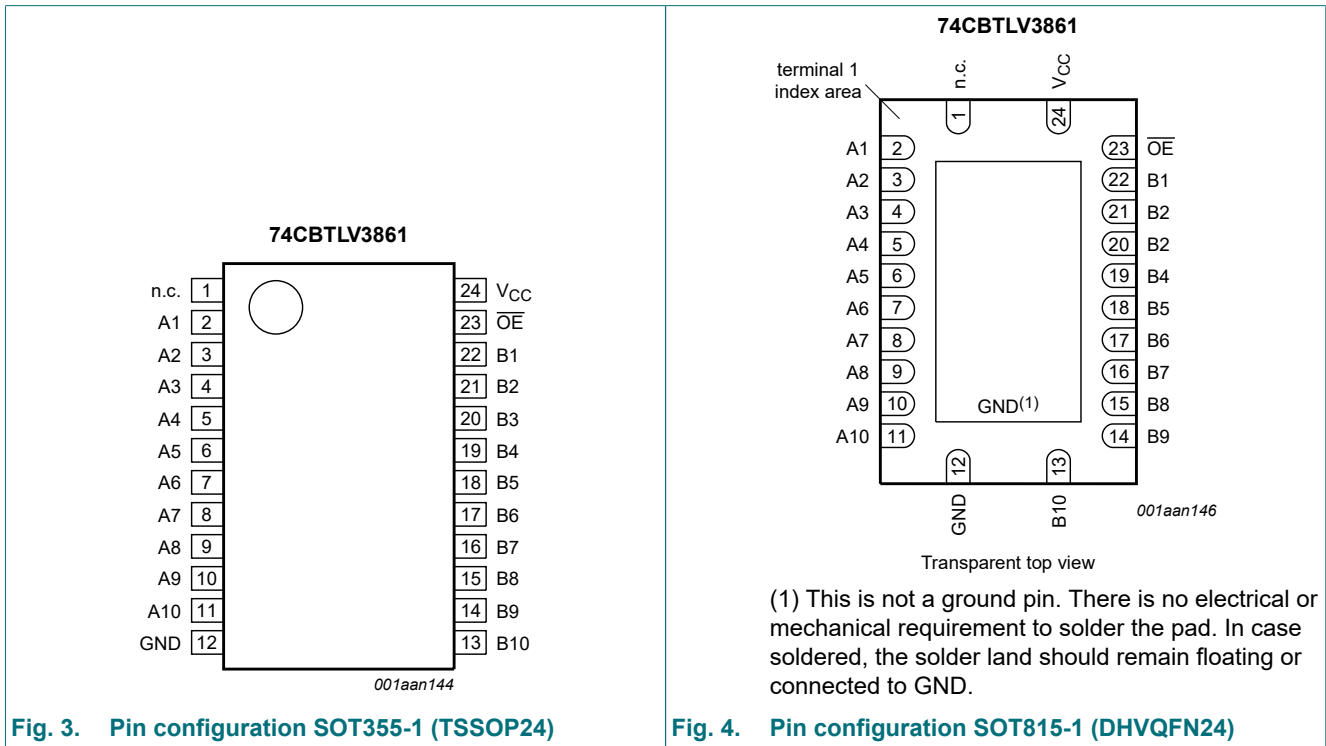
Type number	Package			
	Temperature range	Name	Description	Version
74CBTLV3861PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74CBTLV3861BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A1, A2, A3, A4, A5, A6, A7, A8, A9, A10	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	data input/output (A port)
GND	12	ground (0 V)
B1, B2, B3, B4, B5, B6, B7, B8, B9, B10	22, 21, 20, 19, 18, 17, 16, 15, 14, 13	data input/output (B port)
OE	23	output enable input (active LOW)
V _{CC}	24	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Input/output
OE	An, Bn
L	An = Bn
H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode [1]	-0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SW}	switch current	$V_{SW} = 0$ V to V_{CC}	-	± 128	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT815-1 (DHVQFN24) package: P_{tot} derates linearly with 15.0 mW/K above 117 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage		0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.6 V [1]	-	200	ns/V

[1] Applies to control signal levels.

9. Static characteristics

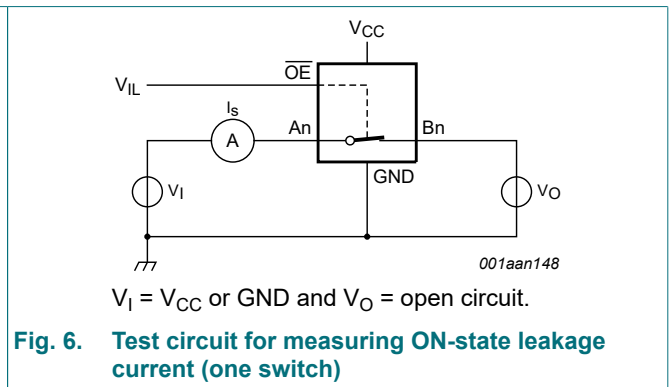
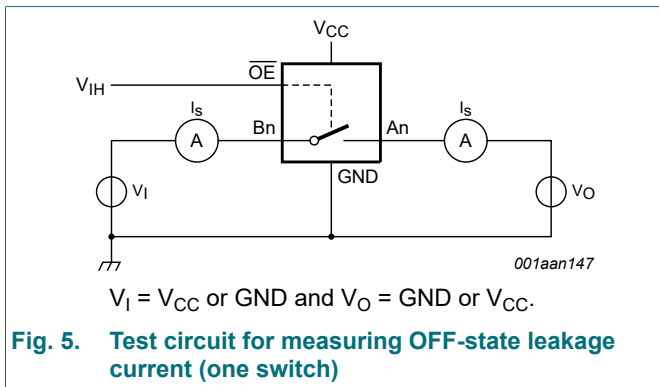
Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I _I	input leakage current	pin \overline{OE} ; V _I = GND to V _{CC} ; V _{CC} = 3.6 V	-	-	±1	-	±20	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see Fig. 5	-	-	±1	-	±20	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see Fig. 6	-	-	±1	-	±20	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±10	-	±50	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	-	-	10	-	50	µA
ΔI _{CC}	additional supply current	pin \overline{OE} ; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V; One input at 3 V, other inputs at V _{CC} or GND.	-	-	300	-	2000	µA
C _I	input capacitance	pin \overline{OE} ; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	5.2	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	14.3	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

9.1. Test circuits



9.2. ON resistance

Table 7. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ [1]	Max	Min	Max	
R_{ON}	ON resistance	$V_{CC} = 2.3\text{ V}$ to 2.7 V ; see Fig. 8 to Fig. 10 [2]						
		$I_{SW} = 64\text{ mA}$; $V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	Ω
		$I_{SW} = 24\text{ mA}$; $V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	Ω
		$I_{SW} = 15\text{ mA}$; $V_I = 1.7\text{ V}$	-	8.4	40	-	60.0	Ω
		$V_{CC} = 3.0\text{ V}$ to 3.6 V ; see Fig. 11 to Fig. 13						
		$I_{SW} = 64\text{ mA}$; $V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	Ω
		$I_{SW} = 24\text{ mA}$; $V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	Ω
$I_{SW} = 15\text{ mA}$; $V_I = 2.4\text{ V}$	-	6.2	15	-	25.5	Ω		

- [1] Typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$ and nominal V_{CC} .
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.3. ON resistance test circuit and graphs

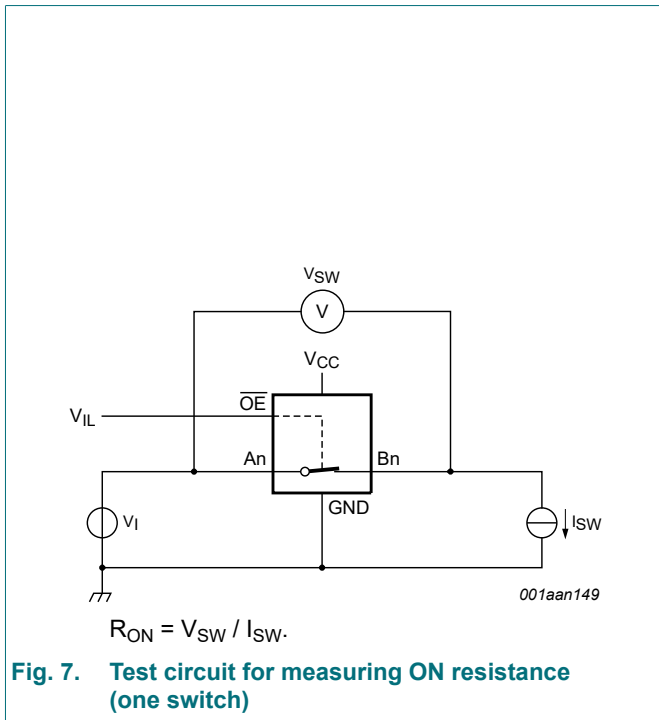
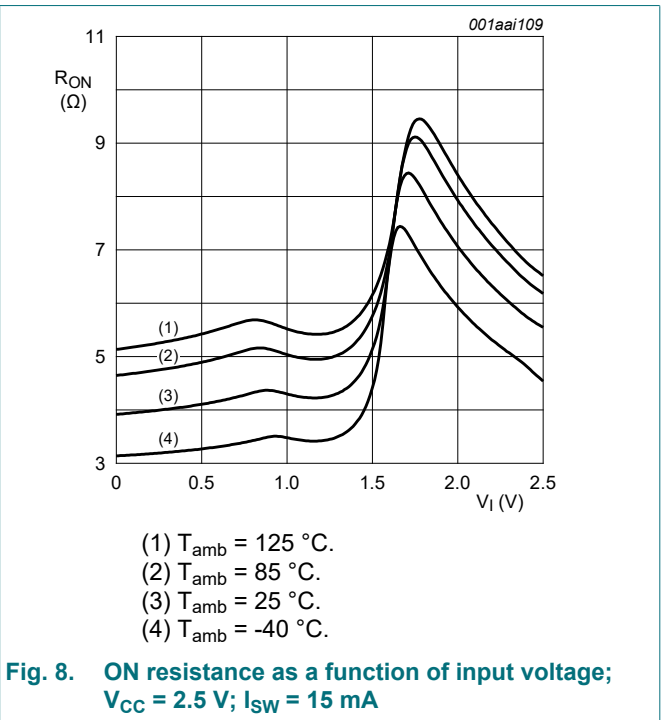
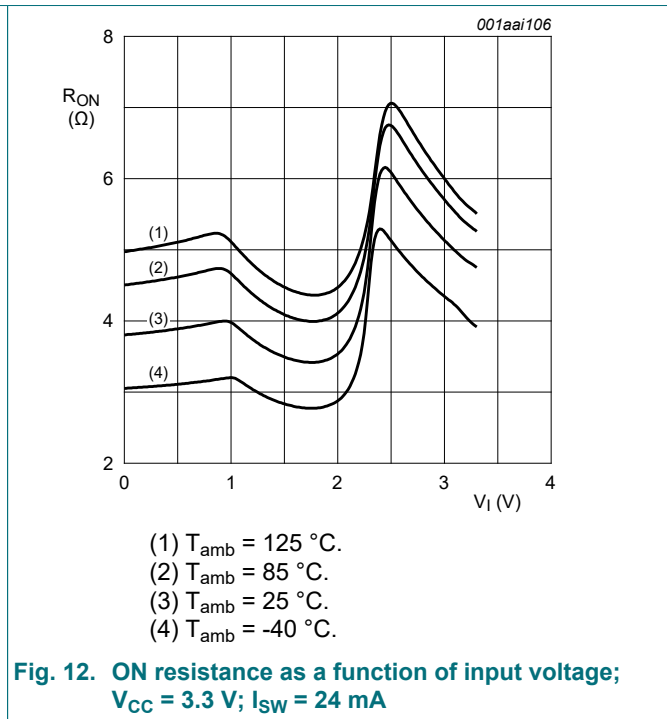
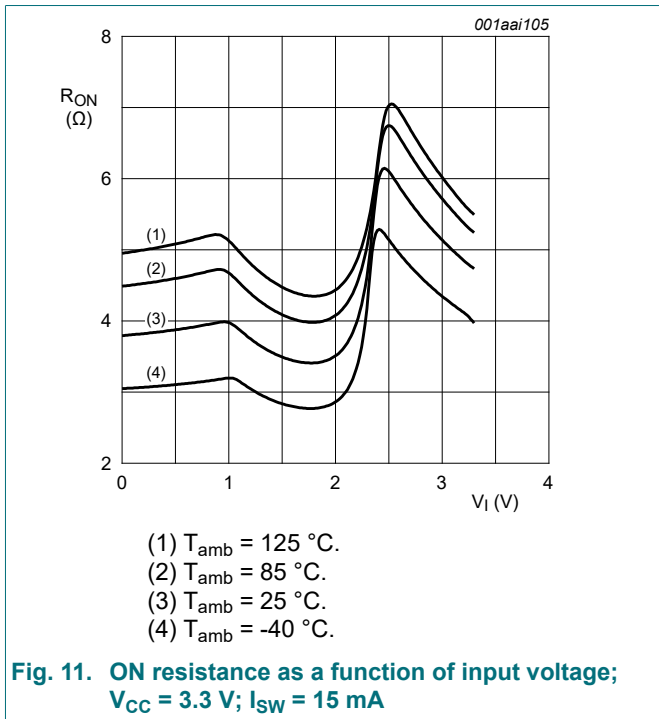
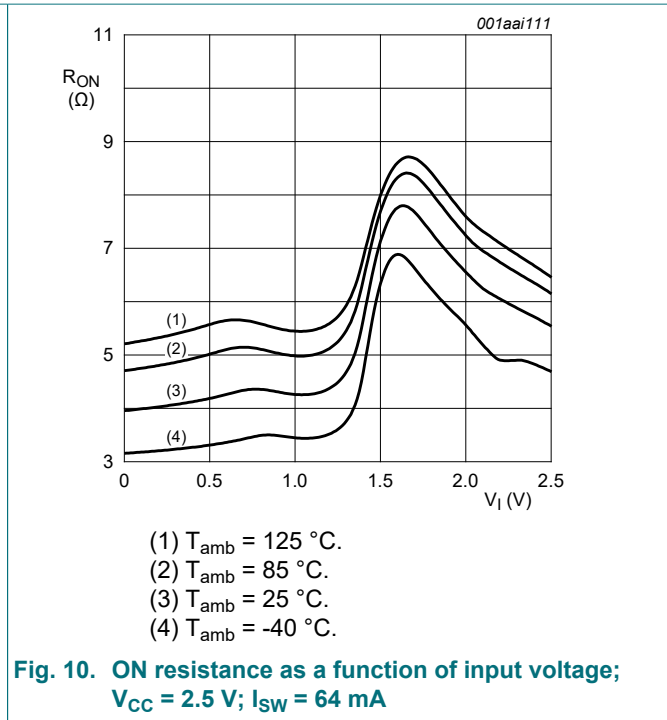
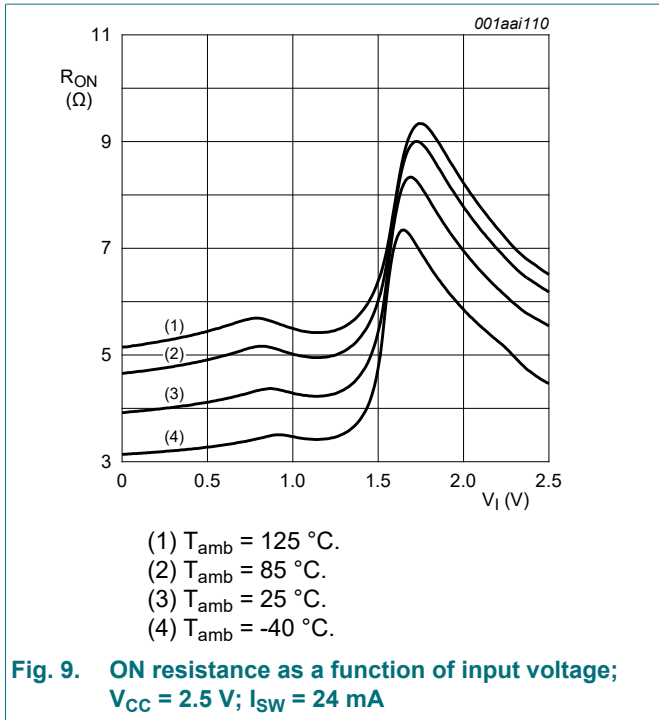
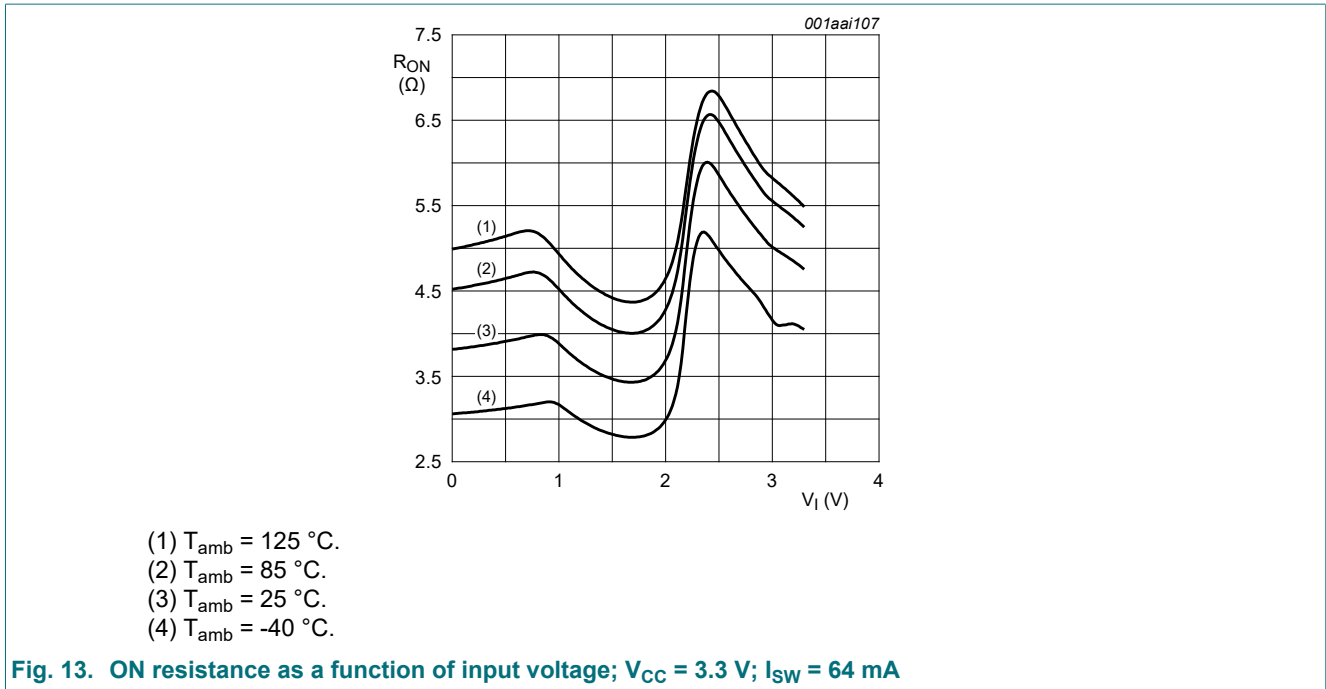


Fig. 7. Test circuit for measuring ON resistance (one switch)







10. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit see Fig. 16

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	An to Bn or Bn to An; see Fig. 14 [2] [3]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.13	-	0.20	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.20	-	0.31	ns
t_{en}	enable time	\overline{OE} to An or Bn; see Fig. 15 [4]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.9	5.5	1.0	8.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.4	4.9	1.0	7.0	ns
t_{dis}	disable time	\overline{OE} to An or Bn; see Fig. 15 [5]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.6	5.5	1.0	8.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.1	5.8	1.0	8.5	ns

[1] All typical values are measured at $T_{amb} = 25\text{ °C}$ and at nominal V_{CC} .

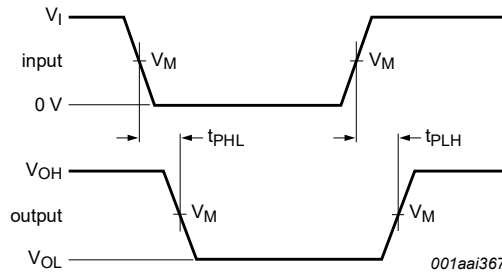
[2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

[3] t_{pd} is the same as t_{PLH} and t_{PHL} .

[4] t_{en} is the same as t_{PZH} and t_{PZL} .

[5] t_{dis} is the same as t_{PHZ} and t_{PLZ} .

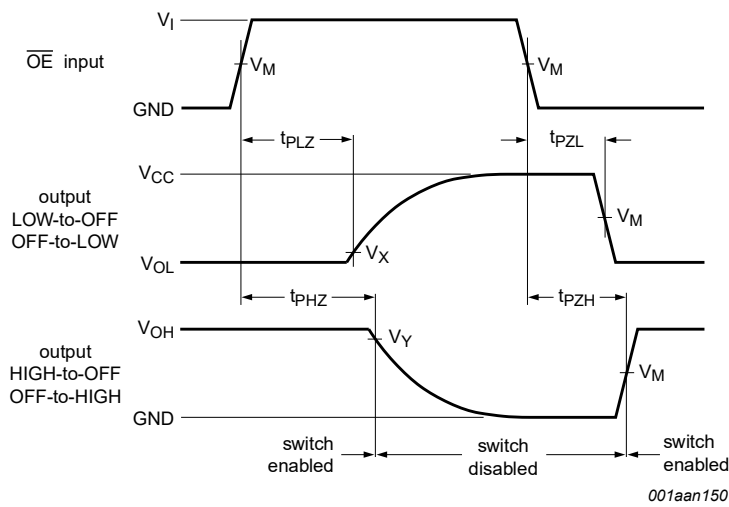
10.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 14. The data input (An, Bn) to output (Bn, An) propagation delay times



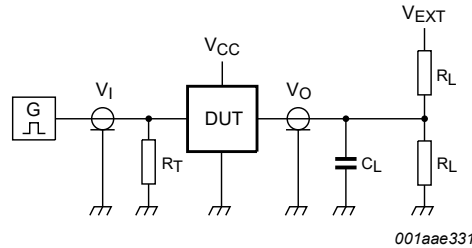
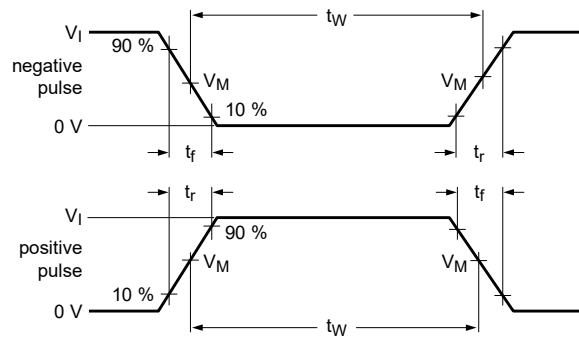
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 15. Enable and disable times

Table 9. Measurement points

Supply voltage	Input			Output		
	V_M	V_I	$t_r = t_f$	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns	$0.5V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	≤ 2.0 ns	$0.5V_{CC}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



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Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 16. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	open	GND	$2V_{CC}$
3.0 V to 3.6 V	50 pF	500 Ω	open	GND	$2V_{CC}$

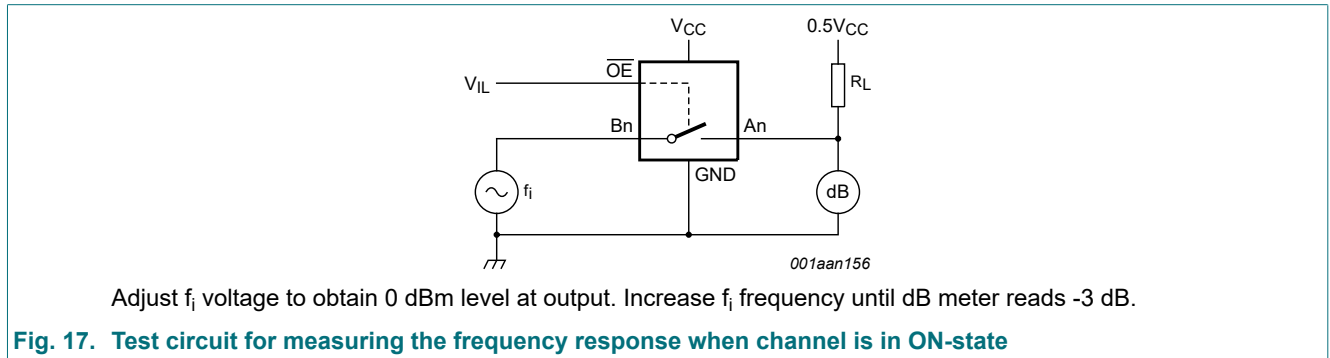
10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

GND = 0 V.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
f _{i(-3dB)}	-3 dB frequency response	V _{CC} = 3.3 V; R _L = 50 Ω; see Fig. 17 [1]	-	406	-	MHz

[1] f_i is biased at 0.5V_{CC}.



11. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

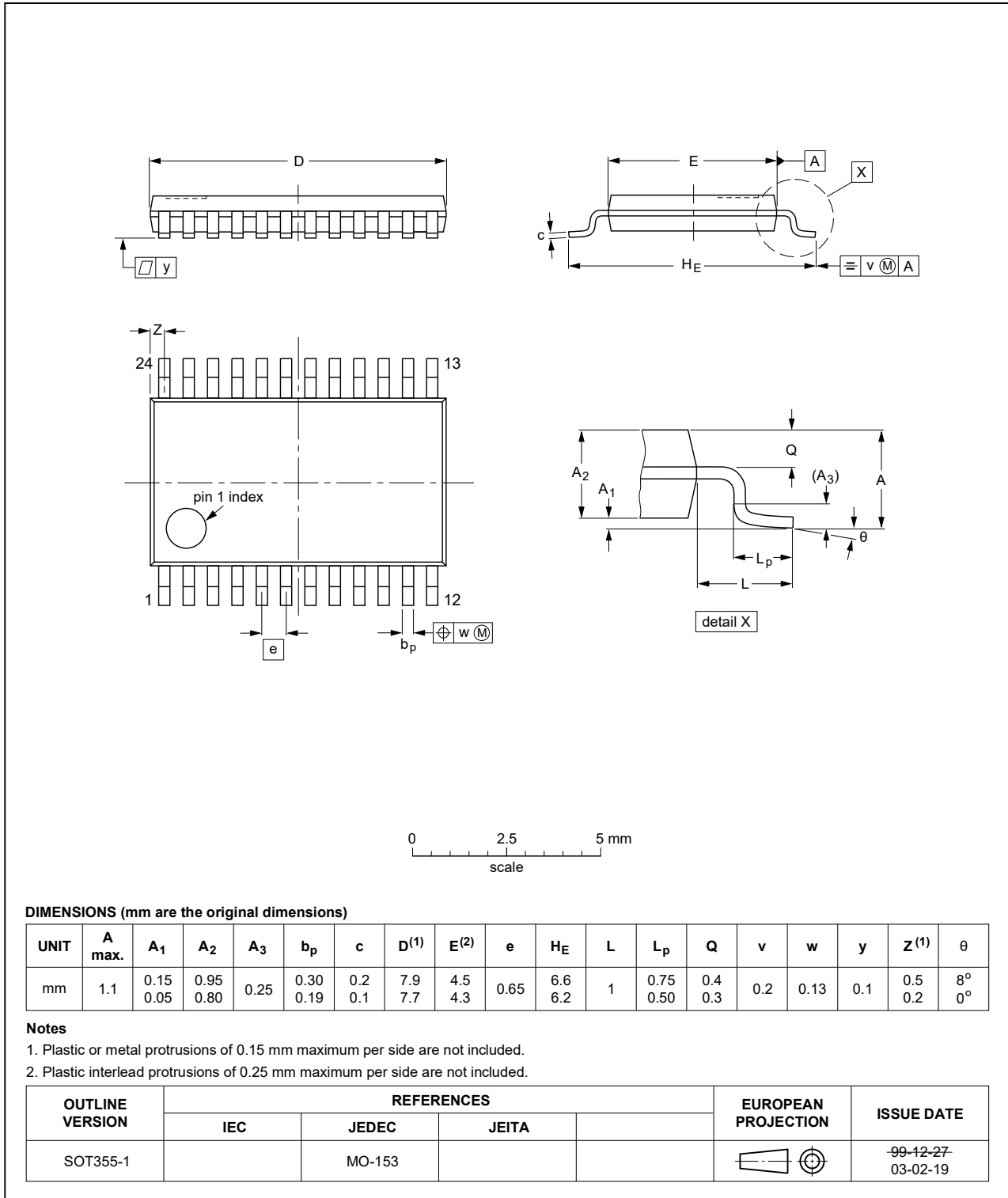


Fig. 18. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

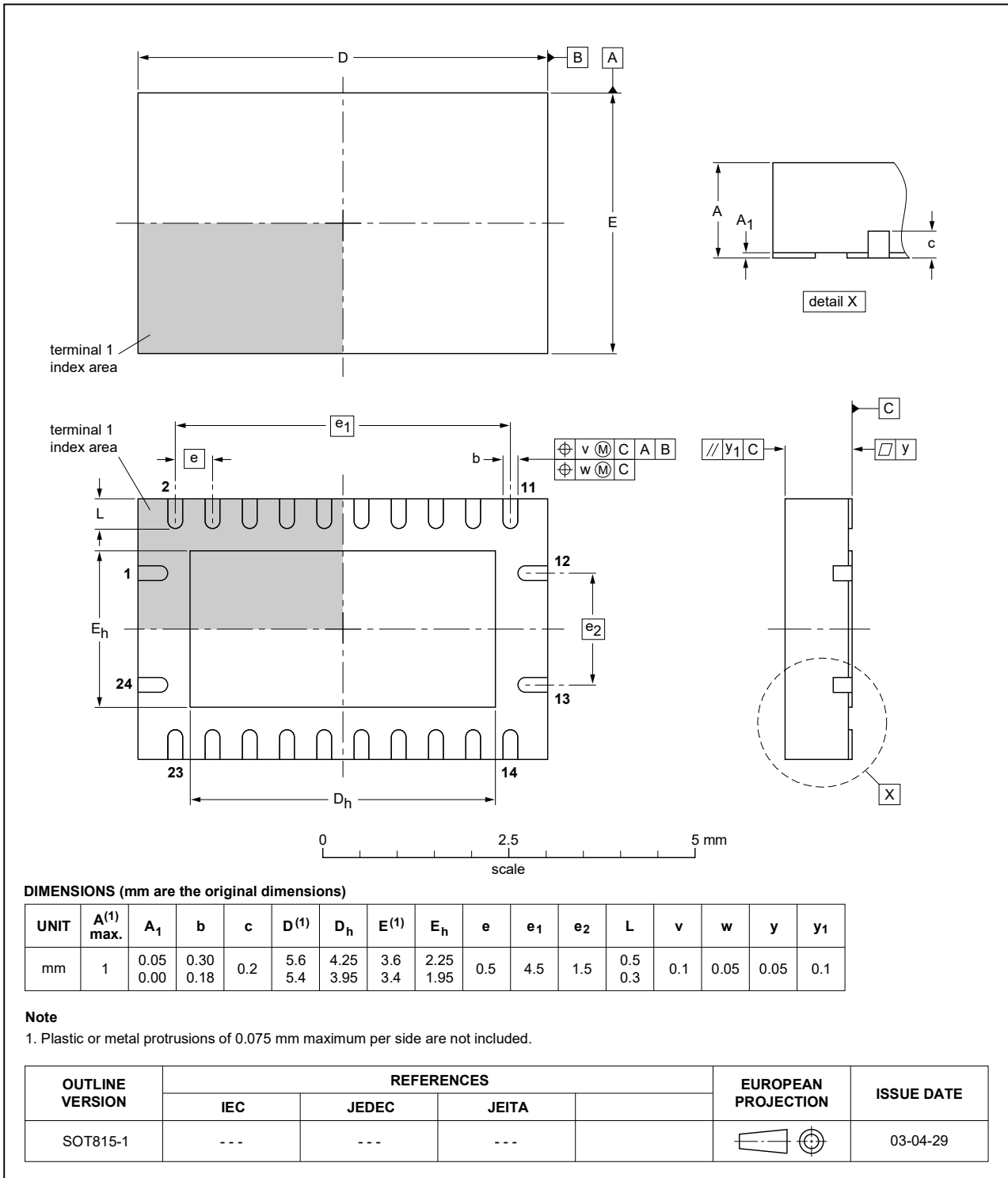


Fig. 19. Package outline SOT815-1 (DHVQFN24)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3861 v.5	20210216	Product data sheet	-	74CBTLV3861 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74CBTLV3861DK (SOT556-1 / SSOP24) removed. Section 7: P_{tot} total power dissipation and it's derating values for updated. 			
74CBTLV3861 v.4	20161111	Product data sheet	-	74CBTLV3861 v.3
Modifications:	<ul style="list-style-type: none"> Section 10.2 added. 			
74CBTLV3861 v.3	20111216	Product data sheet	-	74CBTLV3861 v.2
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74CBTLV3861 v.2	20110120	Product data sheet	-	74CBTLV3861 v.1
74CBTLV3861 v.1	20101206	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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