



**THE DATASHEET OF  
74ALVCH16841DGGY**





# 74ALVCH16841

20-bit bus interface D-type latch; 3-state

Rev. 4 — 10 July 2024

Product data sheet

## 1. General description

The 74ALVCH16841 has two 10-bit D-type latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable (nLE) and output enable (nOE) control gates.

When nOE is LOW, the data in the registers appears at the outputs. When nOE is HIGH the outputs are in High-impedance OFF state. Operation of the nOE input does not affect the state of the flip-flops.

The 74ALVCH16841 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## 2. Features and benefits

- Wide supply voltage range of 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive  $\pm 24$  mA at  $V_{CC} = 3.0$  V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimize noise and ground bounce
- All data inputs have bushold
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- 3-state non-inverting outputs for bus oriented applications
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74ALVCH16841DGG</a>	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	<a href="#">SOT364-1</a>

### 4. Functional diagram

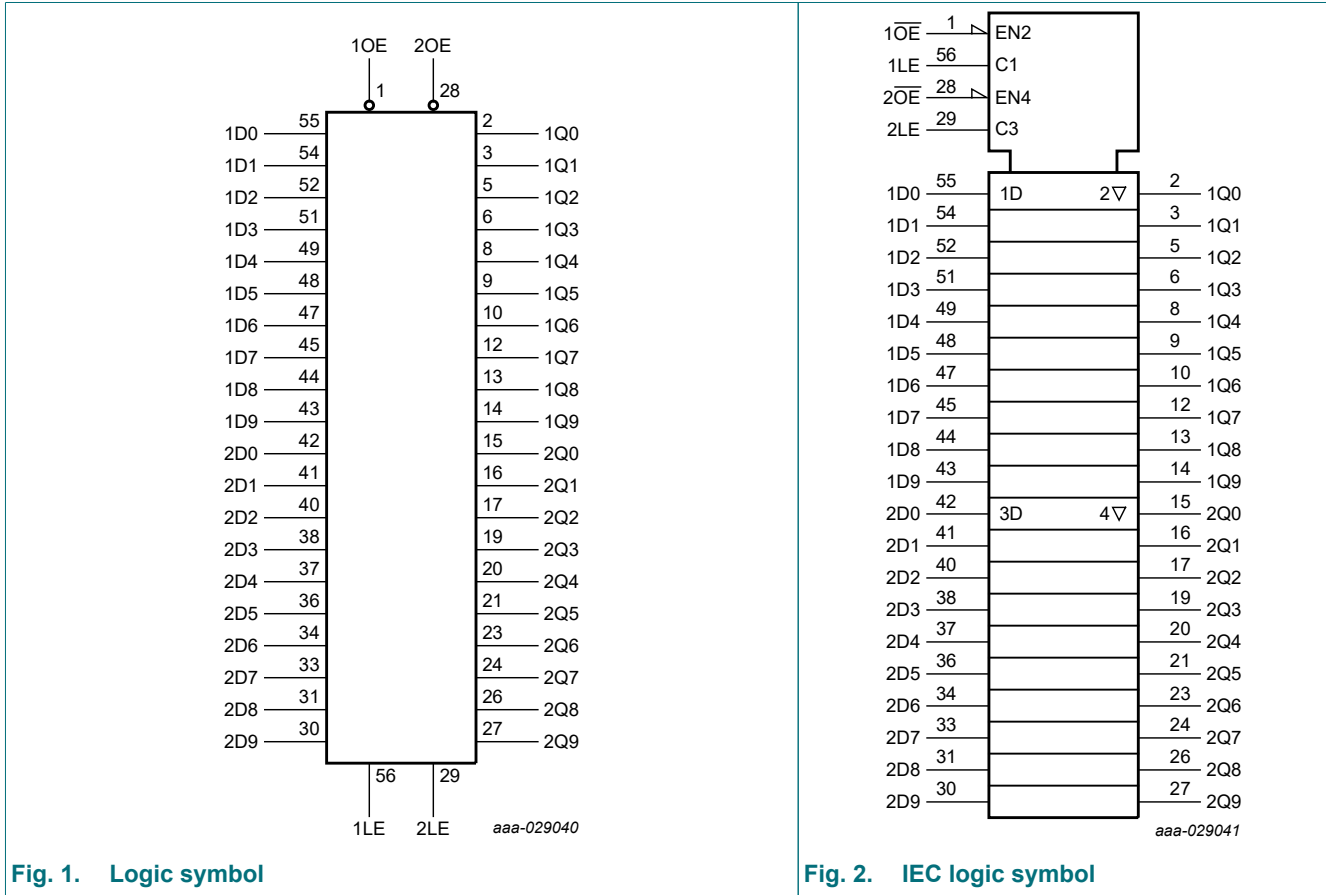


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

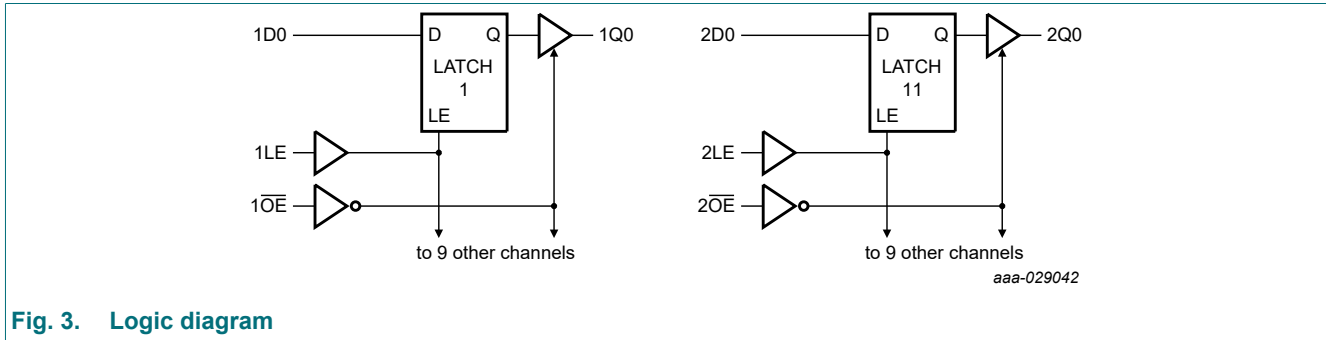


Fig. 3. Logic diagram

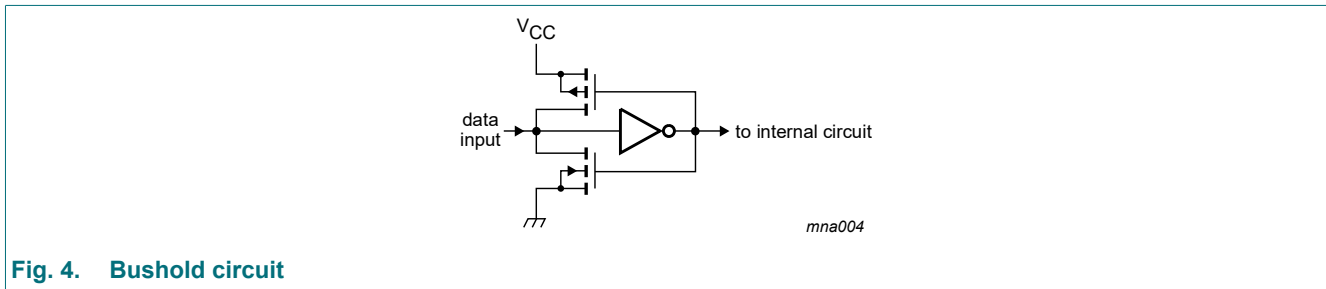
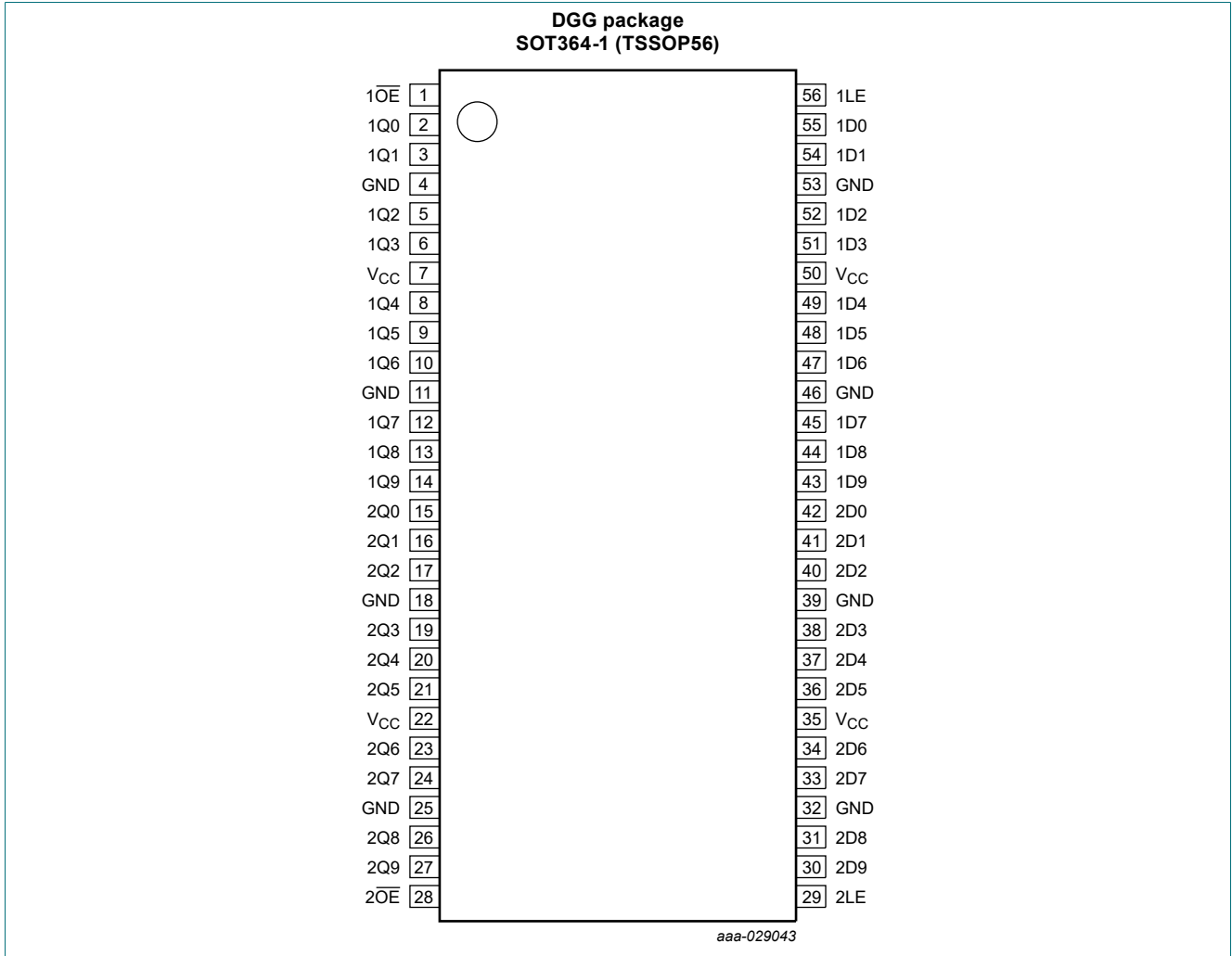


Fig. 4. Bushold circuit

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8, 1D9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data input
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8, 2D9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data input
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8, 1Q9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data output
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8, 2Q9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data output
1OE, 2OE	1, 28	output enable inputs (active-LOW)
1LE, 2LE	56, 29	latch enable inputs
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V <sub>CC</sub>	7, 22, 35, 50	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Inputs			Outputs
nOE	nLE	nDn	nQn
L	H	L	L
L	H	H	H
L	L	X	Q <sub>0</sub>
H	X	X	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage	For control pins [1]	-0.5	+4.6	V
		For data inputs [1]	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	output voltage	[1]	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage	for maximum speed performance; 30 pF output load	2.3	2.7	V
		for maximum speed performance; 50 pF output load	3.0	3.6	V
V <sub>I</sub>	input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.3 V to 3.0 V	-	20	ns/V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 2.3 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 2.3 V to 3.6 V	-	GND	0.20	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.3 V	-	0.07	0.40	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.15	0.70	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.14	0.40	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.27	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	5	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	0.1	10	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	40	µA
ΔI <sub>CC</sub>	additional supply current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	150	750	µA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 0.7 V	45	-	-	µA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V	75	150	-	µA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 1.7 V	-45	-	-	µA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V	-75	-175	-	µA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 3.6 V	500	-	-	µA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6 V	-500	-	-	µA
C <sub>I</sub>	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
$t_{pd}$	propagation delay	nDn to nQn; see Fig. 5 [2]				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.5	5.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.6	4.7	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.4	3.9	ns
		nLE to nQn; see Fig. 6				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.5	5.6	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.6	5.1	ns
$t_{en}$	enable time	$\overline{\text{nOE}}$ to nQn; see Fig. 8 [3]				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.7	6.2	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.1	6.0	ns
$t_{dis}$	disable time	$\overline{\text{nOE}}$ to nQn; see Fig. 8 [4]				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.1	2.2	5.3	ns
		$V_{CC} = 2.7 \text{ V}$	1.3	3.1	4.3	ns
$t_{su}$	set-up time	$\overline{\text{nOE}}$ to nQn; see Fig. 8 [4]				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.1	2.2	5.3	ns
		$V_{CC} = 2.7 \text{ V}$	1.3	3.1	4.3	ns
$t_h$	hold time	nDn to nLE; see Fig. 7				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.4	0.3	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.7	0.2	-	ns
$t_w$	pulse width	nLE HIGH; $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$ ; see Fig. 6	3.3	1.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.4	0.2	-	ns
$C_{PD}$	power dissipation capacitance	per latch; $V_I = \text{GND to } V_{CC}$ [5]				
		outputs enabled	-	19	-	pF
		outputs disabled	-	3	-	pF

[1] Typical values are measured at  $T_{amb} = 25 \text{ °C}$ .

Typical values for  $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$  are measured at  $V_{CC} = 2.5 \text{ V}$ .

Typical values for  $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$  are measured at  $V_{CC} = 3.3 \text{ V}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

[4]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

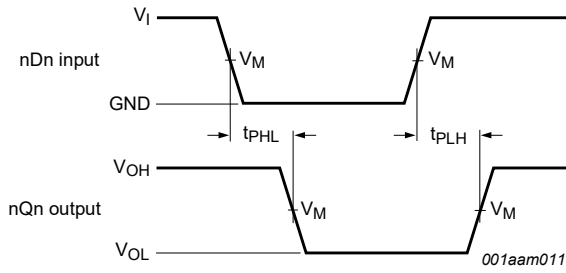
[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz;  $C_L$  = output load capacitance in pF;

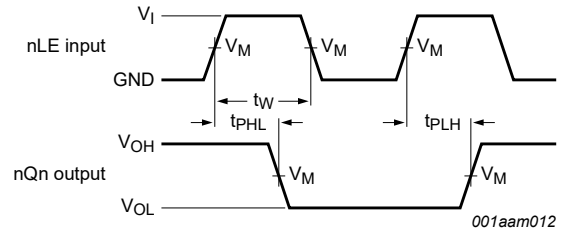
$V_{CC}$  = supply voltage in V;  $N$  = total load switching outputs;  $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

10.1. Waveforms and test circuit



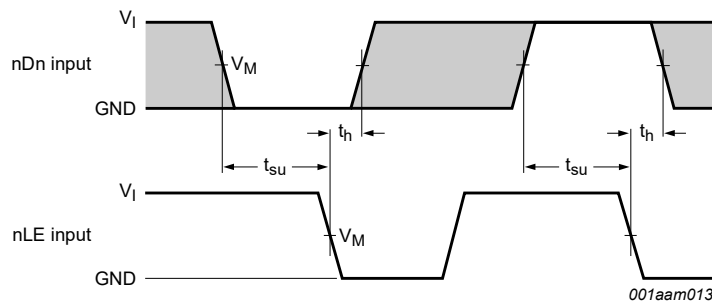
Measurement points are given in [Table 8](#).  $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 5. Input (nDn) to output (nQn) propagation delays**



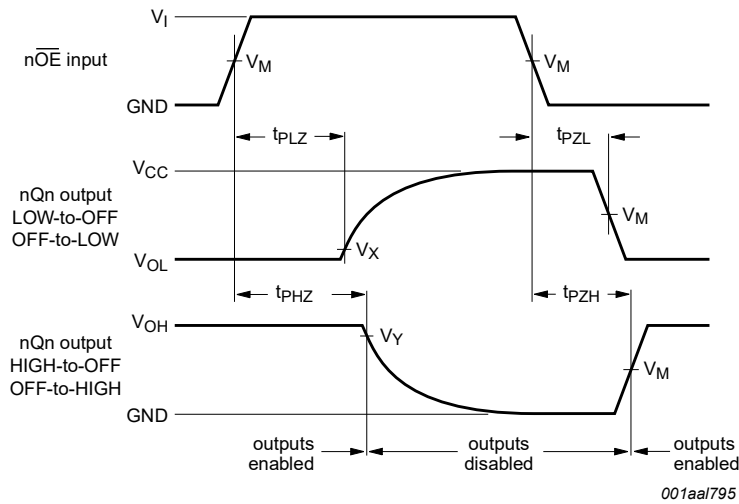
Measurement points are given in [Table 8](#).  $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 6. Latch enable input (nLE) to data output (nQn) propagation delays and pulse width (nLE)**



Measurement points are given in [Table 8](#). The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 7. Data setup and hold times for input (nDn) to input (nLE)**



Measurement points are given in [Table 8](#).  $V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

**Fig. 8. 3-State enable and disable times**

Table 8. Measurement points

Input			Output		
V <sub>CC</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>x</sub>	V <sub>y</sub>
< 2.3 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.3 V to 2.7 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V

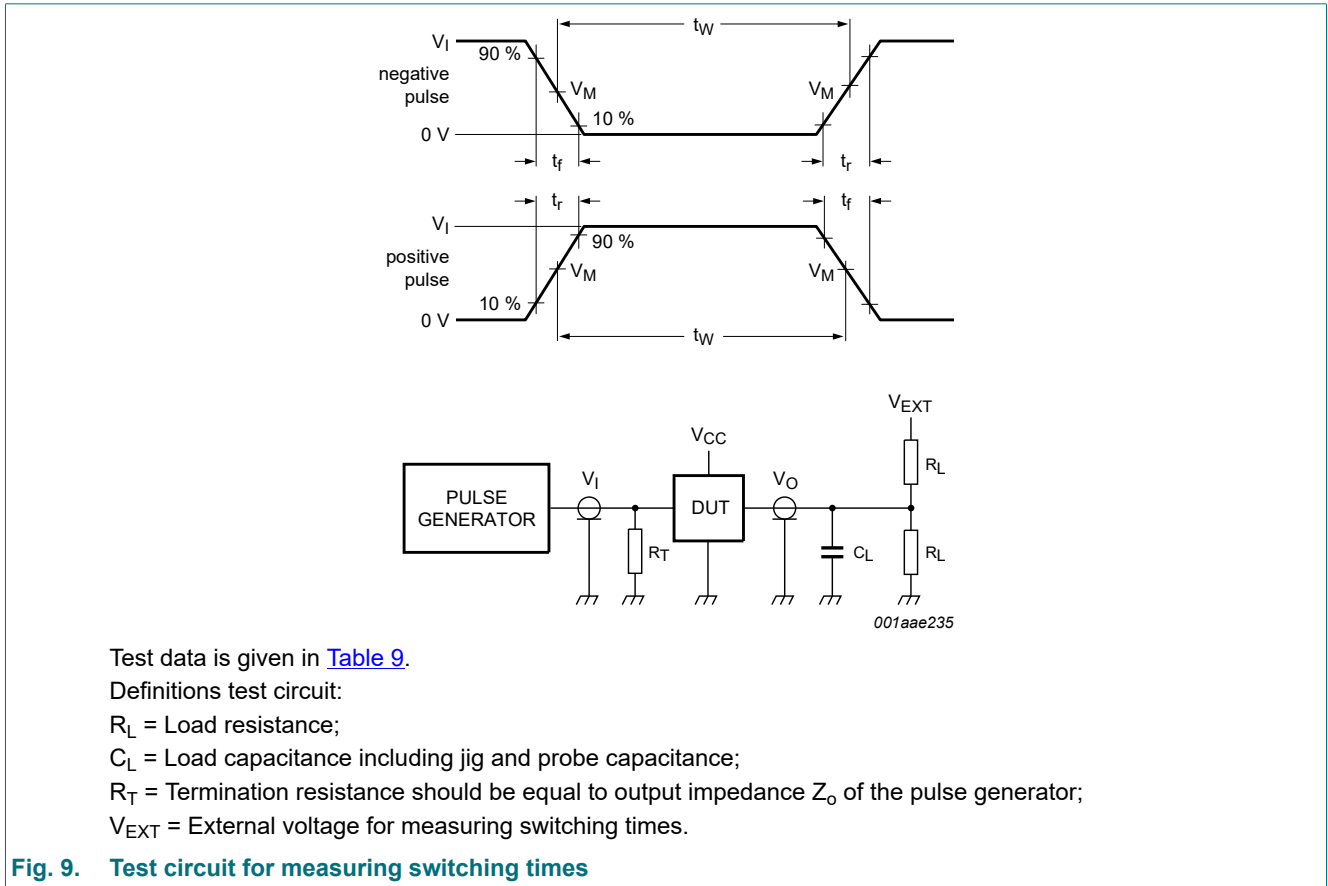


Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Input			Load		V <sub>EXT</sub>		
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	R <sub>L</sub>	C <sub>L</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>
< 2.3 V	V <sub>CC</sub>	≤ 2.0 ns	500 Ω	30 pF	GND	2 × V <sub>CC</sub>	open
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2.0 ns	500 Ω	30 pF	GND	2 × V <sub>CC</sub>	open
2.7 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V <sub>CC</sub>	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V <sub>CC</sub>	open

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

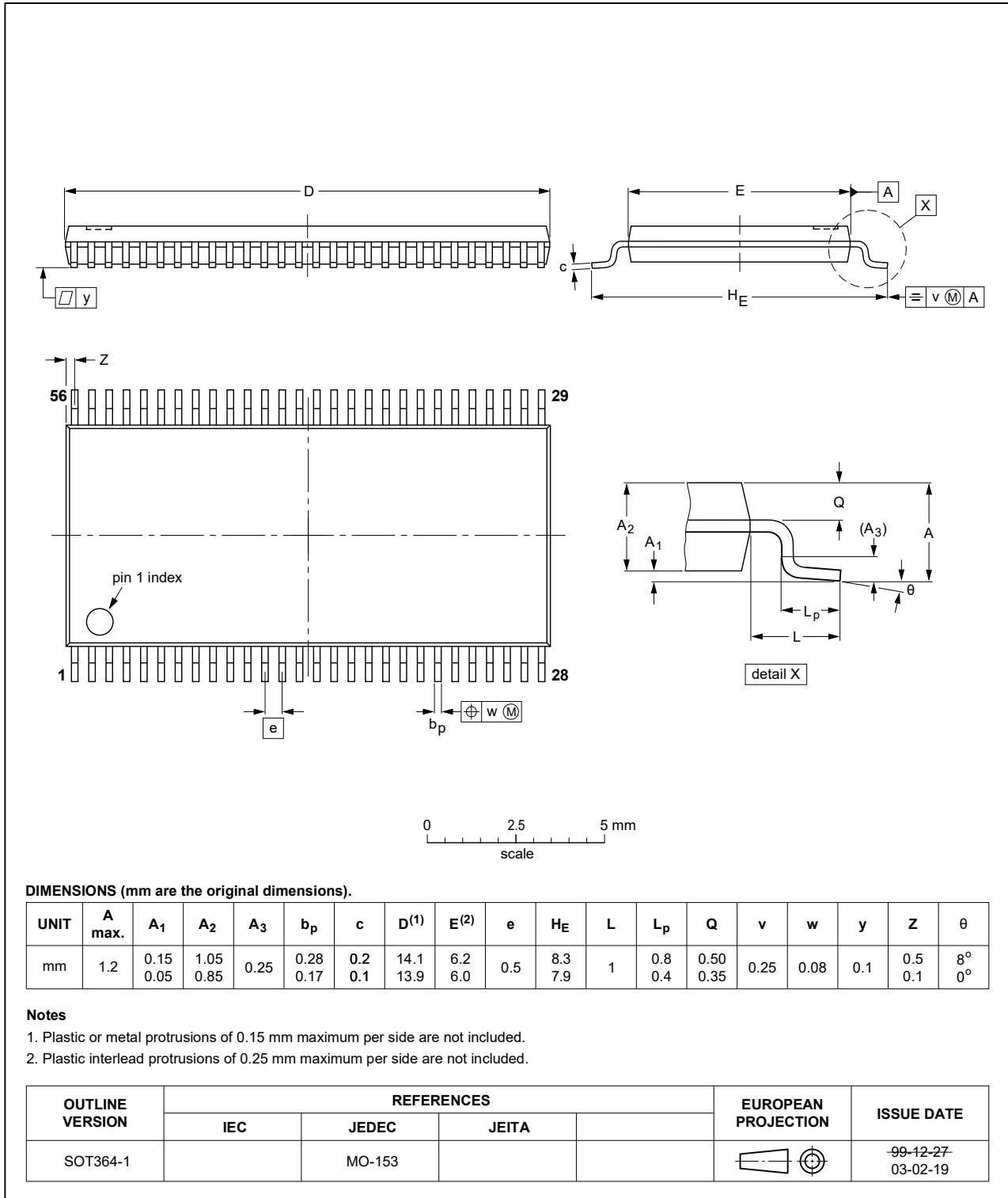


Fig. 10. Package outline SOT364-1 (TSSOP56)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16841 v.4	20240710	Product data sheet	-	74ALVCH16841 v.3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li>• <a href="#">Table 4</a>: <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74ALVCH16841 v.3	20180912	Product data sheet	-	74ALVCH16841 v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74ALVCH16841 v.2	19980727	Product specification	-	74ALVCH16841 v.1
74ALVCH16841 v.1	19980727	Product specification	-	

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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