THE DATASHEET OF

74ALVCH16373DGG:11

74ALVCH16373

2.5 V/3.3 V 16-bit D-type transparent latch; 3-state

Rev. 10 — 18 June 2024 Product data sheet

1. General description

The 74ALVCH16373 is a 16-bit D-type transparent latch with bus hold inputs and 3-state outputs. The device can be used as two 8-bit transparent latches or a single 16-bit transparent latch. The device features two latch enables (1LE and 2LE) and two output enables (1$\overline{OE}$ and 2$\overline{OE}$), each controlling 8-bits. When nLE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When nLE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of nLE. A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the n$\overline{OE}$ input does not affect the state of the latches.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power dissipation
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- Latch-up performance exceeds 100 mA per JESD78 Class II.A
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at V_{CC} = 3.0 V
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVCH16373DGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

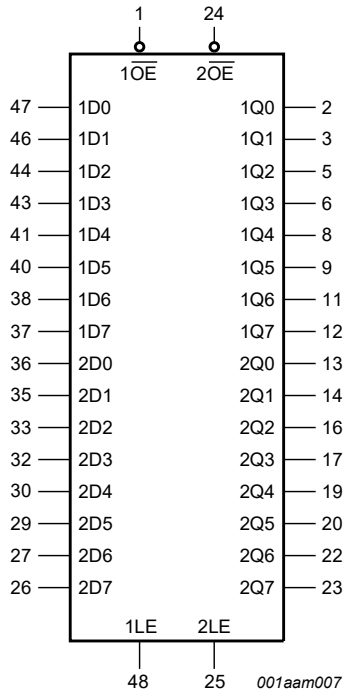


Fig. 1. Logic symbol

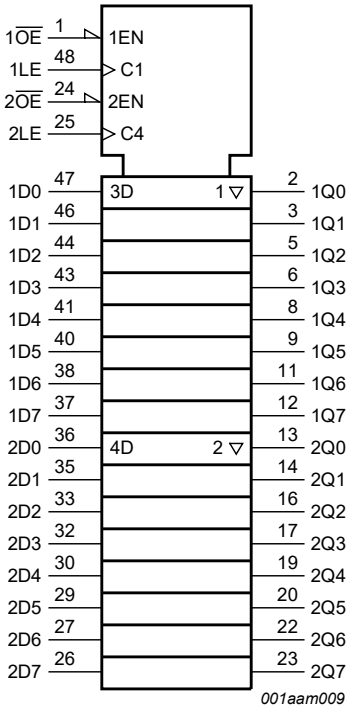


Fig. 2. IEC logic symbol

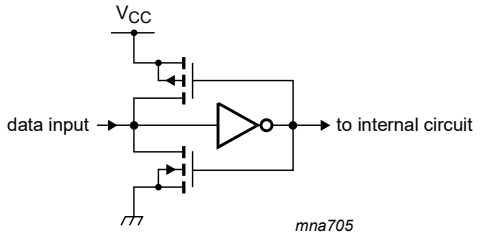


Fig. 3. Bus hold circuit

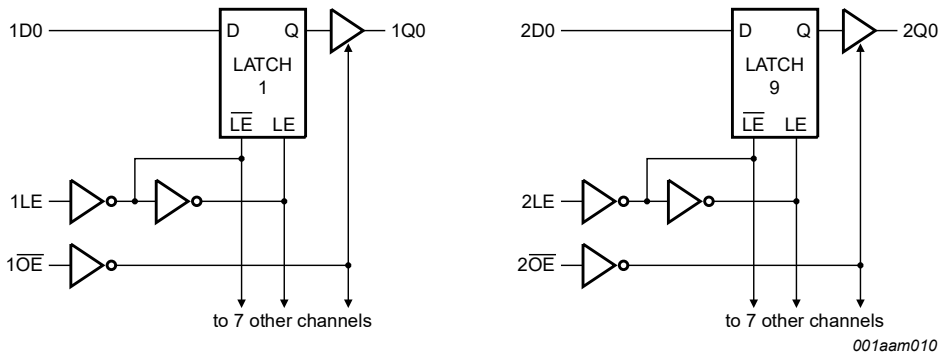
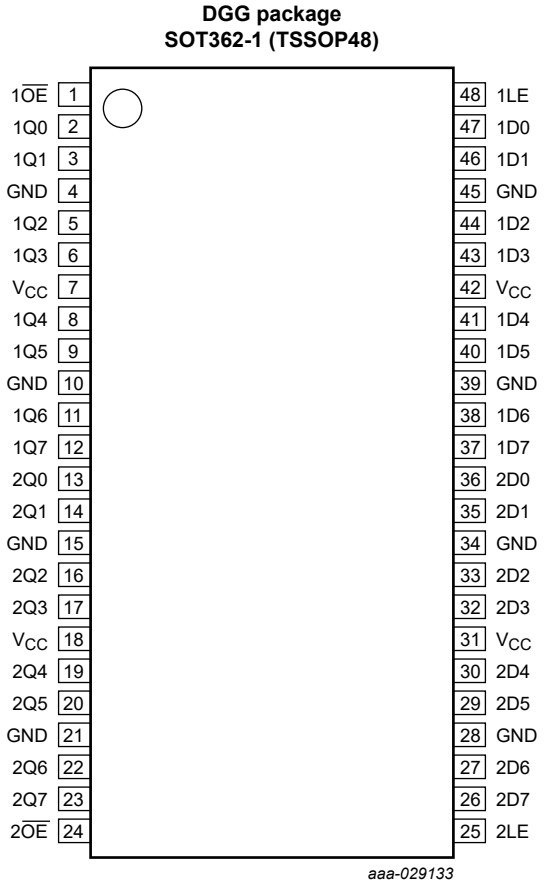


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 24	output enable input (active LOW)
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data outputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	positive supply voltage
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	47, 46, 44, 43, 41, 40, 38, 37	data inputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	36, 35, 33, 32, 30, 29, 27, 26	data inputs
1LE, 2LE	48, 25	latch enable input (active HIGH)

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition;
Z = high-impedance OFF-state.

Inputs			Internal latches	Outputs nQn	Operating mode
$n\overline{OE}$	nLE	nDn			
L	H	L	L	L	enable and read register (transparent mode)
L	H	H	H	H	
L	L	l	L	L	latch and read register (hold mode)
L	L	h	H	H	
H	L	l	L	Z	latch register and disable outputs
H	L	h	H	Z	

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage	control inputs	[1]	-0.5	+4.6	V
		data inputs	[1]	-0.5	V_{CC} + 0.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT362-1 (TSSOP48) packages: P_{tot} derates linearly with 12.2 mW/K above 109 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance				
		C_L = 30 pF	2.3	-	2.7	V
		C_L = 50 pF	3.0	-	3.6	V
		low voltage applications	1.2	-	3.6	V
V_I	input voltage	data inputs	0	-	V_{CC}	V
		control inputs	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	TBD	-	V
		V_{CC} = 1.8 V	0.7V_{CC}	0.9	-	TBD	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	TBD	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	1.5	-	TBD	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0	-	TBD	V
		V_{CC} = 1.8 V	-	0.9	0.2V_{CC}	-	TBD	V
		V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	-	TBD	V
		V_{CC} = 2.7 V to 3.6 V	-	1.5	0.8	-	TBD	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.8 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	TBD	-	V
		I_O = -6 mA; V_{CC} = 1.8 V	V_{CC} - 0.4	V_{CC} - 0.1	-	TBD	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	TBD	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.5	V_{CC} - 0.17	-	TBD	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	TBD	-	V
		I_O = -18 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	TBD	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	TBD	-	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.8 V to 3.6 V	-	0	0.20	-	TBD	V
		I_O = 6 mA; V_{CC} = 1.8 V	-	0.09	0.30	-	TBD	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.20	-	TBD	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.40	-	TBD	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	-	TBD	V
		I_O = 18 mA; V_{CC} = 2.3 V	-	0.23	0.60	-	TBD	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	-	TBD	V
I_I	input leakage current	V_{CC} = 1.8 V to 3.6 V						
		control input; V_I = 5.5 V or GND	-	0.1	5	-	TBD	µA
		data input; V_I = V_{CC} or GND	-	0.1	5	-	TBD	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O = V_{CC} or GND						
		V_{CC} = 1.8 V to 2.7 V	-	0.1	5	-	TBD	µA
		V_{CC} = 2.7 V to 3.6 V	-	0.1	10	-	TBD	µA
I_{LIZ}	OFF-state input leakage current	V_I = V_{CC} or GND						
		V_{CC} = 1.8 V to 2.7 V	-	0.1	10	-	TBD	µA
		V_{CC} = 3.6 V	-	0.1	15	-	TBD	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A;						
		V_{CC} = 1.8 V to 2.7 V	-	0.2	40	-	TBD	µA
		V_{CC} = 2.7 V to 3.6 V	-	0.2	40	-	TBD	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V						
		per control input	-	5	500	-	TBD	µA
		per data I/O input	-	150	750	-	TBD	µA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V [2]	45	-	-	TBD	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V [2]	75	150	-	TBD	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V [2]	-45	-	-	TBD	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V [2]	-75	-175	-	TBD	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 2.7 V [2]	300	-	-	TBD	-	µA
		V_{CC} = 3.6 V [2]	450	-	-	TBD	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 2.7 V [2]	-300	-	-	TBD	-	µA
		V_{CC} = 3.6 V [2]	-450	-	-	TBD	-	µA
C_I	input capacitance		-	5.0	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Valid for data inputs of bus hold parts only.

10. Dynamic characteristics

Table 7. Dynamic characteristics

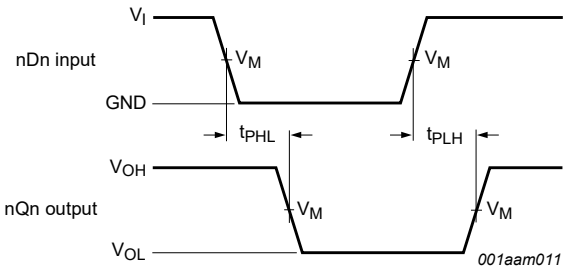
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nDn to nQn; see Fig. 5 [2]						
		V_{CC} = 1.2 V	-	8.8	-	-	-	ns
		V_{CC} = 1.8 V	1.5	3.2	5.7	TBD	TBD	ns
		V_{CC} = 2.3 V to 2.7 V [3]	1.0	2.1	3.9	TBD	TBD	ns
		V_{CC} = 2.7 V	1.0	2.3	3.7	TBD	TBD	ns
		V_{CC} = 3.0 V to 3.6 V [4]	1.0	2.1	3.3	TBD	TBD	ns
		nLE to nQn; see Fig. 6 [2]						
		V_{CC} = 1.2 V	-	7.4	-	-	-	ns
		V_{CC} = 1.8 V	1.5	3.4	5.9	TBD	TBD	ns
		V_{CC} = 2.3 V to 2.7 V [3]	1.0	2.2	3.9	TBD	TBD	ns
		V_{CC} = 2.7 V	1.0	2.2	3.5	TBD	TBD	ns
		V_{CC} = 3.0 V to 3.6 V [4]	1.0	2.2	3.2	TBD	TBD	ns
t_{en}	enable time	$n\overline{OE}$ to nQn; see Fig. 7 [5]						
		V_{CC} = 1.2 V	-	8.9	-	-	-	ns
		V_{CC} = 1.8 V	1.5	4.0	7.3	TBD	TBD	ns
		V_{CC} = 2.3 V to 2.7 V [3]	1.0	2.6	5.2	TBD	TBD	ns
		V_{CC} = 2.7 V	1.0	2.9	4.9	TBD	TBD	ns
		V_{CC} = 3.0 V to 3.6 V [4]	1.0	2.3	4.2	TBD	TBD	ns
t_{dis}	disable time	$n\overline{OE}$ to nQn; see Fig. 7 [6]						
		V_{CC} = 1.2 V	-	8.9	-	-	-	ns
		V_{CC} = 1.8 V	1.5	3.2	5.6	TBD	TBD	ns
		V_{CC} = 2.3 V to 2.7 V [3]	1.0	2.2	4.1	TBD	TBD	ns
		V_{CC} = 2.7 V	1.0	3.1	4.7	TBD	TBD	ns
		V_{CC} = 3.0 V to 3.6 V [4]	1.0	2.8	4.1	TBD	TBD	ns
t_W	pulse width	nLE HIGH; see Fig. 6						
		V_{CC} = 1.8 V	3.5	1.0	-		-	ns
		V_{CC} = 2.3 V to 2.7 V [3]	3.0	1.0	-		-	ns
		V_{CC} = 2.7 V	3.0	1.0	-		-	ns
		V_{CC} = 3.0 V to 3.6 V [4]	2.5	1.0	-		-	ns
t_{su}	set-up time	nDn to nLE; see Fig. 8						
		V_{CC} = 1.8 V	1.0	-0.1	-		-	ns
		V_{CC} = 2.3 V to 2.7 V [3]	1.0	-0.1	-		-	ns
		V_{CC} = 2.7 V	1.0	-0.1	-		-	ns
		V_{CC} = 3.0 V to 3.6 V [4]	1.0	0.0	-		-	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_h	hold time	nDn to nLE; see Fig. 8						
		V_{CC} = 1.8 V	1.2	0.1	-		-	ns
		V_{CC} = 2.3 V to 2.7 V [3]	1.5	0.2	-		-	ns
		V_{CC} = 2.7 V	1.5	0.4	-		-	ns
		V_{CC} = 3.0 V to 3.6 V [4]	1.2	0.2	-		-	ns
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC} [7]						
		outputs enabled	-	16	-	-	-	pF
		outputs disabled	-	10	-	-	-	pF

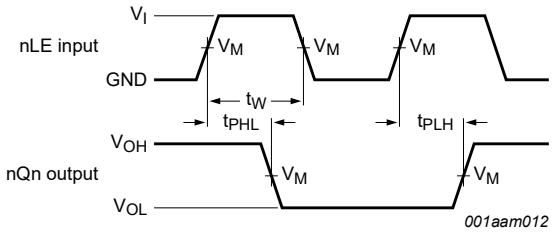
[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] Typical values are measured at V_{CC} = 2.5 V.
[4] Typical values are measured at V_{CC} = 3.3 V.
[5] t_{en} is the same as t_{PZL} and t_{PZH}.
[6] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[7] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



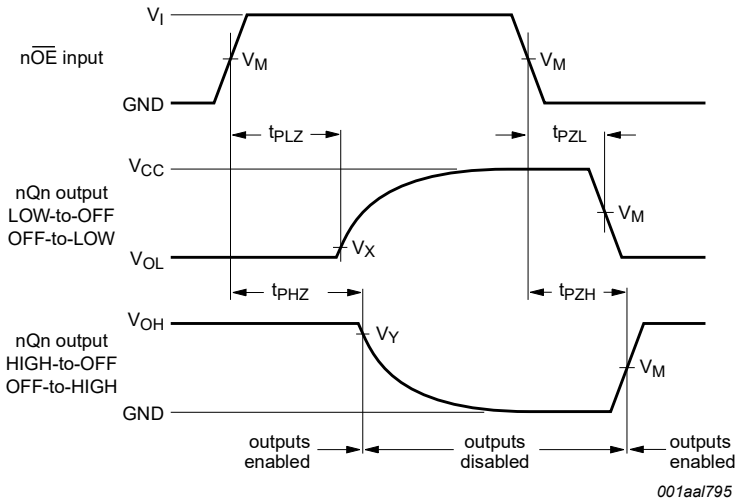
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 5. Propagation delay, input (nDn) to data output (nQn)



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output levels that occur with the output load.

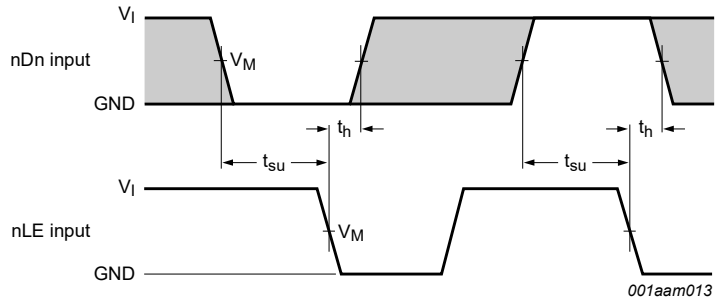
Fig. 6. Propagation delay, latch enable input (nLE) to data output (nQn), and pulse width



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 7. 3-state enable and disable times



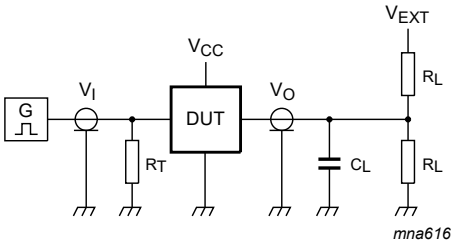
Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 8. Data setup and hold times for input (nDn) to input (nLE)

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V and < 2.3 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times

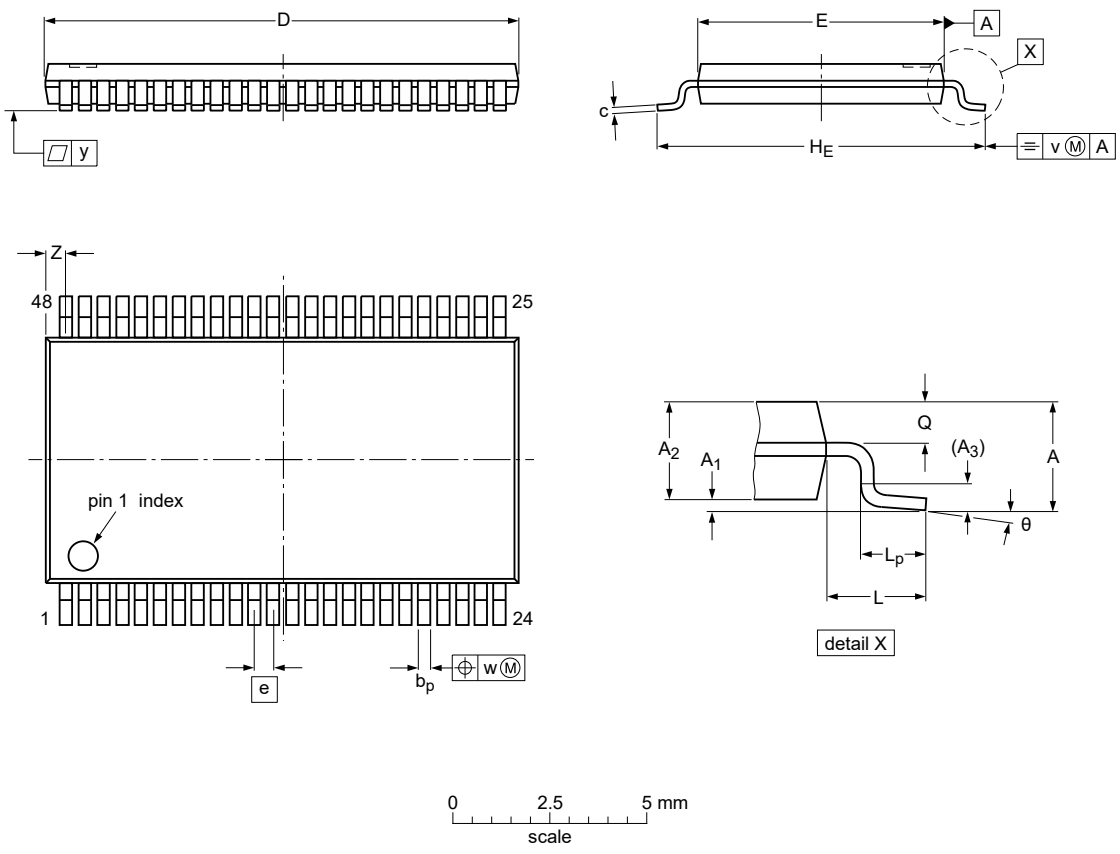
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V and < 2.3 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2V_{CC}$	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	$2V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	$2V_{CC}$	GND

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max	1.2	0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom				0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~13-08-05~~ 24-01-05

Fig. 10. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16373 v.10	20240618	Product data sheet	-	74ALVCH16373 v.9
Modifications:	• Specifications added for T_{amb}= -40 °C to +125 °C. • Table 4: Derating values for P_{tot} total power dissipation updated.			
74ALVCH16373 v.9	20240618	Product data sheet	-	74ALVCH16373 v.8
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 10: Updated package outline drawing SOT362-1 (TSSOP48).			
74ALVCH16373 v.8	20211122	Product data sheet	-	74ALVCH16373 v.7
Modifications:	• Section 1 and Section 2 updated.			
74ALVCH16373 v.7	20190130	Product data sheet	-	74ALVCH16373 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74ALVCH16373DL (SOT370-1) removed. • Package outline drawing SOT362-1 (TSSOP48) updated.			
74ALVCH16373 v.6	20120710	Product data sheet	-	74ALVCH16373 v.5
Modifications:	• Table 8 corrected (errata).			
74ALVCH16373 v.5	20111117	Product data sheet	-	74ALVCH16373 v.4
Modifications:	• Legal pages updated.			
74ALVCH16373 v.4	20100531	Product data sheet	-	74ALVCH16373 v.3
74ALVCH16373 v.3	19990920	Product specification	-	74ALVCH16373 v.2
74ALVCH16373 v.2	19980629	Product specification	-	74ALVCH16373 v.1
74ALVCH16373 v.1	19970321	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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