



**THE DATASHEET OF
74AHC574PW,118**



74AHC574; 74AHCT574

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 3 — 6 September 2023

Product data sheet

1. General description

The 74AHC574; 74AHCT574 is an 8-bit positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable (\overline{OE}) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features and benefits

- Wide supply voltage range:
 - For 74AHC574: from 2.0 V to 5.5 V
 - For 74AHCT574: from 4.5 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- High noise immunity
- 3-state non-inverting outputs for bus orientated applications
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Input levels:
 - For 74AHC574: CMOS input level
 - For 74AHCT574: TTL input level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|---|-------------------|----------|--|--------------------------|
| | Temperature range | Name | Description | Version |
| 74AHC574D 74AHCT574D | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74AHC574PW 74AHCT574PW | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74AHC574BQ 74AHCT574BQ | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram

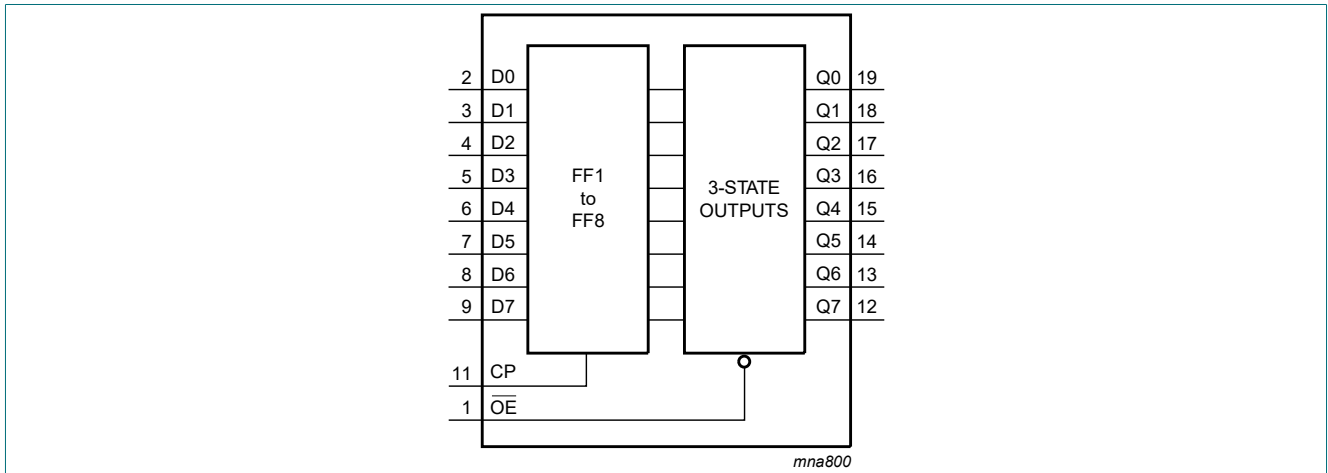


Fig. 1. Functional diagram

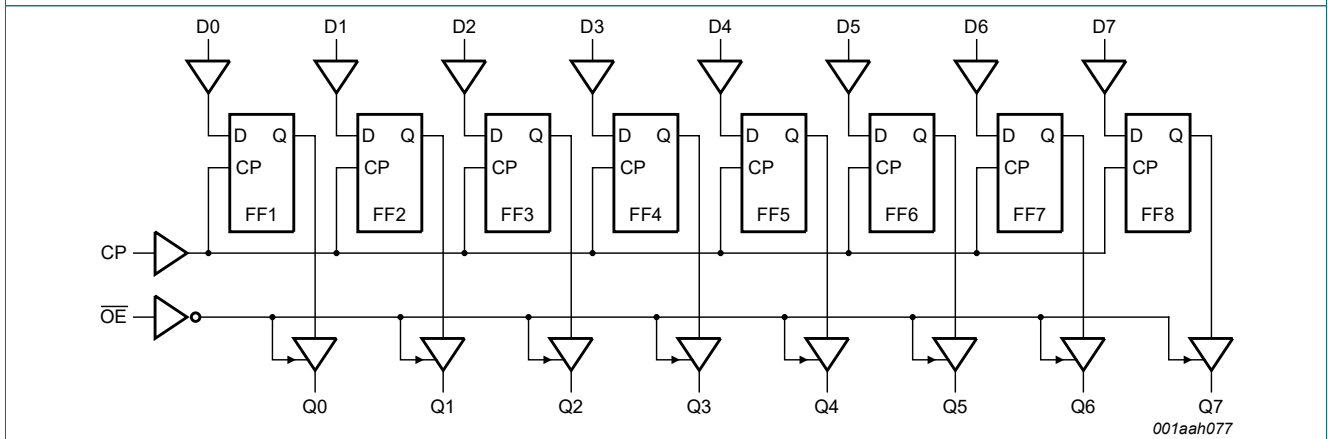


Fig. 2. Logic diagram

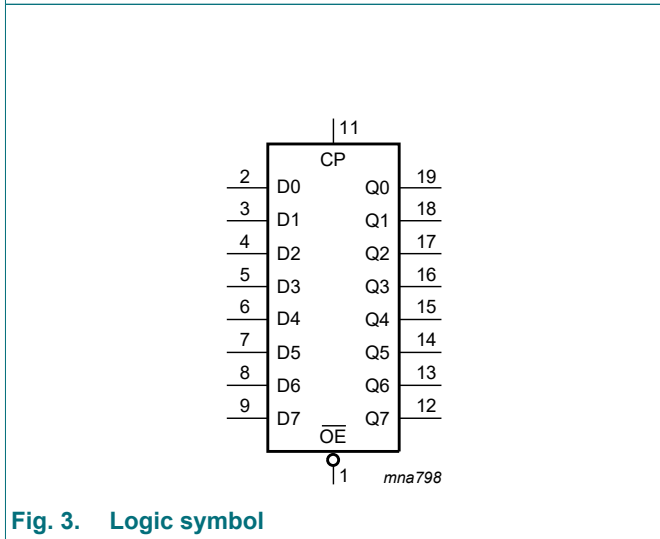


Fig. 3. Logic symbol

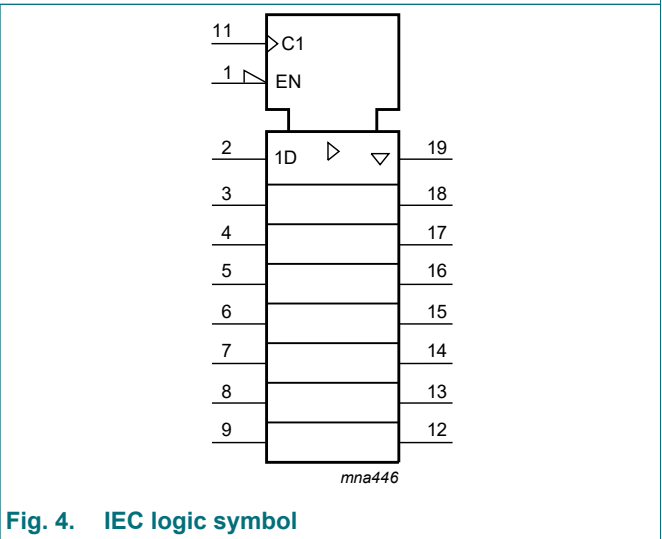
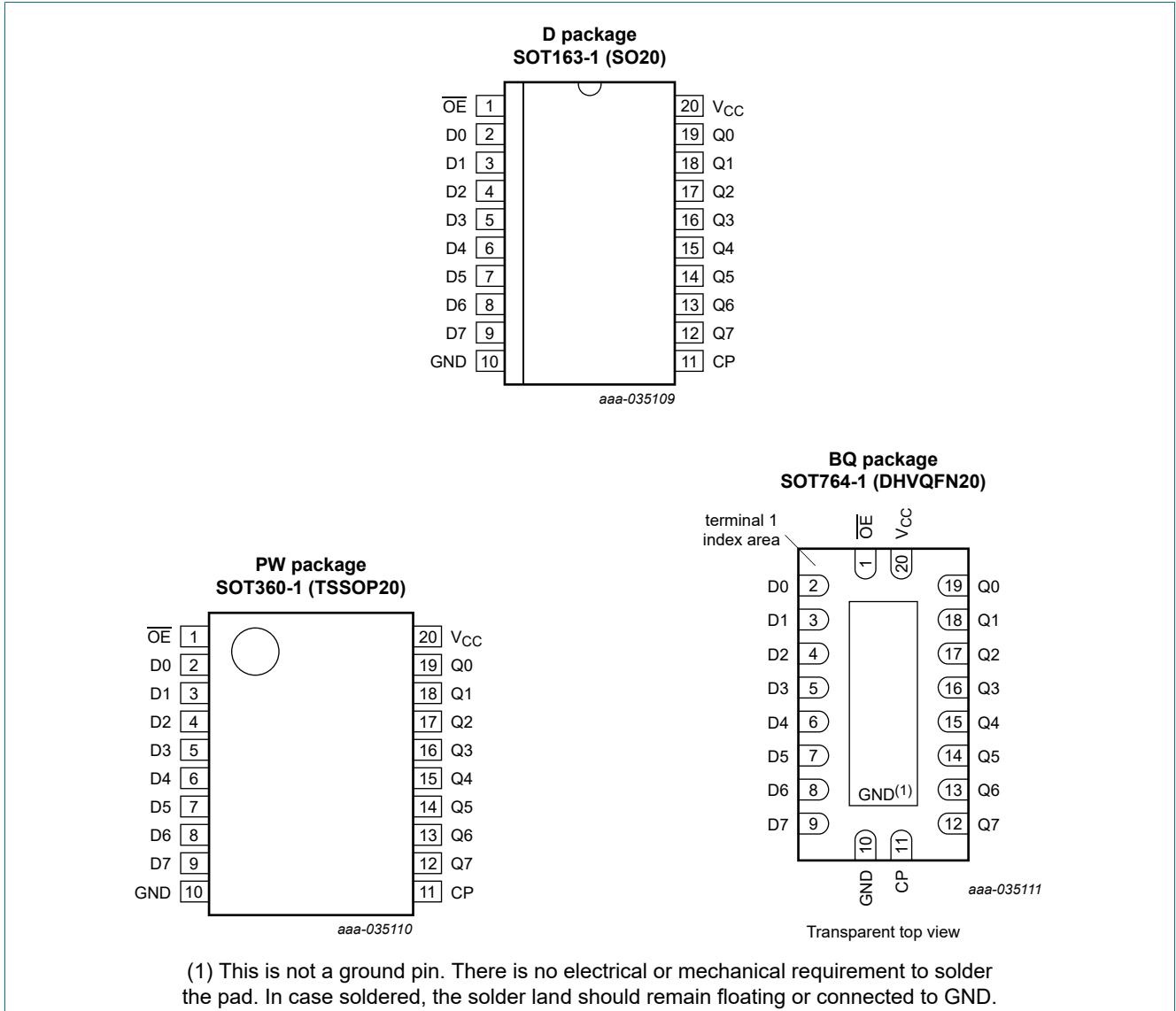


Fig. 4. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------------|--------------------------------|---|
| \overline{OE} | 1 | 3-state output enable input (active LOW) |
| D0, D1, D2, D3, D4, D5, D6, D7 | 2, 3, 4, 5, 6, 7, 8, 9 | data input |
| GND | 10 | ground (0 V) |
| CP | 11 | clock input (LOW-to-HIGH, edge triggered) |
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 19, 18, 17, 16, 15, 14, 13, 12 | 3-state flip-flop output |
| V _{CC} | 20 | supply voltage |

6. Functional description

Table 3. Function table

*H = HIGH voltage level; h = HIGH voltage level one setup time prior to the HIGH-to-LOW CP transition;
L = LOW voltage level; l = LOW voltage level one setup time prior to the HIGH-to-LOW CP transition;
Z = high-impedance OFF-state; ↑ = LOW-to-HIGH clock transition.*

| Operating mode | Input | | | Internal flip-flop | Output |
|----------------------------------|-------|----|----|--------------------|--------|
| | OE | CP | Dn | | Qn |
| Load and read register | L | ↑ | l | L | L |
| | L | ↑ | h | H | H |
| Load register and disable output | H | ↑ | l | L | Z |
| | H | ↑ | h | H | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V [1] | -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1] | - | ±20 | mA |
| I_O | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5)$ V | - | ±25 | mA |
| I_{CC} | supply current | | - | 75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to $+125$ °C [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 74AHC574 | | | 74AHCT574 | | | Unit |
|---------------------|-------------------------------------|--------------------------|----------|-----|----------|-----------|-----|----------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.3$ V ± 0.3 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC} = 5.0$ V ± 0.5 V | - | - | 20 | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------|-----|-------|------------------|------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHC574 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | V _{CC} = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | V _{CC} = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 µA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 µA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 µA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 µA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 µA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 µA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | µA |
| | | I _O = 8.0 mA; V _{CC} = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| C _I | input capacitance | | - | 3.0 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4.0 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|-----|-------|------------------|------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHCT574 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -8.0 mA | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 50 µA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.25 | - | ±2.5 | - | ±10.0 | µA |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other pins at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C _I | input capacitance | | - | 3 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4.0 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$. For test circuit see [Fig. 8](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------|---|-------|--------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| 74AHC574 | | | | | | | | | | |
| t_{pd} | propagation delay | CP to Qn; see Fig. 5 [2] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 6.5 | 13.2 | 1.0 | 15.5 | 1.0 | 16.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 9.3 | 16.7 | 1.0 | 19.0 | 1.0 | 21.0 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 4.4 | 8.6 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| | | $C_L = 50\text{ pF}$ | | 6.2 | 10.6 | 1.0 | 12.0 | 1.0 | 13.5 | ns |
| t_{en} | enable time | \overline{OE} to Qn; see Fig. 7 | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 5.7 | 12.8 | 1.0 | 15.0 | 1.0 | 16.0 | ns |
| | | $C_L = 50\text{ pF}$ | - | 8.2 | 16.3 | 1.0 | 18.5 | 1.0 | 20.5 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 4.2 | 9.0 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 5.9 | 11.0 | 1.0 | 12.5 | 1.0 | 14.0 | ns |
| t_{dis} | disable time | \overline{OE} to Qn; see Fig. 7 [2] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 6.3 | 13.0 | 1.0 | 15.0 | 1.0 | 16.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 9.1 | 15.0 | 1.0 | 17.0 | 1.0 | 19.0 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 4.3 | 9.0 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 6.9 | 10.1 | 1.0 | 11.5 | 1.0 | 13.0 | ns |
| f_{max} | maximum frequency | CP; see Fig. 5 | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | 80 | 125 | - | 65 | - | 65 | - | MHz |
| | | $C_L = 50\text{ pF}$ | 50 | 75 | - | 45 | - | 45 | - | MHz |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | 130 | 180 | - | 110 | - | 110 | - | MHz |
| | | $C_L = 50\text{ pF}$ | 85 | 115 | - | 75 | - | 75 | - | MHz |
| t_W | pulse width | CP; HIGH or LOW; see Fig. 5 | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$ | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$ | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t_{su} | set-up time | Dn to CP; see Fig. 6 | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$ | 3.5 | - | - | 3.5 | - | 3.5 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$ | 3.0 | - | - | 3.0 | - | 3.0 | - | ns |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|--|-------|--------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| t _h | hold time | Dn to CP; see Fig. 6 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF | 1.5 | - | - | 1.5 | - | 1.5 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | 1.5 | - | - | 1.5 | - | 1.5 | - | ns |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f _i = 1 MHz; [3] V _I = GND to V _{CC} | - | 10 | - | - | - | - | - | pF |
| 74AHCT574 | | | | | | | | | | |
| t _{pd} | propagation delay | CP to Qn; see Fig. 5 [2] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 4.4 | 8.6 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| | | C _L = 50 pF | - | 6.3 | 10.6 | 1.0 | 12.0 | 1.0 | 13.5 | ns |
| t _{en} | enable time | OE to Qn; see Fig. 7 | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 4.3 | 9.0 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | C _L = 50 pF | - | 6.1 | 11.0 | 1.0 | 12.5 | 1.0 | 14.0 | ns |
| t _{dis} | disable time | OE to Qn; see Fig. 7 [2] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 4.3 | 9.0 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | C _L = 50 pF | - | 6.2 | 10.1 | 1.0 | 11.5 | 1.0 | 13.0 | ns |
| f _{max} | maximum frequency | CP; see Fig. 5 | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | 130 | 180 | - | 110 | - | 110 | - | MHz |
| | | C _L = 50 pF | 85 | 115 | - | 75 | - | 75 | - | MHz |
| t _w | pulse width | CP; HIGH or LOW; see Fig. 5 | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | 5.0 | - | - | 5.5 | - | 5.5 | - | ns |
| t _{su} | set-up time | Dn to CP; see Fig. 6 | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | 3.0 | - | - | 3.5 | - | 3.5 | - | ns |
| t _h | hold time | Dn to CP; see Fig. 6 | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | 1.5 | - | - | 1.5 | - | 1.5 | - | ns |
| C _{PD} | power dissipation capacitance | per buffer; C _L = 50 pF; [3] f = 1 MHz; V _I = GND to V _{CC} | - | 12 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{pZL} and t_{pZH}.

t_{dis} is the same as t_{pLZ} and t_{pHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

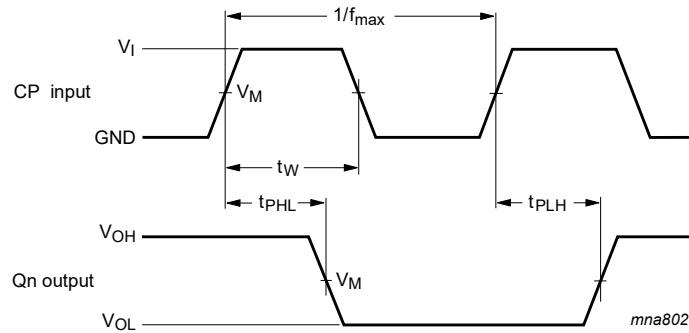
f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

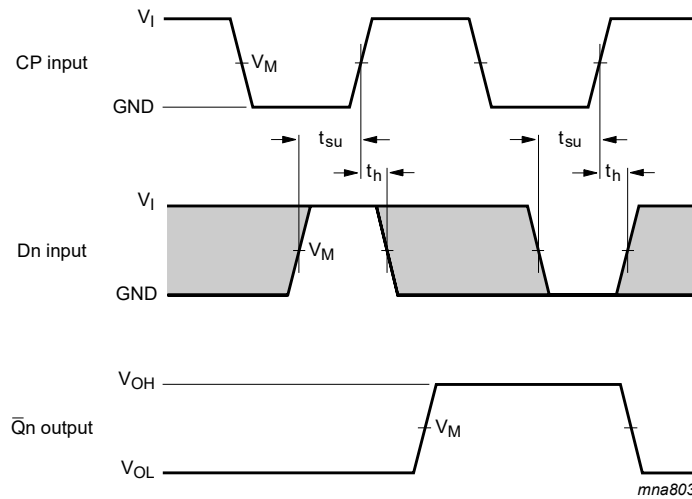
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Propagation delay input (CP) to output (Qn), clock input (CP) pulse width and the maximum frequency (CP)



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predicable output performance.

Fig. 6. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times

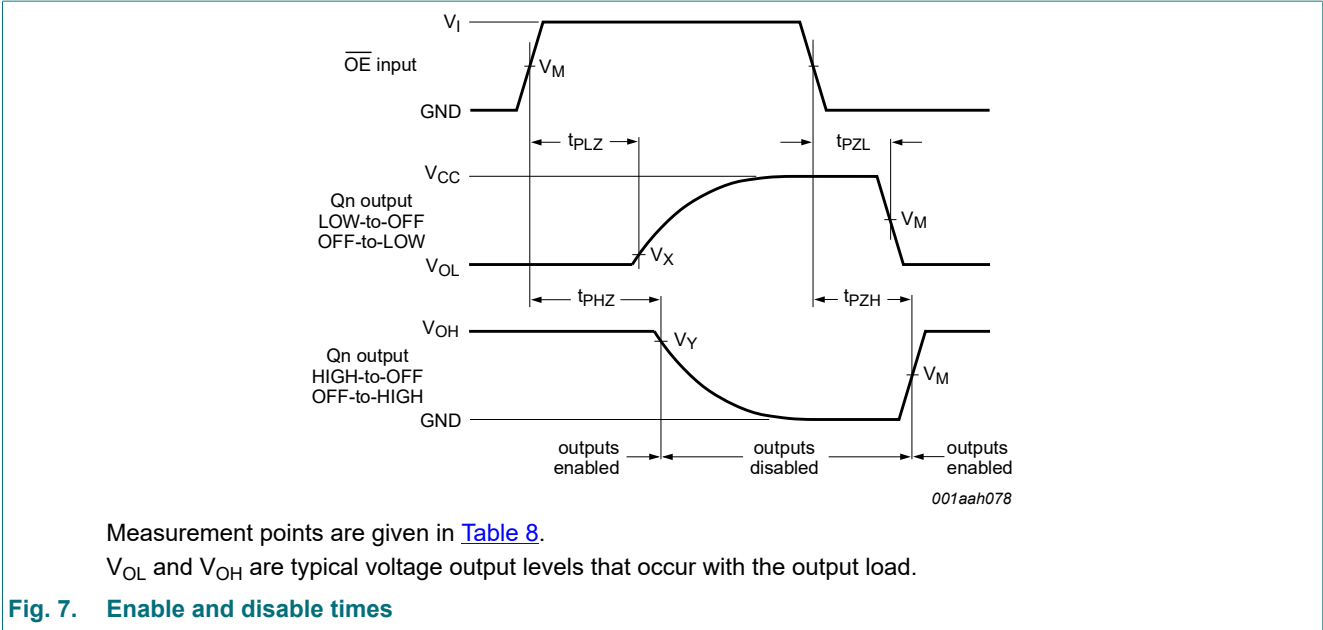


Table 8. Measurement points

| Type | Input | Output | | |
|-----------|---------------------|---------------------|--------------------------|--------------------------|
| | V_M | V_M | V_x | V_y |
| 74AHC574 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |
| 74AHCT574 | 1.5 V | $0.5 \times V_{CC}$ | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |

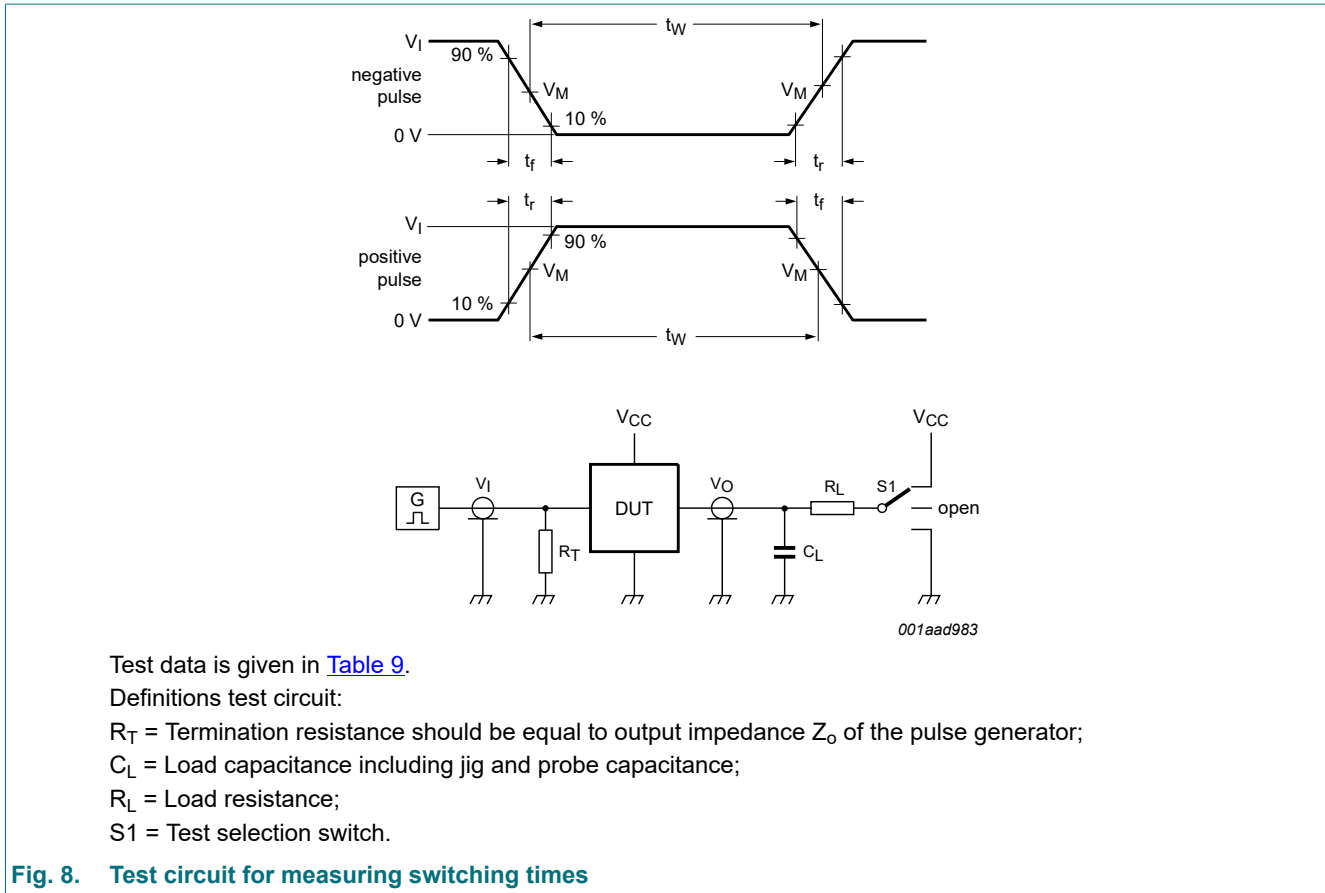


Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|-----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74AHC574 | V_{CC} | 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74AHCT574 | 3.0 V | 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

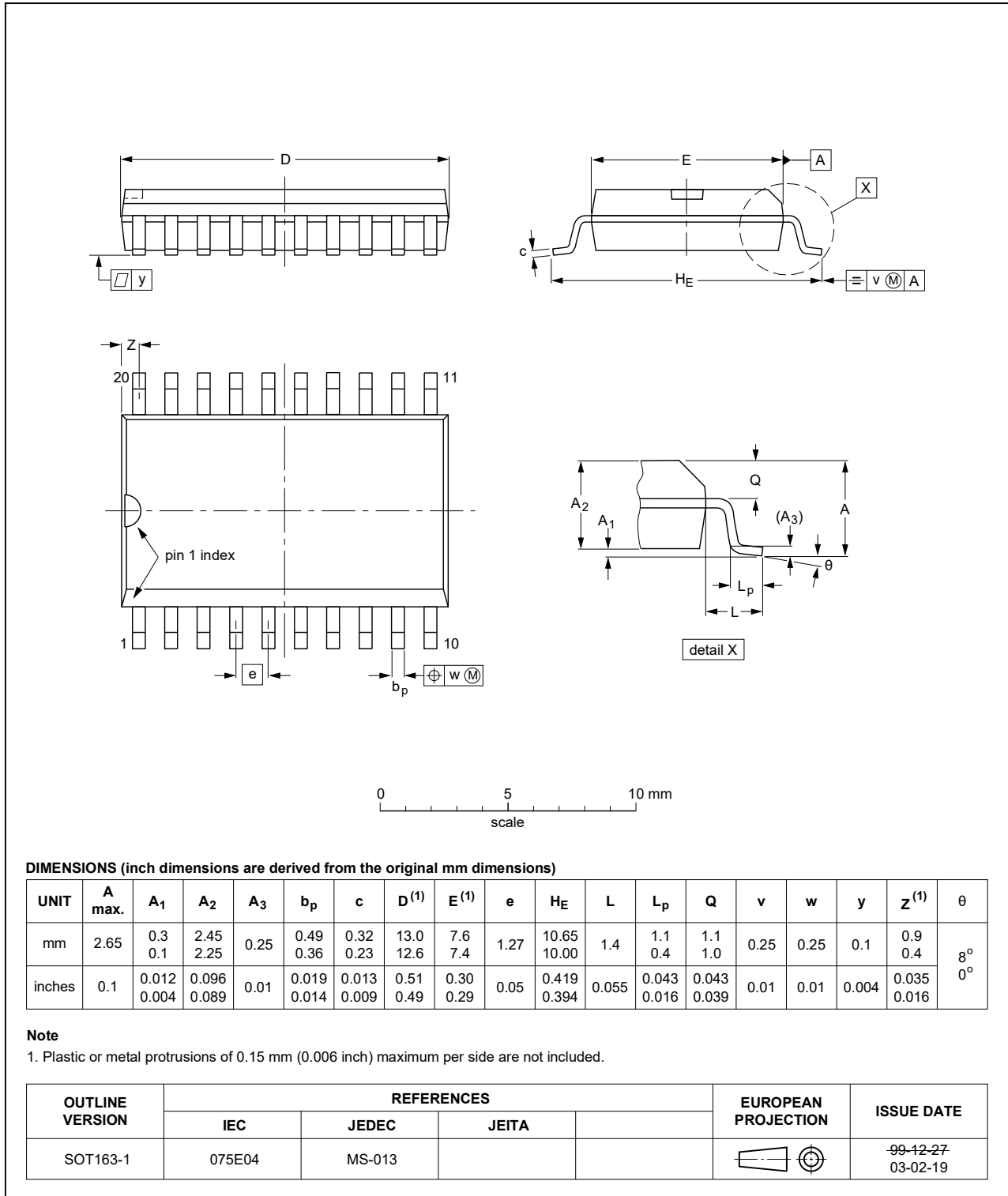


Fig. 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

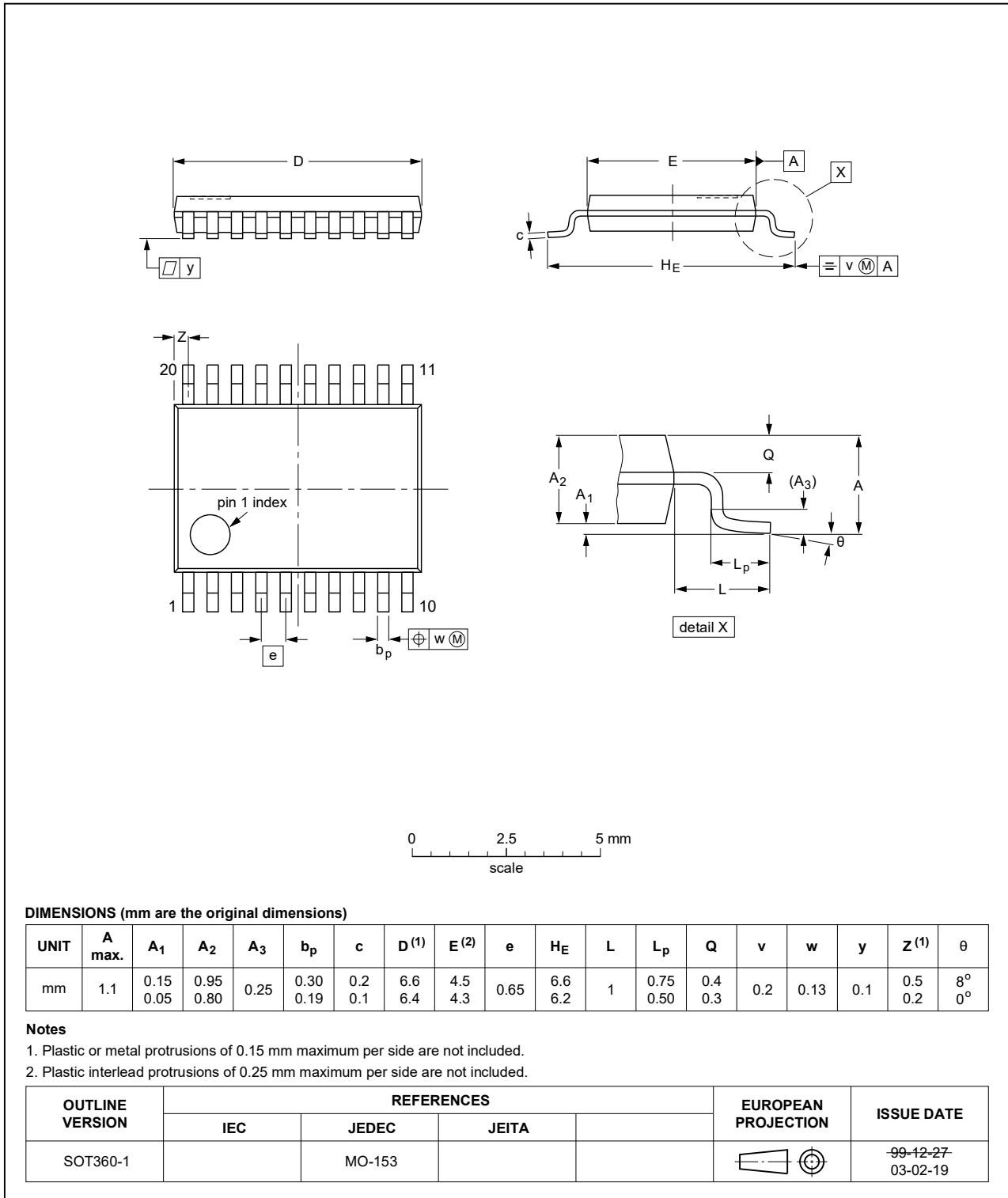


Fig. 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

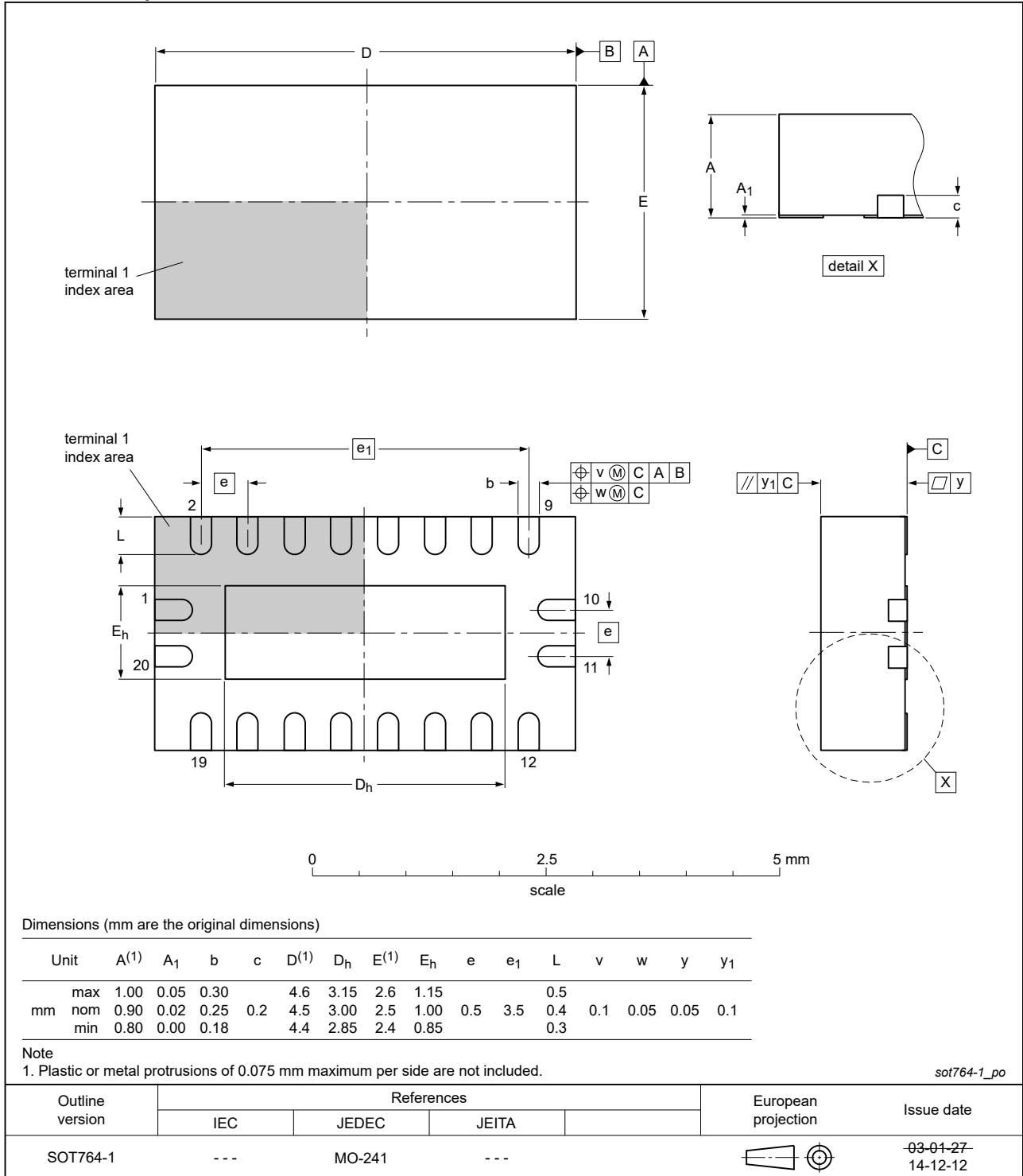


Fig. 11. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|---|-----------------------|---------------|-------------------|
| 74AHC_AHCT574 v.3 | 20230906 | Product data sheet | - | 74AHC_AHCT574 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Section 2: ESD specification updated according to the latest JEDEC standard. Section 7: Derating values for P_{tot} total power dissipation updated. Section 9: For 74AHCT574: Conditions I_{OZ} corrected inline with 74AHC574. Fig. 11: Package outline drawing SOT764-1 (DHVQFN20) has been updated. | | | |
| 74AHC_AHCT574_2 | 20080124 | Product data sheet | - | 74AHC_AHCT574_1 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Section 3: DHVQFN20 package added. Section 7: derating values added for DHVQFN20 package. Section 11: outline drawing added for DHVQFN20 package. | | | |
| 74AHC_AHCT574_1 | 19990616 | Product specification | - | - |

Octal D-type flip-flop; positive edge-trigger; 3-state

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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