



**THE DATASHEET OF
74AHC1G86GW-Q100,1**





74AHC1G86-Q100; 74AHCT1G86-Q100

2-input EXCLUSIVE-OR gate

Rev. 3.1 — 11 October 2023

Product data sheet

1. General description

The 74AHC1G86-Q100; 74AHCT1G86-Q100 is a single 2-input EXCLUSIVE-OR gate. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Symmetrical output impedance
- Balanced propagation delays
- Input levels:
 - For 74AHC1G86-Q100: CMOS level
 - For 74AHCT1G86-Q100: TTL level
- Multiple package options
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G86GW-Q100 74AHCT1G86GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHC1G86GV-Q100 74AHCT1G86GV-Q100	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753

4. Marking

Table 2. Marking codes

Type number	Marking code
74AHC1G86GW-Q100	AH
74AHCT1G86GW-Q100	CH
74AHC1G86GV-Q100	A86
74AHCT1G86GV-Q100	C86

5. Functional diagram

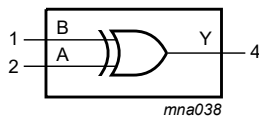


Fig. 1. Logic symbol

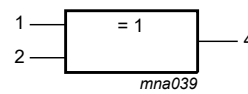


Fig. 2. IEC logic symbol

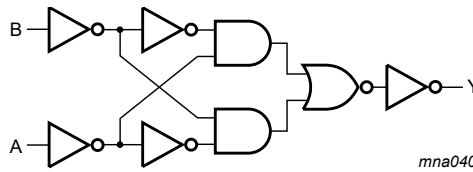
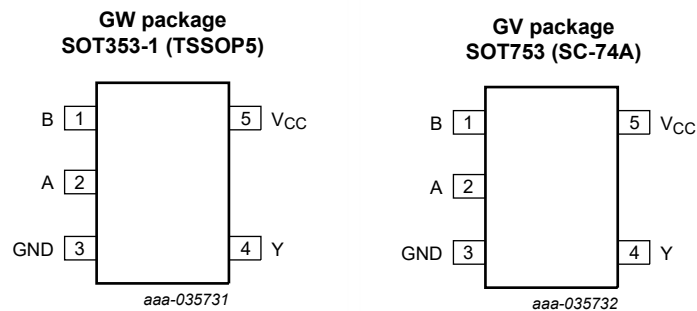


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V	-20	-	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1]	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC1G86-Q100			74AHCT1G86-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G86-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0 \text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5 \text{ V}$	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5 \text{ V}$	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -50 \mu\text{A}$; $V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu\text{A}$; $V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu\text{A}$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 50 \mu\text{A}$; $V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu\text{A}$; $V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu\text{A}$; $V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
		$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	40	μA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT1G86-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = 3.4 V; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; $t_r = t_f = \leq 3.0$ ns. For waveform see Fig. 4. For test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G86-Q100										
t _{pd}	propagation delay	A and B to Y [1]								
		V _{CC} = 3.0 V to 3.6 V [2]								
		C _L = 15 pF	-	4.0	11.0	1.0	13.0	1.0	14.0	ns
		C _L = 50 pF	-	5.8	14.5	1.0	16.5	1.0	18.5	ns
		V _{CC} = 4.5 V to 5.5 V [3]								
		C _L = 50 pF	-	4.9	8.8	1.0	10.0	1.0	11.5	ns
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [4]	-	9	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT1G86-Q100										
t _{pd}	propagation delay	A and B to Y [1]								
		V _{CC} = 4.5 V to 5.5 V [3]								
		C _L = 15 pF	-	3.5	6.9	1.0	8.0	1.0	9.0	ns
		C _L = 50 pF	-	5.0	7.9	1.0	9.0	1.0	10.5	ns
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [4]	-	11	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] Typical values are measured at V_{CC} = 3.3 V.
- [3] Typical values are measured at V_{CC} = 5.0 V.
- [4] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts.

11.1. Waveform and test circuit

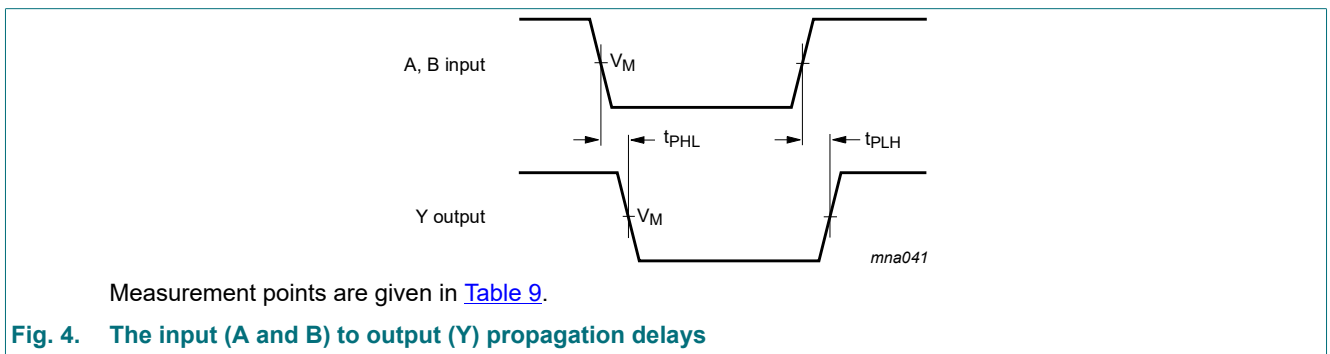
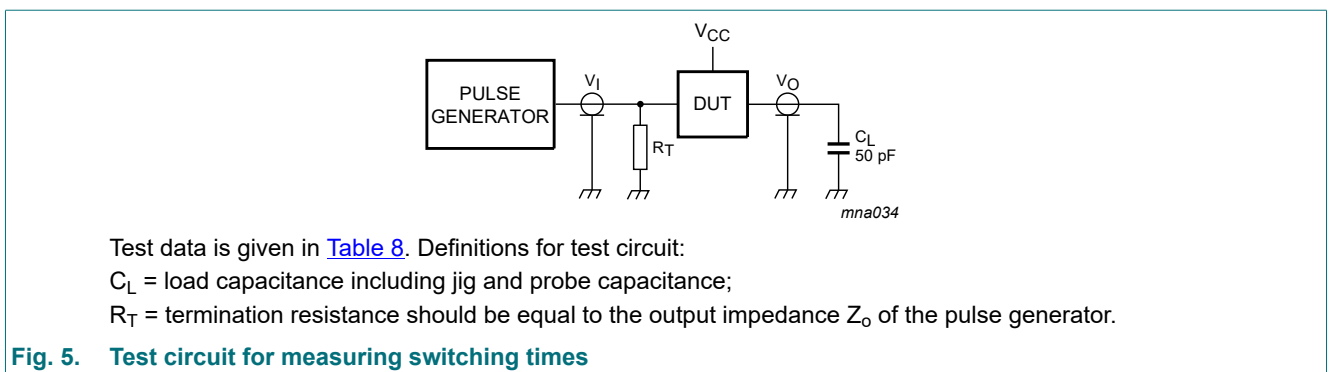


Table 9. Measurement points

Type	Input		Output
	V _I	V _M	V _M
74AHC1G86-Q100	GND to V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}
74AHCT1G86-Q100	GND to 3.0 V	1.5 V	0.5 × V _{CC}



12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig. 6. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

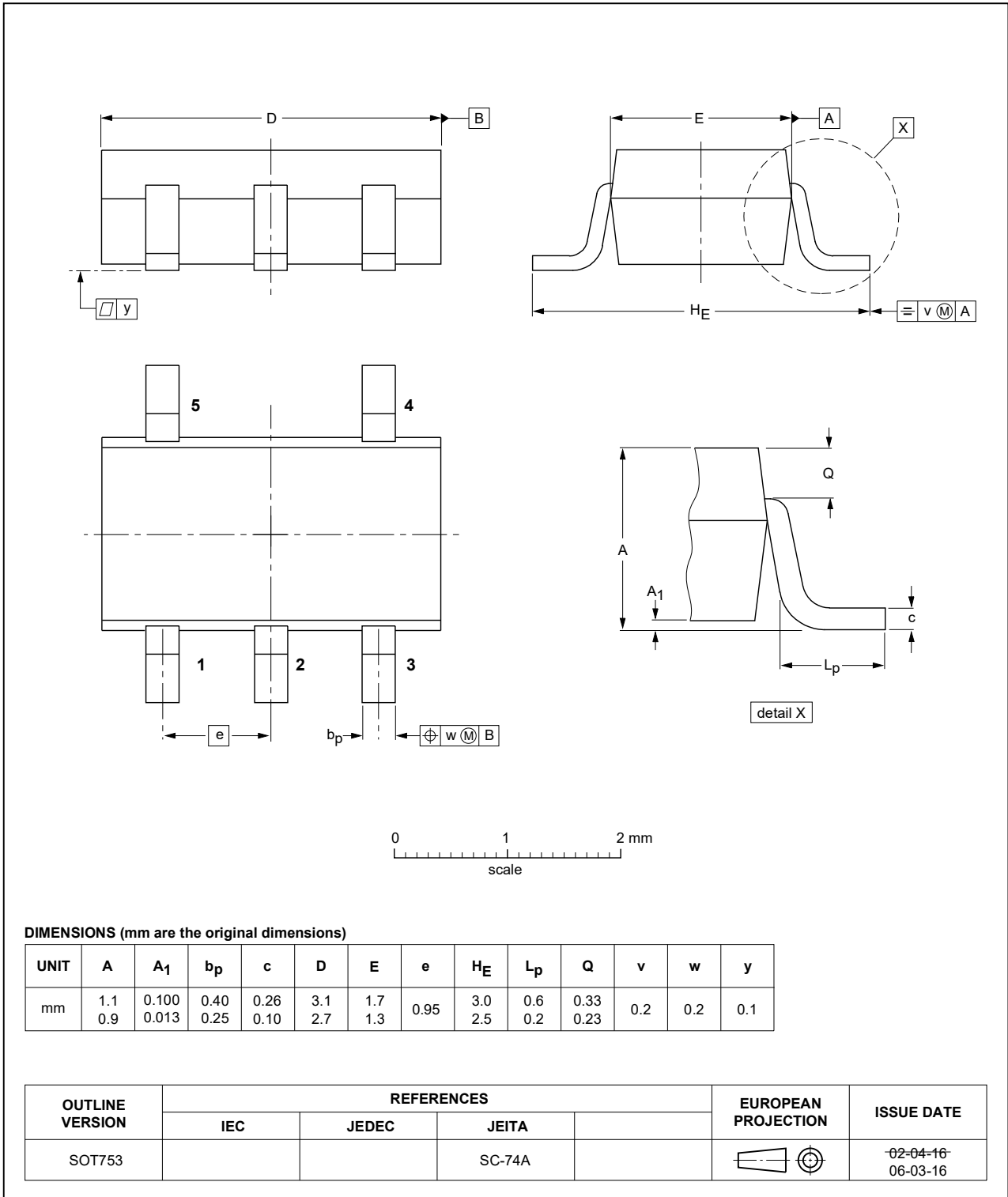


Fig. 7. Package outline SOT753 (SC-74A)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G86_Q100 v.3.1	20231011	Product data sheet	-	74AHC_AHCT1G86_Q100 v.2
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74AHC_AHCT1G86_Q100 v.2	20220111	Product data sheet	-	74AHC_AHCT1G86_Q100 v.1
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • SOT353-1 (TSSOP5) package outline drawing has changed. • Section 8: Derating values for P_{tot} total power dissipation updated. 			
74AHC_AHCT1G86_Q100 v.1	20120716	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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