



**THE DATASHEET OF  
74AHC1G4214GWH**



# 74AHC1G4214

## 14-stage divider and oscillator

Rev. 5 — 3 October 2023

Product data sheet

## 1. General description

74AHC1G4214 is a 14-stage divider and oscillator. It consists of a chain of 14 flip-flops. Each flip-flop divides the frequency of the previous flip-flop by two, consequently the 74AHC1G4214 counts up to  $2^{14} = 16384$ . The single inverting stage (X1 to X2) functions as a crystal oscillator or an input buffer for an external oscillator. When used as a buffer the output X2 should be left floating. The frequency of the output (Q) is the frequency applied to X1 divided by 16384. The divider advances on the negative-going transition of X1.

The X1 input is overvoltage tolerant. This feature allows the use of this device as a voltage level translator in mixed voltage environments.

## 2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74AHC1G4214GW</a>	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	<a href="#">SOT353-1</a>

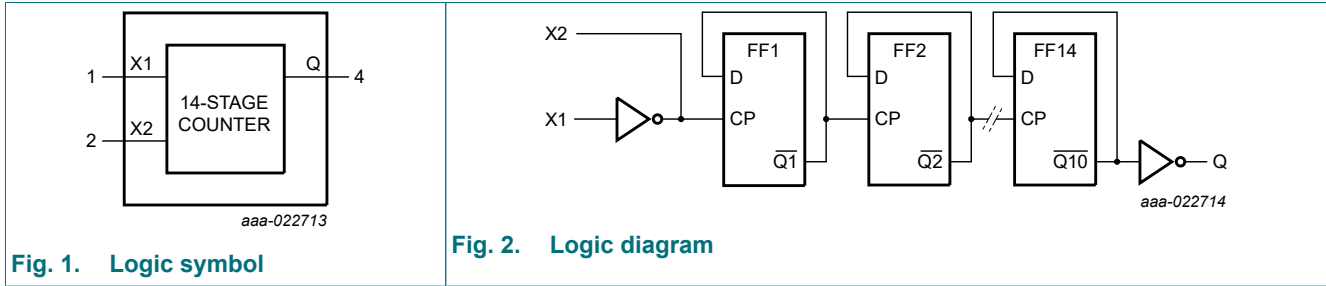
## 4. Marking

Table 2. Marking codes

Type number	Marking[1]
74AHC1G4214GW	C4

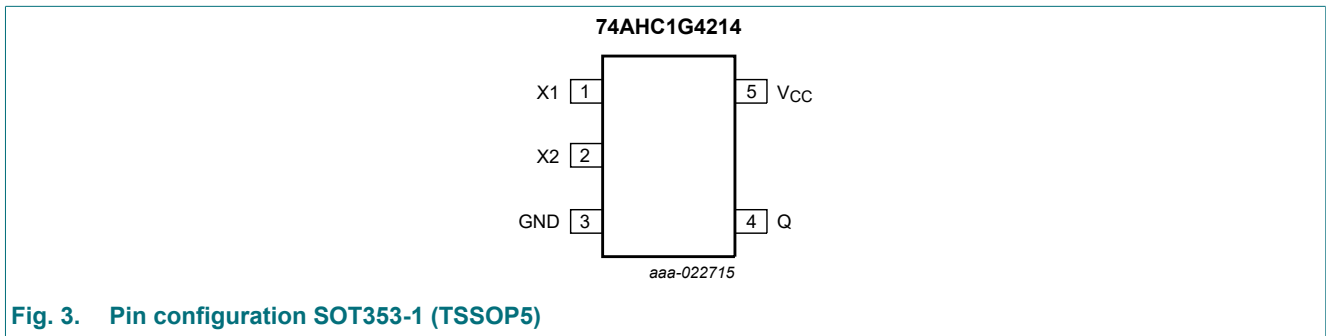
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram



### 6. Pinning information

#### 6.1. Pinning

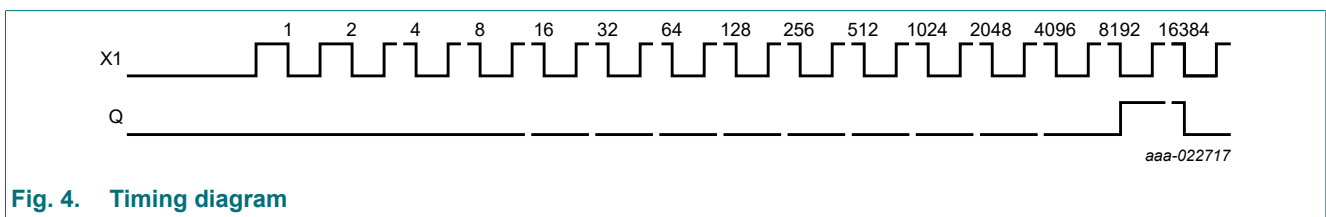


#### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
X1	1	clock input/oscillator pin
X2	2	oscillator pin
GND	3	ground (0 V)
Q	4	divider output
V <sub>CC</sub>	5	supply voltage

### 7. Functional description



## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	±20	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	±25	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	-	-	100	ns/V
		$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	-	-	20	ns/V

## 10. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	X1								
		V <sub>CC</sub> = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
		V <sub>CC</sub> = 3.0 V	2.4	-	-	2.4	-	2.4	-	V
		V <sub>CC</sub> = 5.5 V	4.4	-	-	4.4	-	4.4	-	V
V <sub>IL</sub>	LOW-level input voltage	X1								
		V <sub>CC</sub> = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V <sub>CC</sub> = 3.0 V	-	-	0.6	-	0.6	-	0.6	V
		V <sub>CC</sub> = 5.5 V	-	-	1.1	-	1.1	-	1.1	V
V <sub>OH</sub>	HIGH-level output voltage	Q; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
		X2; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -2.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
I <sub>O</sub> = -3.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V		
V <sub>OL</sub>	LOW-level output voltage	Q; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
		X2; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 2.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>O</sub> = 3.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V		
I <sub>I</sub>	input leakage current	X1; V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	μA
C <sub>I</sub>	input capacitance	X1	-	3	8	-	8	-	8	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f = \leq 3.0\text{ ns}$ . For test circuit see Fig. 7. For waveforms see Fig. 5 and Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_{pd}$	propagation delay	X1 to X2 [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]								
		$C_L = 15\text{ pF}$	-	3	7	1	11	1	13	ns
		$C_L = 50\text{ pF}$	-	7	13	1	16	1	18	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]								
		$C_L = 15\text{ pF}$	-	2	5	1	7	1	9	ns
		$C_L = 50\text{ pF}$	-	6	10	1	11	1	12	ns
		X1 to Q [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2]								
		$C_L = 15\text{ pF}$	-	33	55	1	67	1	78	ns
		$C_L = 50\text{ pF}$	-	35	60	1	71	1	82	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3]								
		$C_L = 15\text{ pF}$	-	23	36	1	44	1	52	ns
		$C_L = 50\text{ pF}$	-	25	40	1	51	1	58	ns
$t_W$	pulse width	X1 HIGH or LOW								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4	-	-	5	-	7	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	3	-	-	4	-	5	-	ns
$f_{max}$	maximum frequency	X1								
		$V_{CC} = 3.3\text{ V}$	125	-	-	100	-	70	-	MHz
		$V_{CC} = 5\text{ V}$	165	-	-	125	-	100	-	MHz
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}$ ; $f_i = 1\text{ MHz}$ ; $V_i = GND\text{ to }V_{CC}$ [4]								
		$V_{CC} = 3.3\text{ V}$	-	4	-	-	-	-	-	pF
		$V_{CC} = 5\text{ V}$	-	5	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2] Typical values are measured at  $V_{CC} = 3.3\text{ V}$ .

[3] Typical values are measured at  $V_{CC} = 5.0\text{ V}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + C_L \times V_{CC}^2 \times f_i / 16384$  where:

$f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  $V_{CC}$  = supply voltage in Volt.

11.1. Waveforms and test circuit

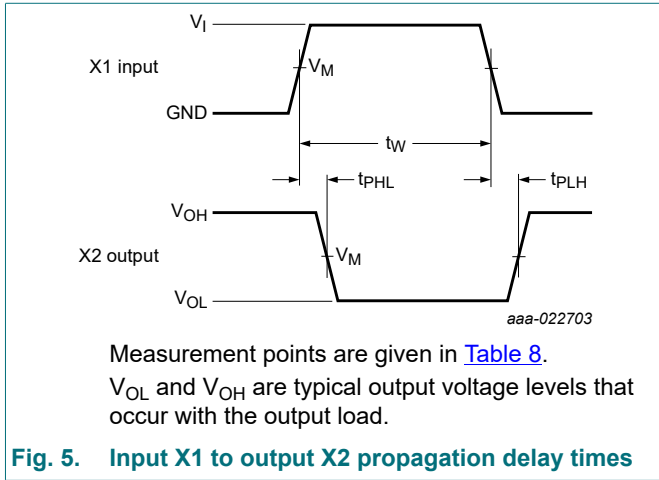


Fig. 5. Input X1 to output X2 propagation delay times

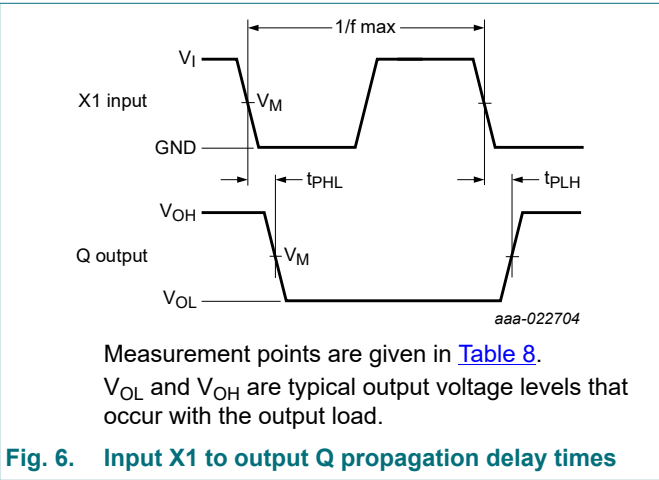


Fig. 6. Input X1 to output Q propagation delay times

Table 8. Measurement points

Inputs		Output
$V_I$	$V_M$	$V_M$
GND to $V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

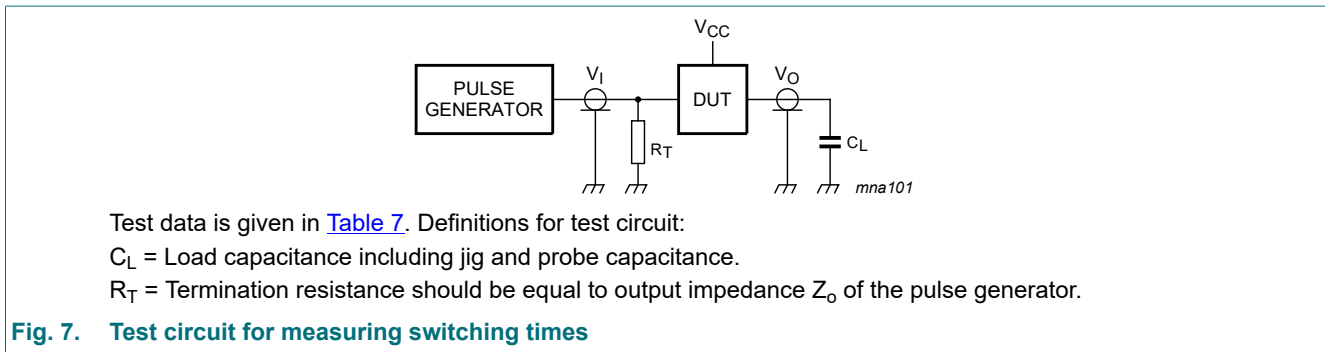
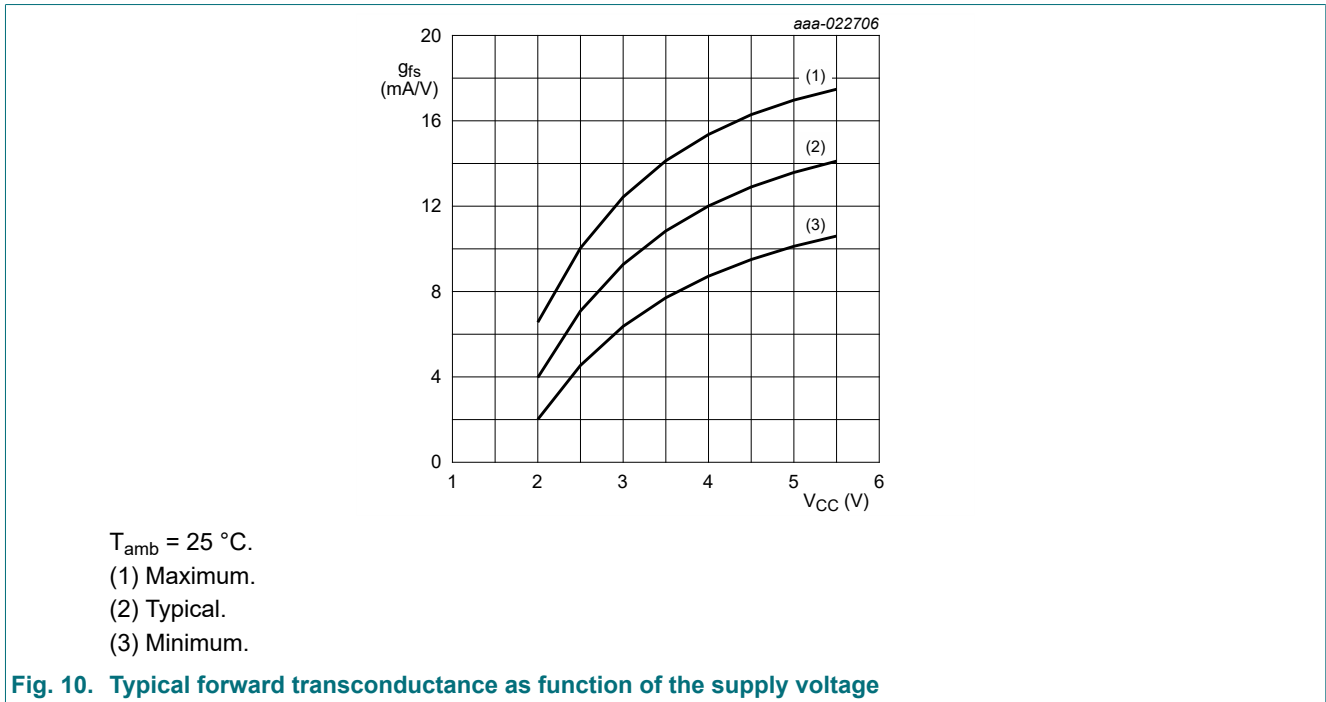
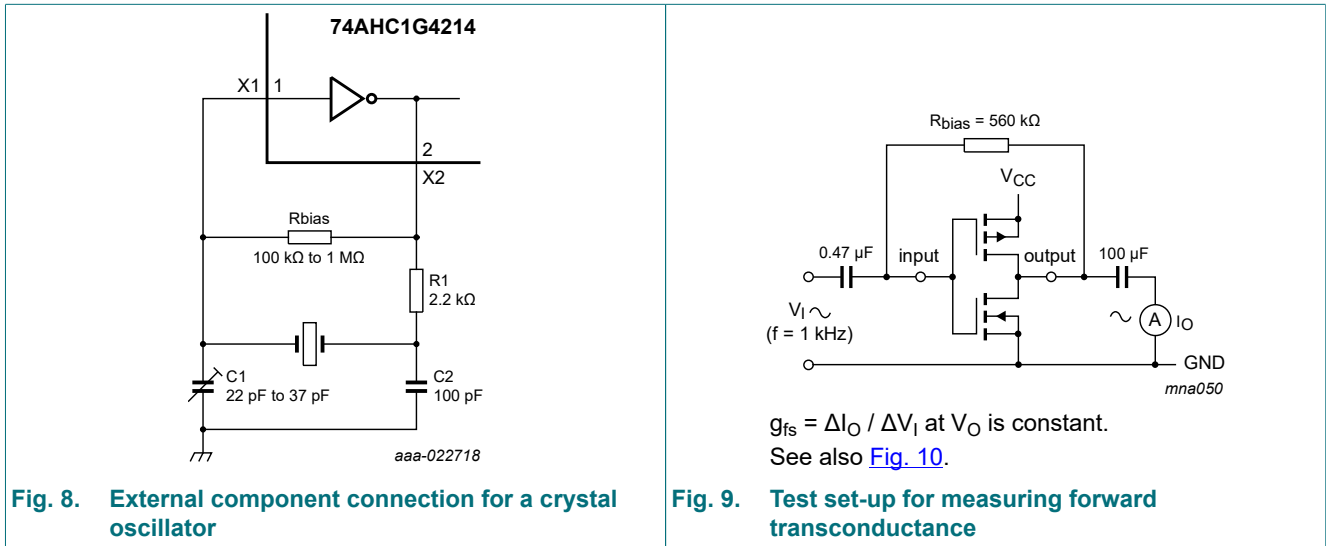


Fig. 7. Test circuit for measuring switching times

## 12. Crystal oscillator

### 12.1. Typical crystal oscillator circuit

A typical crystal oscillator schematic is shown in Fig. 8. R1 is the power limiting resistor, its value depends on the frequency and required stability against changes in  $V_{CC}$  or average  $I_{CC}$ . For starting and maintaining oscillation a minimum transconductance is necessary, so R1 should not be too large. A practical value for R1 is 2.2 k $\Omega$ .



### 13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig. 11. Package outline SOT353-1 (TSSOP5)

## 14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC1G4214 v.5	20231003	Product data sheet	-	74AHC1G4214 v.4
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74AHC1G4214 v.4	20220113	Product data sheet	-	74AHC1G4214 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Fig. 11</a>: Package outline drawing SOT353-1 (TSSOP5) updated.</li> </ul>			
74AHC1G4214 v.3	20180426	Product data sheet	-	74AHC1G4214 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74AHC1G4214 v.2	20161026	Product data sheet	-	74AHC1G4214 v.1
Modifications:	<ul style="list-style-type: none"> <li>Type number 74AHC1G4214GM removed.</li> </ul>			
74AHC1G4214 v.1	20160415	Product data sheet	-	-

## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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