THE DATASHEET OF

670M-01ILF

LOW PHASE NOISE ZERO DELAY BUFFER AND MULTIPLIER ICS670-01

Description

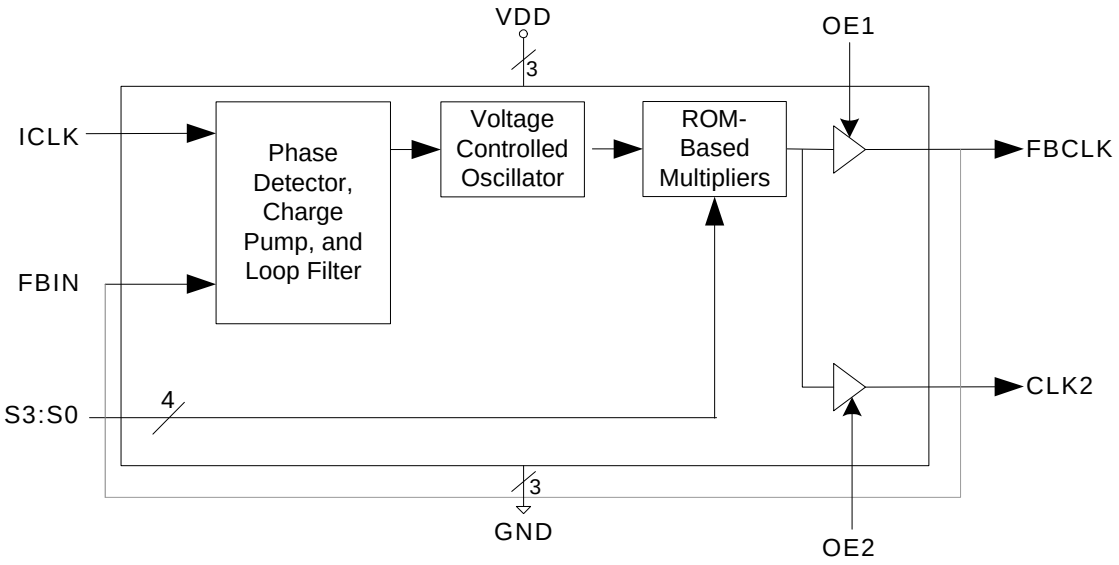
The ICS670-01 is a high-speed, low phase noise, Zero Delay Buffer (ZDB) which integrates IDT's proprietary analog/digital Phase Locked Loop (PLL) techniques. The zero delay feature means that the rising edge of the input clock aligns with the rising edges of the outputs. There are two identical outputs on the chip. FBCLK should be connected to FBIN. Each output has its own output enable pin.

The ICS670-01 is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to video. By allowing off-chip feedback paths, the ICS670-01 can eliminate the delay through other devices. The 15 different on-chip multipliers work in a variety of applications. Arbitrary multiplication factors (including fractions) can be configured on the ICS527.

Features

- Packaged in 16-pin SOIC
- Pb (lead) free package, RoHS compliant
- Clock inputs from 5 to 160 MHz (see page 2)
- Patented PLL with low phase noise
- Output clocks up to 160 MHz at 3.3 V
- 15 selectable on-chip multipliers
- Power down mode available
- Low phase noise: -124 dBc/Hz at 10 kHz
- Output enable function tri-states outputs
- Low jitter–15 ps one sigma
- Full swing CMOS outputs with 25 mA drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- Industrial temperature version available
- Operating voltage of 3.3 V or 5 V

Block Diagram



External Feedback from FBCLK is recommended.

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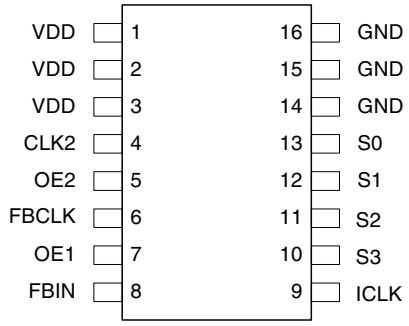
Pin Assignment



Multiplier Select Table

S3	S2	S1	S0	CLK2 (and FBCLK)	Input Range (MHz)
0	0	0	0	Low (Power down entire chip)	-
0	0	0	1	Input x1.333	18 - 120
0	0	1	0	Input x6	5 - 26.67
0	0	1	1	Input x1.5	16.67 - 107
0	1	0	0	Input x3.333	7.5 - 48
0	1	0	1	Input x2.50	10 - 64
0	1	1	0	Input x4	6 - 40
0	1	1	1	Input x1	25 - 160
1	0	0	0	Input x2.333	11 - 69
1	0	0	1	Input x2.666	10 - 60
1	0	1	0	Input x12	5 - 13.33
1	0	1	1	Input x3	8 - 53.33
1	1	0	0	Input x10	5 - 16
1	1	0	1	Input x5	6 - 32
1	1	1	0	Input x8	5 - 20
1	1	1	1	Input x2	12 - 80

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1 - 3	VDD	Input	Power supply. Connect all pins to the same voltage (either 3.3 V or 5 V). Pins 1 and 2 supply the analog sections of the chip.
4	CLK2	Output	Clock output from VCO. Output frequency equals the input frequency times multiplier.
5	OE2	Input	Output clock enable 2. Tri-states the clock 2 output when low.
6	FBCLK	Output	Clock output from VCO. Output frequency equals the input frequency times multiplier.
7	OE1	Input	Output clock enable 1. Tri-states the feedback clock output when low.
8	FBIN	Input	Feedback clock input.
9	ICLK	Input	Clock input. Connect to a 5 - 210 MHz clock.
10	S3	Input	Multiplier select pin 3. Determines outputs per table above. Internal pull-up.
11	S2	Input	Multiplier select pin 2. Determines outputs per table above. Internal pull-up.
12	S1	Input	Multiplier select pin 1. Determines outputs per table above. Internal pull-up.
13	S0	Input	Multiplier select pin 0. Determines outputs per table above. Internal pull-up.
14 - 16	GND	Power	Connect to ground.

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External Components

The ICS670-01 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected from each VDD pin to the ground plane, as close to the device as possible. A series termination resistor of 33Ω should be used to each clock output pin.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS670-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Ambient Operating Temperature, ICS670-01I	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=3.3V ±10%, Ambient temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No Load		35		mA
Short Circuit Current	I_{OS}	Each output		±50		mA
Internal Pull-up Resistor	R_{PU}	OE, select pins		200		kΩ
Input Capacitance	C_{IN}	OE, select pins		5		pF

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AC Electrical Characteristics

VDD = 3.3V ±10%, Ambient Temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency	f_{IN}	See table on page 2	5		160	MHz
Output Clock Frequency					160	MHz
PLL Stabilization Time	t_{STAB}	Input frequency 5 MHz to 160 MHz		4	10	µs
Output Rise Time	t_{OR}	0.8 to 2.0 V, no load			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, no load			1.5	ns
Output Clock Duty Cycle	t_{DC}	measured at VDD/2	45	50	55	%
Input to Output Skew		Note 1		±100		ps
Maximum Absolute Jitter		short term		±45		ps
Maximum Jitter		one sigma		15		ps
Phase Noise, relative to carrier, 125 MHz (x5)		100 Hz offset		-110		dBc/Hz
		1 kHz offset		-122		dBc/Hz
		10 kHz		-124		dBc/Hz
		200 kHz		-117		dBc/Hz

Note 1: Rising edge of ICLK compared with rising edge of CLK2, with FBCLK connected to FBIN, and 15 pF load on CLK2. See graph on page 5 for skew vs. frequency and loading.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

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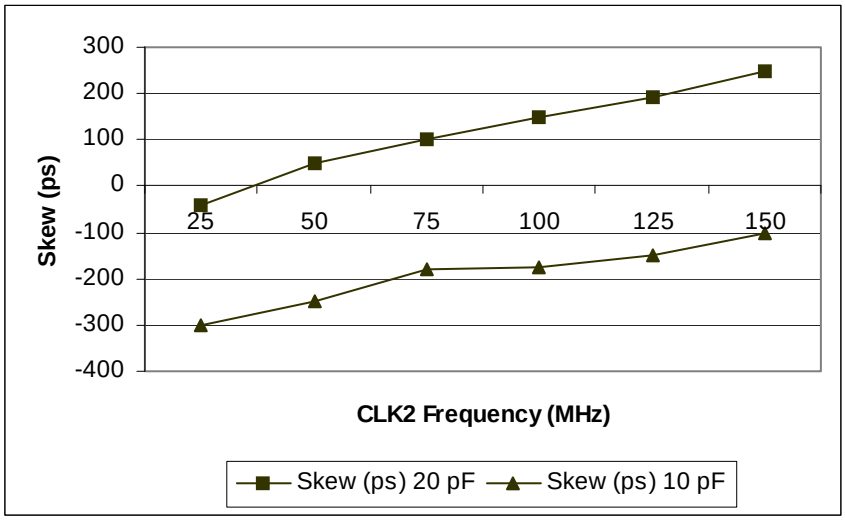
Figure 1. Skew from ICLK to CLK2, with change in load capacitance (VDD = 3.3V)

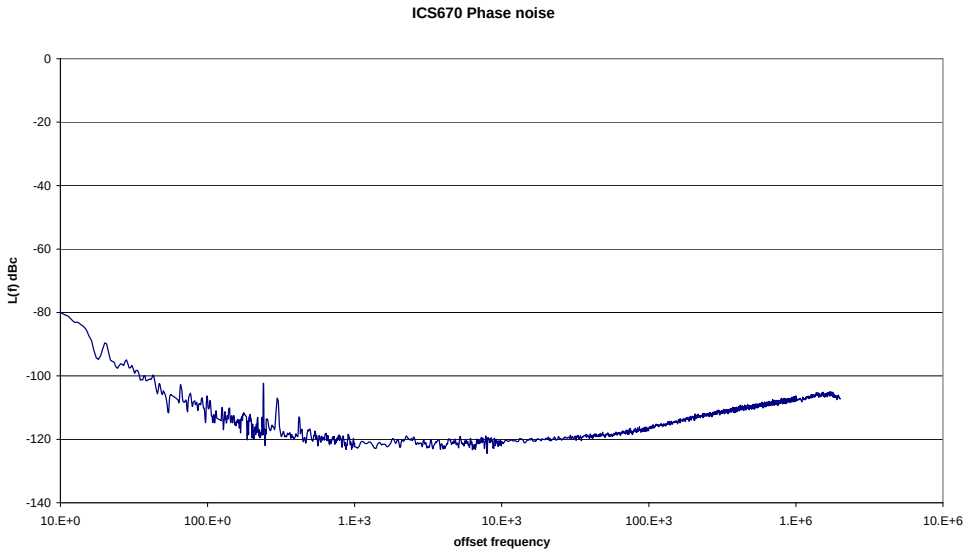


Adjusting Input/Output Skew

The data in Figure 1 can be used to adjust individual circuit characteristics and achieve the minimum possible skew between ICLK and CLK2. With a 125 MHz output, for example, having a total load capacitance of 15 pF will result in nearly zero skew between ICLK and CLK2. Note that the load

capacitance includes board trace capacitance, input capacitance of the load being driven by the ICS670-01, and any additional capacitors connected to CLK2.

Figure 2. Phase Noise for 125 MHz output, 25 MHz clock input (VDD = 3.3V)



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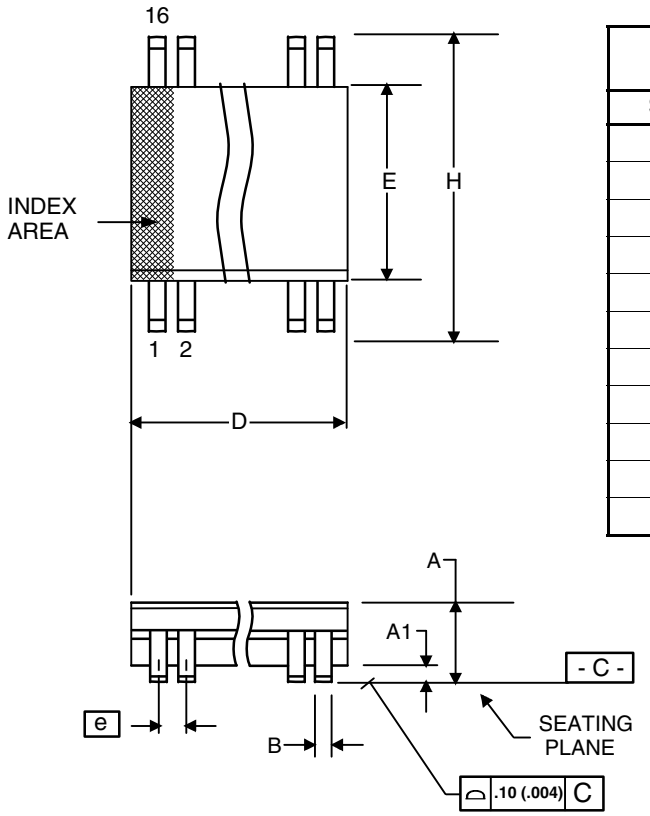
Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
670M-01LF	670M-01LF	Tubes	16-pin SOIC	0 to +70° C
670M-01LFT	670M-01LF	Tape and Reel	16-pin SOIC	0 to +70° C
670M-01ILF	670M-01ILF	Tubes	16-pin SOIC	-40 to +85° C
670M-01ILFT	670M-01ILF	Tape and Reel	16-pin SOIC	-40 to +85° C

"LF" suffix to the part number denotes Pb-Free configuration, RoHS compliant.

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Revision History

Rev.	Date	Originator	Description of Change
L	01/23/15	RDW	Updated AC characterization table with new parameter "PLL Stabilization Time".

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