



**THE DATASHEET OF
656C10005C3T**

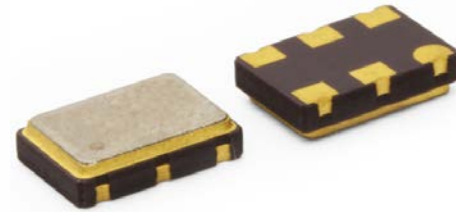


Model 656C

Advanced PLL HCMOS Clock

Features

- Ceramic Surface Mount Package
- Low Phase Jitter Performance, 600fs Typical
- Advanced PLL Design w/ Low Fundamental Crystal
- Frequency Range 10 – 250MHz *
- +2.5V or +3.3V Operation
- Output Enable Standard, Pin 2 Option Available
- Tape and Reel Packaging, EIA-418



Part Dimensions:
7.0 × 5.0 × 1.85mm • 178.462mg

Applications

- Broadcast Video Systems
- Storage Area Networking
- Broadband Access
- PCI Express
- Networking Equipment
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

Standard Frequencies

- 25.00MHz
- 27.00MHz
- 50.00MHz
- 74.25MHz
- 100.00MHz
- 106.25MHz
- 125.00MHz
- 148.50MHz
- 153.60MHz
- 155.52MHz
- 156.25MHz
- 200.00MHz
- 250.00MHz

* See Page 8 for additional developed frequencies.
Check with factory for availability of frequencies not listed.

Description

CTS Model 656C is a low cost, high performance PLL clock oscillator supporting HCMOS output. Employing the latest IC technology, M656C has excellent stability and low phase jitter performance.

Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging																																	
656	C	XXX or XXXX	3	I	3	T																																	
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Notes:

- 1) Refer to document 016-1454-0, Frequency Code Tables.
3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2) 6I Stability/Temperature combination not available.
- 3) Check factory availability when paired with 'I' temperature code.

**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.



Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	4.0	V
Supply Voltage	V_{CC}	±5%	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current	I_{CC}	Maximum Load	-	20	65	mA
Operating Temperature	T_A	-	-20 -40	+25	+70 +85	°C
Storage Temperature	T_{STG}	-	-55	-	+125	°C

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f_O	-		10 - 250		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	-		20, 25 or 50		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC}	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		HCMOS		-
Output Load	C_L	-	-	-	15	pF
Output Voltage Levels	V_{OH} V_{OL}	CMOS Load	0.9 V_{CC} -	- -	- 0.1 V_{CC}	V
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, $C_L = 15$ pF	-	5	10	ns
Start Up Time	T_S	Application of V_{CC}	-	3	5	ms
Enable Function [Tri-State]						
Enable Input Voltage	V_{IH}	Pin 1 or 2 Logic '1', Output Enabled	0.7 V_{CC}	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	-	0.3 V_{CC}	V
Disable Current	I_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	16	22	mA
Enable Time	T_{PLZ}	Pin 1 or 2 Logic '1', Output Enabled	-	-	200	ns
Phase Jitter, RMS	t_{jrms}	Bandwidth 12 kHz - 20 MHz	-	600	<1000	fs
Period Jitter, RMS	p_{jrms}	-	-	3.0	-	ps
Period Jitter, pk-pk	p_{jpk-pk}	-	-	30	-	ps

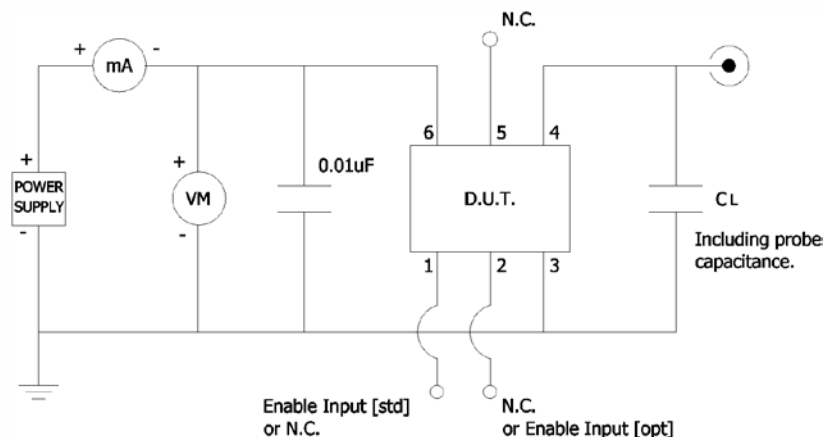
Electrical Specifications

Enable Truth Table

Pin 1 or Pin 2	Pin 4
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

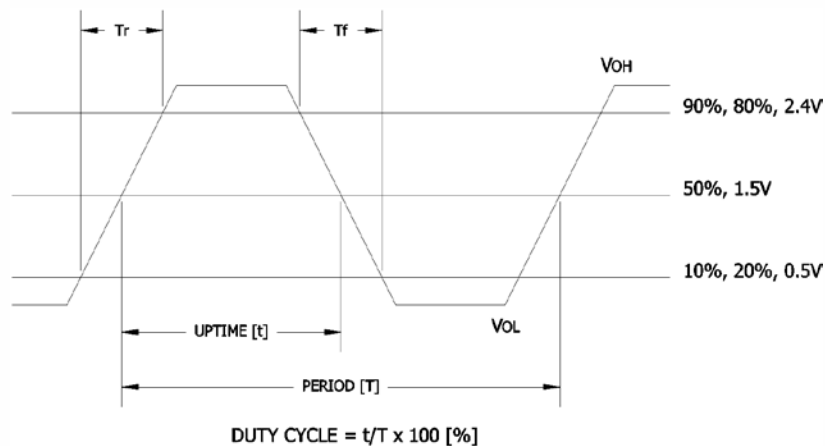
Test Circuit

HCMOS



Output Waveform

HCMOS

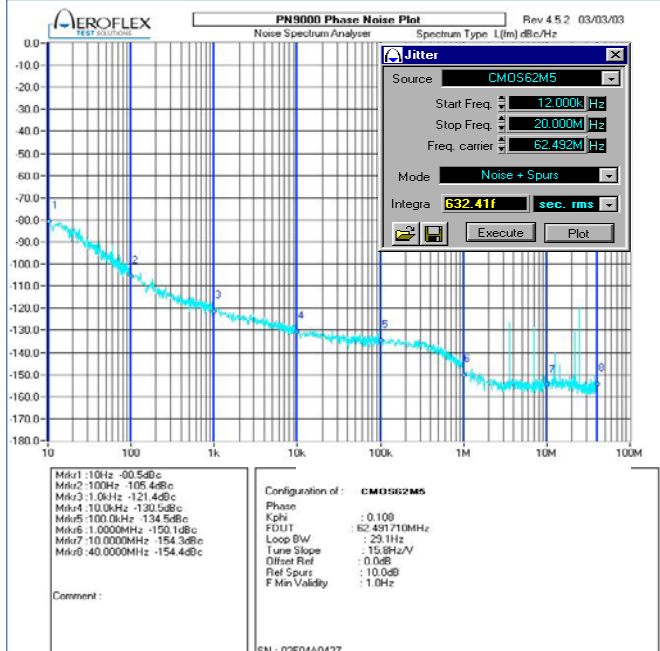


Electrical Specifications

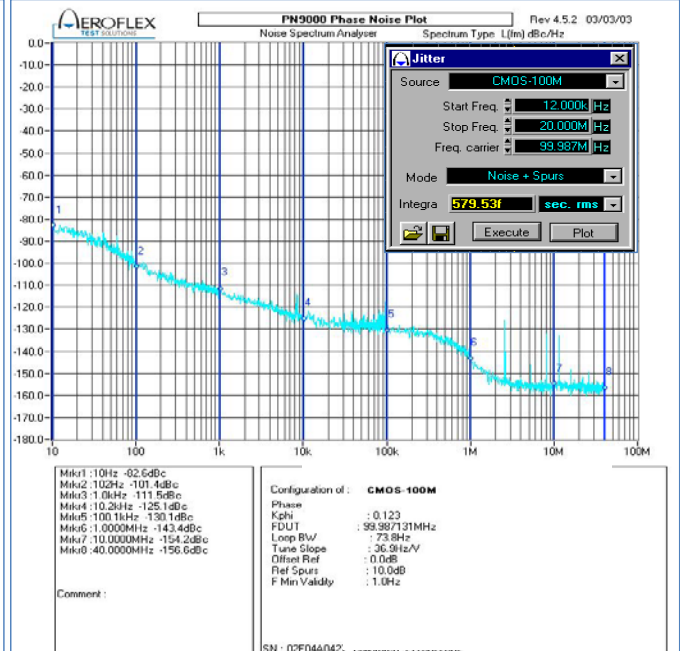
Performance Data

Phase Noise [typical]

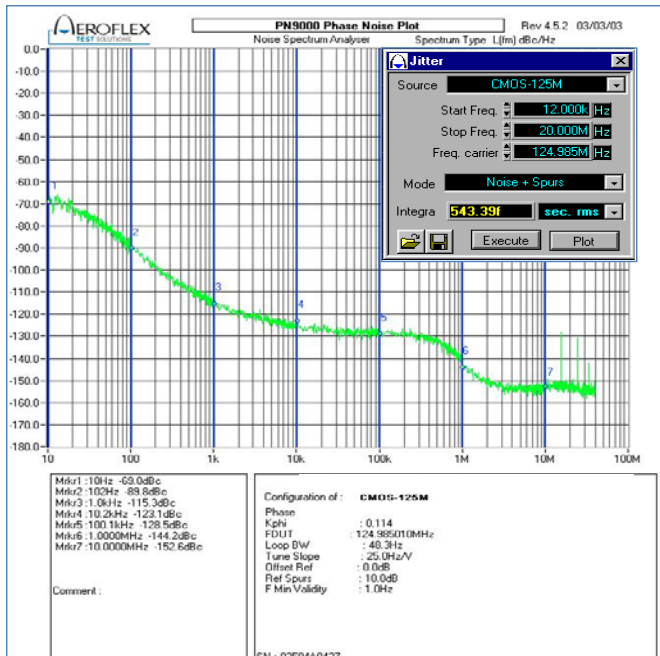
62.50MHz, HCMOS, $V_{CC} = 3.3V$, $T_A = +25^\circ C$



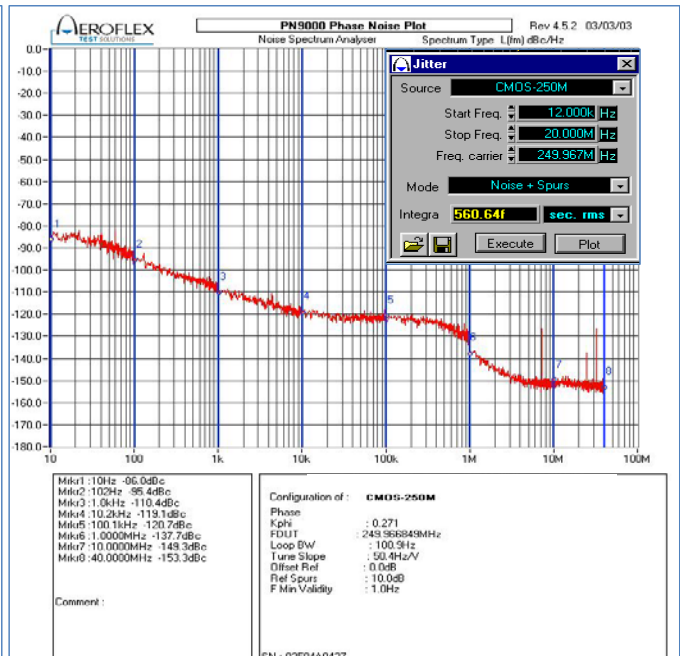
100.00MHz, HCMOS, $V_{CC} = 3.3V$, $T_A = +25^\circ C$



125.00MHz, HCMOS, $V_{CC} = 3.3V$, $T_A = +25^\circ C$



250.00MHz, HCMOS, $V_{CC} = 3.3V$, $T_A = +25^\circ C$





Electrical Specifications

Performance Data

Phase Noise Tabulated

Typical, HCMOS, $V_{CC} = 3.3V$, $T_A = +25^\circ C$

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
HCMOS @ 62.5MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-80.50	
		@ 100Hz	-105.40	
		@ 1kHz	-121.40	
	-	@ 10kHz	-130.50	dBc/Hz
		@ 100kHz	-134.50	
		@ 1MHz	-150.10	
		@ 10MHz	-154.30	
		@ 40MHz	-154.40	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	632.41	fs

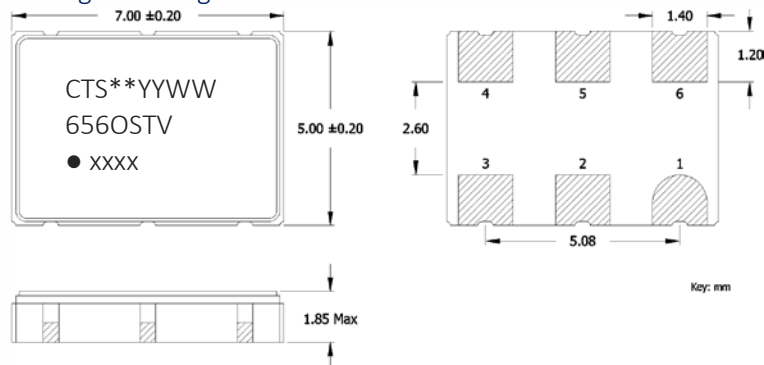
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
HCMOS @ 100.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-82.60	
		@ 100Hz	-101.40	
		@ 1kHz	-111.50	
	-	@ 10kHz	-125.10	dBc/Hz
		@ 100kHz	-130.10	
		@ 1MHz	-143.40	
		@ 10MHz	-154.20	
		@ 40MHz	-156.60	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	579.53	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
HCMOS @ 125.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-69.00	
		@ 100Hz	-89.80	
		@ 1kHz	-115.30	
	-	@ 10kHz	-123.10	dBc/Hz
		@ 100kHz	-128.50	
		@ 1MHz	-144.20	
		@ 10MHz	-152.60	
		@ 40MHz	-153.00	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	543.39	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
HCMOS @ 250.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-86.00	
		@ 100Hz	-95.40	
		@ 1kHz	-110.40	
	-	@ 10kHz	-119.10	dBc/Hz
		@ 100kHz	-120.70	
		@ 1MHz	-137.70	
		@ 10MHz	-149.30	
		@ 40MHz	-153.30	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	560.64	fs

Mechanical Specifications

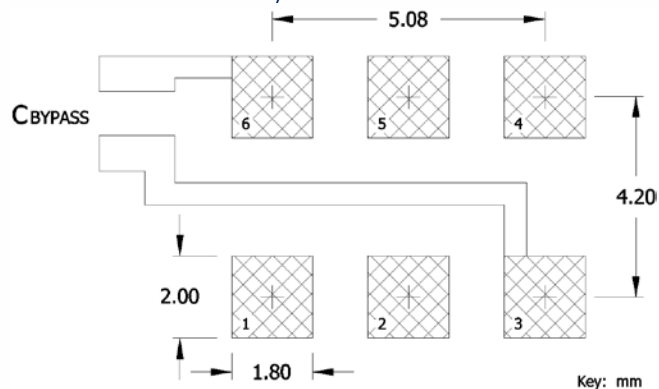
Package Drawing



Marking Information

- ** - Manufacturing Site Code.
- YYWW – Date Code; YY – year, WW – week.
- O – Output Type; C = HCMOS.
- ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
- V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
- xxxx – Frequency Code.
3-digits, frequencies below 100MHz
4-digits, frequencies 100MHz or greater
[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

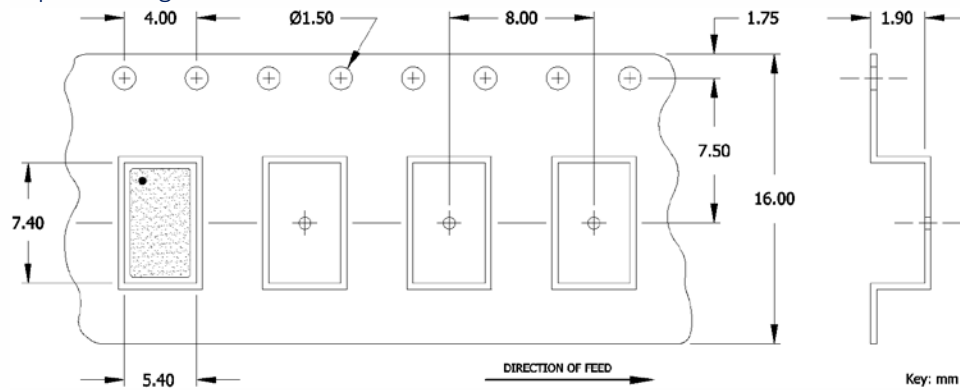
- JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

Pin Assignments

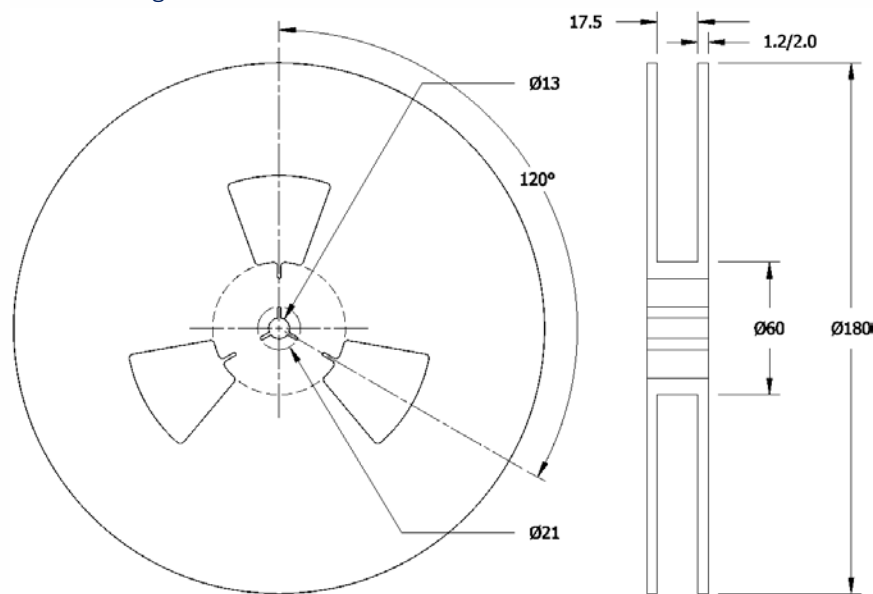
Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	N.C.	No Connect
6	V _{CC}	Supply Voltage

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.



Addendum

Additional Developed Frequencies – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
38.840000	38D	77.760000	777	135.000000	1350	184.320000	1843
38.880000	388	86.700000	867	144.500000	1445	204.800000	2048
43.350000	433	87.351542	873	148.351600	148A	233.000000	2330
45.000000	450	92.160000	921	148.351648	148B	245.760000	2457
54.000000	540	96.000000	960	150.000000	1500		
62.500000	625	104.000000	1040	156.253906	156A		
74.175800	74A	122.880000	1228	160.000000	1600		
76.800000	768	132.000000	1320	161.132800	1611		

Frequency Codes for Cover Page Table – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
25.000000	250	106.250000	1062	156.250000	1562		
27.000000	270	125.000000	1250	200.000000	2000		
50.000000	500	148.500000	1485	250.000000	2500		
74.250000	742	153.600000	1536				
100.000000	1000	155.520000	1555				

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View 656C10005C3T on WIN SOURCE](#)
-  [CTS-Frequency Controls Information](#)

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