



**THE DATASHEET OF  
BQ4013MA-120**



## 128 k × 8 NONVOLATILE SRAM (5 V, 3.3 V)

### FEATURES

- Data Retention for at least 10 Years Without Power
- Automatic Write-Protection During Power-up/Power-down Cycles
- Conventional SRAM Operation, Including Unlimited Write Cycles
- Internal Isolation of Battery before Power Application
- 5-V or 3.3-V Operation
- Industry Standard 32-Pin DIP Pinout

### GENERAL DESCRIPTION

The CMOS bq4013/Y/LY is a nonvolatile 1,048,576-bit static RAM organized as 131,072 words by 8 bits. The integral control circuitry and lithium energy source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single supply for an out-of-tolerance condition. When  $V_{CC}$  falls out of tolerance, the SRAM is unconditionally write-protected to prevent an inadvertent write operation.

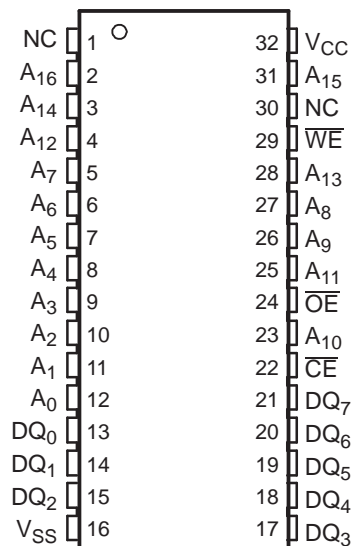
At this time the integral energy source is switched on to sustain the memory until after  $V_{CC}$  returns valid.

The bq4013/Y/LY uses extremely low standby current CMOS SRAMs, coupled with small lithium coin cells to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

The bq4013/Y/LY requires no external circuitry and is compatible with the industry-standard 1-Mb SRAM pinout.

### PIN CONNECTIONS

32-Pin DIP Module  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**DEVICE INFORMATION****Table 1. TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NUMBER		
A <sub>0</sub>	12	I	Address inputs
A <sub>1</sub>	11	I	
A <sub>2</sub>	10	I	
A <sub>3</sub>	9	I	
A <sub>4</sub>	8	I	
A <sub>5</sub>	7	I	
A <sub>6</sub>	6	I	
A <sub>7</sub>	5	I	
A <sub>8</sub>	27	I	
A <sub>9</sub>	26	I	
A <sub>10</sub>	23	I	
A <sub>11</sub>	25	I	
A <sub>12</sub>	4	I	
A <sub>13</sub>	28	I	
A <sub>14</sub>	3	I	
A <sub>15</sub>	31	I	
A <sub>16</sub>	2	I	
$\overline{\text{CE}}$	22	I	Chip-enable input
DQ <sub>0</sub>	13	I/O	Data input/output
DQ <sub>1</sub>	14	I/O	
DQ <sub>2</sub>	15	I/O	
DQ <sub>3</sub>	17	I/O	
DQ <sub>4</sub>	18	I/O	
DQ <sub>5</sub>	19	I/O	
DQ <sub>6</sub>	20	I/O	
DQ <sub>7</sub>	21	I/O	
NC	1	-	No connect
	30	-	
$\overline{\text{OE}}$	24	I	Output enable input
V <sub>CC</sub>	32	I	Supply voltage input
V <sub>SS</sub>	16	-	Ground
$\overline{\text{WE}}$	29	I	Write enable input

**FUNCTIONAL DESCRIPTION**

When power is valid, the bq4013/Y/LY operates as a standard CMOS SRAM. During power-down and power-up cycles, the bq4013/Y/LY acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V<sub>CC</sub> supply for a power-fail-detect threshold V<sub>PFD</sub>. The bq4013 monitors for V<sub>PFD</sub> = 4.62 V typical for use in 5-V systems with 5% supply tolerance. The bq4013Y monitors for V<sub>PFD</sub> = 4.37 V typical for use in 5-V systems with 10% supply tolerance. The bq4013LY monitors for V<sub>PFD</sub> = 2.90 V (typ) for use in 3.3-V systems.

When  $V_{CC}$  falls below the  $V_{PFD}$  threshold, the SRAM automatically write-protects the data. All outputs become high impedance, and all inputs are treated as *don't care*. If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time  $t_{WPT}$ , write-protection takes place.

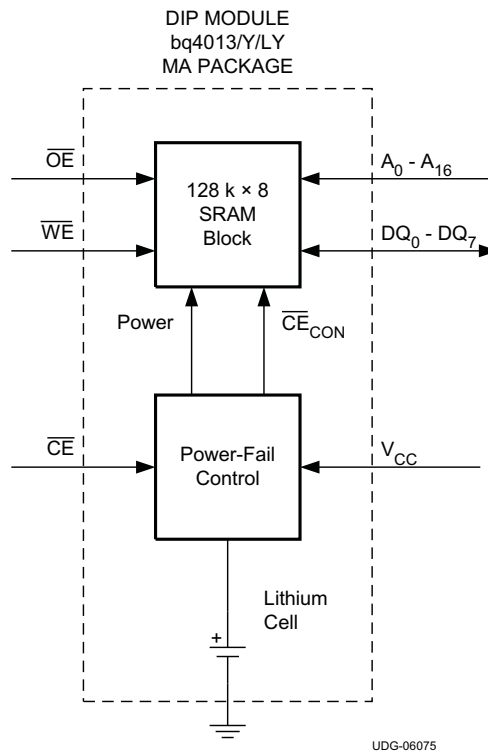
As  $V_{CC}$  falls past  $V_{PFD}$  and approaches  $V_{SO}$ , the control circuitry switches to the internal lithium backup supply, which provides data retention until valid  $V_{CC}$  is applied.

When  $V_{CC}$  returns to a level above the internal backup cell voltage, the supply is switched back to  $V_{CC}$ . After  $V_{CC}$  ramps above the  $V_{PFD}$  threshold, write-protection continues for a time  $t_{CER}$  (120 ms maximum in 5-V system, 85 ms maximum in 3.3-V system) to allow for processor stabilization. Normal memory operation may resume after this time.

The internal coin cells used by the bq4013/Y/LY have an extremely long shelf life and provide data retention for more than 10 years in the absence of system power.

As shipped from TI, the integral lithium cells of the MT-type module are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of  $V_{CC}$ , this isolation is broken, and the lithium backup provides data retention on subsequent power-downs.

### BLOCK DIAGRAM



### TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O OPERATION	POWER
Not selected	H	X	X	High-Z	Standby
Output disable	L	H	H	High-Z	Active
Read	L	H	L	$D_{OUT}$	Active
Write	L	L	X	$D_{IN}$	Active

**ORDERING INFORMATION**

For the most current package and ordering information, see the Package Option Addendum at the end of the datasheet, or see the TI website at [www.ti.com](http://www.ti.com).

**SELECTION GUIDE**

DEVICE NUMBER	MAXIMUM ACCESS TIME (ns)	NEGATIVE SUPPLY TOLERANCE (%)	NOMINAL INPUT VOLTAGE $V_{CC}$ (V)	TEMPERATURE (°C)
bq4013MA-85	85	-5	5	0 to 70
bq4013MA-120	120			
bq4013YMA-70	70	-10		
bq4013YMA-85	85			
bq4013YMA-120	120			
bq4013YMA-70N	70			
bq4013YMA-85N	85			
bq4013LYMA-70N	70		3.3	-40 to 85

**PART NUMBERING**

PRODUCT LINE	MEMORY DENSITY	INPUT VOLTAGE (V)	NEGATIVE SUPPLY TOLERANCE	PACKAGE	SPEED (ns)	TEMPERATURE (°C)
<b>bq40</b>	<b>13</b>	<b>L</b>	<b>Y</b>	<b>MA</b>	<b>70</b>	<b>N</b>
	10 = 8 k × 8 11 = 32 k × 8 13 = 128 k × 8 14 = 256 k × 8 15 = 512 k × 8 16 = 1024 k × 8 17 = 2048 k × 8	Blank = 5 L = 3.3	Blank = 5% Y = 10%	MA = DIP	70 85 100 120 150 200	Blank = Commercial ( 0 to 70)  N = Industrial (-40 to 85)

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

PARAMETER		CONDITION	VALUE	UNIT	
V <sub>CC</sub>	DC voltage applied on VCC relative to VSS		bq4013Y	–0.3 to 7.0	V
			bq4013	–0.3 to 7.0	
			bq4013LY	–0.3 to 6.0	
V <sub>T</sub>	DC voltage applied on any pin excluding VCC relative to VSS	V <sub>VT</sub> ≤ V <sub>CC</sub> + 0.3 V	bq4013Y	–0.3 to 7.0	V
			bq4013	–0.3 to 7.0	
			bq4013LY	–0.3 to (V <sub>CC</sub> + 0.3)	
T <sub>OPR</sub>	Operating temperature	Commercial	0 to 70	°C	
		Industrial	–40 to 85		
T <sub>STG</sub>	Storage temperature	Commercial	–10 to 70		
		Industrial	–40 to 85		
T <sub>BIAS</sub>	Temperature under bias	Commercial	–10 to 70		
		Industrial	–40 to 85		
T <sub>SOLDER</sub>	Soldering temperature	For 10 seconds	260		

(1) Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = T<sub>OPR</sub>)

		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	bq4013Y	4.50	5.00	5.50	V
		bq4013	4.75	5.00	5.50	
		bq4013LY	3.00	3.30	3.60	
V <sub>SS</sub>	Supply voltage	0	0	0		
V <sub>IL</sub>	Low-level input voltage	–0.3		0.8		
V <sub>IH</sub>	High-level Input voltage	2.2		V <sub>CC</sub> + 0.3		

(1) Typical values indicate operation at T<sub>A</sub> = 25°C.

## DC ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = T<sub>OPR</sub>, V<sub>CC(min)</sub> ≤ V<sub>CC</sub> ≤ V<sub>CC(max)</sub>

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>LI</sub>	Input leakage current	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>			±1	μA
I <sub>LO</sub>	Output leakage current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$			±1	
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = –1.0 mA	2.4			V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 2.1 mA			0.4	
I <sub>SB1</sub>	Standby supply current	$\overline{CE} = V_{IH}$		1	2	μA
I <sub>SB2</sub>	Standby supply current	$\overline{CE} \geq V_{CC} - 0.2$ V, 0V ≤ V <sub>IN</sub> ≤ 0.2 V, or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2		0.1	1	mA
I <sub>CC</sub>	Operating supply current	bq4013			50	mA
		bq4013Y	Minimum cycle, duty = 100%, $\overline{CE} = V_{IL}$ , I <sub>I/O</sub> = 0 mA			
		bq4013LY				
V <sub>PFD</sub>	Power-fail-detect voltage	bq4013	4.55	4.62	4.75	V
		bq4013Y	4.30	4.37	4.50	
		bq4013LY	2.85	2.90	2.95	
V <sub>SO</sub>	Supply switch-over voltage	bq4013		3		V
		bq4013Y		3		
		bq4013LY		2.9		

(1) Typical values indicate operation at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V or V<sub>CC</sub> = 3.3 V.

**CAPACITANCE ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{CC} = 5.0\text{ V}$  or  $V_{CC} = 3.3\text{ V}$ )**

PARAMETER <sup>(1)</sup>		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{I/O}$	Input/output capacitance	Output voltage = 0 V			8	pF
$C_{IN}$	Input capacitance	Input voltage = 0 V			10	

(1) Ensured by design. Not production tested.

**AC TEST CONDITIONS**

PARAMETER	TEST CONDITIONS	
	5 V	3.3 V
Input pulse levels	0 V to 3.0 V	0 V to $V_{CC}$
Input rise and fall times	5 ns	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)	50 %
Output load (including scope and jig)	See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>	See <a href="#">Figure 3</a> and <a href="#">Figure 4</a>

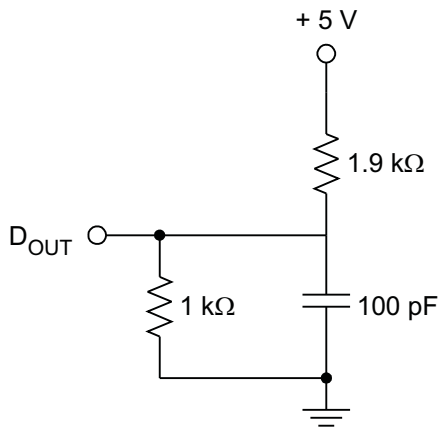


Figure 1. 5-V Output Load A

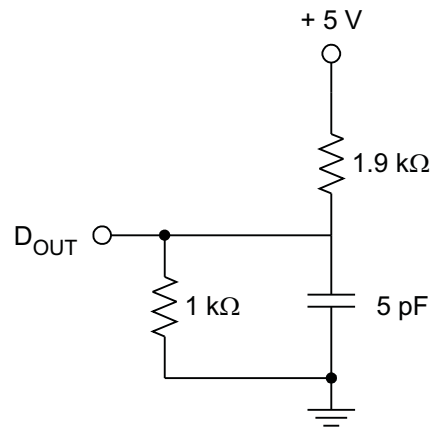


Figure 2. 5-V Output Load B

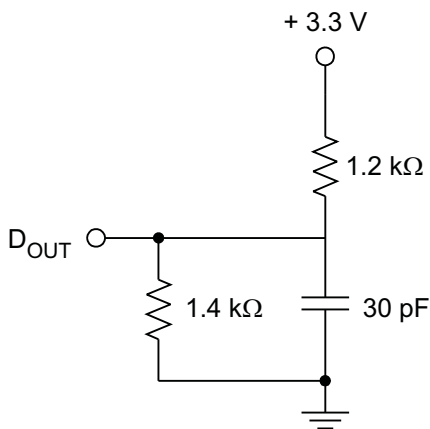


Figure 3. 3.3-V Output Load A

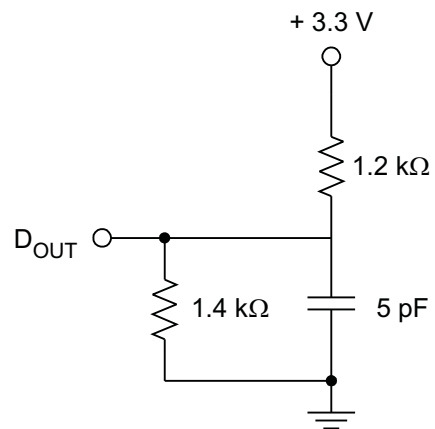
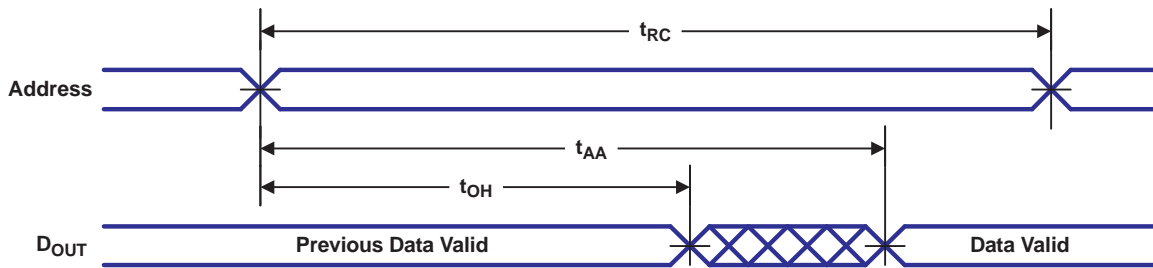


Figure 4. 3.3-V Output Load B

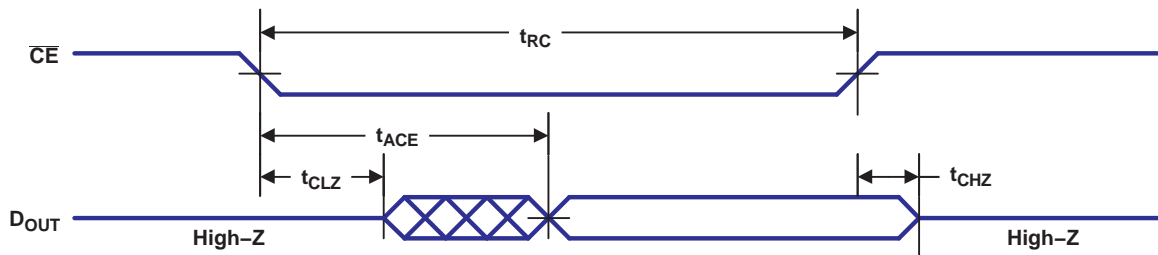
**Table 2. READ CYCLE ( $T_A = T_{OPR}$ ,  $V_{CC(min)} \leq V_{CC} \leq V_{CC(max)}$ )**

PARAMETER		TEST CONDITIONS	-70		-85		-120		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{RC}$	Read cycle time		70		85		120		ns
$t_{AA}$	Address access time	Output load A		70		85		120	
$t_{ACE}$	Chip enable access time			70		85		120	
$t_{OE}$	Output enable to output valid			35		45		60	
$t_{CLZ}$	Chip enable to output in low Z	Output load B	5		5		5		
$t_{OLZ}$	Output enable to output in low Z		0		0		0		
$t_{CHZ}$	Chip disable to output in high Z		0	25	0	35	0	45	
$t_{OHZ}$	Output disable to output in high Z		0	25	0	25	0	35	
$t_{OH}$	Output hold from address change	Output load A	10		10		10		



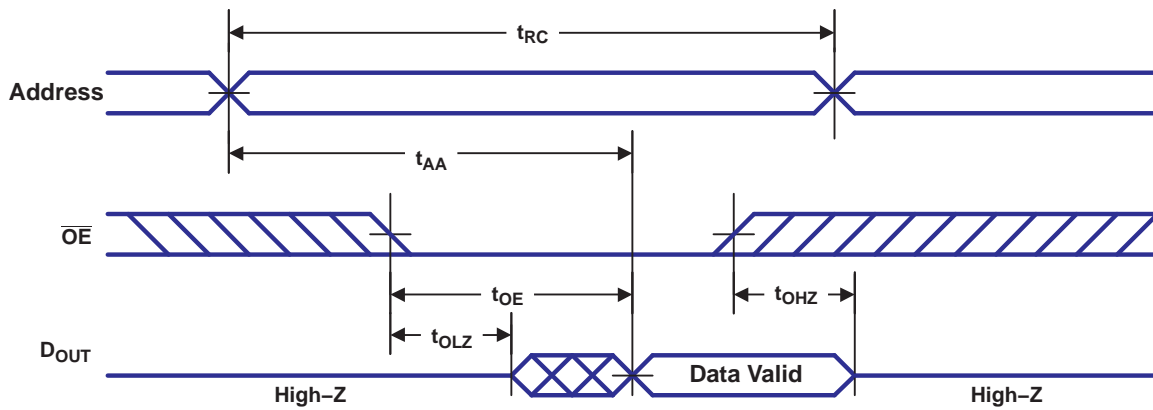
- (1)  $\overline{WE}$  is held high for a read cycle.
- (2) Device is continuously selected:  $\overline{CE} = \overline{OE} = V_{IL}$ .

**Figure 5. Read Cycle No. 1 (Address Access) <sup>(1)(2)</sup>**



- (1)  $\overline{WE}$  is held high for a read cycle.
- (2) Device is continuously selected:  $\overline{CE} = \overline{OE} = V_{IL}$ .
- (3) Address is valid prior to or coincident with  $\overline{CE}$  transition low.

**Figure 6. Read Cycle No. 2 ( $\overline{CE}$  Access) <sup>(1)(2)(3)</sup>**



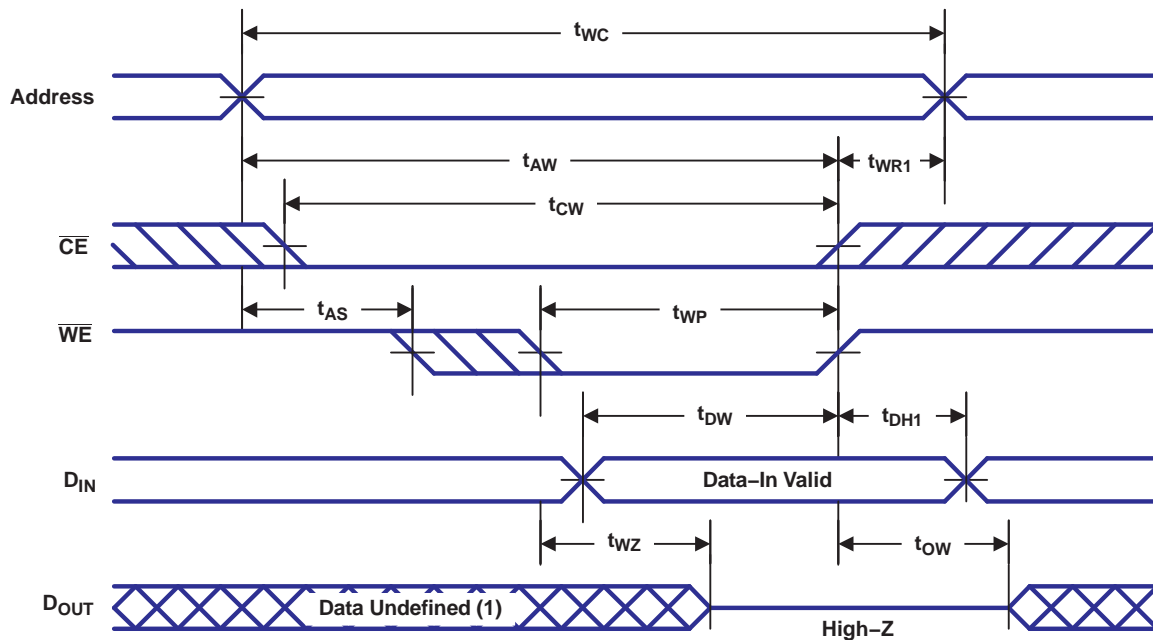
- (1)  $\overline{WE}$  is held high for a read cycle.
- (2) Device is continuously selected:  $\overline{CE} = V_{IL}$ .

Figure 7. Read Cycle No. 3 (OE Access) <sup>(1)(2)</sup>

Table 3. WRITE CYCLE ( $T_A = T_{OPR}$ ,  $V_{CC(min)} \leq V_{CC} \leq V_{CC(max)}$ )

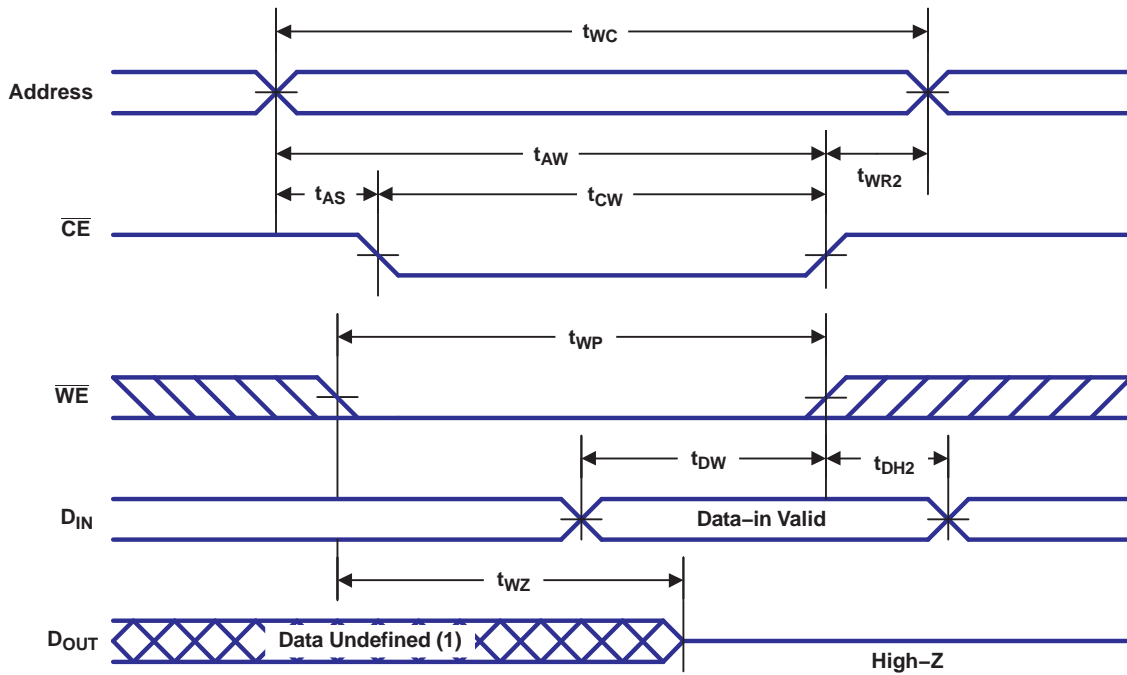
PARAMETER		TEST CONDITIONS	-70		-85		-120		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{WC}$	Write cycle time		70		85		120		ns
$t_{CW}$	Chip enable to end of write	See (1)	65		75		100		
$t_{AW}$	Address valid to end of write	See (1)	65		75		100		
$t_{AS}$	Address setup time	Measured from address valid to beginning of write.(2)	0		0		0		
$t_{WP}$	Write pulse width	Measured from beginning of write to end of write.(1)	55		65		85		
$t_{WR1}$	Write recovery time (write cycle 1)	Measured from $\overline{WE}$ going high to end of write cycle.(3)	5		5		5		
$t_{WR2}$	Write recovery time (write cycle 2)	Measured from $\overline{CE}$ going high to end of write cycle.(3)	15		15		15		
$t_{DW}$	Data valid to end of write	Measured to first low-to- high transition of either $\overline{CE}$ or $\overline{WE}$ .	30		35		45		
$t_{DH1}$	Data hold time (write cycle 1)	Measured from $\overline{WE}$ going high to end of write cycle.(4)	0		0		0		
$t_{DH2}$	Data hold time (write cycle 2)	Measured from $\overline{CE}$ going high to end of write cycle.(4)	0		0		0		
$t_{WZ}$	Write enabled to output in high Z	I/O pins are in output state.(5)	0	25	0	30	0	40	
$t_{OW}$	Output active from end of write	I/O pins are in output state.(5)	5		5		5		

- (1) A write ends at the earlier transition of  $\overline{CE}$  going high and  $\overline{WE}$  going high.
- (2) A write occurs during the overlap of a low  $\overline{CE}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CE}$  going low and  $\overline{WE}$  going low.
- (3) Either  $t_{WR1}$  or  $t_{WR2}$  must be met.
- (4) Either  $t_{DH1}$  or  $t_{DH2}$  must be met.
- (5) If  $\overline{CE}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in high-impedance state.



- (1)  $\overline{CE}$  or  $\overline{WE}$  must be high during address transition.
- (2) Because I/O may be active ( $\overline{OE}$  low) during this period, data input signals of opposite polarity to the outputs must not be applied.
- (3) If  $\overline{OE}$  is high, the I/O pins remain in a state of high impedance.

Figure 8. Write Cycle No. 1 ( $\overline{WE}$ -Controlled) (1)(2)(3)



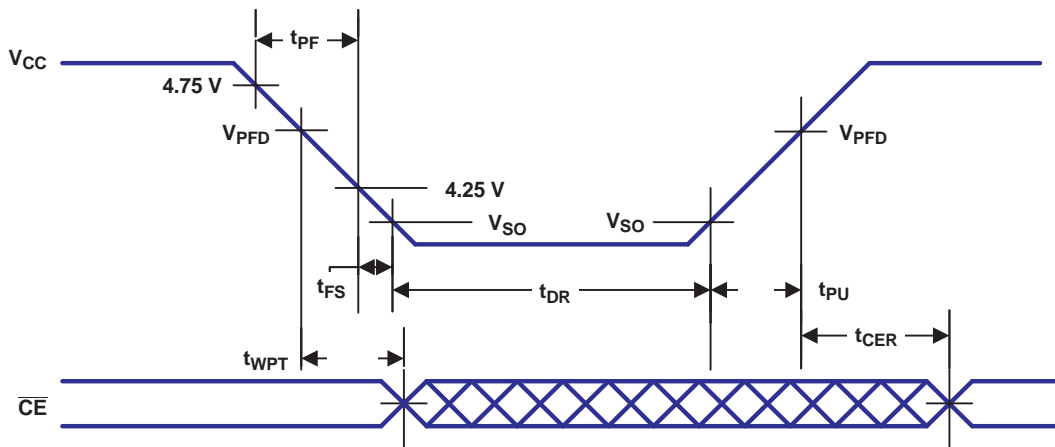
- (1)  $\overline{CE}$  or  $\overline{WE}$  must be high during address transition.
- (2) Because I/O may be active ( $\overline{OE}$  low) during this period, data input signals of opposite polarity to the outputs must not be applied.
- (3) If  $\overline{OE}$  is high, the I/O pins remain in a state of high impedance.
- (4) Either  $t_{WR1}$  or  $t_{WR2}$  must be met.
- (5) Either  $t_{DH1}$  or  $t_{DH2}$  must be met.

**Figure 9. Write Cycle No. 2 ( $\overline{CE}$ -Controlled) (1)(2)(3)(4)(5)**

**Table 4. 5-V POWER-DOWN/POWER-UP ( $T_A = T_{OPR}$ )**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PF}$	$V_{CC}$ slew, 4.75 to 4.25 V		300			$\mu$ s
$t_{FS}$	$V_{CC}$ slew, 4.25 to $V_{SO}$		10			$\mu$ s
$t_{PU}$	$V_{CC}$ slew, $V_{SO}$ to $V_{PFD}$ (max.)		0			$\mu$ s
$t_{CER}$	Chip enable recovery time	Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up.	40	80	120	ms
$t_{DR}$	Data-retention time in absence of $V_{CC}$	$T_A = 25^\circ\text{C}$ <sup>(2)</sup>	10			years
$t_{WPT}$	Write-protect time	Delay after $V_{CC}$ slews down past $V_{PFD}$ before SRAM is writeprotected.	40	100	150	$\mu$ s

- (1) Typical values indicate operation at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .  
 (2) Batteries are disconnected from circuit until after  $V_{CC}$  is applied for the first time.  $t_{DR}$  is the accumulated time in absence of power beginning when power is first applied to the device.

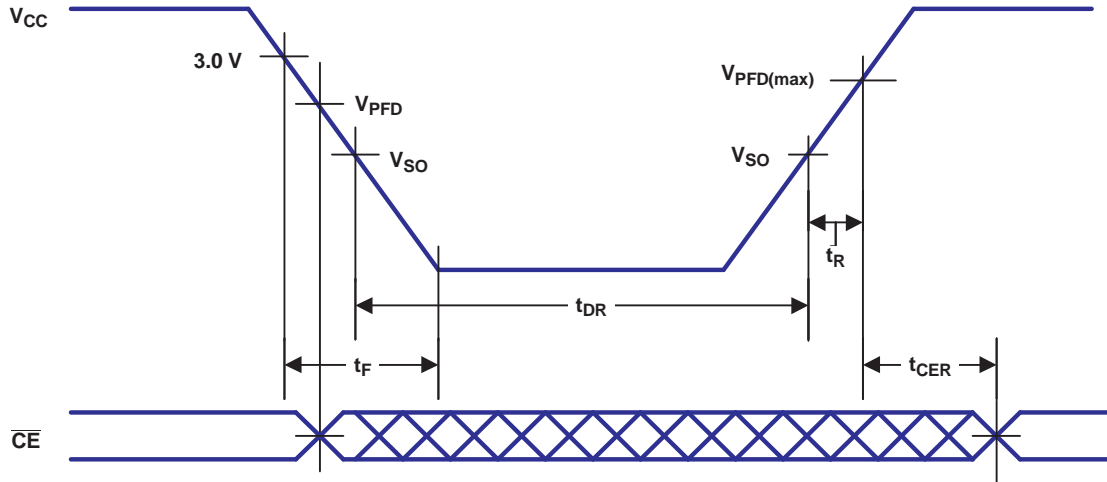


**Figure 10. 5-V Power-Down/Power-Up Timing**

**Table 5. 3.3-V POWER-DOWN/POWER-UP ( $T_A = T_{OPR}$ )**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_F$	$V_{CC}$ slew, 3 V to 0 V		300			$\mu s$
$t_R$	$V_{CC}$ slew, $V_{SO}$ to $V_{PFD(max)}$		100			
$t_{CER}$	Chip enable recovery time	Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up.	10		85	ms
$t_{DR}$	Data-retention time in absence of $V_{CC}$	$T_A = 25^\circ C^{(2)}$	10			years

- (1) Typical values indicate operation at  $T_A = 25^\circ C$ ,  $V_{CC} = 3.3 V$ .
- (2) Batteries are disconnected from circuit until after  $V_{CC}$  is applied for the first time. Data retention time ( $t_{DR}$ ) is the accumulated time in absence of power beginning when power is first applied to the device.



**Figure 11. 3.3-V Power-Down/Power-Up Timing**

**CAUTION:**

Negative undershoots below the absolute maximum rating of -0.3 V in battery-backup mode may affect data integrity.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ4013LYMA-70	OBSOLETE	DIP MODULE	MA	32		TBD	Call TI	Call TI			
BQ4013LYMA-70N	OBSOLETE	DIP MODULE	MA	32		TBD	Call TI	Call TI	-40 to 85		
BQ4013MA-120	OBSOLETE	DIP MODULE	MA	32		TBD	Call TI	Call TI	0 to 70		
BQ4013MA-85	LIFEBUY	DIP MODULE	MA	32		TBD	Call TI	Call TI	0 to 70		
BQ4013YMA-120	OBSOLETE	DIP MODULE	MA	32		TBD	Call TI	Call TI	0 to 70		
BQ4013YMA-70	OBSOLETE	DIP MODULE	MA	32		TBD	Call TI	Call TI	0 to 70		
BQ4013YMA-70N	OBSOLETE	DIP MODULE	MA	32		TBD	Call TI	Call TI	-40 to 85		
BQ4013YMA-85	OBSOLETE	DIP MODULE	MA	32		TBD	Call TI	Call TI	0 to 70		
BQ4013YMA-85N	OBSOLETE	DIP MODULE	MA	32		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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