THE DATASHEET OF

BQ26100DRPRG4

bq26100 SHA-1/HMAC-based security and authentication IC with an SDQ interface

1 Features

- Provides authentication of battery packs through SHA-1 engine based HMAC
- 160-byte one-time programmable (OTP), 16-bytes EEPROM
- Internal time-base eliminates external crystal oscillator
- Low-power operating modes:
  - Active: < 50 μA
  - Sleep: 8 μA typical
- Single-wire SDQ interface
- Powers directly from the communication bus
- 6-lead VSON package

2 Applications

- Cellular phones
- PDA and smart phones
- MP3 players
- Digital cameras
- Internet appliances
- Handheld devices

3 Description

The bq26100 device provides a method to authenticate battery packs, ensuring that only packs manufactured by authorized sub-contractors are used in the end application. The security is achieved using the SHA-1 hash function inside the widely adopted keyed-hash message authentication code (HMAC) construction. A unique 128-bit key is stored in each bq26100 device, allowing the host to authenticate each pack.

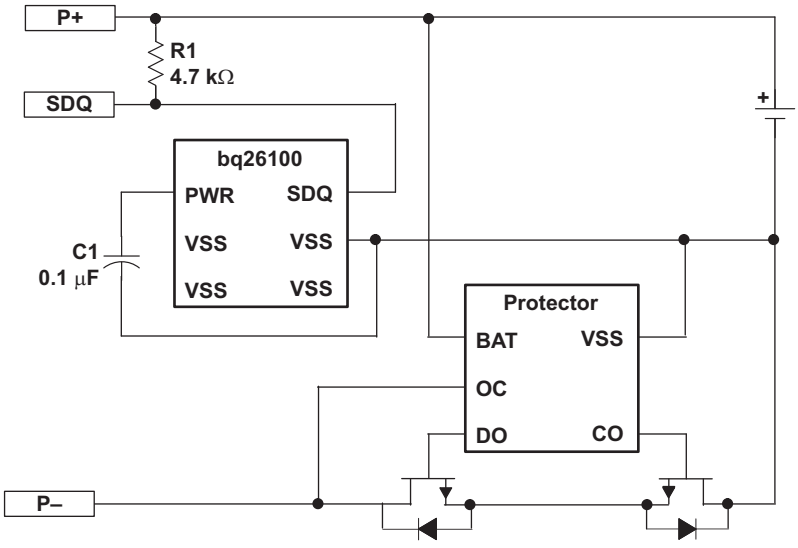
The bq26100 device communicates to the system over a simple one-wire bi-directional serial interface. The 5-kbits/s SDQ bus interface reduces communications overhead in the external microcontroller. The bq26100 device also derives power over the SDQ bus line via an external capacitor.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq26100	VSON (6)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

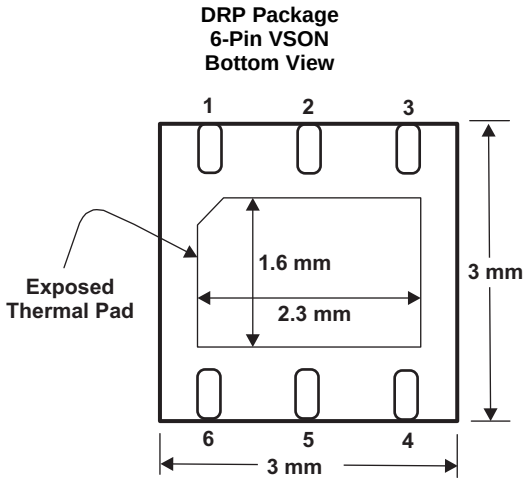
Changes from Revision B (June 2015) to Revision C **Page**

- Changed the pinout view label in *Pin Configuration and Functions* ... 3

Changes from Revision A (February 2007) to Revision B **Page**

- Changed SON to VSON ... 1
- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed formatting of code ... 12

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PWR	1	I/O	Power capacitor connection
SDQ	6	I/O	Single-wire SDQ interface to host
VSS	2, 3, 4, 5	I	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply voltage (SDQ all with respect to VSS)	–0.3	7.7	V
	Output current (SDQ)		5	mA
T_A	Operating free-air temperature	–40	85	°C
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{sdq}	Pull-up voltage	2.5		V
T_J	Operating free-air temperature	–40		°C

6.4 Thermal Information

THERMAL METRIC[1]		BQ26100 DRP (VSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

all parameters over operating free-air temperature and supply voltage range (unless otherwise noted) (memory programming and authentication were tested with R1 = 4.7 kΩ, C1 = 0.1 µF over pullup voltage range)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power up communication delay	Power capacitor charge time		100		ms
I_{sleep}	Sleep current			8	11	µA
$I_{sdq(Vsdq)}$	V_{sdq} Current	$V_{sdq} \geq V_{sdq(min)}$			50	µA
	OTP Memory programming voltage		6.8	7	7.7	V
	OTP Memory programming time			100		µs/byte
	EEPROM Programming current (peak current)			83		µA
	EEPROM Peak current duration			100		µs
	EEPROM Programming time			50		ms
SDQ						
V_{IL}	Input low-level voltage				0.63	V
I_{OL}	Output low sink current	V_{OL} = 0.4 V			1	mA

6.6 Standard Serial Communication (SDQ) Timing

over recommended operating temperature and supply voltage range (unless otherwise noted) (See Figure 1)

		MIN	NOM	MAX	UNIT
t_{RSTL}	Reset time – low	480			µs
t_{RSTH}	Reset time – high	480			µs
t_{PDL}	Presence detect – low	60		240	µs
t_{PDH}	Presence detect – high	15		60	µs
t_{REC}	Recovery time	1			µs
t_{SLOT}	Host bit window	60		120	µs
t_{LOW1}	Host sends 1	1		13	µs
t_{LOW0}	Host sends 0	60		120	µs
t_{LOWR}	Host read bit start	1		13	µs
t_{SLOT}	bq26100 bit window	60		120	µs
t_{SU}	bq26100 data setup			1	µs
t_{RDV}	bq26100 data valid		exactly 15		µs
$t_{RELEASE}$	bq26100 data release	0	15	45	µs

6.7 OTP Programming Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pon}	Program setup time		2			µs
t_{rise}	Pulse rise time		1		10	µs
t_{prog}	Pulse high time	Single byte programming	300			µs
		Key programming	3			µs
t_{fall}	Pulse fall time		1		10	µs

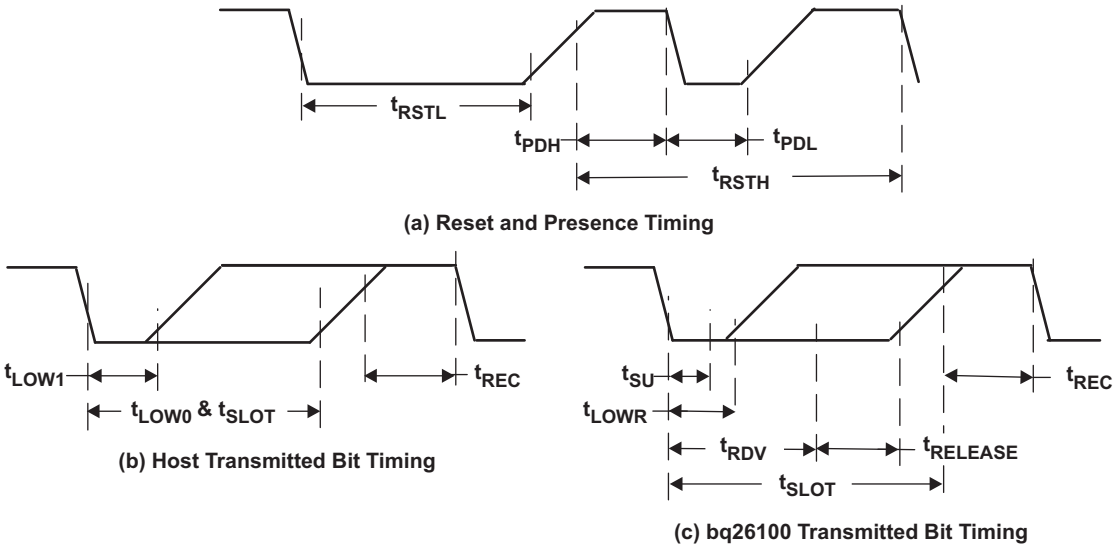


Figure 1. SDQ Timing Diagrams

6.8 Typical Characteristics

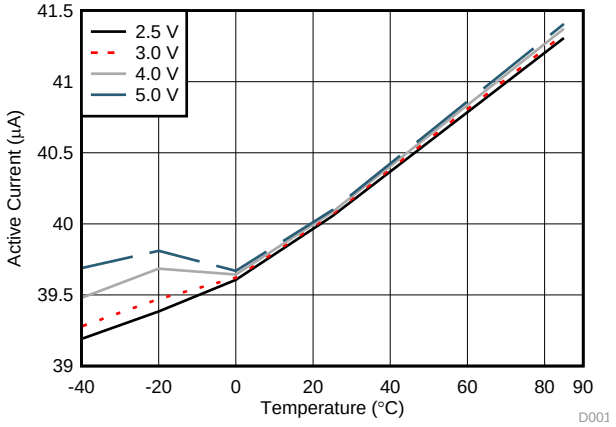


Figure 2. Active Current Across SDQ Voltage and Temperature (Not Authenticating)

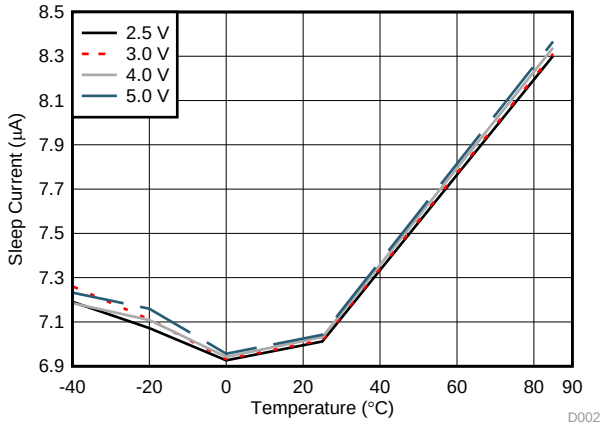


Figure 3. Sleep Current Across SDQ Voltage and Temperature

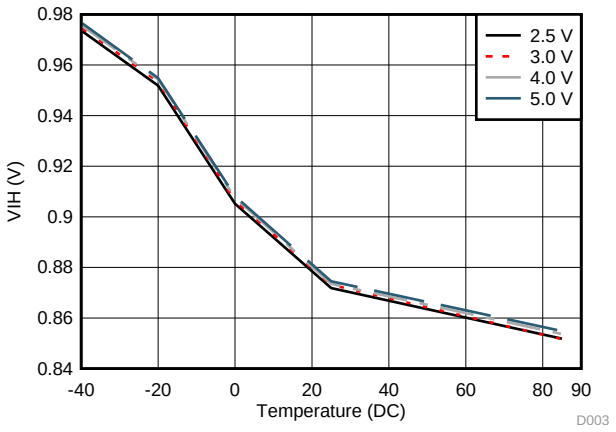


Figure 4. VIH Across SDQ Voltage and Temperature

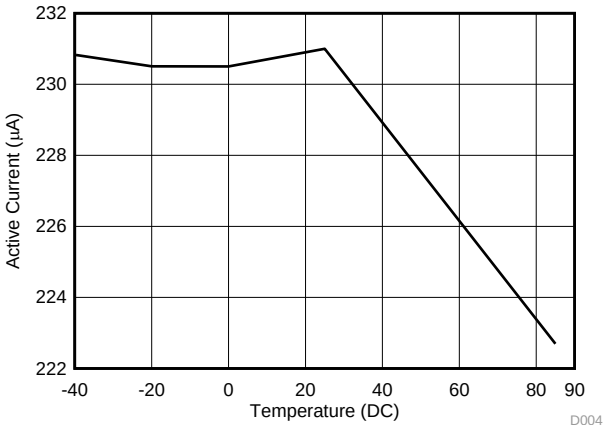


Figure 5. Active Current Across Temperature (While Authenticating)

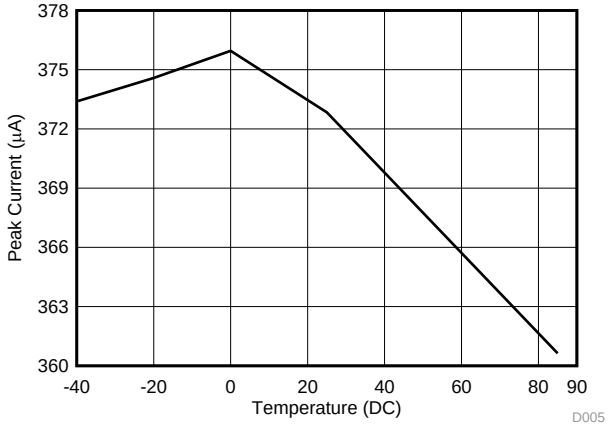


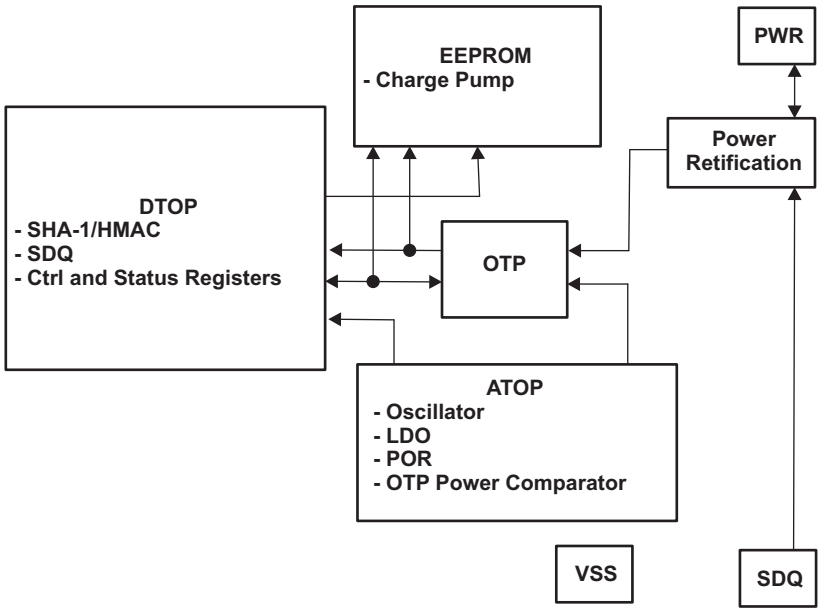
Figure 6. Peak Current Across Temperature (While Authenticating)

7 Detailed Description

7.1 Overview

The bq26100 device is a small memory device for battery packs or accessories. The device contains a mix of One Time Programmable (OTP) and multi-write EEPROM non-volatile memory with authentication functions that can be used to validate the battery/accessory for usage in the host system. The memory consists of five 32-byte pages of general use OTP non-volatile memory and a 16-byte page of EEPROM to be used at the host system designer's discretion. An external high voltage is required for programming the OTP, but is not necessary for programming the EEPROM.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Non-Volatile Memory

The bq26100 device has a bq2022 compatible memory and command structure with new commands to access added memory. The bq26100 device uses a combination of non-volatile OTP and non-volatile EEPROM. The OTP should be programmed in the factory as an external voltage is required to program the bits; the EEPROM can be programmed in the field, with the programming voltage generated automatically by an internal-charge pump.

Four pages of 32x8-bits OTP are accessed with the bq2022 compatible command set, while a fifth page of 32x8-bits are accessed with a new command set. Each page of OTP can be locked once programmed, blocking further writes to the page. There is an additional provision to allow for page redirection at the host in the event that a page is programmed incorrectly. The redirection is not automatic, but a host system can determine where a page redirection is occurring and read the appropriate page for uncorrupted data.

The EEPROM consists of 16x8-bits that can be written in the same way as for RAM-based volatile memory. The timing of the writes is different than writing to RAM to allow for the internal charge pump to create the voltage necessary to set the bit values.

7.3.2 Authentication

The bq26100 device contains a SHA-1 engine to generate a modified version of the FIPS 180 HMAC. The authentication uses a challenge or public message transmitted from the host and a secret key stored on the bq26100 device to generate a 160-bit hash that will be unique. The contents of the challenge are unimportant, but each challenge should be generated randomly to improve the security of the authentication.

To compute the HMAC, let H designate the SHA-1 hash function, M designate the message transmitted to the bq26100 device, and KD designate the unique 128 bit device key of the device. HMAC(M) is defined as:

$$H[KD \,||\, H(KD \,||\, M)] \quad (1)$$

where

- || symbolizes an append operation

The message, *M*, is appended to the device key, *KD*, and padded to become the input to the SHA-1 hash. The output of this first calculation is then appended to the device key, *KD*, padded again, and cycled through the SHA-1 hash a second time. The output is the HMAC digest value.

The secret key is stored in separate OTP available in bq26100 . The key space is split into two 64-bit spaces that can be programmed and locked at separate times, providing an opportunity to split the key between two different programming entities to ensure that no key leak can occur from a single source.

7.3.3 Communication and Power

The bq26100 device uses a single-wire communication protocol, SDQ, that allows for broadcast or targeted communication to a number of devices on the one-wire bus. Each device is programmed with a unique 64-bit address and the protocol consists of an automatic arbitration scheme that allows the host to determine the ID of every device on the bus.

The bq26100 device takes advantage of the pullup on the SDQ line to power a capacitor connected to the PWR pin and the charge on this capacitor is used parasitically when the SDQ line is low. As a result, there is no need for additional power to be supplied to the device.

7.4 Device Functional Modes

7.4.1 Profile Command

Pack manufacturers can use the profile command to determine how the device should be programmed.

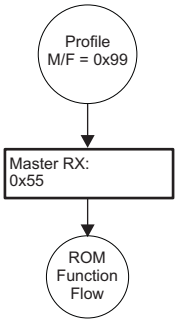


Figure 7. Profile Command Flow

7.4.2 Sleep Mode Description

The bq26100 device enters sleep mode when the SDQ enters a stop state or when SDQ encounters an invalid ID.

7.5 Programming

7.5.1 Communicating with the bq26100 Device

The bq26100 device communication protocol starts when the host pulls the bus low for reset time. All devices on the bus are to respond with a presence pulse, which is active low. The host can then transmit the ROM Function command, which is used to address the devices on the bus. The ROM functions include Match ID, Skip ID, Read ID, and Search ID.

Match ID	The host transmits the 64-bit ID of the 1-wire based device to communicate.
Skip ID	No ID is necessary for communication. Used only if one device is connected to the host.
Read ID	The 1-wire slave transmits its 64 bit address. This command is only useful if there is only one device connected to the host.
Search ID	Useful if there are multiple devices on the bus. This command initiates a communication with a single device, but it is more useful in allowing the host to determine the address of every device on the bus. The Match ID can then be used to communicate with a specific addressed device.

Programming (continued)

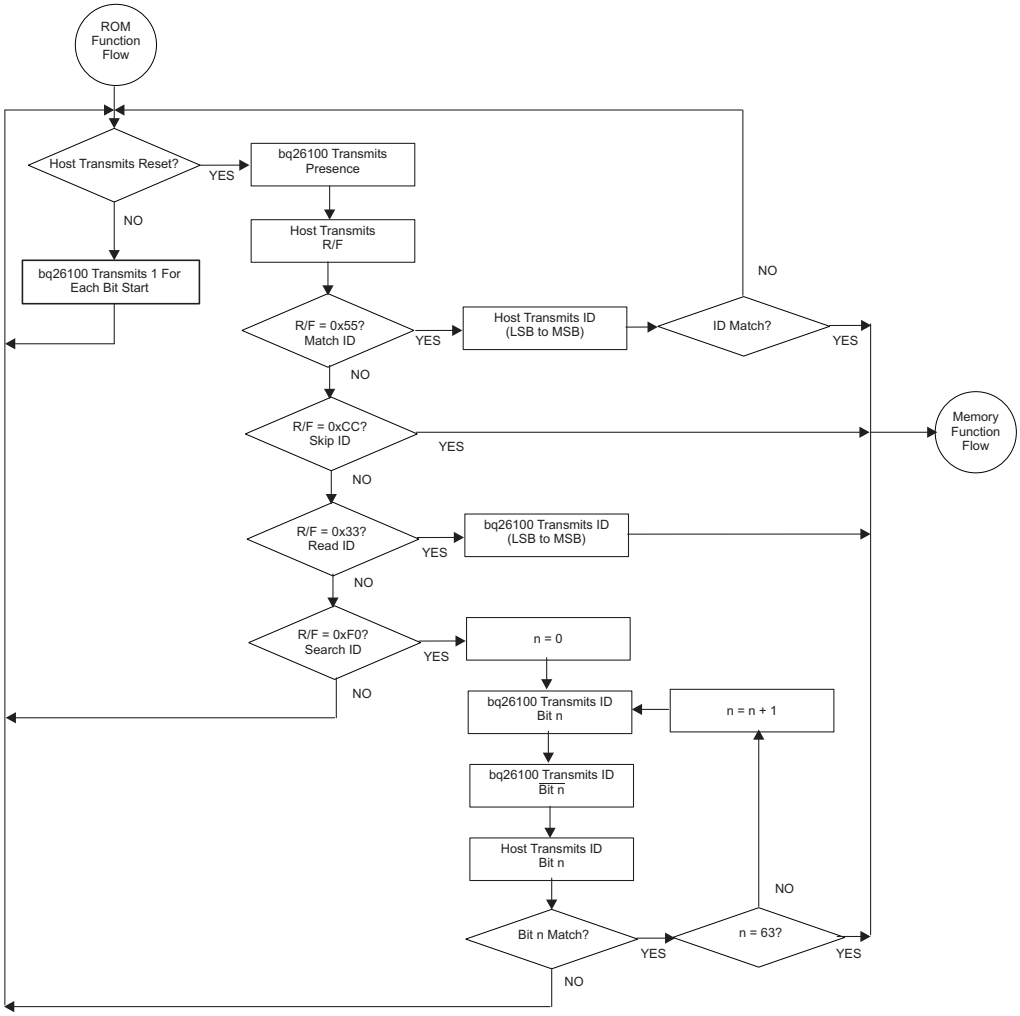


Figure 8. ROM Function Flow Chart

The 64-bit device ID is made up of an 8-bit family code, 48-bit random value, and a final 8-bit CRC (see Table 1).

Table 1. Format of 64-bit Device ID

ID MSB		ID LSB
CRC (8 bits)	Random Data (48 bits)	Family Code (8 bits, defaults to 0x09)

Contact Texas Instruments if specific data should be programmed into the ID.

After the ROM function command is issued and the bq26100 device is selected, a Memory Function command can be issued. The Memory Function commands are Read Memory, Read EEPROM, Read Status, Read Page, Read Page 4, Read Digest, Read Control, Write Memory, Write Page 4, Write EEPROM, Write Status, Write Message, Write Control, and Profile.

Figure 9 shows the flow for the Memory Function selection. Figure 12 through Figure 15 illustrate the flow for each memory function.

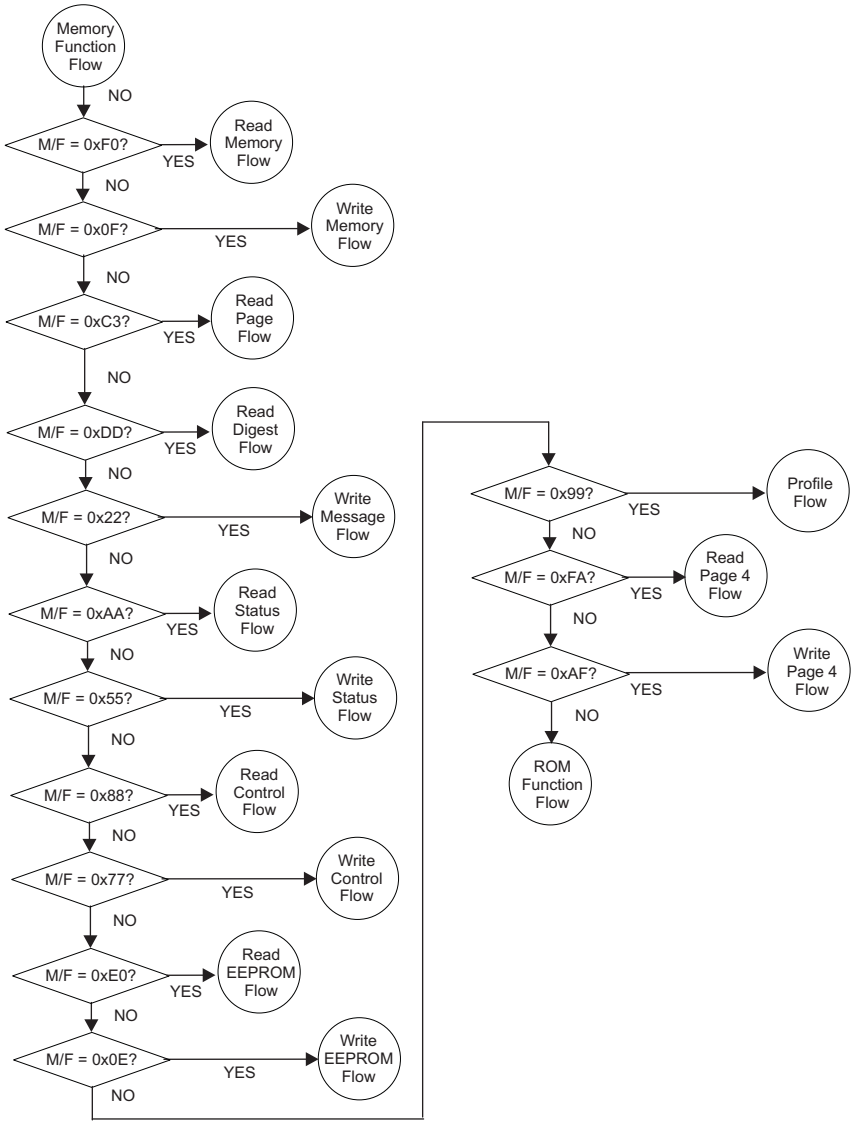


Figure 9. Memory Function Flow Chart

The SDQ protocol requires a CRC calculation as part of the communication flow. The CRC, based on a polynomial of $x^8+x^5+x^4+1$, is computed to determine data integrity and its use varies in the protocol. The Memory Function flows show what data are shifted through the CRC and when the value is transmitted from the slave. Each data byte used in the CRC calculation is pushed through the CRC shift register from LSB to MSB. The byte wide CRC computation is:

```
for (i = 0; i < 8; i++) {
   if (crc[0] ^ input[i])
     crc = (crc >> 1) ^ 0x8C;
   else
     crc = crc >> 1;
}
```

Where did the magic number 0x8C come from? CRC polynomials are defined such that the highest order simply shows the number of bits, so $x^8+x^5+x^4+1$ defines an 8-bit value with a binary value of 00110001 (bits 0, 4, and 5 are 1 and all others are 0). Since the SDQ CRC is computed by shifting in the LSB, the polynomial must be used in reverse bit order – binary 10001100 or hexadecimal 0x8C.

The CRC value is reset to 0 prior to the first byte being shifted through. The CRC is also reset when the CRC is shifted out as part of the SDQ protocol.

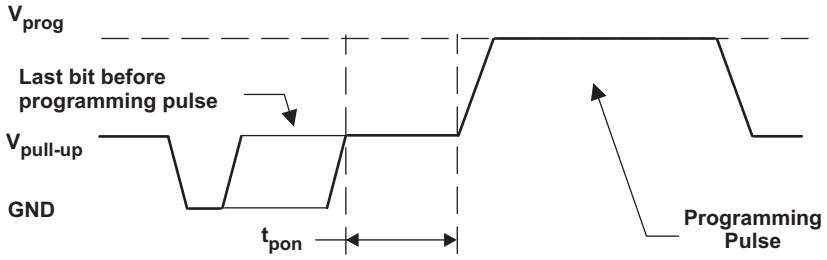


Figure 10. bq26100 Device Communication to OTP Programming Pulse Diagram

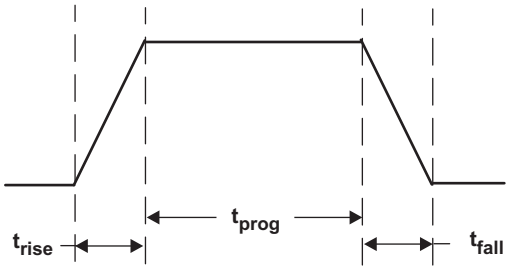


Figure 11. OTP Programming Pulse Detail

7.5.2 Memory Descriptions

The bq26100 device has a memory and command structure that is compatible with the bq2022, however additional memory and commands have been added. The bq26100 device uses a combination of non-volatile One-Time-Programmable (OTP), non-volatile EEPROM, and volatile registers. The memory is split into the following sections:

7.5.2.1 Non-Volatile OTP Memory

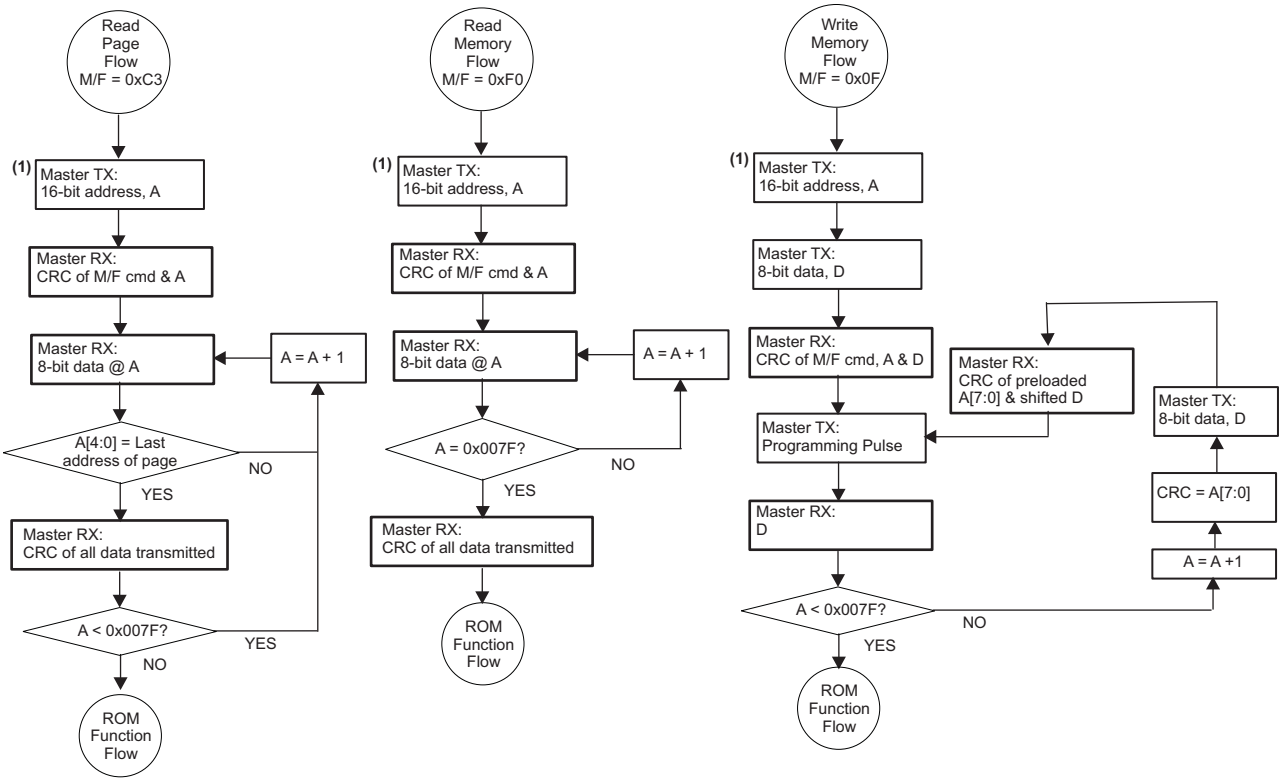
The One Time Programmable (OTP) memory is intended for factory programming. Programming the OTP requires putting a 7-V pulse on the communication pin after writing the data to the intended address.

7.5.2.1.1 General Use – Memory Function Commands 0xF0 (Read) and 0x0F (Write)

The general use space is erased to read 0x00. Data written to the general space is ORed with data already present at the address to be written. A bit can only be flipped from **0** to **1**.

Table 2. General Memory Space Addressing

ADDRESSES	FUNCTION
0x007F – 0x0060	Page 3 – 32 bytes general use
0x005F – 0x0040	Page 2 – 32 bytes general use
0x003F – 0x0020	Page 1 – 32 bytes general use
0x001F – 0x0000	Page 0 – 32 bytes general use



(1) 16-Bit address is sent with lower 8-bit address followed by higher 8-bit address with least significant bit first.

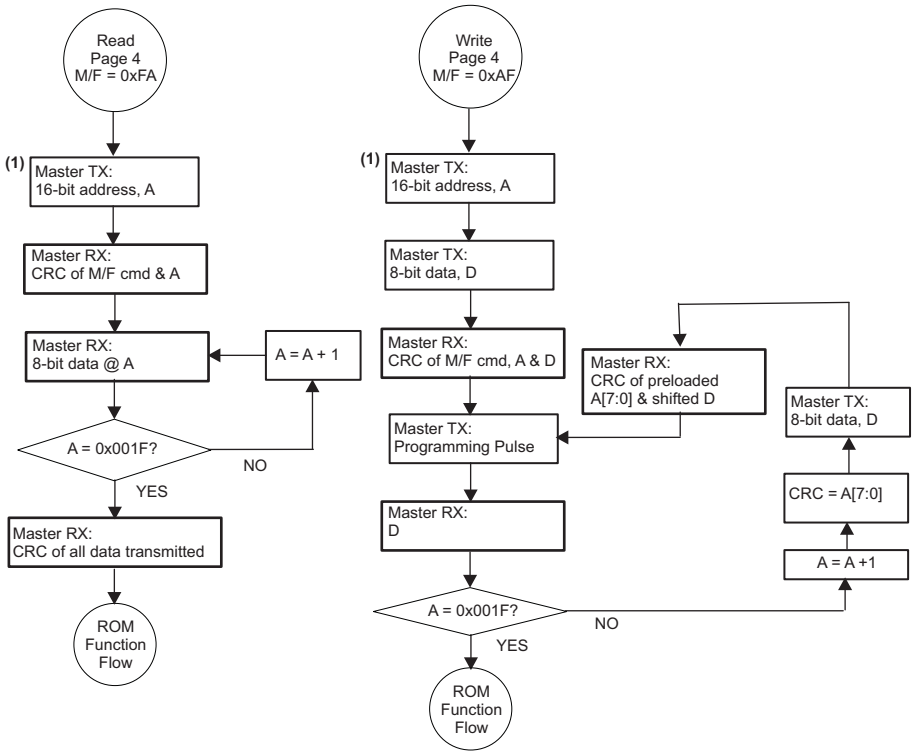
Figure 12. General Memory OTP Write/Read Flows

7.5.2.1.2 General Use — Memory Function Commands 0xFA (Read) and 0xAF (Write)

The general use space is erased to read 0x00. Data written to the general space is ORed with data already present at the address to be written. A bit can only be flipped from **0** to **1**.

Table 3. General Memory Space Addressing

ADDRESSES	FUNCTION
0x001F – 0x0000	Page 4 – 32 bytes general use



(1) 16-Bit address is sent with lower 8-bit address followed by higher 8-bit address with least significant bit first.

Figure 13. General Memory OTP Write/Read Flows

7.5.2.1.3 Status – Memory Function Commands 0xAA (Read) and 0x55 (Write)

Unlike the general use pages, the status bytes read 0xFF when not programmed and a bit is programmed from **1** to **0**. A zero represents the active state.

Address 0x0007 Reserved

Default value is 0xFF

Address 0x0006 Key Index

The host can determine which one of multiple keys was programmed into the bq26100 device by reading the key index value.

Address 0x0005 – 0x0001 Page Redirection

A pointer for alternative page information, these bytes can be used if information in the original page has been invalidated. The host can read these locations and direct reads and/or writes to the page pointed to by the value in the register. For example, if the data in page 2 is corrupted by an incorrectly written data value, and the corrected data is in page 1, the value written to address 0x0003 would be 0xFE (1's complement value of 0x01). Upon reading address 0x0003, the host would receive 0xFE and would take the 1's complement to determine that page 1 contains redirected data.

Table 4. Page Redirection

ADDRESS	PAGE REDIRECTED
0x0005	Page 4
0x0004	Page 3
0x0003	Page 2
0x0002	Page 1
0x0001	Page 0

There is no hardware mapping of the page redirection bytes. The host is responsible for sending the correct address for a redirected page.

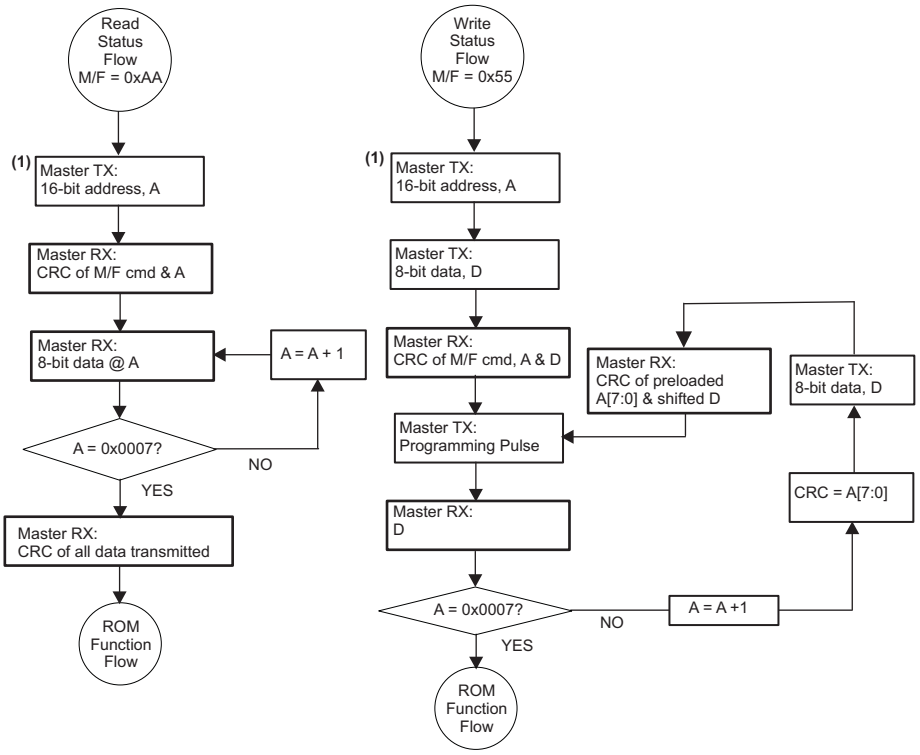
7.5.2.1.3.1 PAGE LOCK (offset = D431h) [reset = 0h]

Figure 14. PAGE LOCK

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	5h	4h	3h	2h	0h

Table 5. PAGE LOCK Field Descriptions

Bit	Field	Type	Reset	Description
7	LOCKK1	R/W	0h	Programming this bit to **0** locks the upper 64 bits of the device key, preventing additional writes. This bit can only be written once.
6	LOCKK0	R/W	0h	Programming this bit to **0** locks the lower 64 bits of the device key, preventing additional writes. This bit can only be written once.
5	RSVD	R/W	0h	Reserved
4	PAGE4	R/W	5h	Programming this bit to **0** locks page designated by x, preventing additional writes. This bit can only be programmed once.
3	PAGE3	R/W	4h	
2	PAGE2	R/W	3h	
1	PAGE1	R/W	2h	
0	PAGE0	R/W	1h	



(1) 16-Bit address is sent with lower 8-bit address followed by higher 8-bit address with least significant bit first.

Figure 15. Status OTP Write/Read Flows

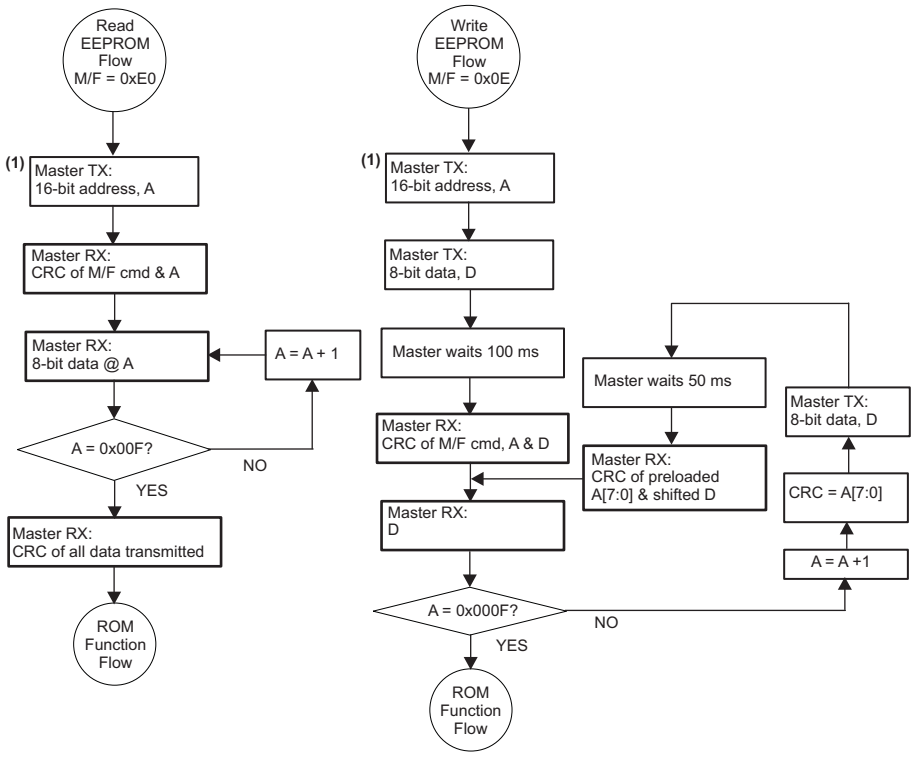
7.5.2.2 Non-Volatile EEPROM Memory

The EEPROM memory is intended for in-field programming. Programming the EEPROM is no different than writing to RAM or registers, but the timing between the write and read back is different. A bit can be written to **1** or cleared to **0** multiple times and the value is retained when power to the device is removed.

7.5.2.2.1 General Use – Memory Function Commands 0xE0 (Read) and 0x0E (Write)

Table 6. General Memory Space Addressing

ADDRESSES	FUNCTION
0x000F – 0x0000	16 Bytes general use



(1) 16-Bit address is sent with lower 8-bit address followed by higher 8-bit address with least significant bit first.

Figure 16. EEPROM Write/Read Flows

7.5.3 SHA-1 Description

The SHA-1 is known as a one-way hash function, meaning there is no known mathematical method of computing the input given only the output. The specification of the SHA-1, as defined by FIPS 180-2, states that the input consists of 512 bit blocks with a total input length less than 2^{64} bits. Inputs which do not conform to integer multiples of 512 bit blocks are padded before any block is input to the hash function. The SHA-1 algorithm outputs 160 bits, commonly referred to as the digest.

The full SHA-1 specification and algorithm can be found at http://csrc.nist.gov/publications/fips under FIPS 180. (As of April 23, 2004, the latest revision is FIPS 180-2.)

The bq26100 device generates an SHA-1 input block of 288 bits (total input = 160 bit message + 128 bit key). To complete the 512 bit block size requirement of the SHA-1, the bq26100 device pads the key and message with a 1, followed by 159 0's, followed by the 64 bit value for 288 (000…00100100000), which conforms to the pad requirements specified by FIPS 180-2 9 (Figure 17).

Figure 17. SHA-1 Message Padding Format Example

7.5.4 Key Programming Description

The 128-bit key used in the HMAC calculation is built from two 64-bit key spaces on the bq26100 device. Each key can be programmed independently, allowing multiple parties to program part of the full 128-bit key without the knowledge necessary to reproduce the full 128-bit key. To further protect the 128-bit key, the value written to each 64-bit non-volatile key space is the output of a SHA-1 calculation on a 160-bit input. Figure 18 provides a flow for the programming of the 128-bit device key. Once KEYx has been programmed, the LOCKKx bit should be programmed to 0 in the status register, preventing another value from overwriting that key space.

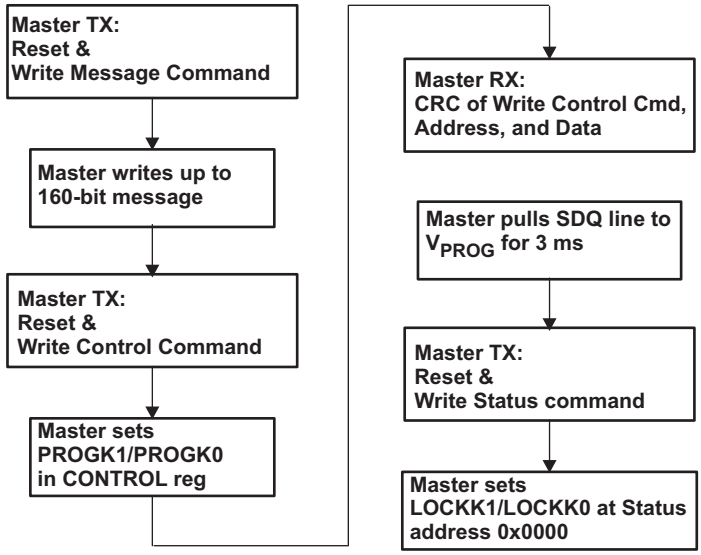


Figure 18. Key Programming Flow

This flow is run twice, for KEY0 and KEY1. An external power source is required on the PWR pin during key programming. Figure 20 shows a typical connection for the external power source.

Since there is no key pre-appended to the message, the key message is padded with a 1, followed by 287 0's, followed by the 64-bit value for 160 (00..01010000), see Figure 19.

Figure 19. Key Programming Message Format Example

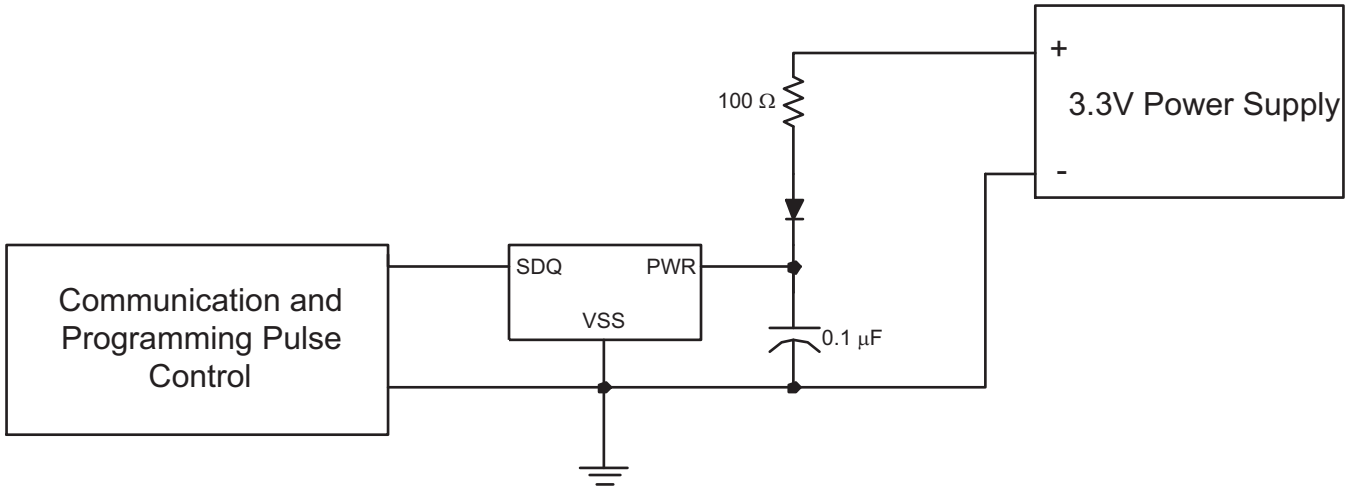


Figure 20. External Power Source Connection

7.6 Register Maps

7.6.1 Volatile Register Memory

The register memory is intended for in-field programming.

7.6.1.1 Message and Digest Registers – Memory Function Command 0xDD (Read) and 0x22 (Write)

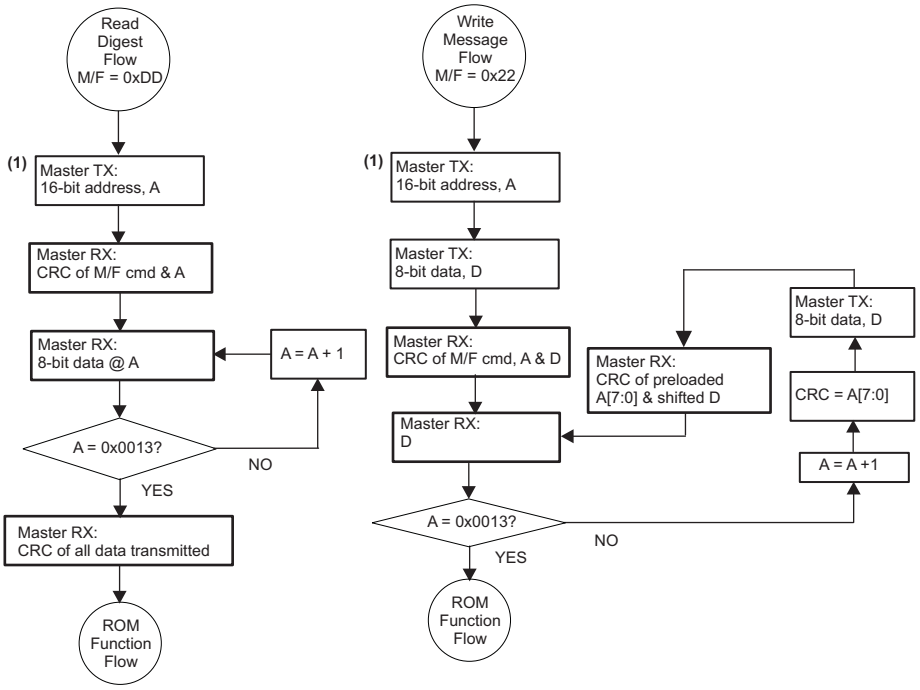
The message is a 160-bit input to the HMAC calculation, and the digest is the 160-bit output of the HMAC calculation. The message and digest share the same memory space, meaning that the message cannot be read back once the digest has been computed. The MSB of the message should be written to address 0x0013, and the LSB written to address 0x0000. The digest overwrites the message in the following manner.

Table 7. Message/Digest Space Addressing

ADDRESS	MESSAGE VALUE	DIGEST VALUE
0x0013 – 0x0010	M[159:128]	A[31:0]
0x000F – 0x000C	M[127:96]	B[31:0]
0x000B – 0x0008	M[95:64]	C[31:0]
0x0007 – 0x0004	M[63:32]	D[31:0]
0x0003 – 0x0000	M[31:0]	E[31:0]

NOTE

See the SHA-1 and HMAC descriptions for more information on the meaning of the variables in the above table.



(1) 16-Bit address is sent with lower 8-bit address followed by higher 8-bit address with least significant bit first.

Figure 21. Message/Digest Write/Read Flows

7.6.1.2 Control and Version Registers – Memory Function Command 0x88 (Read) and 0x77 (Write)

The control register starts authentication, clears the message/digest values, and flags when the authentication process has completed. The version register is used to determine the silicon revision.

Table 8. General Memory Space Addressing

ADDRESSES	FUNCTION
0x0001	Silicon Revision Number
0x0000	Control Register

The bits of the Control register are as follows:

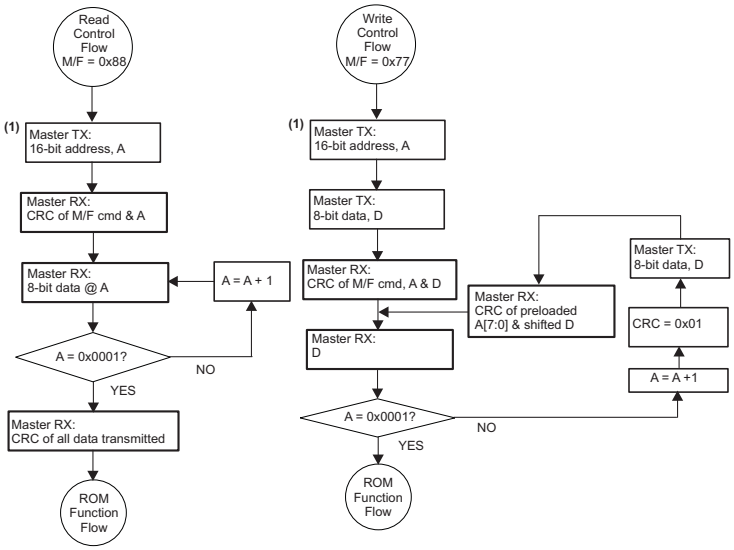
7.6.1.2.1 CTRL Register (address = 0001h) [reset = 1h]

Figure 22. Control Register

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	0h

Table 9. Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PROGK1	R/W	0h	If LOCKK1 is 1 (see Status Register), writing this bit to 1 enables the programming of Device Key 1. Further information about the programming of the keys is found in the SHA-1 section.
6	PROGK0	R/W	0h	If the LOCKK0 bit is 1 (see Status Register), writing this bit to 1 enables the programming of Device Key 0. Further information about the programming of the keys is found in the SHA-1 section.
5	RSVD	R/W	0h	These bits are reserved for future use. They should always be written to 0.
4	CLEAR	R/W	0h	Writing this bit to **1** clears the message/digest registers. This can be done before the message is written to ensure that all data values are known or after the digest is read to clear the HMAC calculation output. The bq26100 device resets the bit back to 0.
3	RSVD	R/W	0h	Reserved
2	POR	R/W	1h	This bit is set when the device comes out of a POR condition. The bit can be written to 0 to clear the flag. Writing the bit to 1 has no effect on device operation.
1	DONE	R/W	0h	This bit is set when the device completes the HMAC calculation. The host should poll for this bit to determine when the digest is available for reading. This bit is automatically cleared when the AUTH bit is written to 1. This bit is also cleared at POR.
0	AUTH	R/W	0h	This bit is set to initiate the HMAC calculation. This bit is automatically cleared when the DONE bit is written to 1.



(1) 16-Bit address is sent with lower 8-bit address followed by higher 8-bit address with least significant bit first.

Figure 23. Control Register Write/Read Flows

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A typical application consists of a host microcontroller as the SDQ master and the bq26100 device as the SDQ slave. The SDQ I/O on the bq26100 device is an open-drain pin and the SDQ master should also be configured as open-drain to allow a pullup resistor to be connected to a voltage that is between 2.5 V and 5.0 V.

8.2 Typical Application

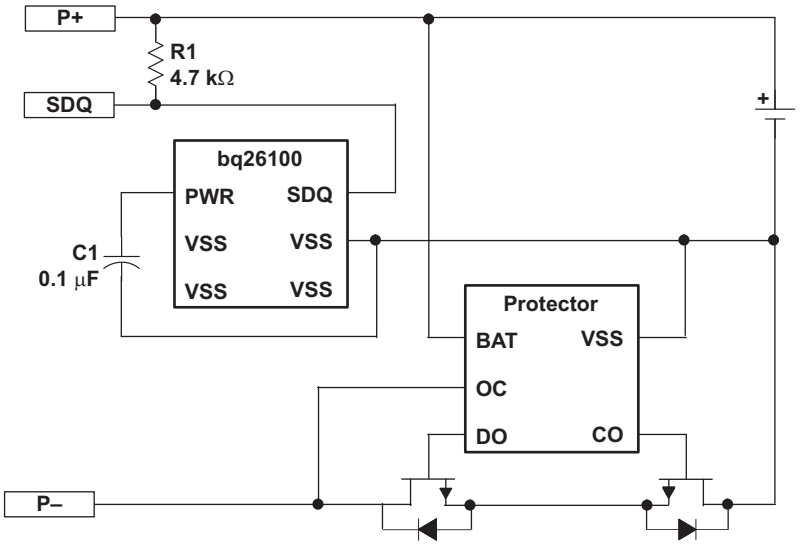


Figure 24. Sample Application

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 10.

Table 10. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Pullup Voltage	2.65 V to 5.0 V
Pullup Resistor	4.7 kΩ

8.2.2 Detailed Design Procedure

The bq26100 device requires a 12-V maximum-pulse signal to program the OTP memory. It is necessary to have a programming test setup for production. shows an example of what the circuit could be for such a setup. The Programming Module contains the microcontroller that acts as SDQ master and also controls the time of the programming pulse and its width. The 12-V supply is the source for the programming pulse. Only SDQ and VSS signals need to exit the test setup as the Application Circuit containing the bq26100 device under test is connected only for programming and verifying data.

The Programming Module typically will connect to a PC using an interface such as USB. The diagram in does not include the interface to a PC, which can vary depending on the system designer's choice.

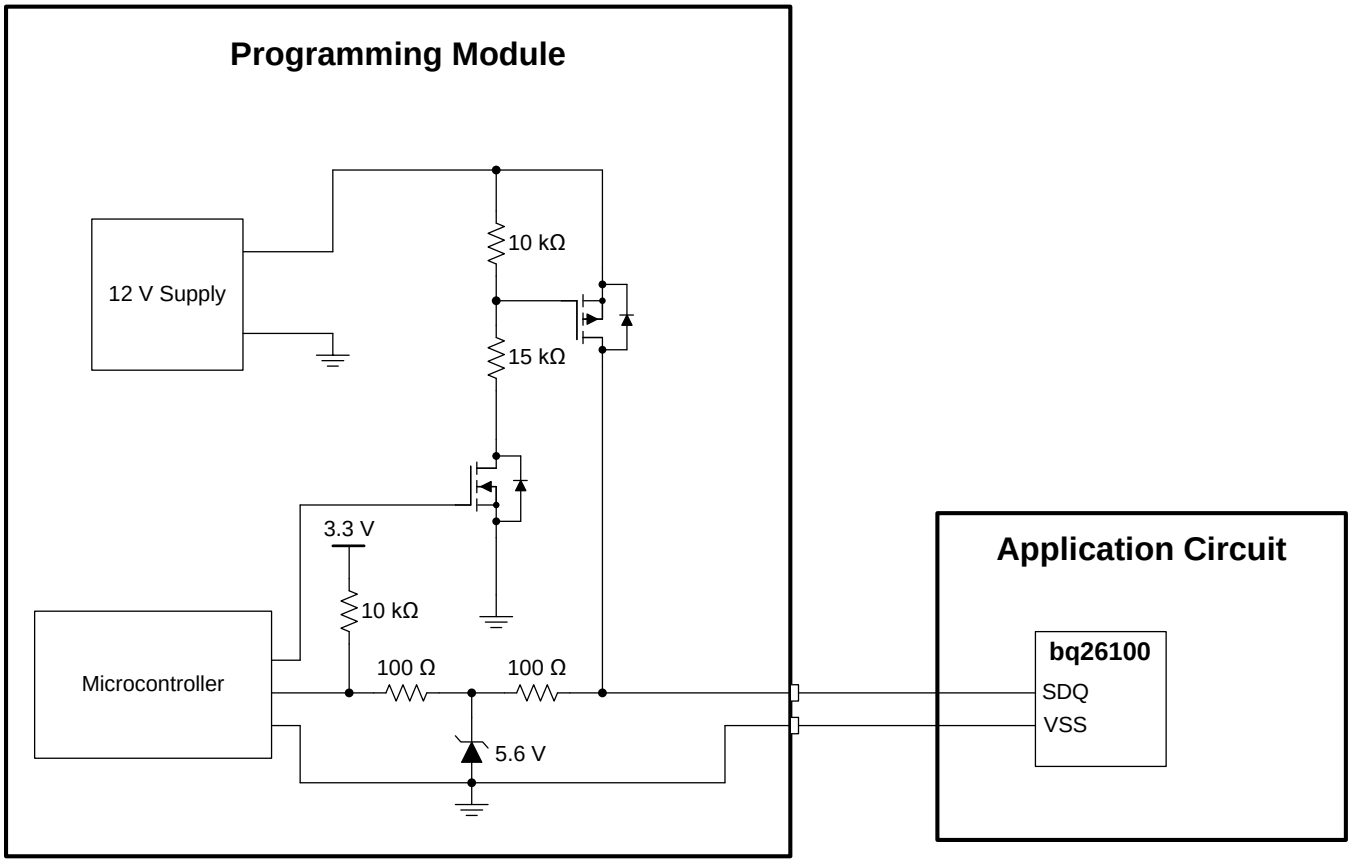


Figure 25. Programming Circuit Example

9 Power Supply Recommendations

The bq26100 device is a low-power device that only needs to be turned on when communicating. The device power comes from the digital I/O and the capacitor connected between the VCC and GND pins. The capacitor on VCC is charged when the SDQ I/O is high and parasitically discharged when the SDQ I/O is pulled low.

10 Layout

10.1 Layout Guidelines

The bq26100 device requires a single-signal trace for the SDQ line and the parasitic capacitor on the PWR input. The best practice is to place the PWR capacitor as close as possible to the device with no via between the capacitor and the PWR pin. There should be two vias connecting the ground plane to VSS pins at the capacitor and additional vias connecting the ground plane to the remainder of ground connection for the thermal pad.

10.2 Layout Example

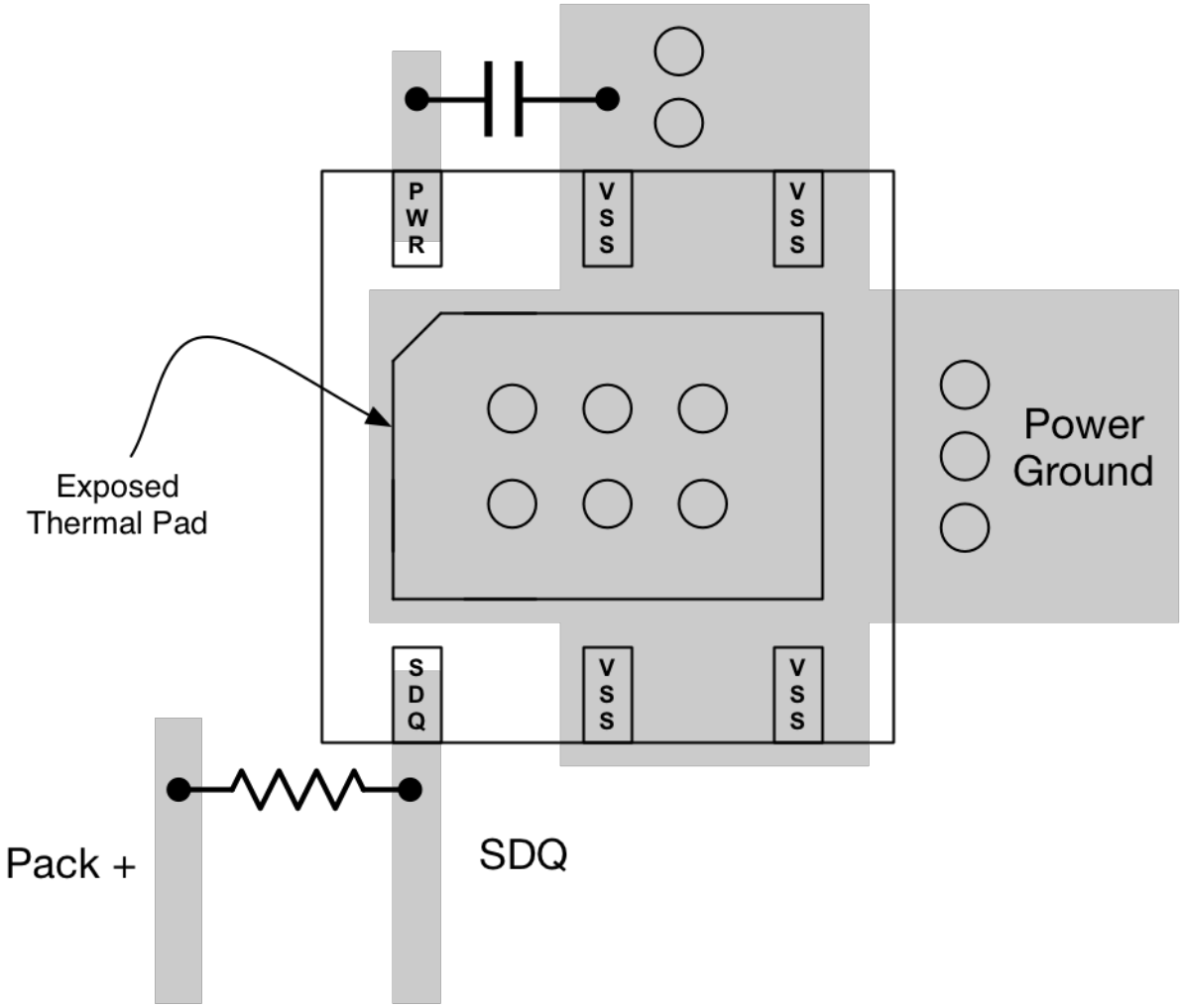


Figure 26. Board Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ26100DRPR	ACTIVE	VSON	DRP	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2610	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

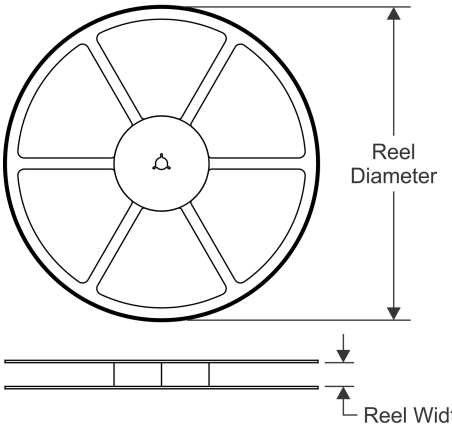
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

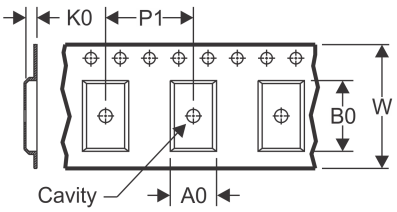
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

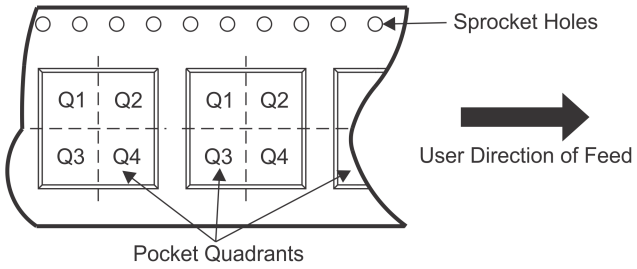


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

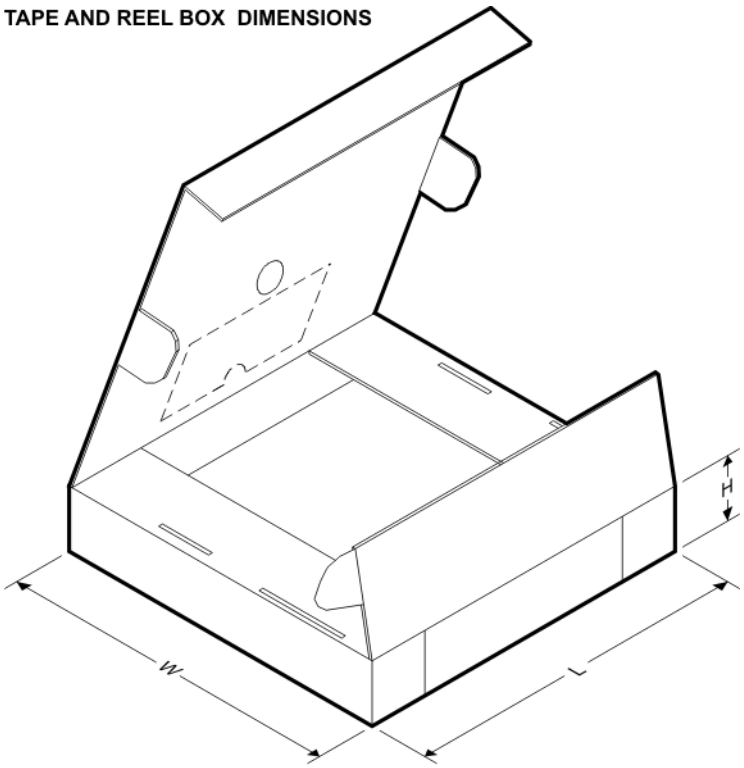
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ26100DRPR	VSON	DRP	6	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

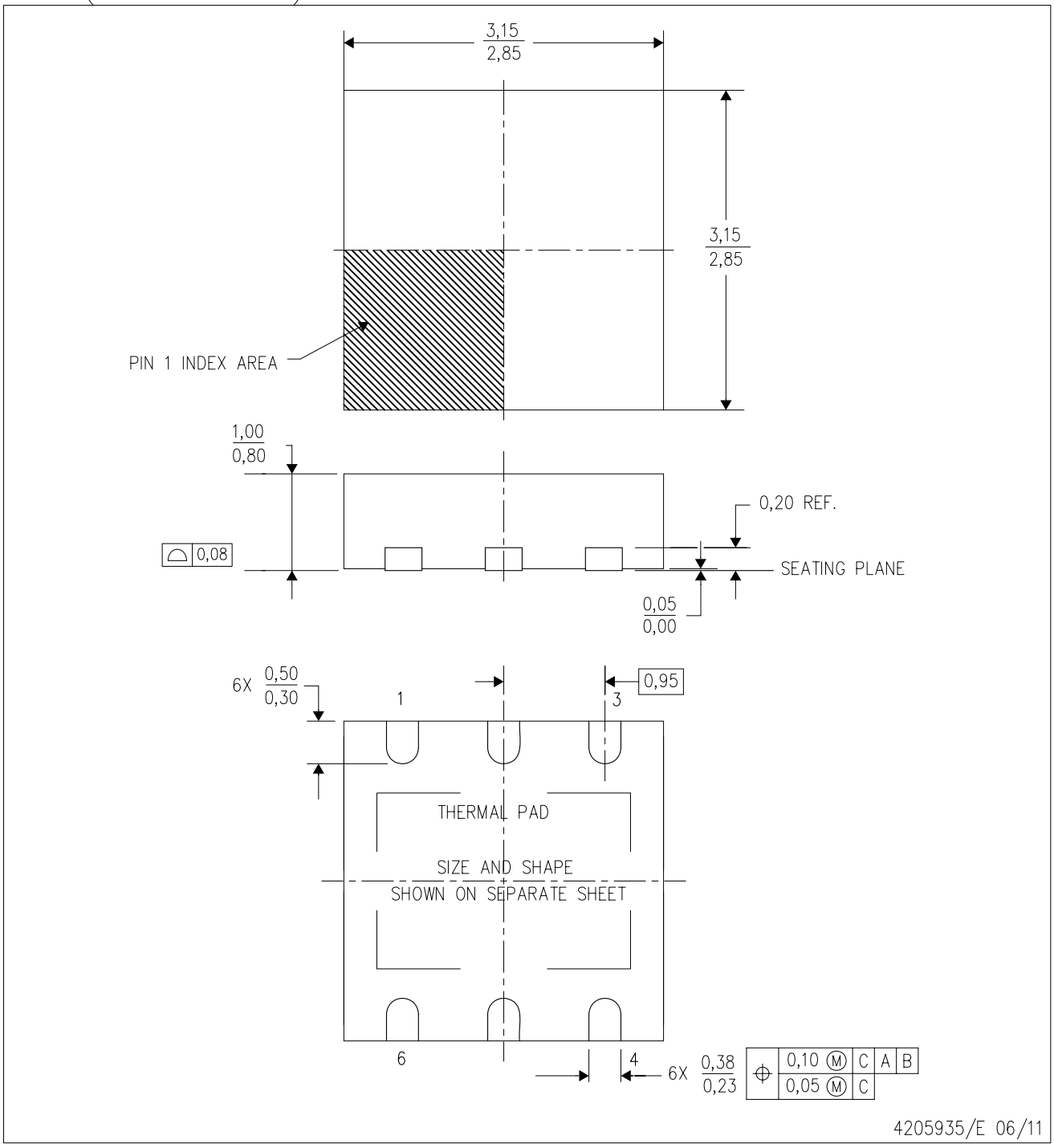
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ26100DRPR	VSON	DRP	6	3000	367.0	367.0	35.0

DRP (S–PVSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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