THE DATASHEET OF

4532-201-LF

Data Sheet

APDS-9999

Digital Proximity and RGB Sensor

Overview

The Broadcom® APDS-9999 is an integrated RGB, proximity detector and VCSEL in an optical module.

The APDS-9999 device uses four individual channels of red, green, blue, and IR in a specially designed matrix arrangement. This allows the device to have optimal angular response and accurate RGB spectral response with high Lux accuracy over various light sources. The device detects light intensity under a variety of lighting conditions and through a variety of attenuation materials, including dark glass. The APDS-9999 could be configured as ambient light sensor (ALS) and RGB sensor.

In smartphones, the proximity sensor senses when the user positions the phone close to the ear so that the touchscreen can be disabled. The device is fast enough to provide proximity information at a high repetition rate needed when answering a phone call.

The APDS-9999 has a wide dynamic range. The current is programmable in two steps. The number of VCSEL pulses can be configured using pulse step, and VCSEL modulation frequency can be set from 60 kHz to 100 kHz in five steps. PS resolution can be varied from 8 bits to 11 bits, and the measurement rate is from 6.25 ms to 400 ms. To offset unwanted reflected light from the cover glass, a PS intelligent cancellation level register allows for an on-chip subtraction of the ADC count contributed by any unwanted reflected light from cover glass.

Both the PS and ALS function independently allowing for maximum flexibility in application.

Features

- RGB and ambient light sensing (RGB and ALS)
  – Accuracy of correlated color temperature (CCT)
  – Individual channels for red, green, blue, and infrared
  – Approximates human eye response with green channel
  – Uses optical coating technology to emulate human eye spectral response
  – Works well under different light source conditions
  – Low-light sensitivity; operates behind darkened glass
  – 50 Hz/60 Hz light flicker immunity
  – Fluorescent light flicker immunity
  – Programmable interrupt function with upper, lower thresholds and persists function
  – Programmable ALS integration time
  – Programmable ALS gain setting
- Proximity detection (PS)
  – 940-nm vertical cavity surface emitting laser (VCSEL)
  – Programmable VCSEL drive current
  – Cancellation of crosstalk
  – Ambient light suppression
  – Programmable interrupt function with upper and lower thresholds and persists function
  – Programmable persists function
- IEC 60825-1 Class 1 Laser Eye Safety
- Supply voltage 1.7V to 3.6V
- Power management
  – Low active current
  – Low standby current
- I^2C interface compatible
  – Up to 400 kHz (I^2C fast-mode)
  – Dedicated interrupt pin
- Small package
  – L 2.80 mm × W 1.60 mm × H 0.70 mm

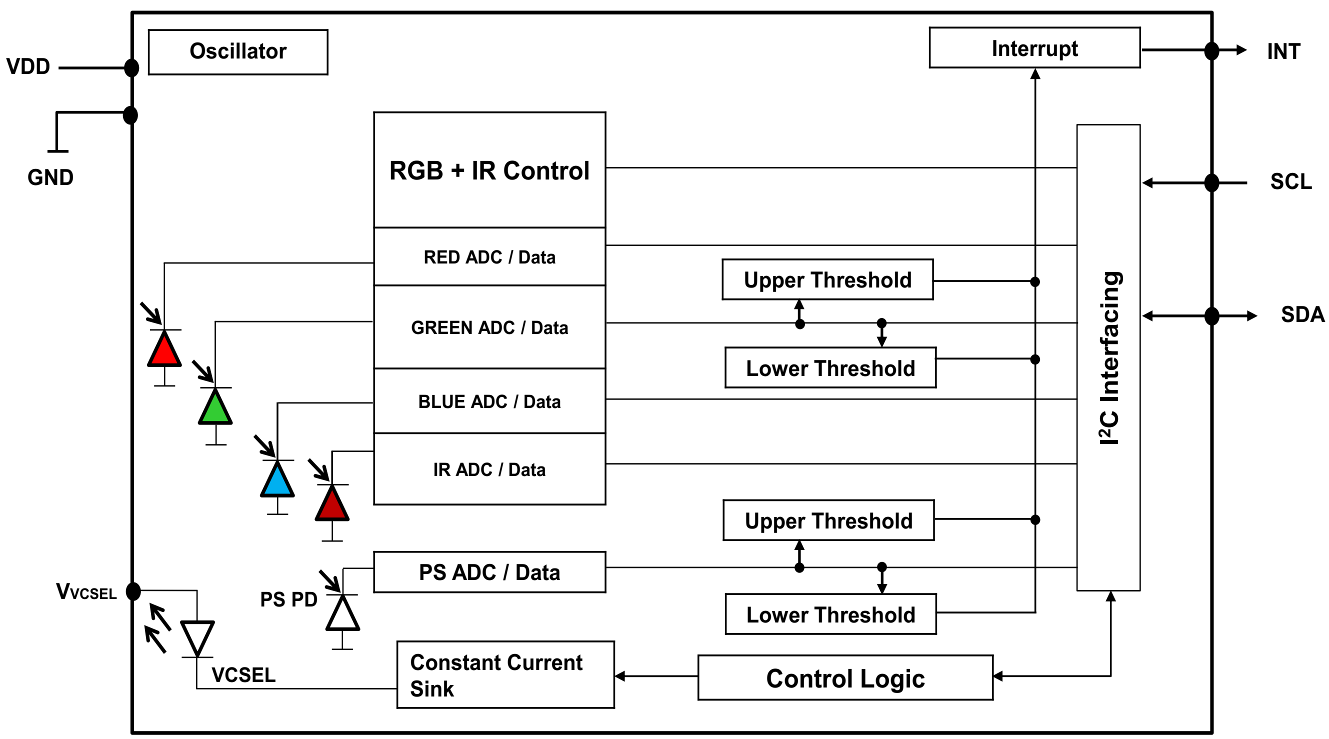
Applications

- Cell phone touch-screen disable
- Notebook/monitor security
- Automatic Speakerphone Enable
- Cell phone backlight dimming

Ordering Information

Part Number	Packaging	Quantity
APDS-9999	Tape and Reel	10,000

Functional Block Diagram



I/O Pins Configuration

Pin	Name	Type	Description
1	GND	Ground	Power supply ground. All voltages are referenced to GND.
2	INT	O	Interrupt. Open drain.
3	V_{VCSEL}	Supply	VCSEL supply voltage.
4	V_{DD}	Supply	Power supply voltage.
5	SDA	I/O	Serial data I/O for I^2C.
6	SCL	I	I^2C serial clock input terminal. Clock signal for I^2C serial data.

Absolute Maximum Ratings

Over operating free-air temperature range (see note).

Parameter	Symbol	Min.	Max.	Units	Conditions
Power Supply Voltage[a]	V_{DD}	—	3.63	V	
Digital Voltage Range		–0.5	3.63	V	
Storage Temperature Range	Tstg	–40	100	°C	

a. All voltages are with respect to GND.

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Ambient Temperature	T_A	–40	—	85	°C
Supply Voltage	V_{DD}	1.7	—	3.6	V
Supply Voltage Accuracy, V_{DD} Total Error Including Transients		–1	—	1	%
VCSEL Supply Voltage	V_{VCSEL}	3.0	—	4.6	V

Operating Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
SCL, SDA Input High Voltage	V_{IH}	1.5	—	V_{DD}	V	
SCL, SDA Input Low Voltage	V_{IL}	0	—	0.4	V	
INT, SDA Output Low Voltage	V_{OL}	0	—	0.4	V	
Leakage Current, SDA, SCL, INT Pins	I_{LEAK}	–5	—	5	μA	

RGB Optical Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Test Condition	Red Channel		Green Channel		Blue Channel		IR Channel		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Irradiance Response	λ = 465	0	8	6	22	85	115	0	4	%
	λ = 525	2	14	85	115	10	30	0	3	
	λ = 625	85	115	18	37	0	3	0	3	
	λ = 850	0	3	0	3	0	3	85	115	

NOTE:

- The percentage shown represents the ratio of the respective red, green, or blue channel value to the IR channel value.
- The 465-nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 22 nm.
- The 525-nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 35 nm.
- The 625-nm input irradiance is supplied by an AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 625 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 15 nm.
- The 850-nm input irradiance is supplied by an AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 850 nm, spectral halfwidth $\Delta\lambda_{1/2}$ = 40 nm.

RGB/ALS Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Current	I_{DD}	—	118	154	µA	Active mode
		—	1	2	µA	Standby mode
Peak Wavelength	$\lambda_{P\_ALS/Green}$	—	550	—	nm	
	λ_{P_Red}	—	610	—	nm	
	λ_{P_Blue}	—	470	—	nm	
Minimum Integration Time	$T_{intmin1}$	—	3.125	—	ms	
	$T_{intmin2}$	—	50	—	ms	With 50 Hz/60 Hz rejection
Maximum Integration Time	$T_{intmax1}$	—	400	—	ms	With 50 Hz/60 Hz rejection
Output Resolution	RES_{ALS}	13	18	20	bit	Programmable
ADC Count Value (ALS/Green)		12500	—	—	counts	White LED 5600 K, 200 lux, 200 ms, Gain = 18x
ADC Count Value (ALS/Green)		1190	1400	1610	counts	λ = 525 nm, 50 ms, Gain = 3x, Ee = 72 µW/cm^2
ADC Count Value (Red)		1275	1500	1725	counts	λ = 625 nm, 50 ms, Gain = 3x, Ee = 78 µW/cm^2
ADC Count Value (Blue)		1190	1400	1610	counts	λ= 465 nm, 50 ms, Gain = 3x, Ee = 73 µW/cm^2
Dark Count Value (ALS/Green)		0	—	3	counts	Gain = 18×, 50 ms, Ee = 0
Dark Count Value (Red)		0	—	3	counts	Gain = 18×, 50 ms, Ee = 0
Dark Count Value (Blue)		0	—	3	counts	Gain = 18×, 50 ms, Ee = 0

VCSEL IR Emitter Characteristics

T_A = 25°C (unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Wavelength	λ_P	—	940	—	nm	
Spectrum Width, Half Power	$\Delta\lambda$	—	10	—	nm	

PS Characteristics

V_{DD} = 2.8V, T_A = 25°C (unless otherwise noted).

Parameter	Min.	Typ.	Max.	Units	Test Conditions
Supply Current (without VCSEL current)	—	99	—	µA	V_{DD} = 2.8V, 100-ms repeat time, 32 pulse, 60 kHz
Supply Current (PS + VCSEL only)	—	126	—	µA	V_{DD} = 2.8V, 100-ms repeat time, 10 mA, 32 pulse, 60 kHz, V_{VCSEL} = 3V
ADC Count Value	—	—	2047	counts	11 bit
PS Resolution	8	—	11	bit	
PS ADC Count Value (no object)	—	—	60	counts	Dedicated duo power supply, VDD = 2.8V and V_{VCSEL} = 3V, VCSEL driving 32 pulses, 10 mA, 11-bits. (0.7 mm thickness clear glass, 0.3-mm air gap and no reflective object above the module)
PS Signal Delta ADC Count Value (30-mm Distance Object)	76	90	104	counts	Dedicated duo power supply, VDD = 2.8V and V_{VCSEL} = 3V, Reflecting object = 73 mm × 83 mm Kodak 18% grey card, 30-mm distance, 11-bits, VCSEL driving 32 pulses, 10 mA. (0.7-mm thickness clear glass, 0.3-mm air gap)

Figure 1: Spectral Response

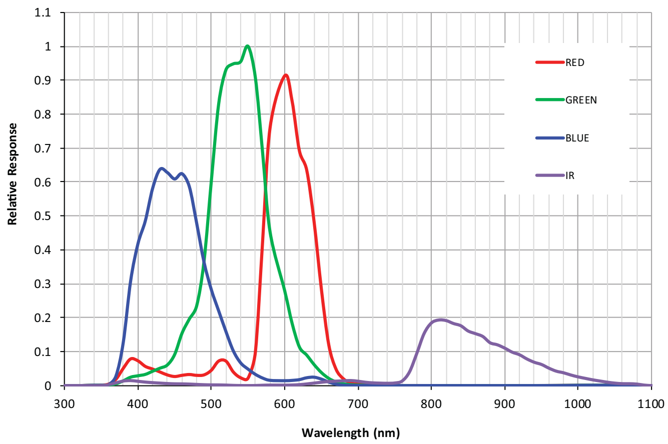


Figure 2: ALS Sensor LUX vs. Meter LUX Using White Light

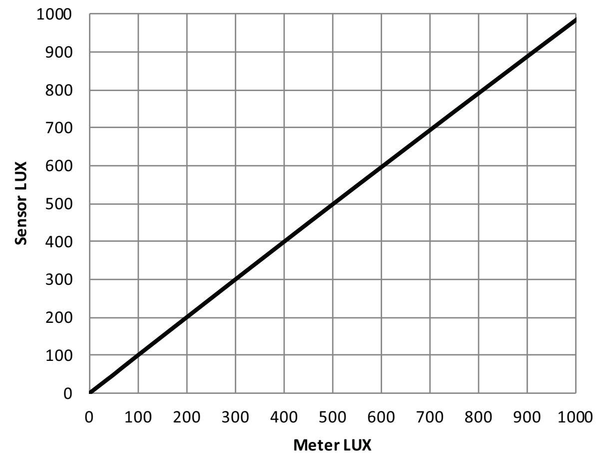


Figure 3: ALS Sensor LUX vs. Meter LUX Using Low LUX White Light

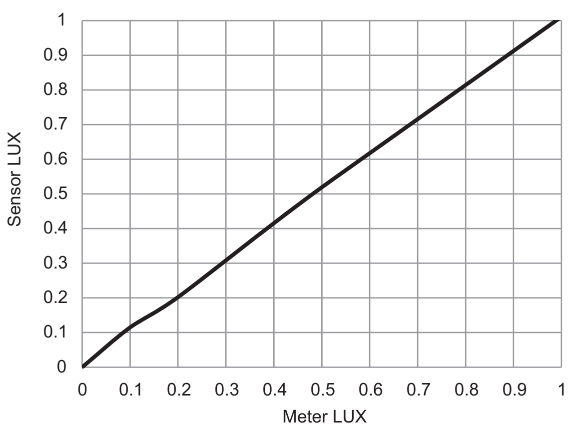


Figure 4: ALS Sensor LUX vs. Meter LUX Using Incandescent Light

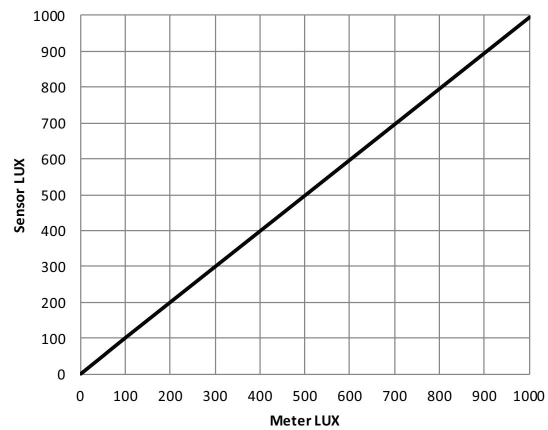


Figure 5: Normalized I_{DD} vs. V_{DD}

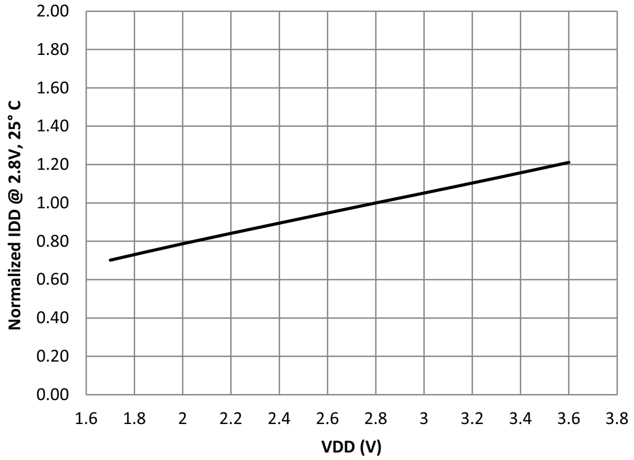


Figure 6: Normalized I_{DD} vs. Temperature

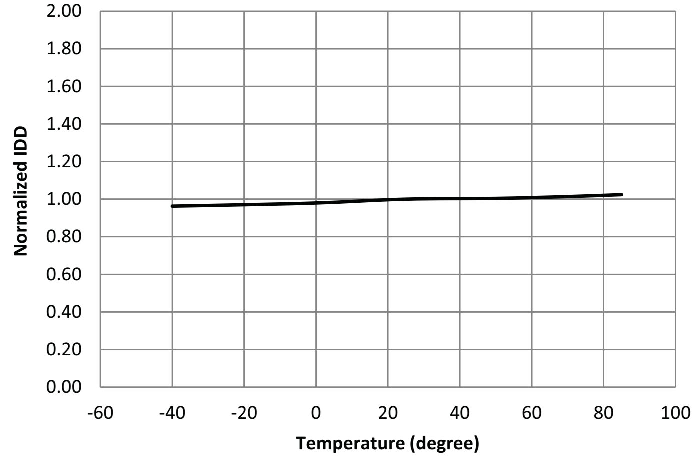


Figure 7: Normalized ALS PD Responsitivity vs. Angular Displacement (Perpendicular Axis)

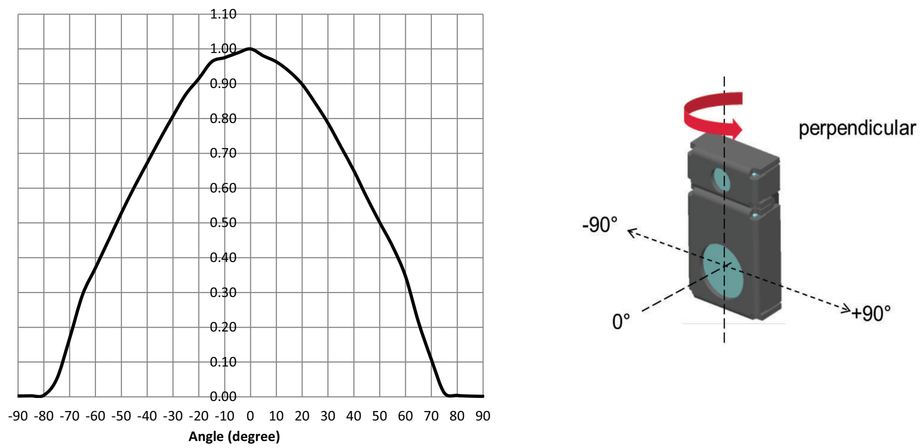
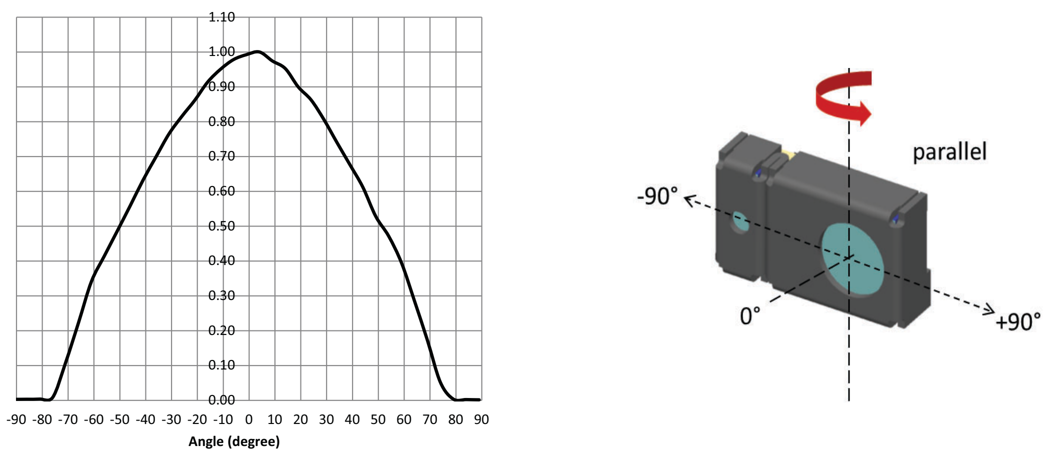


Figure 8: Normalized ALS PD Responsitivity vs. Angular Displacement (Parallel Axis)



ALS Gain and Resolution Characteristics

Gain	Resolution (bits)	Integration Time, itime (ms)	Min. Lux	Max. Lux	Resolution (lux/count)
1x	16	25	2.193	143719	2.193
	17	50	1.099	144035	1.099
	18	**100 (default)**	**0.548**	**143562**	**0.548**
	19	200	0.273	143131	0.273
	20	400	0.136	143092	0.136
3x (default)	16	25	0.722	47318	0.722
	17	50	0.359	47114	0.359
	18	**100 (default)**	**0.180**	**47182**	**0.180**
	19	200	0.090	47212	0.090
	20	400	0.045	47023	0.045
6x	16	25	0.360	23608	0.360
	17	50	0.179	23494	0.179
	18	**100 (default)**	**0.090**	**23544**	**0.090**
	19	200	0.045	23531	0.045
	20	400	0.022	23501	0.022
9x	16	25	0.239	15652	0.239
	17	50	0.119	15619	0.119
	18	**100 (default)**	**0.059**	**15564**	**0.059**
	19	200	0.030	15612	0.030
	20	400	0.015	15630	0.015
18x	16	25	0.117	7655	0.117
	17	50	0.059	7685	0.059
	18	**100 (default)**	**0.029**	**7680**	**0.029**
	19	200	0.015	7688	0.015
	20	400	0.007	7688	0.007

Principles of Operation

System State Machine

Start Up after Power-On or Software Reset

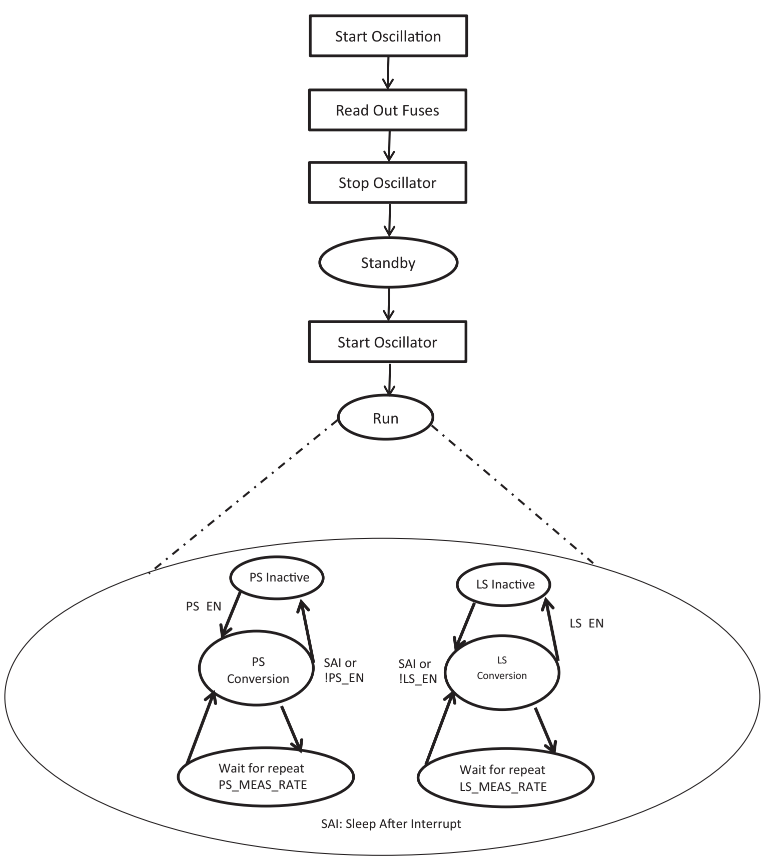
The main state machine is set to Start State during power-on or software reset. As soon as the reset is released, the internal oscillator is started and the programmed I^2C address and the trim values are read from the internal nonvolatile memory (NVM) trimming data block. The device enters Standby Mode as soon as the Idle State is reached.

If any of the sensor operation modes becomes activated through an I^2C command (that is, the LS_EN bit is set to 1 and the sensor mode is selected with the respective bit in the MAIN_CTRL register), the internal support blocks are immediately powered on. When the voltages and currents are settled (typical after 500 µs), the state machine checks for trigger events from a measurement scheduler to start conversions according to the selected measurement repeat rates.

When the user resets the LS_EN bit (or the PS_EN bit) to 0, a running conversion is completed and the relevant ADCs move to Standby Mode thereafter. The support blocks only move to Standby Mode if all sensors are Inactive. If any of the sensors is programmed to *sleep after interrupt* with the according bit in the MAIN_CTRL register, the relevant ADCs move to Standby Mode after the interrupt condition occurred. Also the sensor's Enable bit LS_EN or PS_EN is reset after following read out of Main Status register.

The deactivation LS or PS in the MAIN_CTRL register does not clear the related status bit in the MAIN_STATUS register. They are always reset upon activation of the respective sensor.

Figure 9: System Main State Machine



Light Sensor Operation and Proximity Sensor Operation

The Light Sensor (LS) can be operated independently and in parallel to the Proximity Sensor (PS). It can be configured to run in ALS mode or in RGB mode. The difference between both sub-modes of the Light Sensor is in the activation of the sensor channels. ALS mode is offered for power saving if the full RGB functionality is not needed.

The proximity sensor can be operated independently and in parallel to the light sensor. To reduce the influence of crosstalk, the APDS-9999 has an analog and a digital crosstalk cancellation built in. By using the analog cancellation, a reduction of the sensor's dynamic range can be avoided. Additionally, a digital cancellation value can still be automatically subtracted from the PS conversion result if needed. Both values are accessible using a register, and the external application must determine the appropriate cancellation values prior to the start of the measurement.

Light Sensor Interrupt

The interrupt is configured by the bit in the INT_CFG register. It can function as either threshold triggered (LS_VAR_MODE = 0) or variance triggered (LS_VAR_MODE = 1).

The threshold interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 0. The interrupt is set when the respective *_DATA register of the selected interrupt source channel is above the upper or below the lower threshold configured in the LS_THRES_UP and LS_THRES_LOW registers for a specified number of consecutive measurements as configured in the INT_PST register (1+LS_PERSIST).

The variance interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 1. It is set when the absolute value difference between the preceding and the current output data of the selected interrupt source channel is above the decoded variance threshold for a specified number of consecutive measurements (1+LS_PERSIST).

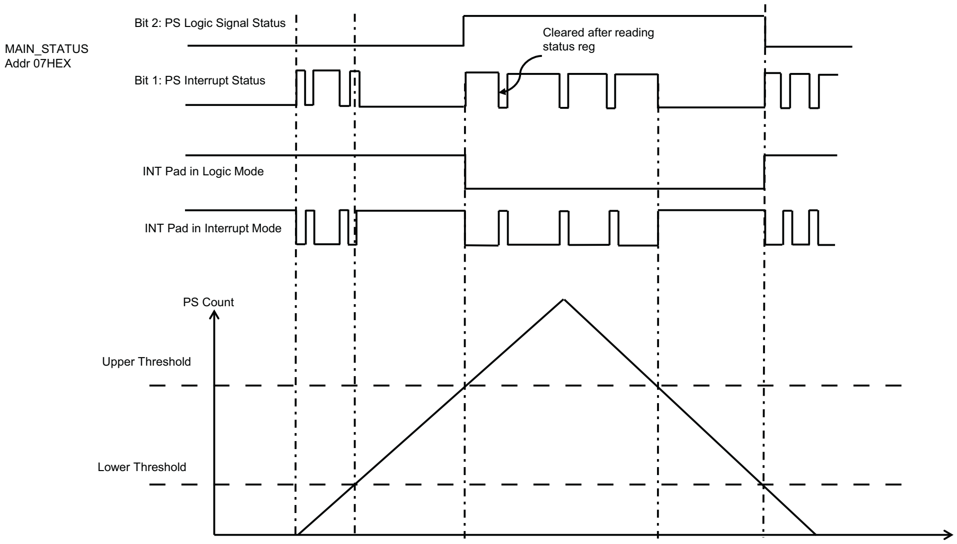
Proximity Sensor Interrupt

The interrupt is configured by the bit in the INT_CFG register. It is threshold triggered.

The interrupt is enabled with PS_INT_EN = 1. The interrupt is set when the PS_DATA register content is above the upper or below the lower threshold configured in the PS_THRES_UP and PS_THRES_LOW registers for a specified number of consecutive measurements as configured in the INT_PST register (1+PS_PERSIST).

The ps_logic signal (PS_LOGIC_STAT bit in the MAIN_STATUS register) is set to 0 if the PS data is below the lower PS threshold, and it is set to 1 if the PS data is above the upper PS threshold.

Figure 10: PS Interrupt Behavior



NOTE: The MAIN_STATUS register should be read out closely after an interrupt transition occurred on the INT pad. The interrupt is not reset automatically; an interrupt event caused by crossing the opposite threshold could be missed.

Interrupt

The APDS-9999 generates independent LS and PS interrupt signals.

For LS, an interrupt can also be triggered if the output variation of consecutive conversions has exceeded a defined limit.

The PS logic output mode has priority over any other interrupt signal. If selected (PS_LOGIC_MODE = 1), no LS interrupt can be signaled at the INT pad. The LS and PS, as well as PS_LOGIC_MODE are active low at the INT pin. A cleared LS interrupt status or PS interrupt status flag also clears the interrupt signal on the INT pin.

Another feature is the option to deactivate both sensors after and interrupt event occurred. Therefore, a bit for the respective sensor has to be set in the MAIN_CTRL register (SAI_PS and SAI_LS). This feature is independently available for both sensors.

Optical Design Consideration

The spacing between the cover glass bottom surface and the package top surface is critical to minimizing the unwanted reflected IR light from the VCSEL to the sensor's photodetector. Excessive reflection can adversely affect the performance of the sensor. For details of mechanical and optical design recommendations, refer to the APDS-9999 application notes.

Figure 11: PS Output vs. Distance at 10 mA at 64 Pulse, 11 bit. No glass in front of module, 18% Kodak grey card.

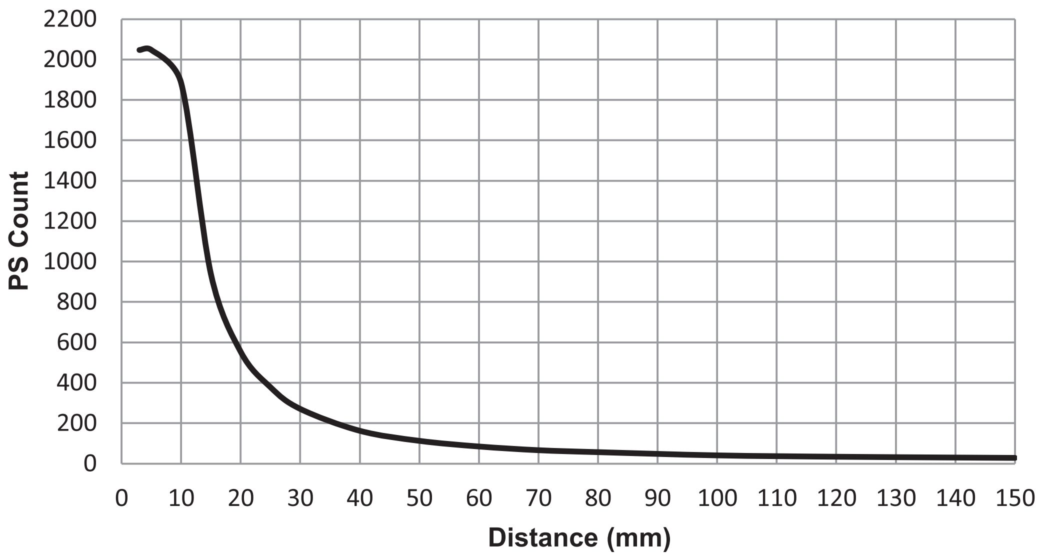
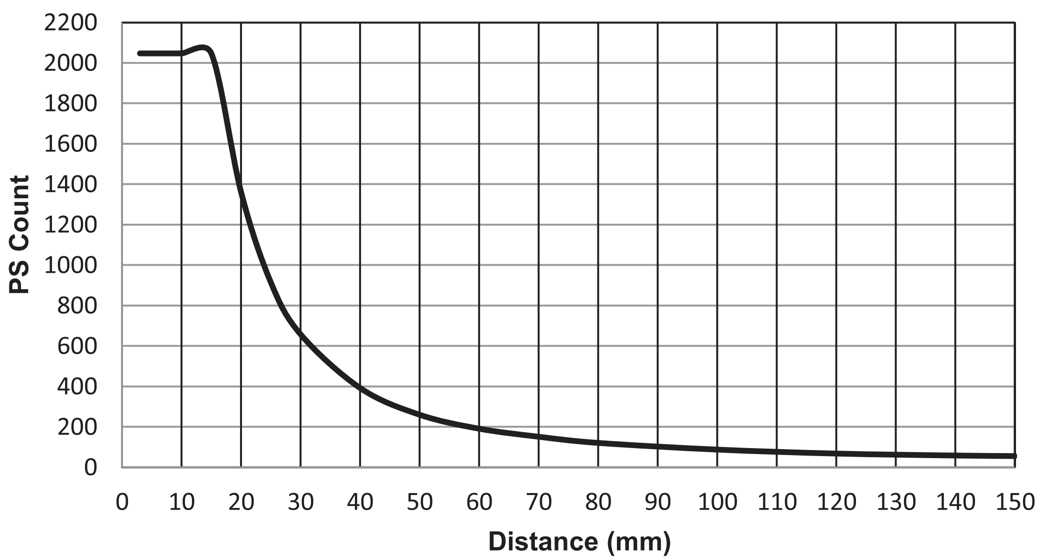


Figure 12: PS Output vs. Distance at 25 mA at 64 Pulse, 11 bit. No glass in front of module, 18% Kodak grey card.



I^2C Protocol

Interface and control of the APDS-9999 is accomplished through an I^2C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The device supports a single slave address of 0x52 hex using a 7-bit addressing protocol. (Contact the factory for other addressing options.)

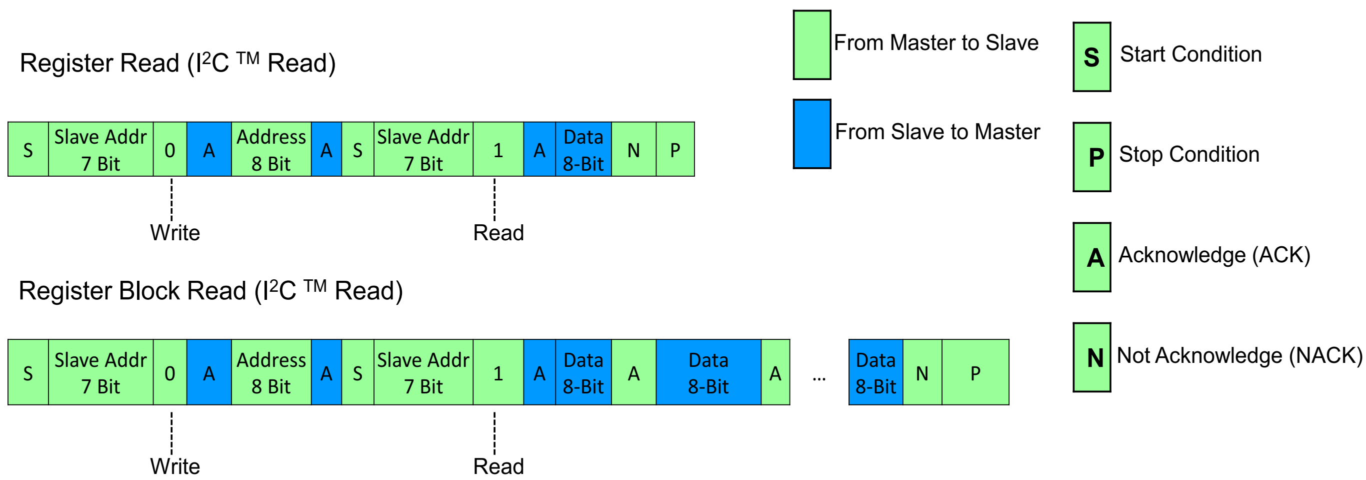
I²C Register Read

The registers can be read individually or in block read mode. When two or more bytes are read in block read mode, reserved register addresses are skipped and the next valid address is referenced. If the last valid address has been reached, but the master continues with the block read, the address counter in the device does not roll over, and the device returns 00HEX for every subsequent byte read.

The block read operation is the only way to ensure correct data read out of multi-byte registers and to avoid splitting of results with HIGH and LOW bytes originating from different conversions. During block read access on the ALS result registers, the result update is blocked.

If a read access is started on an address belonging to a non-readable register, the APDS-9999 returns NACK until the I²C operation is ended.

Read operations must follow this timing diagram.



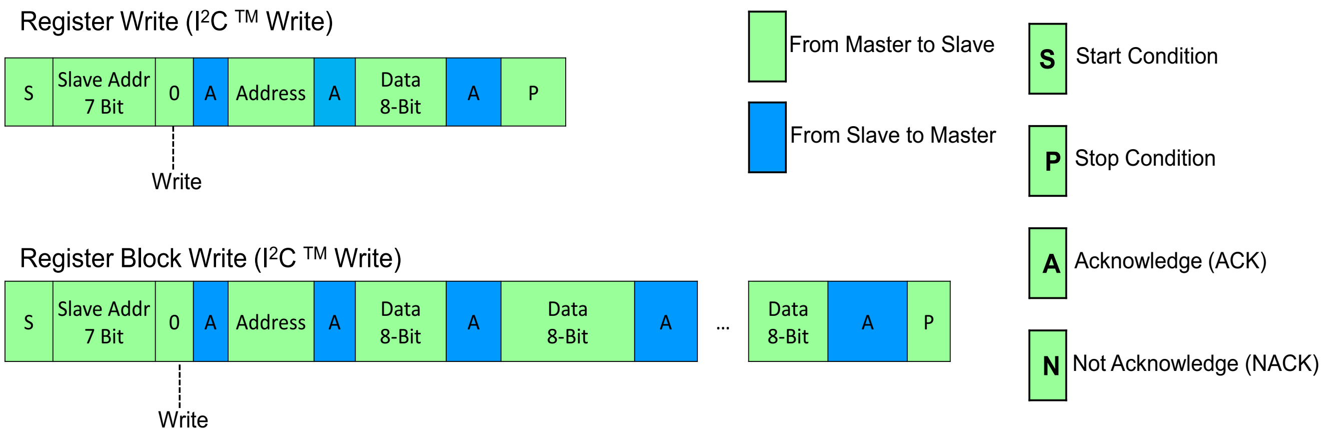
I²C Register Write

The APDS-9999 registers can be written to individually or in block write mode. When two or more bytes are written in block write mode, reserved registers and read-only registers are skipped. The transmitted data is automatically applied to the next writable register. If a register includes read (R) and read/write (RW) bit, the register is not skipped. Data written to the read-only bit is ignored.

If the last valid address of the APDS-9999 address range is reached but the master attempts to continue the block write operation, the address counter of the APDS-9999 does not roll over. The APDS-9999 returns NACK for every following byte sent by the master until the I²C operation is ended.

If a write access is started on an address belonging to a non-writable register, the APDS-9999 returns NACK until the I²C operation is ended.

Write operations must follow this timing.



Register Set

The APDS-9999 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

Address	Type	Name	Description	Reset Value
00HEX	RW	MAIN_CTRL	Operation mode control, SW reset	00HEX
01HEX	RW	PS_VCSEL	PS VCSEL settings	36HEX
02HEX	RW	PS_PULSES	PS number of VCSEL pulses	08HEX
03HEX	RW	PS_MEAS_RATE	PS measurement rate in active mode	05HEX
04HEX	RW	LS_MEAS_RATE	LS measurement rate and resolution	22HEX
05HEX	RW	LS_GAIN	LS analog gain range	01HEX
06HEX	R	PART_ID	Part number ID and revision ID	C2HEX
07HEX	R	MAIN_STATUS	Power-on status, interrupt status, data status	20HEX
08HEX	R	PS_DATA_0	PS measurement data, least significant bit	00HEX
09HEX	R	PS_DATA_1	PS measurement data, most significant bit, and overflow	00HEX
0AHEX	R	LS_DATA_IR_0	IR ADC measurement data - LSB	00HEX
0BHEX	R	LS_DATA_IR_1	IR ADC measurement data	00HEX
0CHEX	R	LS_DATA_IR_2	IR ADC measurement data - MSB	00HEX
0DHEX	R	LS_DATA_GREEN_0	ALS / Green ADC measurement data - LSB	00HEX
0EHEX	R	LS_DATA_ GREEN_1	ALS / Green ADC measurement data	00HEX
0FHEX	R	LS_DATA_ GREEN_2	ALS / Green ADC measurement data - MSB	00HEX
10HEX	R	LS_DATA_BLUE_0	Blue ADC measurement data - LSB	00HEX
11HEX	R	LS_DATA_ BLUE_1	Blue ADC measurement data	00HEX
12HEX	R	LS_DATA_ BLUE_2	Blue ADC measurement data - MSB	00HEX
13HEX	R	LS_DATA_RED_0	RED ADC measurement data - LSB	00HEX
14HEX	R	LS_DATA_RED_1	RED ADC measurement data	00HEX
15HEX	R	LS_DATA_ RED_2	RED ADC measurement data - MSB	00HEX
19HEX	RW	INT_CFG	Interrupt configuration	10HEX
1AHEX	RW	INT_PST	Interrupt persist setting	00HEX
1BHEX	RW	PS_THRES_UP_0	PS interrupt upper threshold, LSB	FFHEX
1CHEX	RW	PS_THRES_UP_1	PS interrupt upper threshold, MSB	07HEX
1DHEX	RW	PS_THRES_LOW_0	PS interrupt lower threshold, LSB	00HEX
1EHEX	RW	PS_THRES_LOW_1	PS interrupt lower threshold, MSB	00HEX
1FHEX	RW	PS_CAN_0	PS intelligent cancellation level setting, LSB	00HEX
20HEX	RW	PS_CAN_1, PS_CAN_ANA	PS intelligent cancellation level setting, MSB	00HEX
21HEX	RW	LS_THRES_UP_0	LS Interrupt upper threshold, LSB	FFHEX
22HEX	RW	LS_THRES_UP_1	LS Interrupt upper threshold	FFHEX
23HEX	RW	LS_THRES_UP_2	LS Interrupt upper threshold, MSB	0FHEX
24HEX	RW	LS_THRES_LOW_0	LS Interrupt lower threshold, LSB	00HEX
25HEX	RW	LS_THRES_LOW_1	LS Interrupt lower threshold	00HEX
26HEX	RW	LS_THRES_LOW_2	LS Interrupt lower threshold, MSB	00HEX
27HEX	RW	LS_THRES_VAR	LS Interrupt variance threshold	00HEX

MAIN_CTRL

Default Value: 00HEX

Address: 00HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	SAI_PS	SAI_LS	SW RESET	0	RGB_MODE	LS_EN	PS_EN

Field	Bit	Description
SAI_PS	6	Sleep after Interrupt for PS: When this bit is set, the proximity sensor returns to standby (PS_EN is cleared when the measurement is finished and the MAIN_STATUS register is read), once an interrupt occurs. This bit reacts on PS interrupt status bit in the MAIN_STATUS register.
SAI_LS	5	Sleep after Interrupt for LS: When this bit is set, the light sensor returns to standby (LS_EN is cleared when the measurement is finished and the MAIN_STATUS register is read), once an interrupt occurs. This bit reacts on the LS interrupt status bit in the MAIN_STATUS register.
SW RESET	4	1: If bit is set to 1, a software reset will be triggered immediately and therefore the I^2C bus command is *not* answered with ACK.
RGB_MODE	2	0: ALS and IR channels are activated **(default)**. 1: All Light Sensor (RGB and IR) channels are activated.
LS_EN	1	0: Ambient light sensor standby **(default)**. 1: Light Sensor active.
PS_EN	0	0: Proximity sensor standby **(default)**. 1: Proximity Sensor active.

PS_VCSEL

Default Value: 36HEX

Address: 01HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	VCSEL PULSE MODULATION FREQUENCY			0	VCSEL CURRENT		

Field	Bit	Description
VCSEL PULSE MODULATION FREQUENCY	6:4	000: Reserved. 001: Reserved. 010: Reserved. 011: VCSEL pulse frequency = 60 kHz **(default)**. 100: VCSEL pulse frequency = 70 kHz. 101: VCSEL pulse frequency = 80 kHz. 110: VCSEL pulse frequency = 90 kHz. 111: VCSEL pulse frequency = 100 kHz.
VCSEL CURRENT	2:0	010: VCSEL pulse current level = 10 mA. 011: VCSEL pulse current level = 25 mA.

Writing to this register stops the ongoing measurements and starts new measurements (depending on the enable bit).

PS_PULSES

Default Value: 08HEX

Address: Address: 02HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS NUMBER OF VCSEL PULSES							

Field	Bit	Description
PS_PULSES	7:0	00000000: 0 pulses (no light emission). … …. 00001000: 8 pulses **(default)**. … …. 00100000: 32 pulses. … …. 11111111: 255 pulses.

Writing to this register resets PS state machine and starts new measurements.

PS_MEAS_RATE

Default Value: 05HEX

Address: 03HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	PS RESOLUTION		PS MEASUREMENT RATE		

Field	Bit	Description
PS RESOLUTION	4:3	00: 8 bit **(default)**. 01: 9 bit. 10: 10 bit. 11: 11 bit.
PS MEASUREMENT RATE	2:0	000: Reserved. 001: 6.25 ms. 010: 12.5 ms. 011: 25 ms. 100: 50 ms. 101: 100 ms **(default)**. 110: 200 ms. 111: 400 ms.

Bit 2:0 register controls the timing of the periodic measurements of the PS in active mode.

When the measurement repeat rate is programmed to be faster than possible for the programmed ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register stops the ongoing measurements and starts new measurements (depending on the respective enable bits).

LS_MEAS_RATE

Default Value: 22HEX

Address: 04HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	LS RESOLUTION			0	LS MEASUREMENT RATE		

Field	Bit	Description
LS RESOLUTION	6:4	000: 20 bit – 400 ms. 001: 19 bit – 200 ms. 010: 18 bit – 100 ms **(default)**. 011: 17 bit – 50 ms. 100: 16 bit – 25 ms. 101: 13 bit – 3.125 ms. 110: Reserved. 111: Reserved.
LS MEASUREMENT RATE	2:0	000: 25 ms. 001: 50 ms. 010: 100 ms **(default)**. 011: 200 ms. 100: 500 ms. 101: 1000 ms. 110: 2000 ms. 111: 2000 ms.

When the measurement repeat rate is programmed to be faster than possible for the programmed ADC measurement time, the repeat rate will be lower than programmed (maximum speed).

Writing to this register stops the ongoing measurement and starts new measurements (depending on the respective bits).

LS_GAIN

Default Value: 01HEX

Address: 05HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LS GAIN RANGE		

Field	Bit	Description
LS GAIN RANGE	2:0	000: Gain 1. 001: Gain 3 **(default)**. 010: Gain 6. 011: Gain 9. 100: Gain 18.

Writing to this register resets the LS state machine and starts new measurements.

PART_ID

Default Value: C2HEX

Address: 06HEX

B7	B6	B5	B4	B3	B2	B1	B0
PART ID				REVISION ID			

Field	Bit	Description
PART ID	7:4	Part number ID.
REVISION ID	3:0	Revision ID of the component.

MAIN_STATUS

Default Value: 20HEX

Address: 07HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	POWER ON STATUS	LS INTERRUPT STATUS	LS DATA STATUS	PS LOGIC SIGNAL STATUS	PS INTERRUPT STATUS	PS DATA STATUS

Field	Bit	Description
POWER ON STATUS	5	1: Part went through a power-up event, either because the part was turned on or because there was power supply disturbance (default at first register read). All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if necessary. The flag is cleared after the register is read.
LS INTERRUPT STATUS	4	0: Interrupt condition is not fulfilled **(default)**. 1: Interrupt condition is fulfilled (cleared after read).
LS DATA STATUS	3	0: Old data, already read **(default)**. 1: New data, not yet read (cleared after read).
PS LOGIC SIGNAL STATUS	2	0: Object is far **(default).** 1: Object is close.
PS INTERRUPT STATUS	1	0: Interrupt condition is not fulfilled **(default)**. 1: Interrupt condition is fulfilled (cleared after read).
PS DATA STATUS	0	0: Old data, already read **(default)**. 1: New data, not yet read (cleared after read).

PS_DATA

Default Value: 00HEX, 00HEX

Address: 08HEX, 09HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_DATA_0							
0	0	0	0	OVERFLOW	PS_DATA_1		

If an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, both registers PS_DATA_0 and PS_DATA_1 are locked until the I^2C read operation is completed or the specified address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual PS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

The PS conversion result is always written LSB-aligned into the PS_DATA registers, regardless of the conversion resolution selected in the PS_MEAS_RATE register. PS_DATA_1 is filled with 0 for resolutions lower than 11 bit. If the PS data is outside of the measurable range, the Overflow flag (PS_DATA_1, Bit [3]) is set in any resolution mode.

PS_DATA is automatically corrected by the value of the PS cancellation register (PS_CAN).

PS_DATA = PS_MEAS – PS_CAN

PS_MEAS is the internal raw value obtained from the PS ADC. If PS_MEAS is already full-scale, the value of PS_DATA is set to its maximum value without subtracting the PS cancellation value.

Reg 08HEX	Bit [7:0]	PS measurement least significant data byte, bit 0 is the LSB of the data word.
Reg 09HEX	Bit [3]	0: Valid PS data **(default).** 1: Overflow of PS data.
	Bit [2:0]	PS measurement most significant data byte, bit 2 is the MSB in 11-bit mode.

LS_DATA_IR

Default Value: 00HEX, 00HEX, 00HEX

Address: 0AHEX, 0BHEX, 0CHEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_DATA_IR_0							
LS_DATA_IR_1							
0	0	0	0	LS_DATA_IR_2			

IR channel output data (unsigned integer, 13 to 20 bit, LSB aligned).

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 0AHEX	Bit [7:0]	IR diode data least significant data byte.
Reg 0BHEX	Bit [7:0]	IR diode data intervening data byte.
Reg 0CHEX	Bit [3:0]	IR diode data most significant data byte.

LS_DATA_GREEN

Default Value: 00HEX, 00HEX, 00HEX

Address: 0DHEX, 0EHEX, 0FHEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_DATA_GREEN_0							
LS_DATA_ GREEN_1							
0	0	0	0	LS_DATA_ GREEN_2			

ALS/Green channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 0DHEX	Bit [7:0]	ALS/Green diode data least significant data byte.
Reg 0EHEX	Bit [7:0]	ALS/Green diode data intervening data byte.
Reg 0FHEX	Bit [3:0]	ALS/Green diode data most significant data byte.

LS_DATA_BLUE

Default Value: 00HEX, 00HEX, 00HEX

Address: 10HEX, 11HEX, 12HEX

<table>
<tr><th>B7</th><th>B6</th><th>B5</th><th>B4</th><th>B3</th><th>B2</th><th>B1</th><th>B0</th></tr>
<tr><td colspan="8">LS_DATA_BLUE_0</td></tr>
<tr><td colspan="8">LS_DATA_ BLUE_1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="4">LS_DATA_ BLUE_2</td></tr>
</table>

Blue channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 10HEX	Bit [7:0]	Blue diode data least significant data byte.
Reg 11HEX	Bit [7:0]	Blue diode data intervening data byte.
Reg 12HEX	Bit [3:0]	Blue diode data most significant data byte.

LS_DATA_RED

Default Value: 00HEX, 00HEX, 00HEX

Address: 13HEX, 14HEX, 15HEX

<table>
<tr><th>B7</th><th>B6</th><th>B5</th><th>B4</th><th>B3</th><th>B2</th><th>B1</th><th>B0</th></tr>
<tr><td colspan="8">LS_DATA_RED_0</td></tr>
<tr><td colspan="8">LS_DATA_RED_1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="4">LS_DATA_ RED_2</td></tr>
</table>

Red channel digital output data (unsigned integer, 13 to 20 bit, LSB aligned).

When an I^2C read operation is active and points to an address in the range 07HEX to 18HEX, all registers in this range are locked until the I^2C read operation is completed or this address range is left.

This ensures that the data in the registers comes from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the actual LS_DATA registers are updated as soon as there is no ongoing I^2C read operation to the address range 07HEX to 18HEX.

Reg 13HEX	Bit [7:0]	Red diode data least significant data byte.
Reg 14HEX	Bit [7:0]	Red diode data intervening data byte.
Reg 15HEX	Bit [3:0]	Red diode data most significant data byte.

INT_CFG

Default Value: 10HEX

Address: 19HEX

B7	B6	B5	B4	B3	B2	B1	B0
0	0	LS_INT_SEL		LS_VAR_MODE	LS_INT_EN	PS_LOGIC_MODE	PS_INT_EN

Field	Bit	Description
LS_INT_SEL	5:4	00: IR channel. 01: ALS channel/Green channel **(default)**. 10: Red channel. 11: Blue channel.
LS_VAR_MODE	3	0: LS threshold interrupt mode **(default)**. 1: LS variation interrupt mode.
LS_INT_EN	2	0: LS Interrupt disabled **(default)**. 1: LS Interrupt enabled.
PS_LOGIC_MODE	1	0: Normal interrupt function: After an interrupt event, the INT pad maintains at an active level until the MAIN_STATUS register is read **(default)**. 1: PS Logic Output Mode: The INT pad is updated after every measurement and maintains an output state between measurements.
PS_INT_EN	0	0: PS Interrupt disabled **(default)**. 1: PS Interrupt enabled.

INT_PST

Default Value: 00HEX

Address: 1AHEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_PERSIST				PS_PERSIST			

Field	Bit	Description
LS_PERSIST	7:4	0000: Every LS value out of threshold range **(default)** asserts an interrupt. 0001: 2 consecutive LS values out of threshold range assert an interrupt. … 1111: 16 consecutive LS values out of threshold range assert an interrupt.
PS_PERSIST	3:0	0000: Every PS value out of threshold range **(default)** asserts an interrupt. 0001: 2 consecutive PS values out of threshold range assert an interrupt. … 1111: 16 consecutive PS values out of threshold range assert an interrupt.

This register sets the number of similar consecutive LS interrupt events that must occur before the interrupt is asserted.

PS_THRES_UP

Default Value: FFHEX, 07HEX

Address: 1BHEX,1CHEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_THRES_UP_0							
0	0	0	0	0	PS_THRES_UP_1		

PS_THRES_UP sets the upper threshold value for the PS interrupt. The interrupt controller compares the value in PS_THRES_UP against measured data in the PS_DATA registers of the selected LS interrupt channel. It generates an interrupt event if PS_DATA exceeds the upper threshold level.

The data format for PS_THRES_UP must match that of the PS_DATA registers.

For resolutions below 11 bit, the threshold is evaluated LSB-aligned.

Reg 1BHEX	Bit [7:0]	PS upper interrupt threshold value, LSB.
Reg 1CHEX	Bit [2:0]	PS upper interrupt threshold value, MSB.

PS_THRES_LOW

Default Value: 00HEX, 00HEX

Address: 1DHEX, 1EHEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_THRES_LOW_0							
0	0	0	0	0	PS_THRES_LOW_1		

PS_THRES_LOW sets the lower threshold value for the PS interrupt. The interrupt controller compares the value in PS_THRES_LOW against measured data in the PS_DATA registers of the selected LS interrupt channel. It generates an interrupt event if PS_DATA is lower than the lower the threshold level.

The data format for PS_THRES_LOW must match that of the PS_DATA registers.

For resolutions below 11 bit, the threshold is evaluated LSB-aligned.

Reg 1DHEX	Bit [7:0]	PS lower interrupt threshold value, LSB.
Reg 1EHEX	Bit [2:0]	PS lower interrupt threshold value, MSB.

PS_CAN

Default Value: 00HEX, 00HEX

Address: 1FHEX, 20HEX

B7	B6	B5	B4	B3	B2	B1	B0
PS_CAN_0							
PS_CAN_ANA					PS_CAN_1		

The PS cancellation level is expected to be written by the MCU during system startup. The digital value is subtracted from the measured PS data before the data is transferred to the PS_DATA registers and evaluated by the interrupt controller.

Writing to these registers resets the PS state machine and starts new measurements.

Reg 1FHEX	Bit [7:0]	PS digital cancellation level, LSB.
Reg 20HEX	Bit [7:3]	PS analog cancellation level, MSB.
	Bit [2:0]	PS digital cancellation level, MSB

LS_THRES_UP

Default Value: FFHEX, FFHEX, 0FHEX

Address: 21HEX, 22HEX, 23HEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_THRES_UP_0							
LS_THRES_UP_1							
0	0	0	0	LS_THRES_UP_2			

LS_THRES_UP sets the upper threshold value for the LS interrupt. The interrupt controller compares the value in LS_THRES_UP against measured data in the LS_DATA registers of the selected LS interrupt channel. It generates an interrupt event if DATA exceeds the threshold level.

The data format for LS_THRES_UP must match that of the LS_DATA registers.

Writing to these registers resets the LS state machine and starts new measurements.

Reg 21HEX	Bit [7:0]	LS upper interrupt threshold value, LSB.
Reg 22HEX	Bit [7:0]	LS upper interrupt threshold value, intervening byte.
Reg 23HEX	Bit [3:0]	LS upper interrupt threshold value, MSB.

LS_THRES_LOW

Default Value: 00HEX, 00HEX, 00HEX

Address: 24HEX, 25HEX, 26HEX

B7	B6	B5	B4	B3	B2	B1	B0
LS_THRES_LOW_0							
LS_THRES_LOW_1							
0	0	0	0	LS_THRES_LOW_2			

LS_THRES_LOW sets the lower threshold value for the LS interrupt. The interrupt controller compares the value in LS_THRES_LOW against measured data in the LS_DATA registers of the selected LS interrupt channel. It generates an interrupt event if DATA is below the threshold level.

The data format for LS_THRES_LOW must match that of the LS_DATA registers.

Reg 24HEX	Bit [7:0]	LS lower interrupt threshold value, LSB.
Reg 25HEX	Bit [7:0]	LS lower interrupt threshold value, intervening byte.
Reg 26HEX	Bit [3:0]	LS lower interrupt threshold value, MSB.

LS_THRES_VAR

Default Value: 00HEX

Address: 27HEX

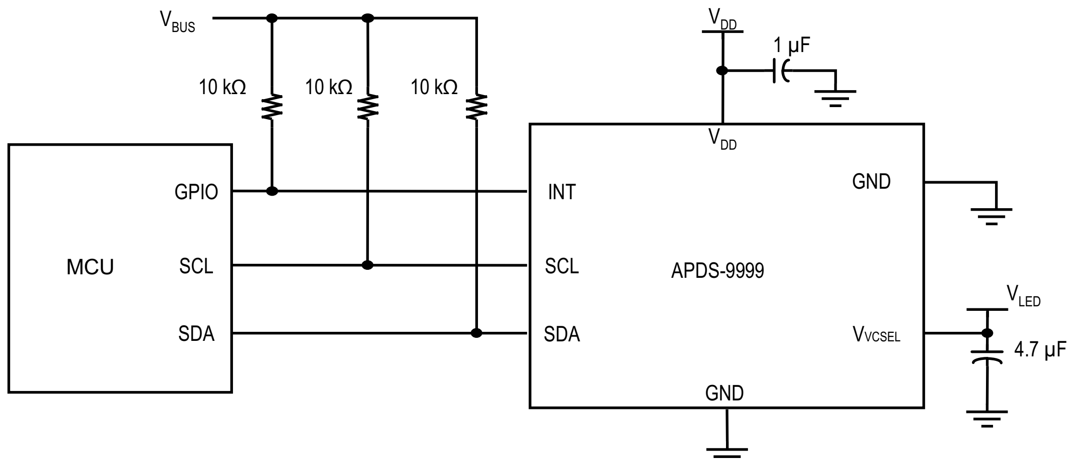
B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LS_THRES_VAR		

Field	Bit	Description
LS_THRES_VAR	2:0	000: LS result varies by 8 counts compared to previous result **(default)**. 001: LS result varies by 16 counts compared to previous result. 010: LS result varies by 32 counts compared to previous result. 011: LS result varies by 64 counts compared to previous result. … 111: LS result varies by 1024 counts compared to previous result.

Application Information: Hardware

The application hardware circuit for implementing an RGB and Proximity sensing solution is simple with the APDS-9999 and is shown in Figure 13. The 1-µF and 4.7-µF decoupling capacitors should be of low ESR to reduce noise. To maximize system performance, the use of power and ground planes is recommended in the PCB. If mounted on a flexible circuit, the power and ground traces back to the PCB should be sufficiently wide enough to have a low resistance of < 1 ohm.

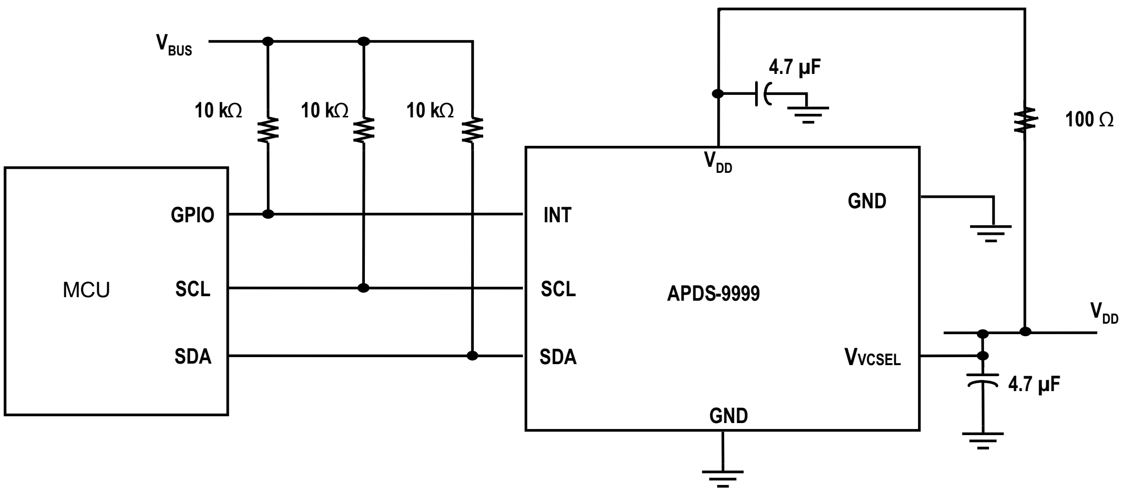
Figure 13: APDS-9999 Dual Supply Application Circuit



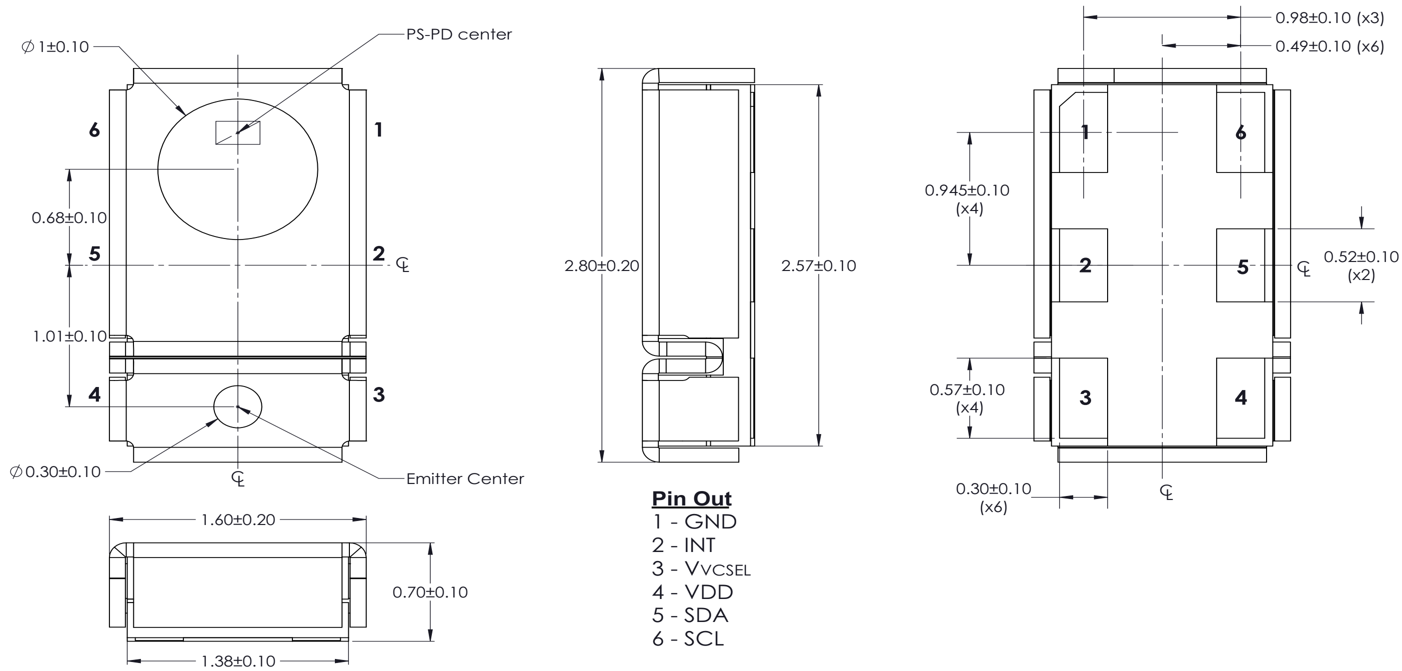
The external components count is minimized for object proximity distance detection with sensor APDS-9999. In a proximity sensing system, the included VCSEL is pulsed with of rapidly switching current; therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise from being coupled back into the device during the VCSEL pulses. The recommendation is to use two power supplies; one for the device VDD and the other for the V_{VCSEL} pin. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the VDD pin and the noisy supply to the V_{VCSEL} pin, the key goal can be met. Place a 1-µF low-ESR decoupling capacitor as close as possible to the VDD pin and another at the LEDA pin, of at least 4.7-µF of bulk capacitance to supply the any current surge.

In situations where only a single supply is available, refer to Figure 14 for the application circuit. The two 4.7-µF decoupling capacitors should be of low ESR to reduce noise. To maximize system performance, the use of power and ground planes is recommended in the PCB. If mounted on a flexible circuit, the power and ground traces back to the PCB should be sufficiently wide enough to have a low resistance of < 1 ohm.

Figure 14: Single Supply Application Circuit

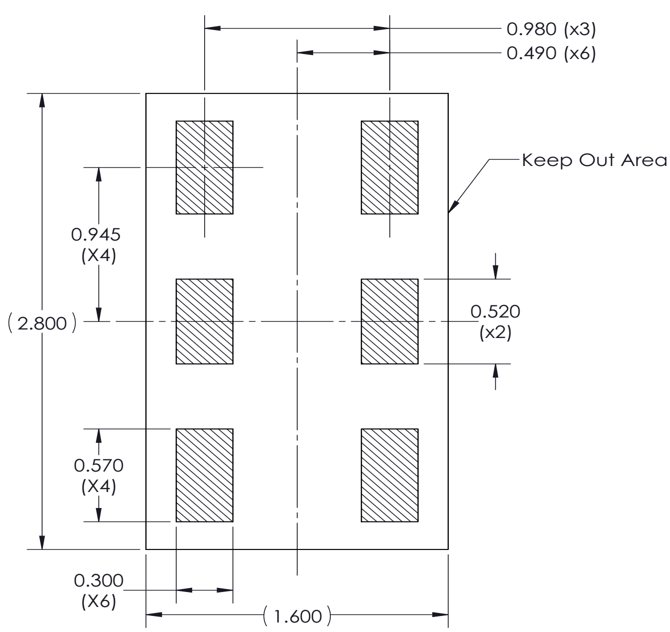


Package Outline Dimensions



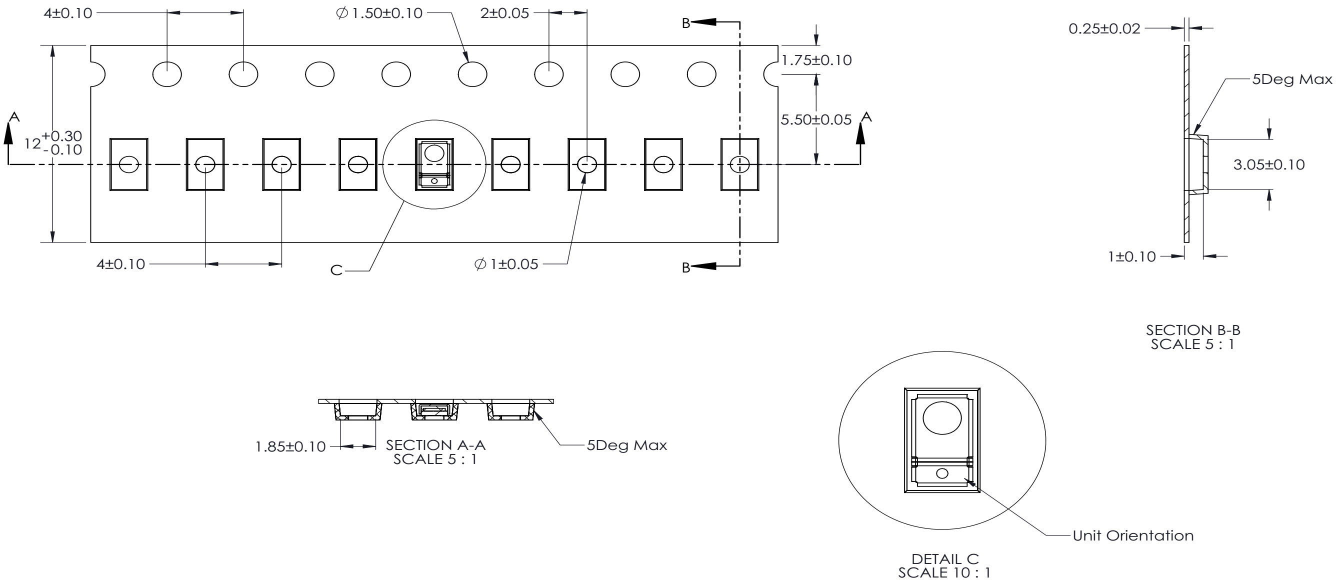
NOTE: All dimensions are in mm.

PCB Pad Layout



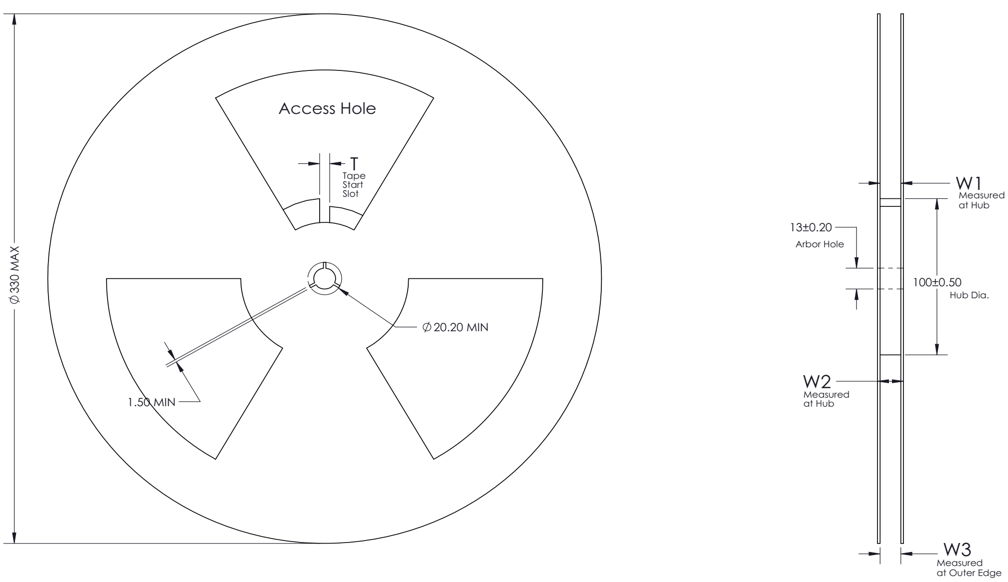
NOTE: All dimensions are in mm.

Tape Dimensions



NOTE: All dimensions are in mm.

Reel Dimensions



Tape Width	T	W1	W2	W3
12 mm	4 ± 0.50	12.4 + 2.0 – 0.0	18.4 Max.	11.9 Min. 15.4 Max.

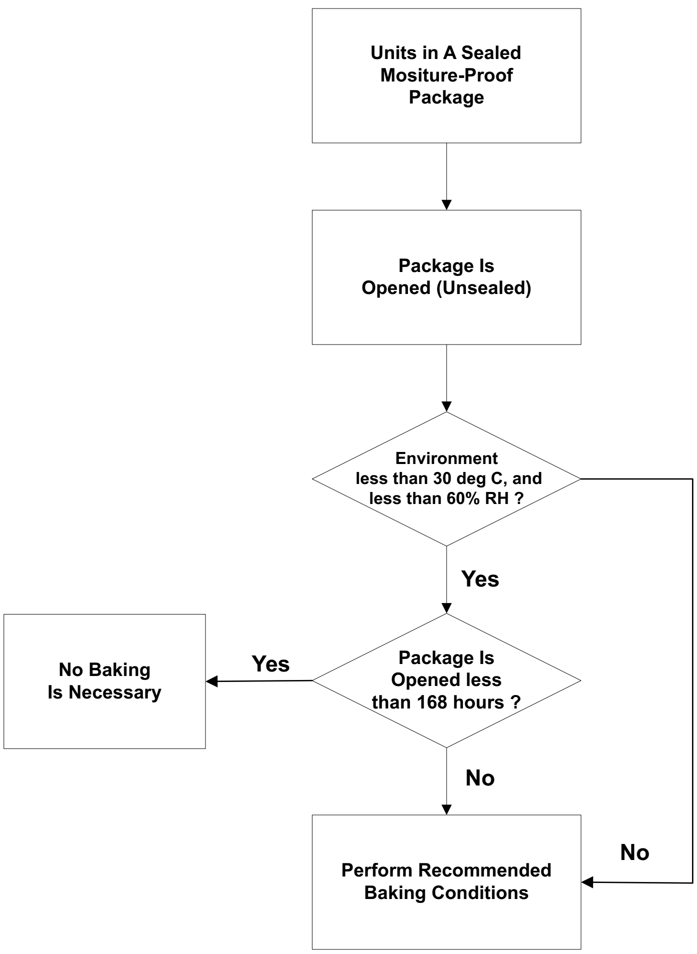
NOTE: All dimensions are in mm.

Laser Safety Considerations

The APDS-9999 contains a laser emitter and is compliance within Class 1 laser safety limits of IEC 60825-1, Edition 2: 2007, Clauses 8 and 9. When use within Broadcom recommended operating conditions and device settings as specified in this data sheet, APDS-9999 remains within Class 1 limits. Under no circumstances should the laser power be increased.

Moisture Proof Packaging

All APDS-9999 options are shipped in a moisture-proof package. When opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions

Package	Temperature	Time
In Reel	60°C	48 hours
In Bulk	100°C	4 hours

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

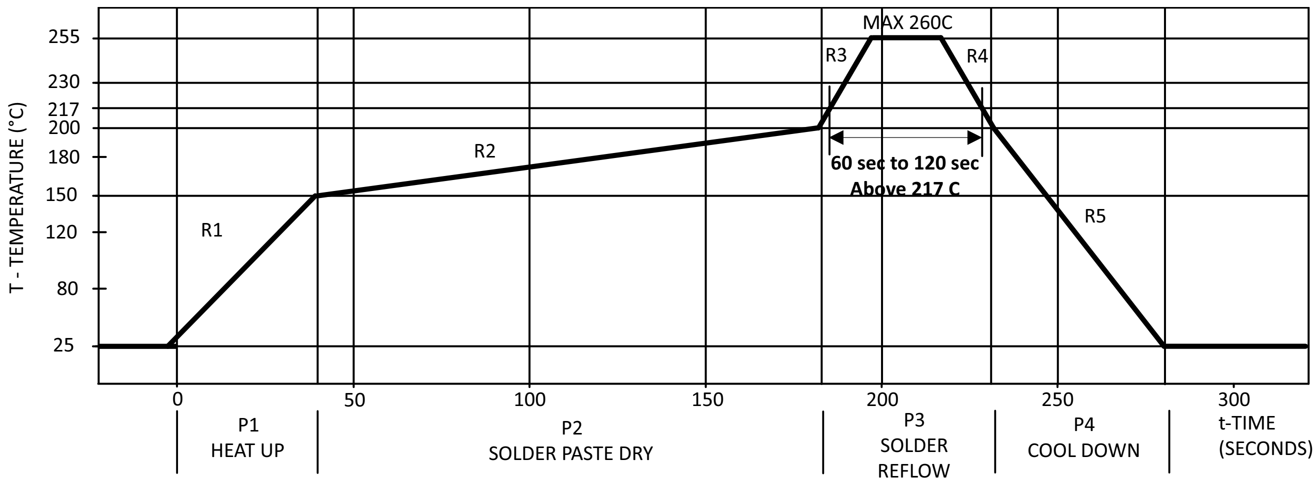
Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3 P3, R4	200°C to 260°C 260°C to 200°C	3°C/s –6°C/s
Cool Down	P4, R5	200°C to 25°C	–6°C/s
Time Maintained above Liquidus Point, 217°C		> 217°C	60s to 120s
Peak Temperature		260°C	—
Time within 5°C of Actual Peak Temperature		> 255°C	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8 minutes

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the previous table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100s to 180s) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60s and 120s. This is to ensure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.