THE DATASHEET OF

BQ24088DRCR

TEXAS INSTRUMENTS

bq24085, bq24086, bq24087, bq24088

SLUS784E – DECEMBER 2007 – REVISED DECEMBER 2015

bq2408x 750-mA Single-Chip Li-Ion and Li-Pol Charge Management IC With Thermal Regulation

1 Features

- Ideal for Low-Dropout Designs for Single-Cell Li-Ion or Li-Pol Packs in Space Limited Applications
- Integrated Power FET and Current Sensor for up to 750-mA Charge Applications
- Reverse Leakage Protection Prevents Battery Drainage
- ±0.5% Voltage Regulation Accuracy
- Thermal Regulation Maximizes Charge Rate
- Charge Termination by Minimum Current and Time
- Precharge Conditioning With Safety Timer
- Status Outputs for LED or System Interface Indicate Charge, Fault, and Power Good Outputs
- Short-Circuit and Thermal Protection
- Automatic Sleep Mode for Low Power Consumption
- Small 3×3 mm MLP Package
- Selectable Battery Insertion and Battery Absent Detection
- Input Overvoltage Protection
  - 6.5 V and 10.5 V Options

2 Applications

- PDA, MP3 Players, Digital Cameras
- Internet Appliances and Handheld Devices

3 Description

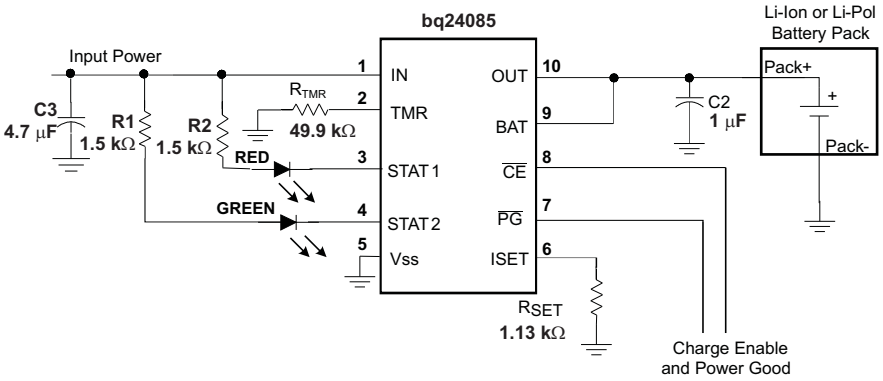
The bq2408x series are highly integrated Li-Ion and Li-Pol linear chargers, targeted at space-limited portable applications. The bq2408x series offers a variety of protection features and functional options, while still implementing a complete charging system in a small package. The battery is charged in three phases: conditioning, constant or thermally regulated current, and constant voltage. Charge is terminated based on minimum current. An internal programmable charge timer provides a backup protection feature for charge termination and is dynamically adjusted during the thermal regulation phase. The bq2408x automatically restarts the charge if the battery voltage falls below an internal threshold; sleep mode is set when the external input supply is removed. Multiple versions of this device family enable easy design of the bq2408x in cradle chargers or in the end equipment, while using low cost or high-end AC adapters.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq2408x	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2009) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

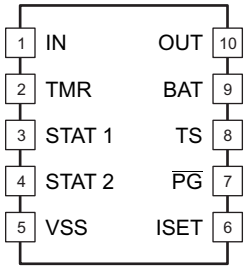
5 Device Options

CHARGE VOLTAGE	INPUT OVERVOLTAGE	TERMINATION ENABLE	SAFETY TIMER ENABLE	POWER GOOD STATUS	IC ENABLE	PACK TEMP	PACK VOLTAGE DETECTION (ABSENT)	DEVICES(1)(2)
4.2 V	6.5 V	TMR pin	TMR pin	$\overline{PG}$ pin	No	TS pin	With timer enabled	bq24086DRCR
								bq24086DRCT
4.2 V	6.5 V	TMR pin	TMR pin	$\overline{PG}$ pin	$\overline{CE}$ pin	No	With timer enabled	bq24085DRCR
								bq24085DRCT
4.2 V	6.5 V	$\overline{TE}$ pin	TMR pin	No	$\overline{CE}$ pin	No	With termination enabled	bq24087DRCR
								bq24087DRCT
4.2 V	10.5 V	TMR pin	TMR pin	$\overline{PG}$ pin	No	TS pin	With timer enabled	bq24088DRCR
								bq24088DRCT

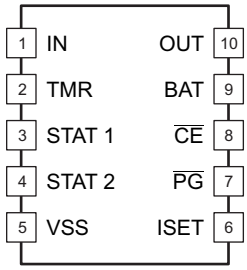
(1) The bq24085/6/7/8 are only available taped and reeled. Add suffix R to the part number for quantities of 3,000 devices per reel (for example, bq24085DRCR). Add suffix T to the part number for quantities of 250 devices per reel (for example, bq24085/6/7DRCT).
(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

6 Pin Configuration and Functions

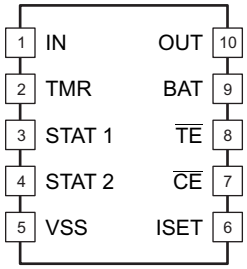
bq24086 and bq24088 DRC Package
10-Pin VSON
Top View



bq24085 DRC Package
10-Pin VSON
Top View



bq24087 DRC Package
10-Pin VSON
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	bq24086/8	bq24085	bq24087		
BAT	9	9	9	I	Battery voltage sense input. Connect to the battery positive terminal. Connect a 390-Ω resistor from BAT to OUT for $I_{(OUT)}$ < 200 mA.
$\overline{CE}$	–	8	7	I	Charge enable input. $\overline{CE}$ = LO enables charger. $\overline{CE}$ = HI disables charger.
IN	1	1	1	I	Charge input voltage and internal supply. Connect a 1-µF (minimum) capacitor from IN to VSS. $C_{IN} \geq C_{OUT}$
ISET	6	6	6	O	Charge current set point, resistor connected from ISET to VSS sets charge current value. Connect a 0.1-µF capacitor from BAT to ISET for $I_{(OUT)}$ < 200 mA.
OUT	10	10	10	O	Charge current output. Connect to the battery positive terminal. Connect a 1-µF (minimum) capacitor from OUT to VSS.
$\overline{PG}$	7	7		O	Power good status output (open-collector), active low.
STAT1	3	3	3	O	Charge status output 1 (open-collector, see Table 3).
STAT2	4	4	4	O	Charge status output 2 (open-collector, see Table 3).
$\overline{TE}$	–	–	8	I	Termination enable input. $\overline{TE}$ = LO enables termination detection and battery absent detection. $\overline{TE}$ = HI disables termination detection and battery absent detection.
TMR	2	2	2	I	Safety timer program input, timer disabled if floating. Connect a resistor to VSS pin to program safety timer timeout value.
TS	8	–	–	I	Temperature sense input, connect to battery pack thermistor. Connect an external resistive divider to program temperature thresholds.
VSS	5	5	5	I	Ground
Exposed Thermal Pad	Pad	Pad	Pad	–	There is an internal electrical connection between the exposed thermal pad and Vss pin of the IC. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the IC. VSS pin must be connected to ground at all times.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
	Supply voltage (IN with respect to Vss)	–0.3	20	V(2)
	Input voltage on IN, STATx, $\overline{PG}$, TS, $\overline{CE}$, TMR (all with respect to Vss)	–0.3	V(IN)	V
	Input voltage on OUT, BAT, ISET (all with respect to Vss)	–0.3	7	V
	Output sink current (STATx) + PG		15	mA
	Output current (OUT pin)		2	A
T_A	Operating free-air temperature	–40	155	°C
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) The bq24085/6/7/8 family can withstand up to 18 V maximum continuously, 20 V for maximum of 2000 hours and 26 V for a maximum for 87 hours.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{(IN)}$	Supply voltage	Battery absent detection not functional	3.5	4.35	V
$V_{(IN)}$	Supply voltage	Battery absent detection functional	4.35	6.5	V
$R_{(TMR)}$	Safety timer program resistor		33	100	KΩ
T_J	Junction temperature		0	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		bq2408x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating range, T_J = 0 –125°C range, See the *Application and Implementation* section, typical values at T_J = 25°C (unless otherwise noted), R_{TMR} = 49.9 KΩ

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER DOWN THRESHOLD – UNDERVOLTAGE LOCKOUT							
V_{UVLO}	Power down threshold	$V_{(IN)}$ = 0 V, increase $V_{(OUT)}$: 0 → 3 V OR $V_{(OUT)}$ = 0 V, increase $V_{(IN)}$: 0 → 3 V, $\overline{CE}$ = LO (1)		1.5		3	V
INPUT POWER DETECTION (2)							
$V_{IN(DT)}$	Input power detection threshold	$V_{(IN)}$ detected at [$V_{(IN)}$ – $V_{(OUT)}$] > $V_{IN(DT)}$				130	mV
$V_{HYS(INDT)}$	Input power detection hysteresis	Input power not detected at [$V_{(IN)}$ – $V_{(OUT)}$] < [$V_{IN(DT)}$ – $V_{HYS(INDT)}$]		30			mV
INPUT OVERVOLTAGE PROTECTION							
$V_{(OVP)}$	Input overvoltage detection threshold	$V_{(IN)}$ increasing	bq24088	10.2	10.5	11.7	V
			bq24085/6/7	6.2	6.5	7	
$V_{HYS(OVP)}$	Input overvoltage hysteresis	$V_{(IN)}$ decreasing	bq24088		0.5		V
			bq24085/6/7		0.2		
QUIESCENT CURRENT							
$I_{CC(CHGOFF)}$	IN pin quiescent current, charger off	Input power detected, $\overline{CE}$ = HI	$V_{(IN)}$ = 6 V		100	200	μA
			$V_{(IN)}$ = 16.5 V		350		
$I_{CC(CHGON)}$	IN pin quiescent current, charger on	Input power detected, $\overline{CE}$ = LO, V_{BAT} = 4.5 V			4	6	mA
$I_{BAT(DONE)}$	Battery leakage current after termination into IC	Input power detected, charge terminated, $\overline{CE}$ = LO			1	5	μA
$I_{BAT(CHGOFF)}$	Battery leakage current into IC, charger off	Input power detected, $\overline{CE}$ = HI **OR** input power not detected, $\overline{CE}$ = LO			1	5	μA
TS PIN COMPARATOR							
$V_{(TS1)}$	Lower voltage temperature threshold	Hot detected at V(TS) < $V_{(TS1)}$; NTC thermistor		29	30	31	%V(IN)
$V_{(TS2)}$	Upper voltage temperature threshold	Cold detected at V(TS) > $V_{(TS2)}$; NTC thermistor		60	61	62	%V(IN)
$V_{HYS(TS)}$	Hysteresis	Temp OK at V(TS) > [$V_{(TS1)}$ + $V_{HYS(TS)}$] OR $V_{(TS)}$ < [$V_{(TS2)}$ – $V_{HYS(TS)}$]			2		%V(IN)
$\overline{CE}$ INPUT							
V_{IL}	Input (low) voltage	$V_{(/CE)}$		0		1	V
V_{IH}	Input (high) voltage	$V_{(/CE)}$		2			V
STAT1, STAT2 AND $\overline{PG}$ OUTPUTS (3)							
V_{OL}	Output (low) saturation voltage	I_{out} = 1 mA (sink)				200	mV
THERMAL SHUTDOWN							
$T_{(SHUT)}$	Temperature trip	Junction temperature, temp rising			155		°C
$T_{(SHUTHYS)}$	Thermal hysteresis	Junction temperature			20		°C
VOLTAGE REGULATION (4)							
$V_{O(REG)}$	Output voltage				4.20		V
$V_{O(TOL)}$	Voltage regulation accuracy	T_A = 25°C		–0.5%		0.5%	
				–1%		1%	
$V_{(DO)}$	Dropout voltage, V(IN) – V(OUT)	$I_{(OUT)}$ = 750 mA				600	mV
CURRENT REGULATION (5)							
$I_{O(OUT)}$	Output current range	$V_{(BAT)}$ > $V_{(LOWV)}$, $I_{O(OUT)}$ = $I_{(OUT)}$ = $K_{(SET)}$ × $V_{(SET)}/R_{(SET)}$		50		750	mA
$V_{(SET)}$	Output current set voltage	$V_{(ISET)}$ = $V_{(SET)}$, $V_{(LOWV)}$ < $V_{(BAT)}$ ≤ $V_{O(REG)}$		2.45	2.5	2.55	V

(1) Specified by design, not production tested.
(2) $\overline{CE}$ = HI or LOW, $V_{(IN)}$ > 3.5 V
(3) $V_{(IN)}$ ≥ $V_{O(REG)}$ + $V_{(DO-MAX)}$
(4) $V_{(IN)}$ ≥ $V_{O(REG)}$ + $V_{(DO-MAX)}$, $I_{(TERM)}$ < $I_{(OUT)}$ < $I_{O(OUT)}$, charger enabled, no fault conditions detected.
(5) $V_{(IN)}$ > $V_{(OUT)}$ > $V_{(DO-MAX)}$, charger enabled, no fault conditions detected.

Electrical Characteristics (continued)

over recommended operating range, T_J = 0 –125°C range, See the *Application and Implementation* section, typical values at T_J = 25°C (unless otherwise noted), R_{TMR} = 49.9 KΩ

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$K_{(SET)}$	Output current set factor	100 mA ≤ $I_{O(OUT)}$ ≤ 750 mA		175	182	190	
		10 mA ≤ $I_{O(OUT)}$ < 100 mA		180	215	250	
R_{ISET}	External resistor range	Resistor connected to ISET pin		0.6		10	kΩ
PRECHARGE AND OUTPUT SHORT-CIRCUIT CURRENT REGULATION(6)							
$V_{(LOWV)}$	Precharge to fast-charge transition threshold	$V_{(BAT)}$ increasing		2.8	2.95	3.15	V
$V_{(SC)}$	Precharge to short-circuit transition threshold	$V_{(BAT)}$ decreasing		1.2	1.4	1.6	V
$V_{(SCIND)}$	Short-circuit indication	$V_{(BAT)}$ decreasing		1.6	1.8	2	
$I_{O(PRECHG)}$	Precharge current range	$V_{(SC)}$ < $V_{I(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$ $I_{O(PRECHG)}$ = $K_{(SET)}$ × $V_{(PRECHG)}$/$R_{(ISET)}$		5		75	mA
$V_{(PRECHG)}$	Precharge set voltage	$V_{(ISET)}$ = $V_{(PRECHG)}$, $V_{(SC)}$ < $V_{I(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$		225	250	280	mV
$I_{O(SHORT)}$	Output shorted regulation current	V_{SS} ≤ $V_{(BAT)}$ ≤ $V_{(SCI)}$, $I_{O(SHORT)}$ = $I_{(OUT)}$, $V_{(BAT)}$= VSS, Internal pullup resistor, T_J = 25°C	V_{POR} < V_{IN} < 6.0 V	7	15	24	mA
			6.0 V < V_{IN} < V_{OVP}		15		
TEMPERATURE REGULATION (Thermal regulation™)(7)							
$T_{J(REG)}$	Temperature regulation limit	$V_{(IN)}$ = 5.5 V, V(BAT) = 3.2 V, Fast charge current set to 1 A		101	112	125	°C
$I_{(MIN\_TJ(REG))}$	Minimum current in thermal regulation	$V_{(LOWV)}$ < V(BAT) < VO(REG), 0.7 kΩ < $R_{(ISET)}$ < 1.18 kΩ			105	125	mA
CHARGE TERMINATION DETECTION(8)							
$I_{(TERM)}$	Termination detection current range	$V_{(BAT)}$ > $V_{(RCH)}$, $I_{(TERM)}$ = $K_{(SET)}$ × $V_{(TERM)}$/$R_{(ISET)}$		5		75	mA
$V_{(TERM)}$	Charge termination detection set voltage(9)	$V_{(BAT)}$ > $V_{(RCH)}$		225	250	275	mV
BATTERY RECHARGE THRESHOLD							
$V_{(RCH)}$	Recharge threshold detection	[$V_{O(REG)}$–V(BAT)] > $V_{(RCH)}$		75	100	135	mV
TIMERS(10)							
$V_{TMR(OFF)}$	Charge timer and termination enable threshold	Charge timer AND termination disabled at: $V_{(TMR)}$ > $V_{TMR(OFF)}$	bq24085/86/88	2.5	3	3.5	V
	Charge timer enable threshold	Charge timer disabled at: $V_{(TMR)}$ > $V_{TMR(OFF)}$	bq24087				
BATTERY DETECTION THRESHOLDS							
$I_{DET(DOWN)}$	Battery detection current (sink)	2 V < $V_{(BAT)}$ < $V_{O(REG)}$		1	2	3.2	mA
$I_{DET(UP)}$	Battery detection current (source)	2 V < $V_{(BAT)}$ < $V_{O(REG)}$			$I_{O(PRECHG)}$		mA
TIMER FAULT RECOVERY							
$I_{(FAULT)}$	Fault Current (source)	$V_{(OUT)}$ < $V_{(RCH)}$			0.8	1.1	mA
OUTPUT CURRENT SAFETY LIMIT(11)							
$I_{(SETSC)}$	Charge overcurrent safety	$V_{(ISET)}$ = VSS			1.5		A

(6) V(IN)–V(OUT) > V(DO-MAX) , V(IN) ≥ 4.5 V, charger enabled, no fault conditions detected, RTMR = 50 K or V(TMR)=OPEN; thermal regulation loop not active.
(7) Charger enabled, no fault conditions detected.
(8) $V_{O(REG)}$ = 4.2 V, charger enabled, no fault conditions detected, thermal regulation loop not active, R_{TMR} = 50 K or TMR pin open.
(9) The voltage on the ISET pin is compared to the $V_{(TERM)}$ voltage to determine when the termination should occur.
(10) $\overline{CE}$ = LO, charger enabled, no fault conditions detected, V(TMR) < 3 V, timers enabled.
(11) $V_{(IN)}$ ≥ 4.5 V, charger enabled, ISET shorted to GND.

7.6 Timing Requirements

over recommended operating range, T_J = 0 –125°C range, See the *Application and Implementation* section, typical values at T_J = 25°C (unless otherwise noted), R_{TMR} = 49.9 KΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER DOWN THRESHOLD – UNDERVOLTAGE LOCKOUT						
$t_{DGL(PG)}$	Deglitch time on power good	$\overline{V_{(IN)}}$ = 0 V → 5 V in 1 µs to $\overline{PG}$:HI → LO		2		ms
INPUT POWER DETECTION(1)						
$t_{DGL(NOIN)}$	Delay time, input power not detected status(2)	$\overline{PG}$: LO →HI after $t_{DGL(NOIN)}$			10	µs
$t_{DLY(CHGOFF)}$	Charger off delay	Charger turned off after $t_{DLY(CHGOFF)}$, Measured from $\overline{PG}$: LO → HI; Timer reset after $t_{DLY(CHGOFF)}$		25		ms
INPUT OVERVOLTAGE PROTECTION						
$t_{DGL(OVDET)}$	Input overvoltage detection delay	$\overline{CE}$ = HI or LO, Measured from $V_{(IN)}$ > $V_{(OVP)}$ to $\overline{PG}$: LO → HI; VIN increasing			100	µs
$t_{DGL(OVNDET)}$	Input overvoltage not detected delay(2)	$\overline{CE}$ = HI or LO, Measured from $V_{(IN)}$ < $V_{(OVP)}$ to $\overline{PG}$: HI → LO; V(IN) decreasing			100	µs
VOLTAGE AND CURRENT REGULATION TIMING(3)						
$t_{PWRUP(CHG)}$	Input power detection to full charge current time delay	Measured from $\overline{PG}$:HI → LO to $I_{(OUT)}$ > 100 mA, $\overline{CE}$ = LO, $I_{O(OUT)}$ = 750 mA, V(BAT) = 3.5 V		25		ms
$t_{PWRUP(EN)}$	Charge enable to full charge current delay	Measured from $\overline{CE}$:HI → LO to $I_{(OUT)}$ >100 mA, $I_{O(OUT)}$ = 750 mA, $V_{(BAT)}$= 3.5 V, $V_{(IN)}$ = 4.5 V, Input power detected		25		ms
$t_{PWRUP(LDO)}$	Input power detection to voltage regulation delay, LDO mode set, no battery or load connected	Measured from $\overline{PG}$:HI → LO to $V_{(OUT)}$ > 90% of charge voltage regulation; $V_{(TMR)}$ = OPEN, LDO mode set, no battery and no load at OUT pin, $\overline{CE}$ = LO		25		ms
CHARGE TERMINATION DETECTION(4)						
$t_{DGL(TERM)}$	Deglitch time, termination detected	$V_{(ISET)}$ decreasing		50		ms
BATTERY RECHARGE THRESHOLD						
$t_{DGL(RCH)}$	Deglitch time, recharge detection	$V_{(BAT)}$ decreasing		350		ms
TIMERS(5)						
$t_{(CHG)}$	Charge safety timer range	$t_{(CHG)}$ = $K_{(CHG)}$ × R_{TMR} ; thermal loop not active	3		10	hours
$K_{(CHG)}$	Charge safety timer constant	$V_{(BAT)}$ > $V_{(LOWV)}$	0.08	0.1	0.12	hr/kΩ
$t_{(PCHG)}$	Pre-charge safety timer range	$t_{(PCHG)}$ = $K_{(PCHG)}$ × $t_{(CHG)}$; Thermal regulation loop not active	1080		3600	s
$K_{(PCHG)}$	Pre-charge safety timer constant	$V_{(BAT)}$ < $V_{(LOWV)}$	0.08	0.1	0.12	
BATTERY DETECTION THRESHOLDS						
$t_{(DETECT)}$	Battery detection time	2 V < $V_{(BAT)}$ < $V_{O(REG)}$, Thermal regulation loop not active; R_{TMR} = 50 kΩ, $I_{DET(down)}$ or $I_{DET\ (UP)}$		125		ms

(1) $\overline{CE}$ = HI or LOW, $V_{(IN)}$ > 3.5 V
(2) Specified by design, not production tested.
(3) $V_{(IN)}$ > $V_{(OUT)}$ + $V_{(DO-MAX)}$, charger enabled, no fault conditions detected, R_{TMR} = 50 K or V(TMR) = OPEN; thermal regulation loop not active.
(4) $\overline{V_{O(REG)}}$ = 4.2 V, charger enabled, no fault conditions detected, thermal regulation loop not active, R_{TMR} = 50 K or TMR pin open.
(5) $\overline{CE}$ = LO, charger enabled, no fault conditions detected, V(TMR) < 3 V, timers enabled.

7.7 Dissipation Ratings(1)

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)
10-pin DRC	3.21	46.87

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2×3 via matrix.

7.8 Typical Characteristics

Measured using the typical application circuit shown previously.

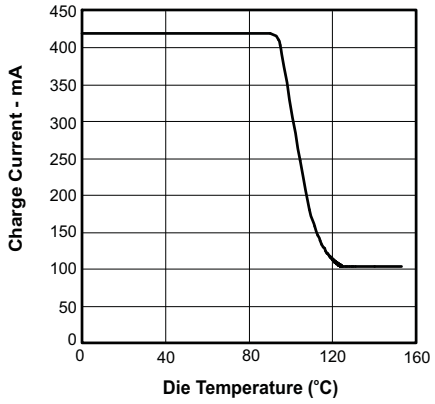


Figure 1. Thermal Regulation

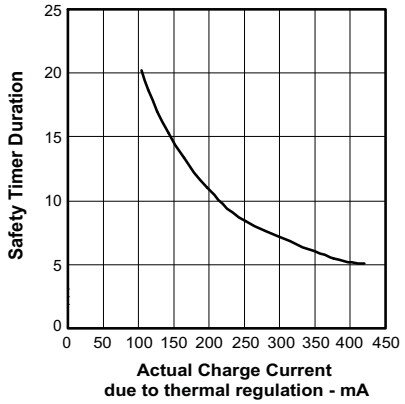


Figure 2. DTC Operation

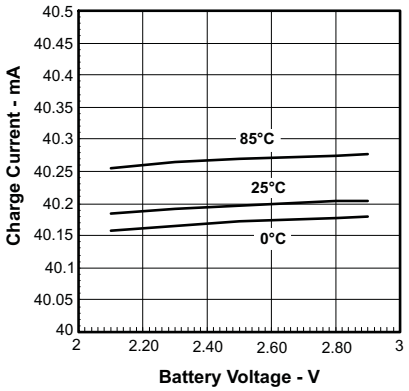


Figure 3. Pre-Charge Current vs Battery Voltage

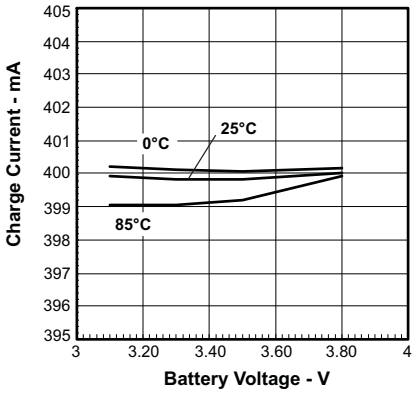


Figure 4. Fast-Charge Current vs Battery Voltage

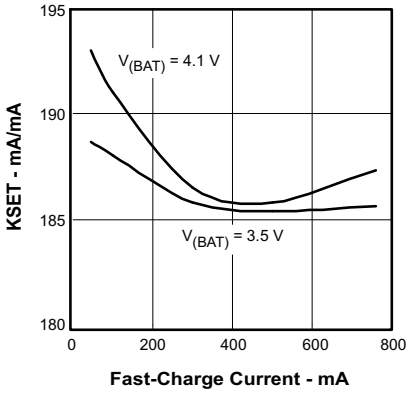


Figure 5. KSET Linearity vs Fast-Charge Current

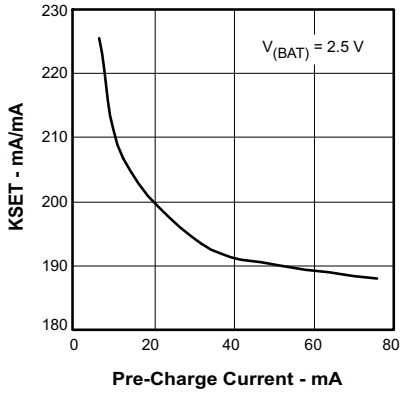


Figure 6. KSET Linearity vs Pre-Charge Current

Typical Characteristics (continued)

Measured using the typical application circuit shown previously.

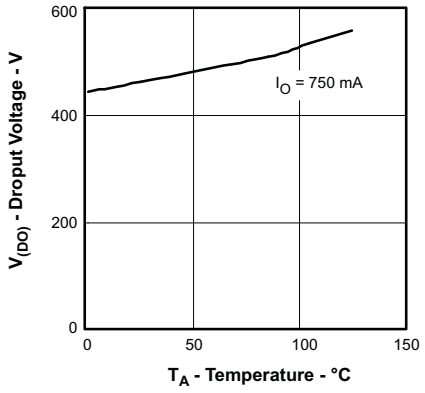


Figure 7. Dropout Voltage vs Temperature

8 Detailed Description

8.1 Overview

The charge current is programmable using external components (R_{ISET} resistor). The charge process starts when an external input power is connected to the system, the charger is enabled by $\overline{CE}$ = LO and the battery voltage is below the recharge threshold, V(BAT) < $V_{(RCH)}$. When the charge cycle starts a safety timer is activated, if the safety timer function is enabled. The safety timer timeout value is set by an external resistor connected to TMR pin.

When the charger is enabled two control loops modulate the battery switch drain to source impedance to limit the BAT pin current to the programmed charge current value (charge current loop) or to regulate the BAT pin voltage to the programmed charge voltage value (charge voltage loop). If $V_{(BAT)}$ < $V_{(LOWV)}$ (3 V typical) the BAT pin current is internally set to 10% of the programmed charge current value.

A typical charge profile for an operation condition that does not cause the IC junction temperature to exceed $T_{J(REG)}$, (112°C typical), is shown in Figure 8.

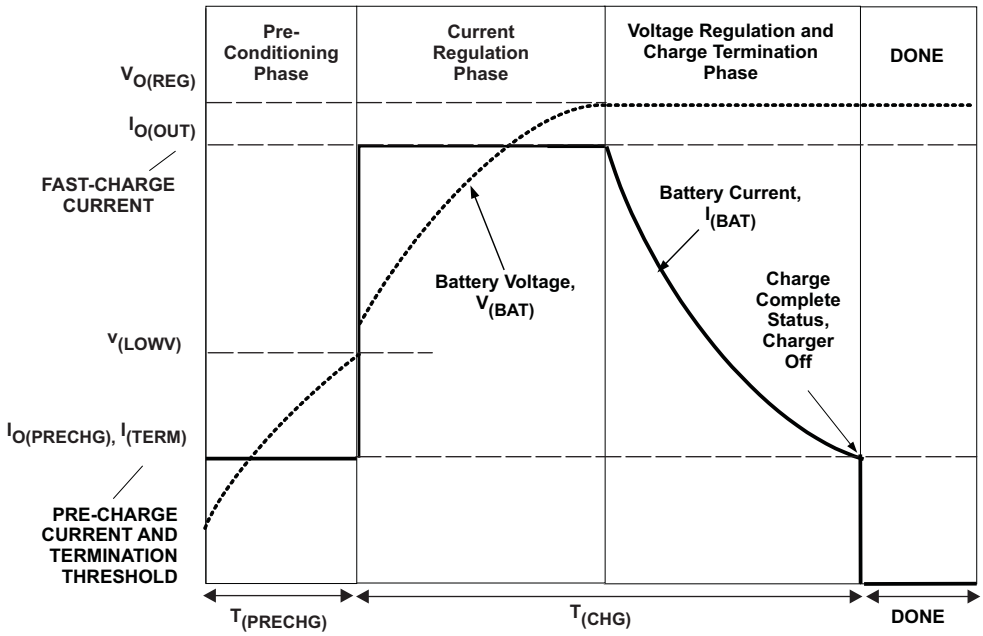


Figure 8. Charging Profile With $T_{J(REG)}$

If the operating conditions cause the IC junction temperature to exceed $T_{J(REG)}$, the charge cycle is modified, with the activation of the integrated thermal control loop. The thermal control loop is activated when a internal junction temperature monitoring voltage is lower than a fixed, temperature stable internal voltage. The junction temperature monitoring voltage is inversely proportional to the IC junction temperature. The thermal loop overrides the other charger control loops and reduces the charge current until the IC junction temperature returns to $T_{J(REG)}$, effectively regulating the IC junction temperature.

Overview (continued)

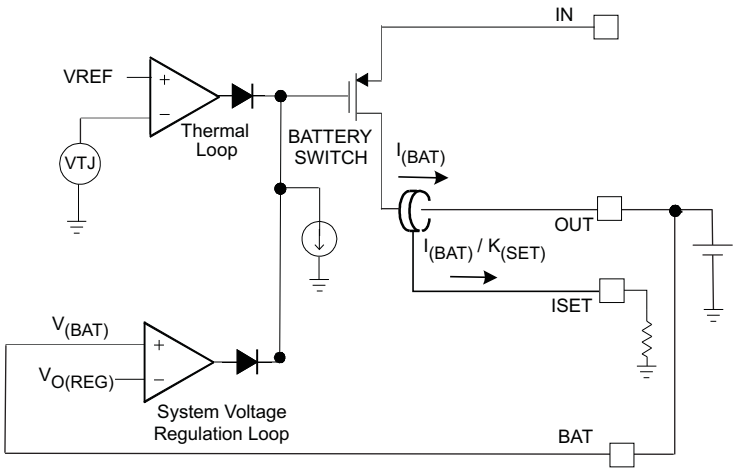


Figure 9. Thermal Regulation Circuit

A modified charge cycle, with the thermal loop active, is shown in Figure 10.

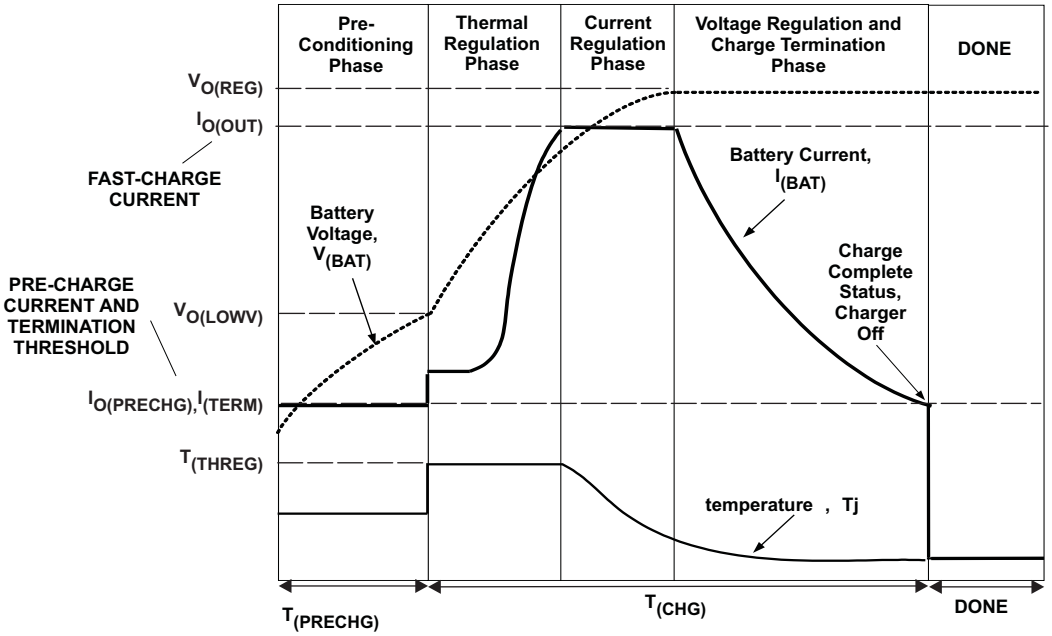
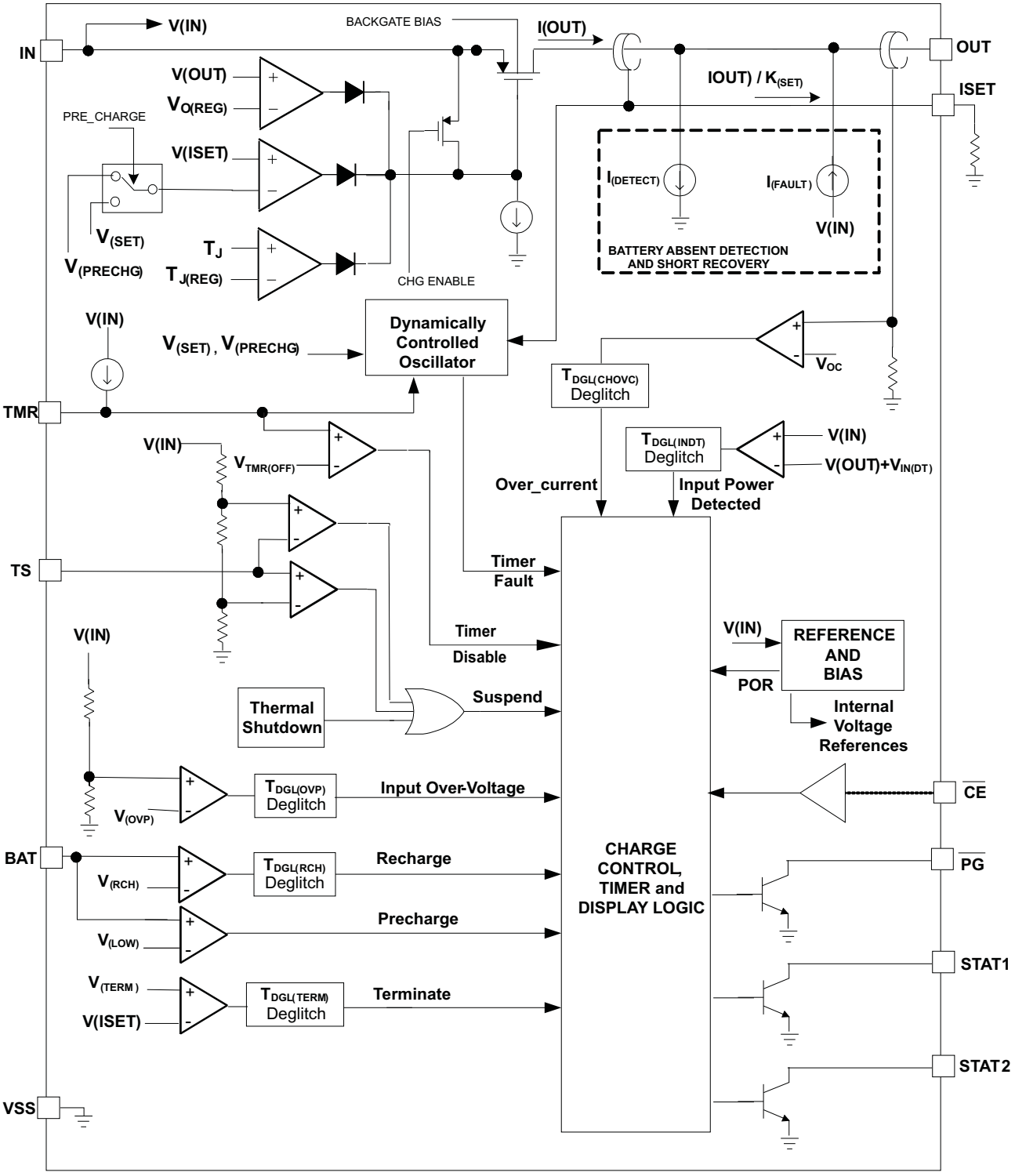


Figure 10. Charge Profile, Thermal Loop Active

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Control Logic Overview

An external host can enable or disable the charging process by using a dedicated control pin, $\overline{CE}$. A low-level signal on this pin enables the charge, and a high-level signal disables the charge. The bq24085/6/7/8 is in stand-by mode with $\overline{CE}$ = HI. When the charger function is enabled ($\overline{CE}$ = LO) a new charge is initiated.

Table 1 describes the charger control logic operation. In bq24085/6/7/8, the pack temperature status is internally set to OK without the TS pin.

Table 1. Control Logic Functionality

bq24085/6/7/8 OPERATION MODE	$\overline{CE}$	INPUT POWER	TIMER FAULT (latched)	OUTPUT SHORT CIRCUIT	TERMINATION (latched)	PACK TEMP	THERMAL SHUTDOWN	POWER DOWN	CHARGER POWER STAGE
POWER DOWN	LO	Low	X	X	X	X	X	Yes	***OFF***
SLEEP	X	Not Detected	X	X	X	X	X	No	***OFF***
STANDBY	HI	Detected	X	X	X	X	X	No	***OFF***
SEE STATE DIAGRAM	LO	Detected	X	Yes	X	X	X	No	
	LO	Detected	No	No	Yes	X	X	No	***OFF***
	LO	Detected	Yes	No	No	X	X	No	***IFAULT***
	LO	Detected	No	No	Yes	Absent	$T_J < T_{SHUT}$	No	***IDETECT***
	LO	Detected	No	No	No	Hot or Cold	$T_J < T_{SHUT}$	No	***OFF***
	LO	Detected	No	No	No	Ok	$T_J < T_{SHUT}$	No	***OFF***
	LO	Over Voltage	No	No	No	Ok	$T_J < T_{SHUT}$	No	***OFF***
CHARGING	LO	Detected	No	No	No	Ok	$T_J < T_{SHUT}$	No	***ON***

In both STANDBY and SUSPEND modes the charge process is disabled. In the STANDBY mode all timers are reset; in SUSPEND mode the timers are held at the count stored when the suspend mode was set.

The timer fault, termination and output short circuit variables shown in the control logic table are latched in the detection circuits, outside the control logic. Refer to the *Pre-Charge Timer*, *Dynamic Timer Function*, *Charge Safety Timer*, *Charge Termination Detection and Recharge*, and *Short-Circuit Protection* sections for additional details on how those latched variables are reset.

8.3.2 Temperature Qualification (Applies Only to Versions With TS Pin Option)

The bq24085/6/7/8 devices continuously monitor the battery temperature by measuring the voltage between the TS and VSS pins. The IC compares the voltage on the TS pin against the internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds is detected, the IC immediately suspends the charge. The IC suspends charge by turning off the power FET and holding the timer value (that is, timers are NOT reset). Charge is resumed when the temperature returns to the normal range.

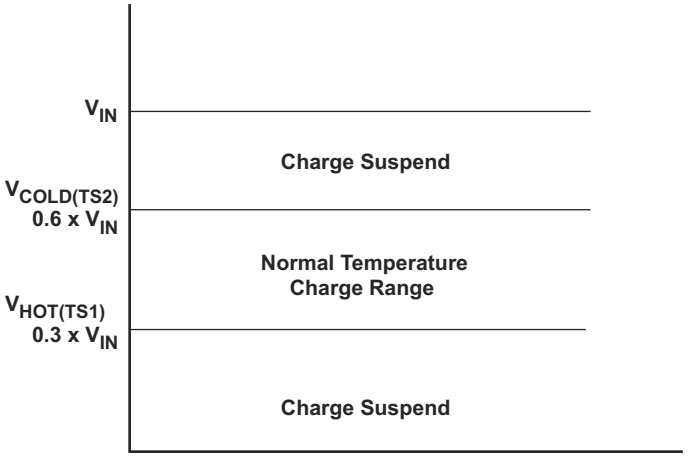


Figure 11. Battery Temperature Qualification With NTC Thermistor

The external resistors R_{T1} and R_{T2} (see Figure 18) enable selecting a temperature window. If R_{TC} and R_{TH} are the thermistor impedances for the Cold and Hot thresholds the values for R_{T1} and R_{T2} can be calculated as follows for a NTC (negative temperature coefficient) thermistor. Solve for R_{T2} first and substitute into R_{T1} equation. R_{TC} and R_{TH} can be found in the NTC thermistor datasheet specification.

$$R_{T2} = \frac{2.5 R_{TC} R_{TH}}{R_{TC} - 3.5 R_{TH}} \quad (1)$$

$$R_{T1} = \frac{7 R_{TH} R_{T2}}{3\left[R_{TH} + R_{T2}\right]} \quad (2)$$

Applying a fixed voltage, 1/2 Vin (50% resistor divider from Vin to ground), to the TS pin to disable the temperature sensing feature.

8.3.3 Input Overvoltage Detection, Power Good Status Output

The input power detection status for pin IN is shown at the open collector output pin $\overline{PG}$.

Table 2. Input Power Detection Status

INPUT POWER DETECTION (IN)	$\overline{PG}$ STATE
NOT DETECTED	High impedance
DETECTED, NO OVERVOLTAGE	LO
DETECTED, OVERVOLTAGE	High impedance

The bq24085/6/7/8 detects an input overvoltage when $V_{(IN)} > V_{(OVP)}$. When an overvoltage protection is detected the charger function is turned off and the bq24085/6/7/8 is set to standby mode of operation. Since the OVP detection is not latched, the IC returns to normal operation when fault condition is removed.

8.3.4 Charge Status Outputs

The open-collector STAT1 and STAT2 outputs indicate various charger operations as shown in Table 3. These status pins can be used to drive LEDs or communicate to the host processor.

NOTE

OFF indicates the open-collector transistor is turned off. When termination is disabled (TMR pin floating, or $\overline{TE}$ = Hi for bq24087) the Done state is not available; the status LEDs indicate fast charge if $V_{(BAT)} > V_{(LOWV)}$ and precharge if $V_{(BAT)} < V_{(LOWV)}$. The available output current is a function of the OUT pin voltage, See Figure 16.

Table 3. Charge Status(1)

Charge State	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Done (termination enabled only)	OFF	ON
Charge Suspend (temperature)	OFF	OFF
Timer Fault		
Charger off		
Selected Input power overvoltage detected		
Battery absent		
Batteryshort		

(1) Pulse loading on the OUT pin may cause the IC to cycle between Done and charging states (LEDs *Flashing*)

8.3.5 Battery Charging: Constant Current Phase

The bq24085/6/7/8 family offers on-chip current regulation. The current regulation is defined by the value of the resistor connected to ISET pin.

During a charge cycle the fast charge current $I_{O(OUT)}$ is applied to the battery if the battery voltage is above the $V_{(LOWV)}$ threshold (2.95 V typical):

$$I(OUT) = I_{O(OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{ISET}} \quad (3)$$

where

- $K_{(SET)}$ is the output current set factor and $V_{(SET)}$ is the output current set voltage.

During a charge cycle if the battery voltage is below the $V_{(LOWV)}$ threshold a pre-charge current $I_{(PRECHG)}$ is applied to the battery. This feature revives deeply discharged cells.

$$I(OUT) = I_{(PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{ISET}} \sim \frac{I_{O(OUT)}}{10} \quad (4)$$

where

- $K_{(SET)}$ is the output current set factor and $V_{(PRECHG)}$ is the precharge set voltage.

At low constant current charge currents, less than 200 mA, TI recommends that a 0.1-µF capacitor be placed between the ISET and BAT pins to insure stability.

8.3.6 Charge Current Translator

When the charge function is enabled, internal circuits generate a current proportional to the charge current at the ISET pin. This current, when applied to the external charge current programming resistor R_{ISET} generates an analog voltage that can be monitored by an external host to calculate the current sourced from the OUT pin.

$$V(ISET) = I(OUT) \times \frac{R_{ISET}}{K_{(SET)}} \quad (5)$$

8.3.7 Battery Voltage Regulation

The battery pack voltage is sensed through the BAT pin, which is tied directly to the positive side of the battery pack. The bq24085/6/7/8 monitors the battery pack voltage between the BAT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold, the battery charging enters the voltage regulation phase, and charging current begins to taper down. The voltage regulation threshold $V_{O(REG)}$ is fixed by an internal IC voltage reference.

8.3.8 Pre-Charge Timer

The bq24085/6/7/8 family activates an internal safety timer during the battery pre-conditioning phase. The charge safety timer time-out value is set by the external resistor connected to TMR pin, R_{TMR}, and the timeout constants $K_{(PCHG)}$ and $t_{(CHG)}$:

$$t_{(PCHG)} = K_{(PCHG)} \times t_{(CHG)} \quad (6)$$

The pre-charge timer operation is detailed in Table 4.

Table 4. Pre-Charge Timer Operational Modes

bq24085/6/7/8 MODE	V(OUT) > $V_{(LOWV)}$	PRE-CHARGE TIMER MODE
STANDBY ($\overline{CE}$ = Hi)	X	***RESET***
CHARGING	Yes	***RESET***
SUSPEND (TS out of range)	Yes	***RESET***
SUSPEND (TS out of range)	No	***Hold***
CHARGING, TMR PIN NOT OPEN	No	***COUNTING, EXTERNAL PROGRAMMED RATE***
CHARGING, TMR PIN OPEN	X	***RESET***

In SUSPEND mode the pre-charge timer is put on hold (that is, pre-charge timer is not reset). Once normal operation resumes when the timer returns to the normal operating mode (COUNTING). If $V_{(BAT)}$ does not reach the internal voltage threshold $V_{(LOWV)}$ within the pre-charge timer period, a fault condition is detected. The charger is then turned off, and the pre-charge safety timer fault condition is latched.

When the pre-charge timer fault latch is set the charger is turned off. Under these conditions a small current I_{FAULT} is applied to the OUT pin, as long as input power (IN) is detected **AND** $V_{(OUT)} < V_{(LOWV)}$, as part of a timer fault recovery protocol. This current allows the output voltage to rise above the pre-charge threshold $V_{(LOWV)}$, resetting the pre-charge timer fault latch when the pack is removed. Table 5 further details the pre-charge timer fault latch operation.

Table 5. Pre-Charge Timer Latch Functionality

PRE-CHARGE TIMER FAULT ENTERED WHEN	PRE-CHARGE TIMER FAULT LATCH RESET AT
Pre-charge timer timeout **AND** $V_{(OUT)} < V_{(LOW\ V)}$	$\overline{CE}$ rising edge or OVP detected
	Input power removed (not detected)
	Timer function disabled

8.3.9 Thermal Protection Loop

An internal control loop monitors the bq24085/6/7/8 junction temperature (T_J) to ensure safe operation during high power dissipations and increased ambient temperatures. This loop monitors the bq24085/6/7/8 junction temperature and reduces the charge current as necessary to keep the junction temperature from exceeding, $T_{J(REG)}$, (112°C, typical).

The bq24085/6/7/8's thermal loop control can reduce the charging current down to approximately 105 mA if needed. If the junction temperature continues to rise, the IC will enter thermal shutdown.

8.3.10 Thermal Shutdown And Protection

Internal circuits monitor the junction temperature, T_J, of the die and suspends charging if T_J exceeds an internal threshold $T_{(SHUT)}$ (155°C typical). Charging resumes when T_J falls below the internal threshold $T_{(SHUT)}$ by approximately 20°C.

8.3.11 Dynamic Timer Function

The charge and pre-charge safety timers are programmed by the user to detect a fault condition if the charge cycle duration exceeds the total time expected under normal conditions. The expected charge time is usually calculated based on the fast charge current rate.

When the thermal loop is activated the charge current is reduced, and bq24085/6/7/8 activates the dynamic timer control. The dynamic timer control is an internal circuit that slows down the safety timer's clock frequency. The dynamic timer control circuit effectively extends the safety time duration for either the precharge or fast charge timer modes. This minimizes the chance of a safety timer fault due to thermal regulation.

The bq24085/6/7/8 dynamic timer control (DTC) monitors the voltage on pin ISET during pre-charge and fast charge, and if in thermal regulation slows the clock frequency proportionately to the change in charge current. The time duration is based on a 2^{24} ripple counter, so slowing the clock frequency is a real time correction. The DTC circuit changes the safety timers clock period based on the $V_{(SET)}/V_{(ISET)}$ ratio (fast charge) or $V_{(PRECHG)}/V_{(SET)}$ ratio (pre-charge). Typical safety timer multiplier values relative to the $V_{(SET)}/V_{(ISET)}$ ratio is shown in Figure 12 and Figure 13.

The device deglitch timers are set by the same oscillators as the safety and precharge timers. In thermal regulation, the timers are scaled appropriately, see Figure 2.

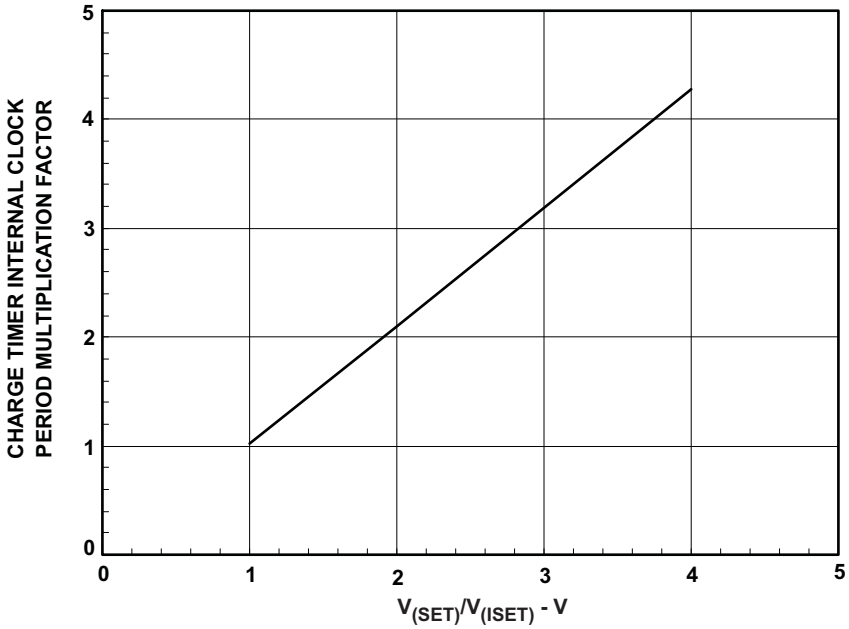


Figure 12. Safety Timer Linearity Internal Clock Period Multiplication Factor

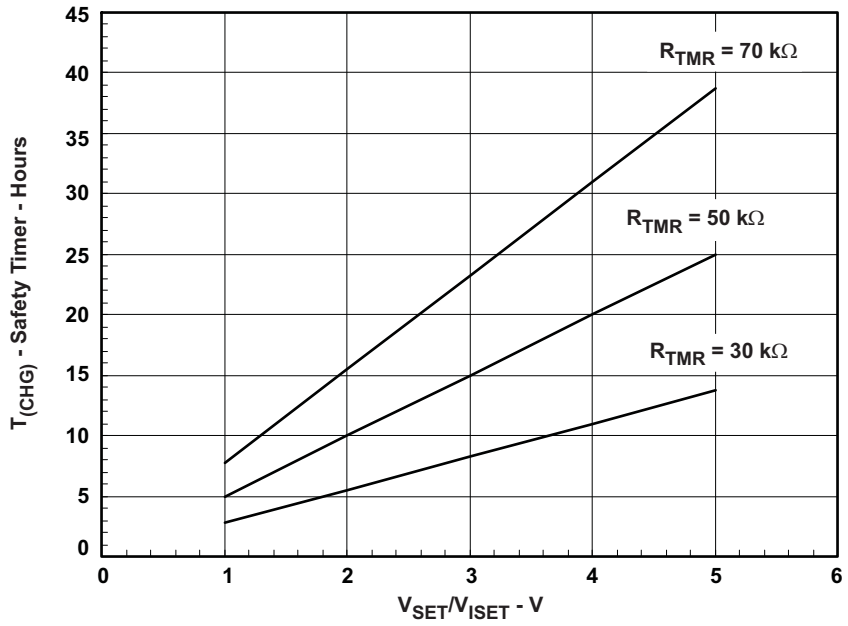


Figure 13. bq24085/6/78 Safety Timer Linearity for R_{TMR} Values

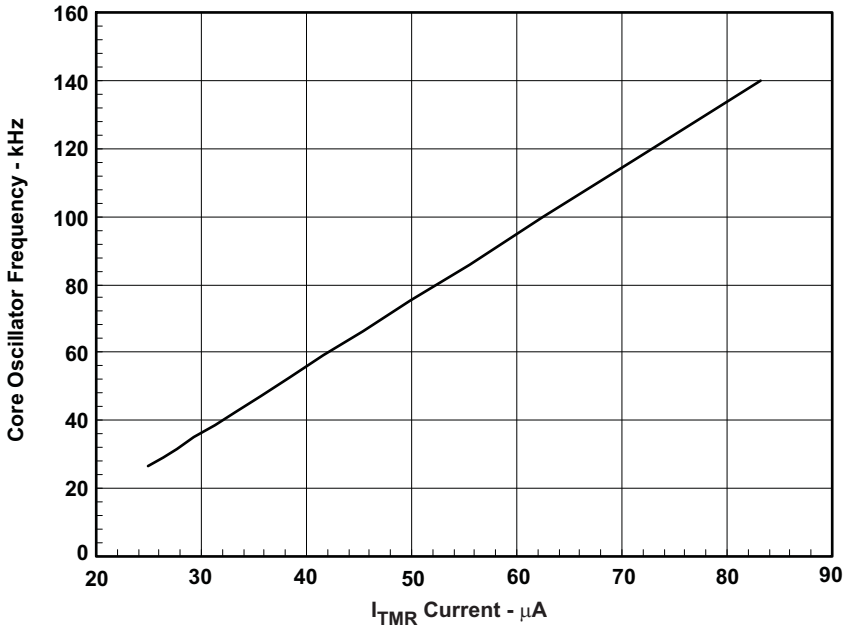


Figure 14. bq24085/6/7/8 Oscillator Linearity vs I_{TMR}
R_{TMR} 30 KΩ – 100 KΩ

8.3.12 Charge Termination Detection and Recharge

The charging current is monitored during the voltage regulation phase. Charge termination is indicated at the STATx pins (STAT1 = Hi-Z; STAT2 = Low) once the charge current falls below the termination current threshold $I_{(TERM)}$. A deglitch period $t_{DGL(TERM)}$ is added to avoid false termination indication during transient events.

Charge termination is not detected if the charge current falls below the termination threshold as a result of the thermal loop activation. Termination is also not detected when charger enters the suspend mode, due to detection of invalid pack temperature or internal thermal shutdown.

Table 6 describes the termination latch functionality.

Table 6. Termination Latch Functionality

TERMINATION DETECTED LATCHED WHEN	TERMINATION LATCH RESET AT
$I_{(OUT)} < I_{(TERM)}$ **AND** $t > t_{DGL(TERM)}$ **AND** $V_{(OUT)} > V_{(RCH)}$	$\overline{CE}$ rising edge or OVP detected
	New charging cycle started; see state diagram
	Termination disabled

The termination function is DISABLED:

1. In bq24085/6/7/8 the termination is disabled when the TMR pin is left open (floating).
2. In bq24087, leaving the TMR pin open (floating) does not disable the termination. The only way to disabled termination in bq24087 is to have $\overline{TE}$ = high.
3. Thermal regulation or thermal shutdown.
4. Invalid battery pack temperature (TS fault).

8.3.13 Battery Absent Detection – Voltage Mode Algorithm

The bq24085/6/7/8 provides a battery absent detection scheme to reliably detect insertion and removal of battery packs. The detection circuit applies an internal current to the battery terminal, and detects battery presence based on the terminal voltage behavior. Figure 15 has a typical waveform of the output voltage when the battery absent detection is enabled and no battery is connected.

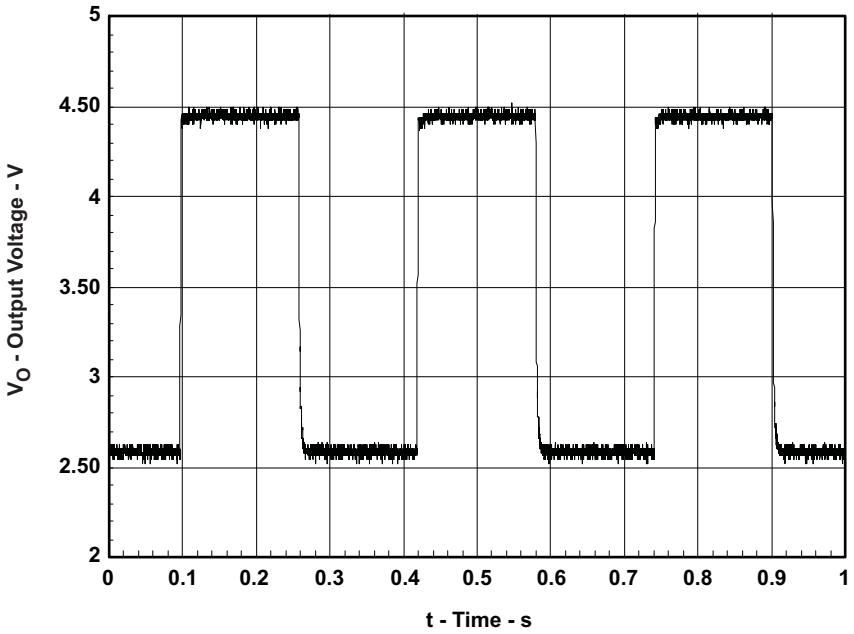


Figure 15. Battery-Absent Detection Waveforms

The battery absent detection function is disabled if the voltage at the BAT pin is held above the battery recharge threshold, $V_{(RCH)}$, after termination detection. When the voltage at the BAT pin falls to the recharge threshold, either by connection of a load to the battery or due to battery removal, the bq24085/6/7/8 begins a battery absent detection test. This test involves enabling a detection current, $I_{DET(DOWN)}$, for a period of $t_{(DETECT)}$ and checking to see if the battery voltage is below the pre-charge threshold, $V_{(LOWV)}$. Following this, the precharge current, $I_{DET(UP)}$ is applied for a period of $t_{(DETECT)}$ and the battery voltage checked again to be above the recharge threshold.

Passing both of the discharge and charging tests (battery terminal voltage being below the pre-charge and above the recharge thresholds on the battery detection test) indicates a battery absent fault at the STAT1 and STAT2 pins. Failure of either test starts a new charge cycle. For the absent battery condition, the voltage on the BAT pin rises and falls between the $V_{(LOWV)}$ and $V_{O(REG)}$ thresholds indefinitely. See the *Operational Flow Chart*, Figure 17, for more details on this algorithm. If it is desired to power a system load without a battery, TI recommends to float the TMR pin which puts the charger in *LDO mode* (disables termination).

The battery absent detection function is disabled when the termination is disabled.

After termination, the bq24085/6/7/8 provides a small battery leakage current, $I_{BAT(DONE)}$ (1 µA typical), to pull down the BAT pin voltage in the event of battery removal. If the leakage on the OUT pin is higher than this pulldown current, then the voltage at the pin remains above termination and a battery-absent state will not be detected. This problem is fixed with the addition of a pulldown resistor of 2 MΩ to 4 MΩ from the OUT pin to VSS. A resistor too small (< 2 MΩ) can cause the OUT pin voltage to drop below the $V_{(LOWV)}$ threshold before the recharge deglitch (typical 25 ms) expires, causing a fault condition. In this case, the bq24085/6/7/8 provides a fault current (typical 750 µA) to pull the pin above the termination threshold.

8.3.14 Charge Safety Timer

As a protection mechanism, the bq24085/6/7/8 has a user-programmable timer that monitors the total fast charge time. This timer (charge safety timer) is started at the beginning of the fast charge period. The safety charge timeout value is set by the value of an external resistor connected to the TMR pin (R_{TMR}); if pin TMR is left open (floating) the charge safety timer is disabled.

Use Equation 7 to calculate the charge safety timer time-out value:

$$t_{(CHG)} = [K_{(CHG)} \times R_{(TMR)}] \quad (7)$$

The safety timer operation modes are shown in Table 7

Table 7. Charge Safety Timer Operational Modes

bq24085/6/7/8	V(OUT) > $V_{(LOWV)}$	CHARGE SAFETY TIMER MODE
STANDBY	X	***RESET***
CHARGING	No	***RESET***
SUSPEND	No	***RESET***
SUSPEND	Yes	***SUSPEND***
CHARGING, TMR PIN NOT OPEN	Yes	***COUNTING***
CHARGING, TMR PIN OPEN	X	***RESET***

In SUSPEND mode, the charge safety timer is put on hold (that is, charge safety timer is not reset), normal operation resumes when the TS fault is removed and the timer returns to the normal operating mode (COUNTING). If charge termination is not reached within the timer period, a fault condition is detected. Under those circumstances, the LED status is updated to indicate a fault condition and the charger is turned off.

When the charge safety timer fault latch is set and the charger is turned off, a small current IFAULT is applied to the OUT pin, as long as input power (IN) is detected **AND** $V_{(OUT)} < V_{(RCHG)}$, as part of a timer fault recovery protocol. This current allows the output voltage to rise above the recharge threshold $V_{(RCHG)}$ if the pack is removed, and assures that the charge safety timer fault latch is reset if the pack is removed and re-inserted. Table 8 further details the charge safety timer fault latch operation.

Table 8. Charge Safety Timer Latch Functionality

CHARGE SAFETY TIMER FAULT ENTERED	CHARGE SAFETY TIMER FAULT LATCH RESET AT
$V_{(OUT)} > V_{(LOW\ V)}$	$\overline{CE}$ rising edge, or OVP detected
	Input power removed (not detected)
	New charging cycle started; see state diagram

8.3.15 Short-Circuit Protection

The internal comparators monitor the battery voltage and detect when a short circuit is applied to the battery terminal. If the voltage at the BAT pin is less than the internal threshold $V_{(SCIND)}$ (1.8 V typical), the STAT pins indicate a fault condition (STAT1 = STAT2 = Hi-Z). When the voltage at the BAT pin falls below a second internal threshold $V_{(SC)}$ (1.4 V typical), the charger power stage is turned off. A recovery current, $I_{(SHORT)}$ (15 mA typical), is applied to the BAT pin, enabling detection of the short circuit removal. The battery output current versus battery voltage is shown in the graph, Figure 16.

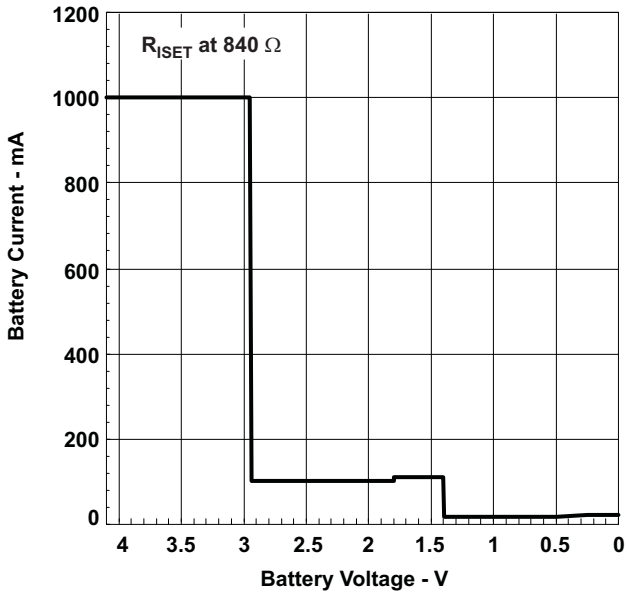


Figure 16. bq24085/6/7/8 Short Circuit Behavior

See the *Application and Implementation* section for additional details on start-up operation with $V_{(BAT)} < V_{(SC)}$.

8.3.16 Startup With Deeply Depleted Battery Connected

The bq24085/6/7/8 charger furnishes the programmed charge current if a battery is detected. If no battery is connected the bq24085/6/7/8 operates as follows:

- The output current is limited to 15 mA (typical), if the voltage at BAT pin is below the short circuit detection threshold $V_{(SC)}$, 1.8 V typical.
- The output current is regulated to the programmed pre-charge current if $V_{(SC)} < V_{(BAT)} < V_{(LOWV)}$.
- The output current is regulated to the programmed fast charge current If $V_{(BAT)} > V_{(LOWV)}$ **AND** voltage regulation is not reached.

The output voltage collapses if no battery is present and the end equipment requires a bias current larger than the available charge current.

8.4 Device Functional Modes

8.4.1 Power Down

The bq24085/6/7/8 family is in a power-down mode when the input power voltage (IN) is below the power-down threshold $V_{(PDWN)}$. During the power-down mode all IC functions are off, and the host commands at the control pins are not interpreted. The integrated power MOSFET connected between IN and OUT pins is off, the status output pins STAT1 and STAT2 are set to high impedance mode and $\overline{PG}$ output is set to the high impedance state.

8.4.2 Sleep Mode

The bq24085/6/7/8 enters the sleep mode when the input power voltage (IN) is above the power-down threshold V(PDWN) but still lower than the input power detection threshold, V(IN) < V(OUT) + $V_{IN(DT)}$.

During the sleep mode the charger is off, and the host commands at the control pins are not interpreted. The integrated power mosfet connected between IN and OUT pins is off, the status output pins STAT1 and STAT2 are set to the high impedance state and the $\overline{PG}$ output indicates input power not detected.

The sleep mode is entered from any other state, if the input power (IN) is not detected.

8.4.3 Overvoltage Lockout

The input power is detected when the input voltage V(IN) > V(OUT) + $V_{IN(DT)}$. When the input power is detected the bq24085/6/7/8 transitions from the sleep mode to the power-on-reset mode. In this mode of operation, an internal timer $T_{(POR)}$ is started and internal blocks are reset (power-on-reset). Until the timer expires, the STAT1 and STAT2 outputs indicate charger OFF, and the $\overline{PG}$ output indicates the input power status as not detected.

At the end of the power-on-reset delay, the internal comparators are enabled, and the STAT1, STAT2 and $\overline{PG}$ pins are active.

8.4.4 Stand-By Mode

In the bq24085/6/7/8, the stand-by mode is started at the end of the power-on-reset phase, if the input power is detected and $\overline{CE}$ = HI. In the stand-by mode, selected blocks in the IC are operational, and the control logic monitors system status and the control pins to define if the charger will be set to ON or OFF mode. The quiescent current required in stand-by mode is 100 µA typical.

If the $\overline{CE}$ pin is not available, the bq24085/6/7/8 enters the begin charge mode at the end of the power-on-reset phase.

8.4.5 Begin Charge Mode

All blocks in the IC are powered up, and the bq24085/6/7/8 is ready to start charging the battery pack. A new charge cycle is started when the control logic decides that all conditions required to enable a new charge cycle are met. During the begin charge phase all timers are reset, then the IC enters the charging mode.

Device Functional Modes (continued)

8.4.6 Charging Mode

When the charging mode is active, the bq24085/6/7/8 executes the charging algorithm, as described in the *Operational Flow Chart*, Figure 17.

8.4.7 Suspend Mode

The suspend mode is entered when the pack temperature is not within the valid temperature range. During the suspend mode, the charger is set to OFF, but the timers are not reset.

The normal charging mode resumes when the pack temperature returns to the valid temperature range.

8.4.8 LDO Mode Operation

The *LDO Mode* (TMR pin open circuit) disables the charging termination circuit, disables the battery detect routine and holds the safety timer clock in reset. This is often used for operation without a battery or in production testing. This mode is different than a typical LDO since it has different modes of operation, and delivers less current at lower output voltages. See Figure 16 for the output current versus the output voltage.

NOTE

A load on the output prior to powering the device may keep the part in short-circuit mode. Also, during normal operation, exceeding the programmed fast charge level causes the output to drop, further restricting the output power, and soon ends up in short-circuit mode.

Operation with a battery or keeping the average load current below the programmed current level prevents this type of latch up. The OUT pin current can be monitored through the ISET pin. If the device is in LDO mode and battery is absent, TI recommends to use a 350-Ω feedback resistor between the BAT and OUT pins.

Device Functional Modes (continued)

8.4.9 State Machine Diagram

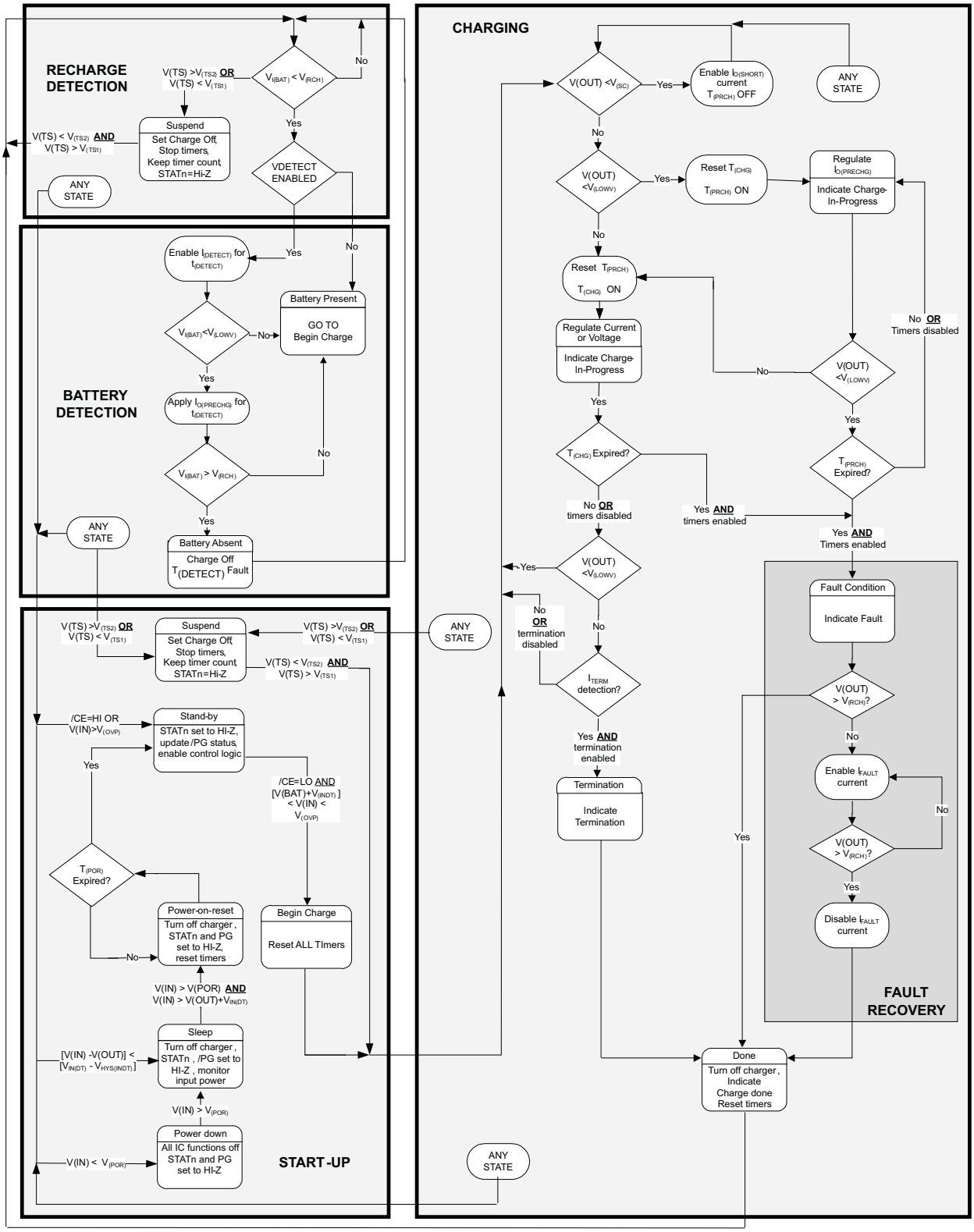


Figure 17. Operational Flow Chart

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq24085/6/7/8 series are highly integrated Li-Ion and Li-Pol linear chargers, targeted at space-limited portable applications. The battery is charged in three phases: conditioning, constant or thermally regulated current, and constant voltage. An internal programmable charge timer provides a backup protection feature for charge termination and is dynamically adjusted during the thermal regulation phase.

9.2 Typical Applications

The typical application diagrams shown here are configured for 400 mA fast charge current, 40 mA pre-charge current, 5 hour safety timer and 30 min pre-charge timer.

9.2.1 bq24086 and bq24088 Typical Application

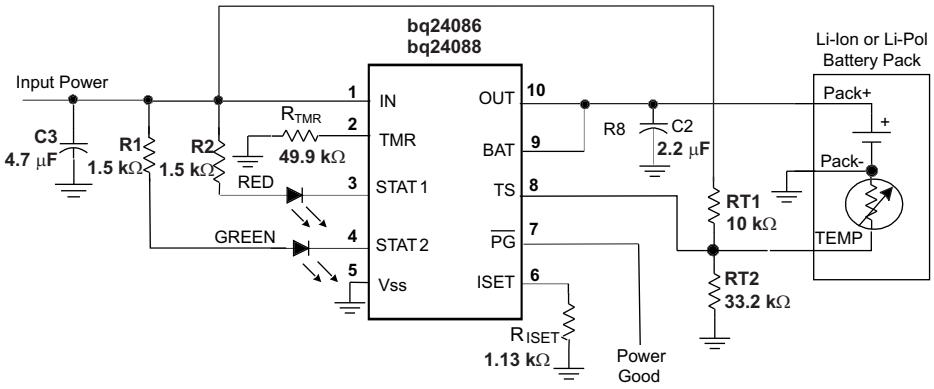


Figure 18. bq24086 and bq24088 Application Schematic

9.2.1.1 Design Requirements

- Supply voltage = 5 V
- Safety timer duration of 5 hours for fast charge
- Fast charge current of approximately 400 mA
- Battery temp sense is not used

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Selecting Input and Output Capacitor

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. A 1-µF ceramic capacitor, placed in close proximity to the IN pin and GND pad, works fine. In some applications, depending on the power supply characteristics and cable length, it may be necessary to increase the input filter capacitor to avoid exceeding the IN pin maximum voltage rating during adapter hot plug events.

The bq2408x, at low charge currents, requires a small output capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the BAT and ISET pad is typically sufficient.

Typical Applications (continued)

9.2.1.2.2 Using Adapters With Large Output Voltage Ripple

Some low cost adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with low cost adapters under those conditions the bq2408x family keeps the charger on for at least 25 msec (typical) after the input power puts the part in sleep mode. This feature enables use of external low cost adapters using 50-Hz networks.

The backgate control circuit prevents any reverse current flowing from the battery to the adapter terminal during the charger off delay time.

NOTE

The $\overline{PG}$ pin is not deglitched, and it indicates input power loss immediately after the input voltage falls below the output voltage. If the input source frequently drops below the output voltage and recovers, a small capacitor can be used from $\overline{PG}$ to VSS to prevent $\overline{PG}$ flashing events.

9.2.1.2.3 Calculations

Program the charge current for 400 mA:

$$R_{(ISET)} = [V_{(SET)} \times K_{(SET)} / I_{(OUT)}]$$

where

- from the *Electrical Characteristics* table. . . $V_{(SET)} = 2.5$ V
- from the *Electrical Characteristics* table. . . $K_{(SET)} = 182$ (8)

$$R_{(ISET)} = [2.5\ V \times 187 / 0.4\ A] = 1137\ \Omega \quad (9)$$

Selecting the closest standard value, use a 1.13-kΩ resistor connected between ISET (pin 6) and ground.

Program 5-hour safety timer timeout:

$$R_{(TMR)} = [T_{(CHG)} / K_{(CHG)}]$$

where

- from the *Electrical Characteristics* table. . . $K_{(CHG)} = 0.1$ hr / kΩ (10)

$$K_{(TMR)} = [5\ hrs / (0.1\ hr / k\Omega)] = 50\ k\Omega \quad (11)$$

Selecting the closest standard value, use a 49.9-kΩ resistor connected between TMR (pin 2) and ground.

Disable the temp sense function:

A constant voltage between V_{TS1} and V_{TS2} on the TS input disables the temp sense function.

from the *Electrical Characteristics* table. . . $V_{(TS1)} = 30\% \times V_{IN}$

from the *Electrical Characteristics* table. . . $V_{(TS2)} = 61\% \times V_{IN}$

A constant voltage of 50% × Vin disables the temp sense function, so a divide-by-2 resistor divider connected between Vin and ground can be used. Two 1-MΩ resistors keeps the power dissipated in this divider to a minimum.

For a 0 to 45°C range with a Semitec 103AT thermistor, the thermistor values are 4912 at 45°C and 27.28 k at 0°C. RT1 (top resistor) and RT2 (bottom resistor) are calculated in Equation 12:

$$R_{T2} = \frac{2.5\ R_{TC}R_{TH}}{R_{TC} - 3.5R_{TH}} = \frac{2.5\ (27.28k)\ (4.912k)}{27.28k - 3.5(4.912k)} = 33.2k$$

$$R_{T1} = \frac{7\ R_{TH}R_{T2}}{3\ (R_{TH} + R_{T2})} = \frac{7\ (4.921k)\ (33.2k)}{3\ (4.921k + 33.2k)} = 10k \quad (12)$$

Typical Applications (continued)

PIN	COMPONENTS
IN	In most applications, the minimum input capacitance needed is a 0.1-µF ceramic decoupling capacitor near the input pin connected to ground (preferably to a ground plane through vias). The recommended amount of input capacitance is 1 µF or at least as much as on the output pin. This added capacitance helps with hot plug transients, input inductance and initial charge transients.
OUT	There is no minimum value for capacitance for this output, but TI recommends to connect a 1-µF ceramic capacitor between OUT and ground. This capacitance helps with termination, and cycling frequency between *charge done* and refresh charge when no battery is present. It also helps cancel out any battery lead inductance for long leaded battery packs. TI also recommends to put as much ceramic capacitance on the input as the output so as not to cause a drop out of the input when charging is initiated.
ISET/BAT	For stability reasons, it may be necessary to put a 0.1-µF capacitor between the ISET and BAT pin..
STAT1/2 and $\overline{PG}$	Optional (LED STATUS – See below, Processor Monitored; or no status)
STAT1	Connect the cathode of a red LED to the open-collector STAT1 output, and connect the anode of the red LED to the input supply through a 1.5-kΩ resistor that limits the current.
STAT2	Connect the cathode of a green LED to the open-collector STAT2 output, and connect the anode of the green LED to the input supply through a 1.5-kΩ resistor that limits the current.
$\overline{PG}$	Connect the cathode of an LED to the open-collector $\overline{PG}$ output, and connect the anode of the LED to the input supply through a 1.5-kΩ resistor to limit the current.

9.2.1.3 Application Curves

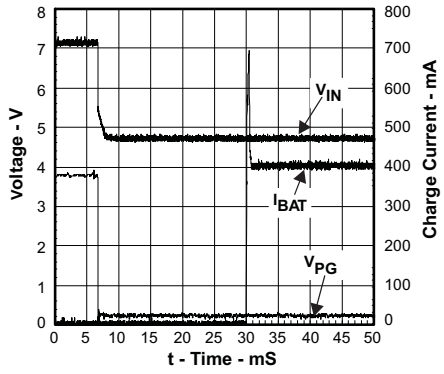


Figure 19. Input OVP Recovery Transients

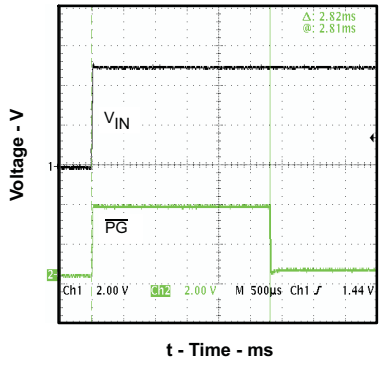


Figure 20. PG Deglitch Time

Typical Applications (continued)

9.2.2 bq24085 Typical Application

Figure 21 illustrates the typical application circuit for bq24085.

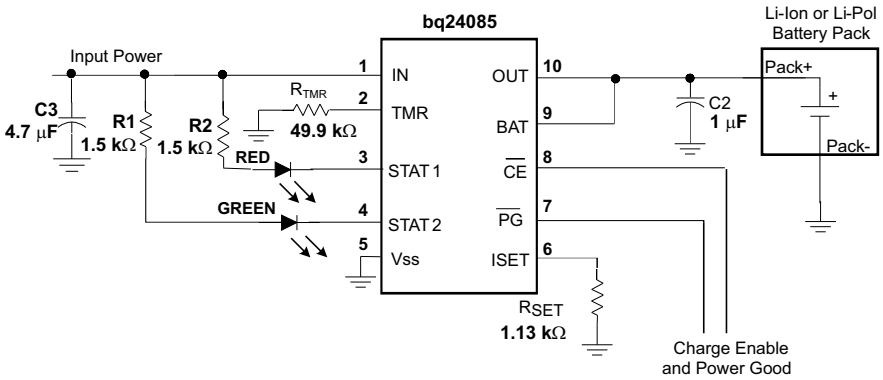


Figure 21. bq24085 Application Schematic

9.2.2.1 Design Requirements

Follow the design requirements in *bq24086 and bq24088 Typical Application*.

9.2.3 bq24087 Typical Application

Figure 22 shows the typical application circuit for bq24087.

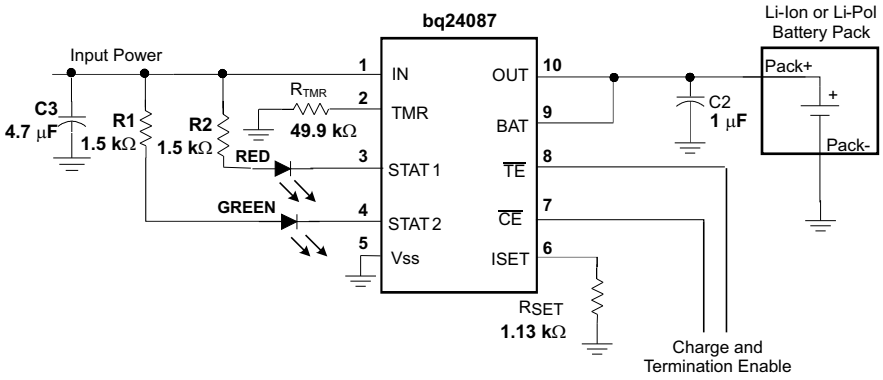


Figure 22. bq24087 Application Schematic

9.2.3.1 Design Requirements

Follow the design requirements in *bq24086 and bq24088 Typical Application*.

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.5 V and 6.5 V and current capability of at least the maximum designed charge current. This input supply should be well regulated. If located more than a few inches from the bq24085/6/7/8 IN and GND terminals, a larger capacitor is recommended.

11 Layout

11.1 Layout Guidelines

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq2408x, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq2408x family are packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note*, SLUA271.

11.2 Layout Example

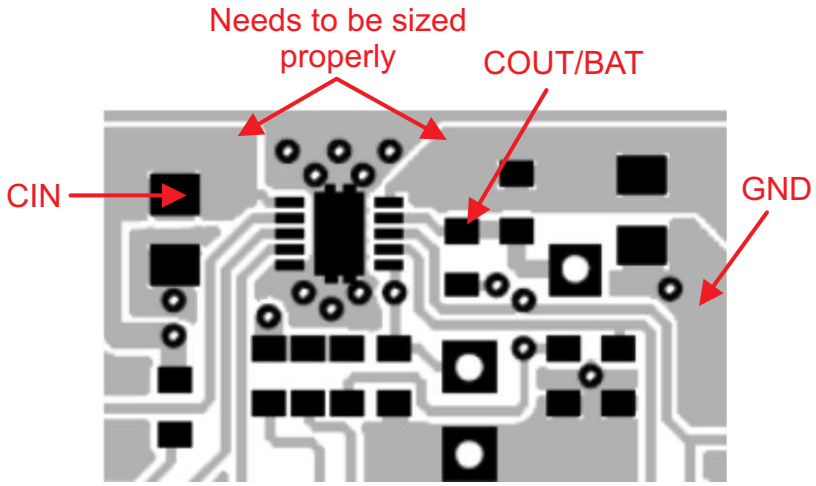


Figure 23. bq2408x PCB Layout

11.3 Thermal Considerations

The bq2408x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note*, SLUA271.

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). Use Equation 13 as the mathematical expression for θ_{JA}:

$$\theta_{(JA)} = \frac{T_J - T_A}{P} \quad (13)$$

where

- T_J = chip junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. Use Equation 14 to calculate the device power dissipation when a battery pack is being charged:

$$P = [V_{(IN)} – V_{(OUT)}] \times I_{(OUT)} \quad (14)$$

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile, Figure 8.

If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active effectively reducing the charge current to avoid excessive IC junction temperature.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

User's Guide, *bq24085/6/7/8 Evaluation Module*, SLUU305

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq24085	Click here	Click here	Click here	Click here	Click here
bq24086	Click here	Click here	Click here	Click here	Click here
bq24087	Click here	Click here	Click here	Click here	Click here
bq24088	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24085DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	0 to 125	CDV	Samples
BQ24085DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-2-260C-1 YEAR	0 to 125	CDV	Samples
BQ24086DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	CDW	Samples
BQ24086DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	CDW	Samples
BQ24087DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	CDX	Samples
BQ24087DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	CDX	Samples
BQ24088DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	CHE	Samples
BQ24088DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 125	CHE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

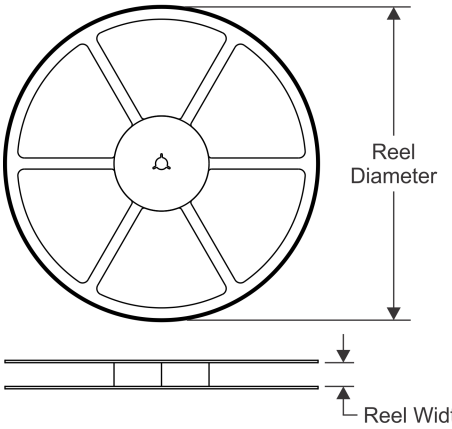
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

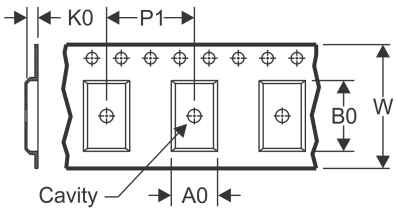
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

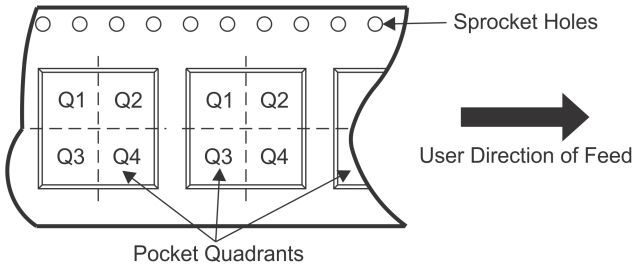


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

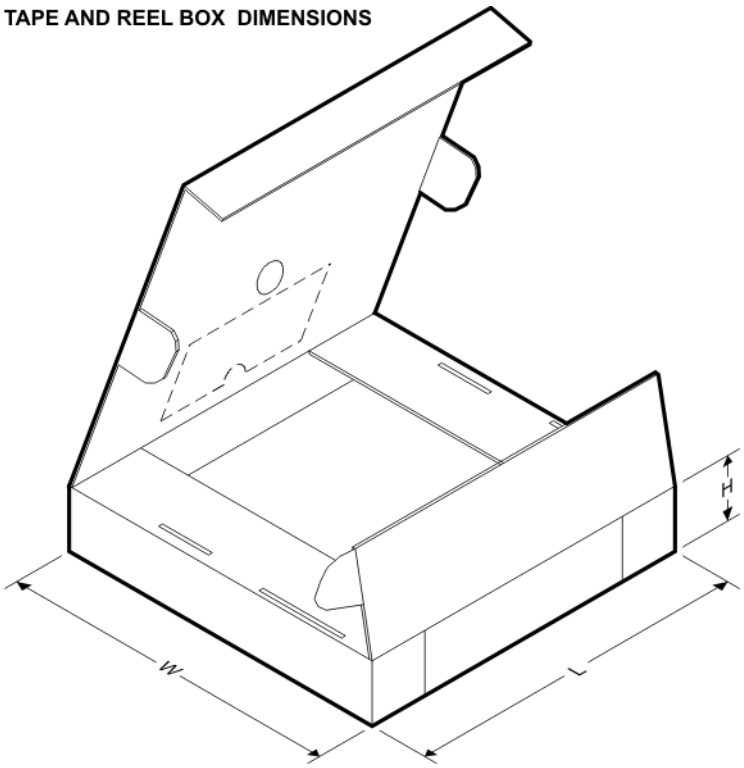
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24085DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24085DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24085DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24085DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
BQ24086DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24086DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24086DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
BQ24086DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24087DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24087DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24088DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24088DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



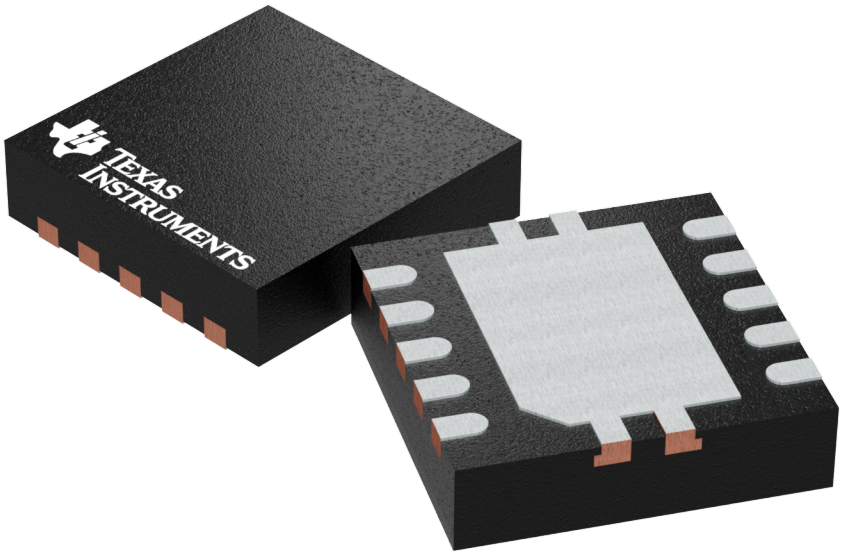
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24085DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
BQ24085DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24085DRCT	VSON	DRC	10	250	210.0	185.0	35.0
BQ24085DRCT	VSON	DRC	10	250	205.0	200.0	33.0
BQ24086DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
BQ24086DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24086DRCT	VSON	DRC	10	250	338.0	355.0	50.0
BQ24086DRCT	VSON	DRC	10	250	210.0	185.0	35.0
BQ24087DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24087DRCT	VSON	DRC	10	250	210.0	185.0	35.0
BQ24088DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
BQ24088DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC 10

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



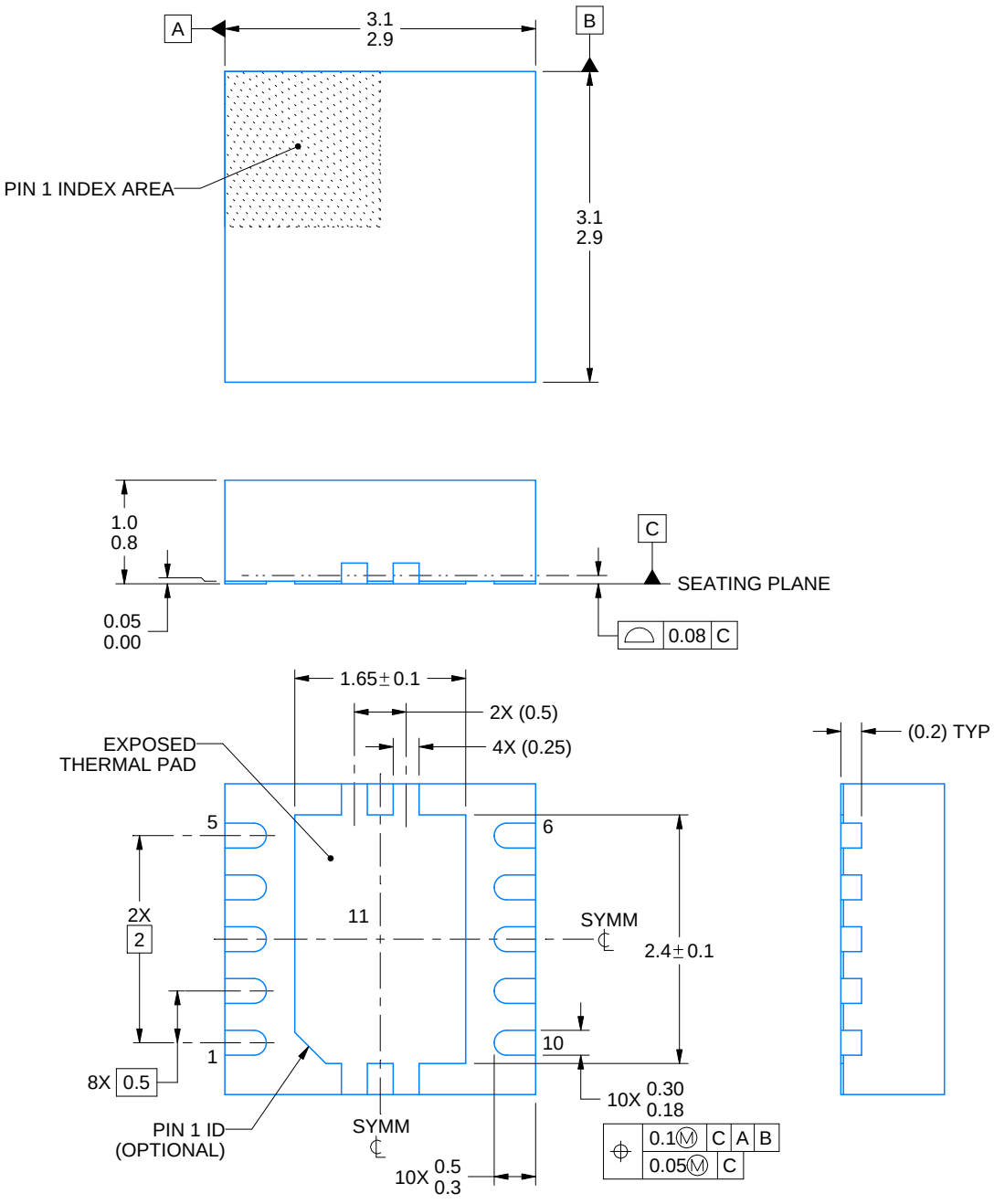
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRC0010J

PACKAGE OUTLINE

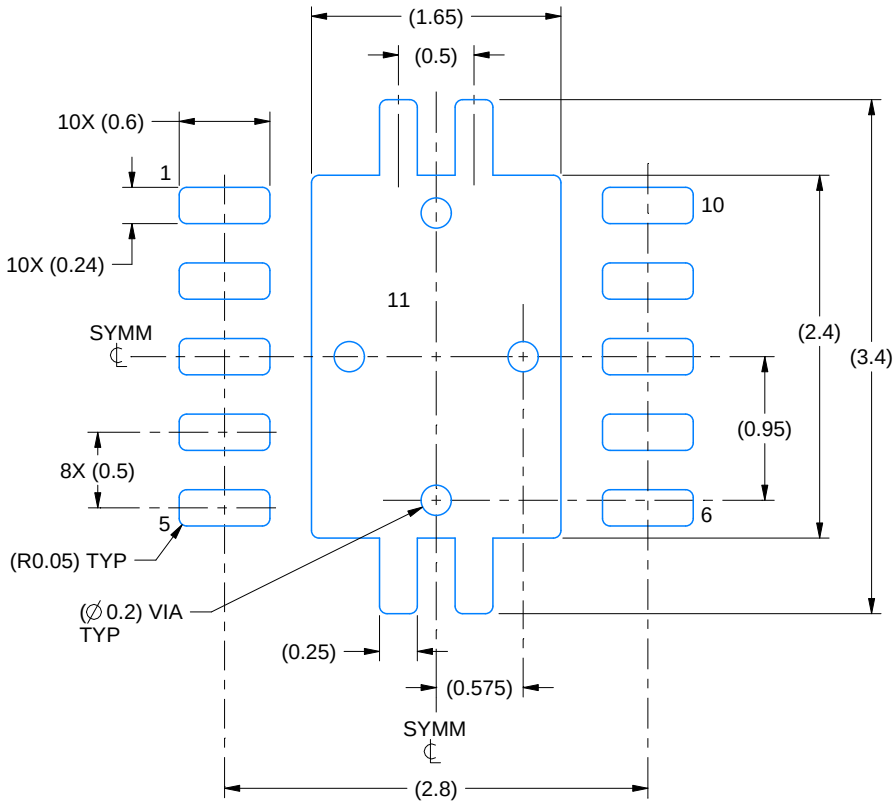
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

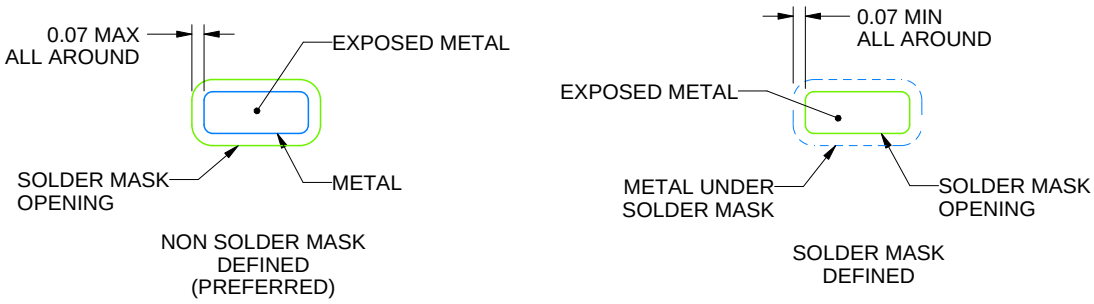


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

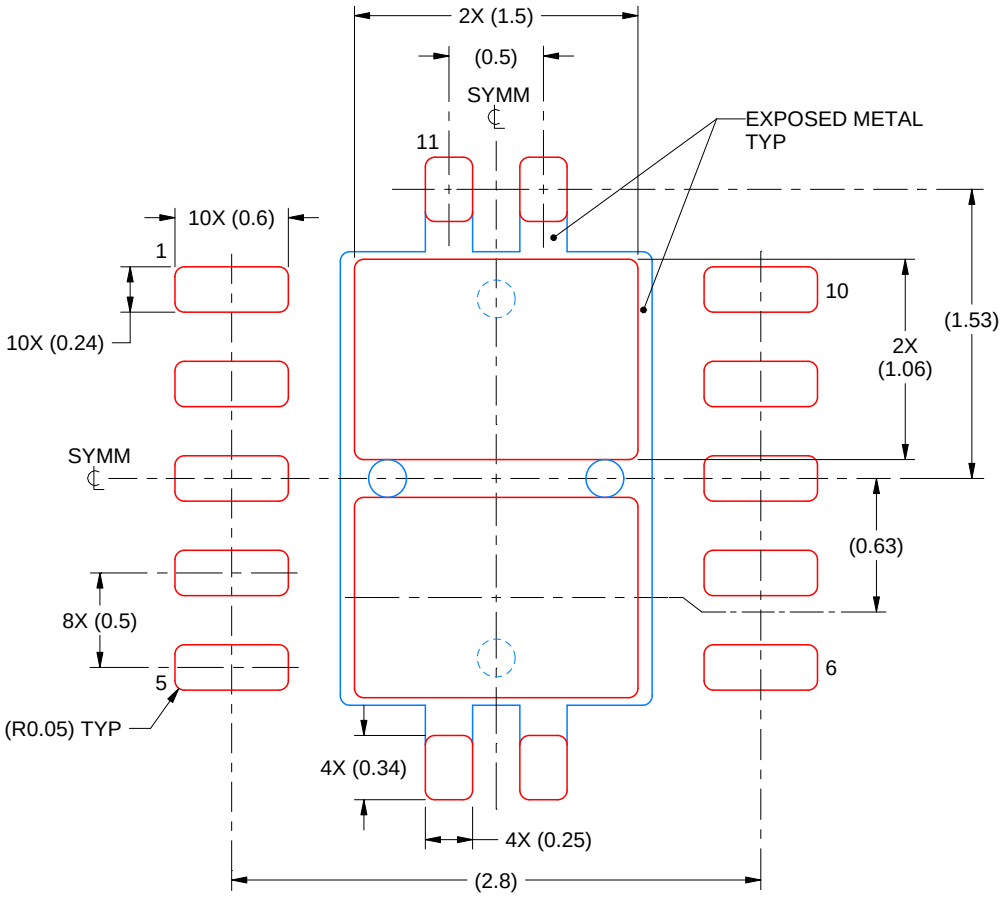
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



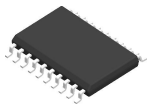
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

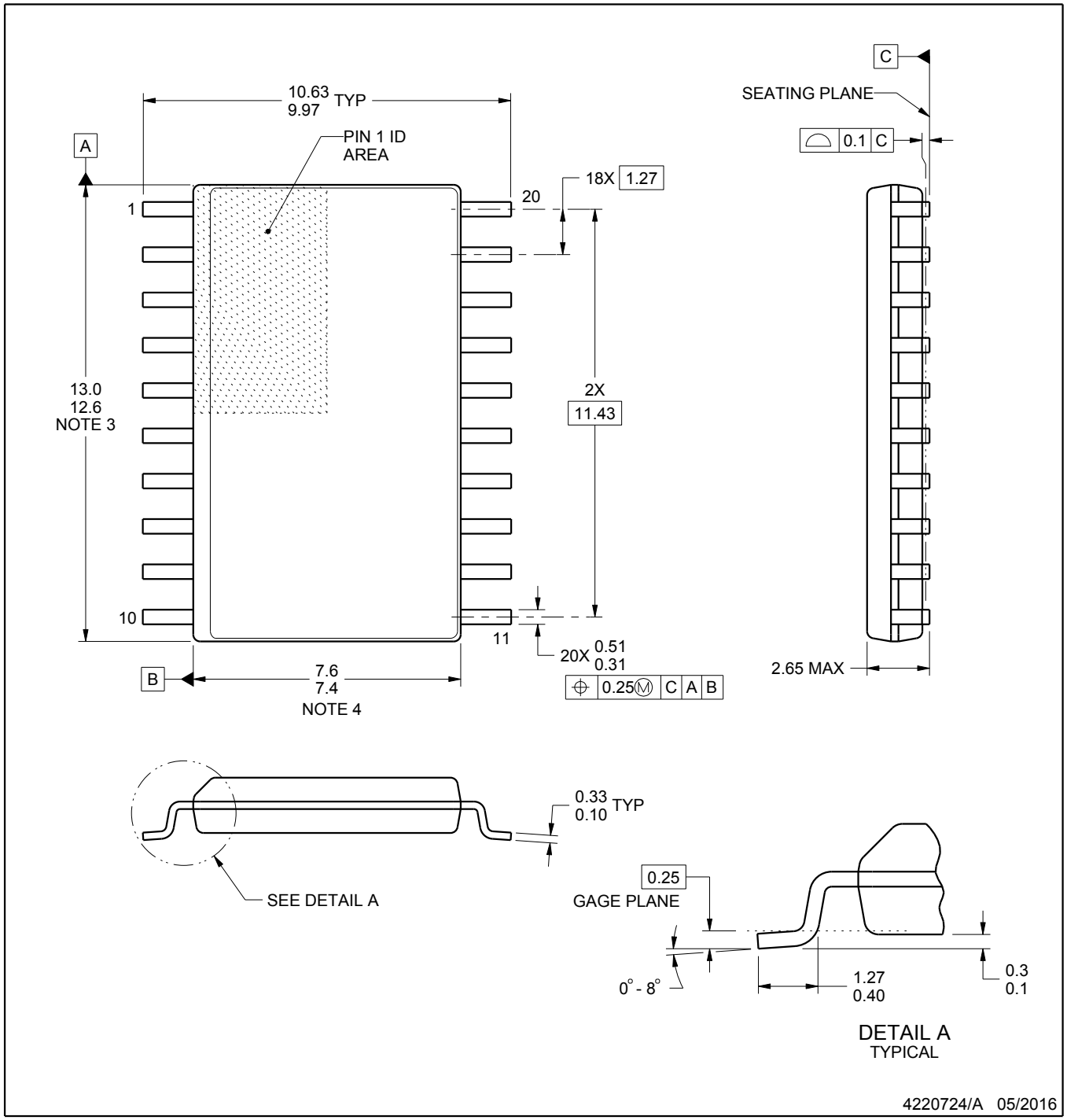


PACKAGE OUTLINE

DW0020A

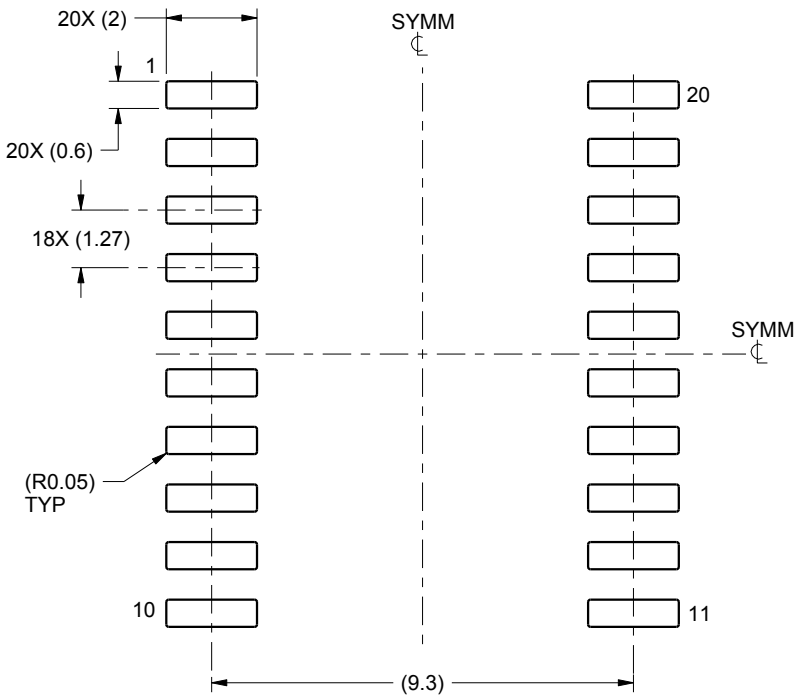
SOIC - 2.65 mm max height

SOIC

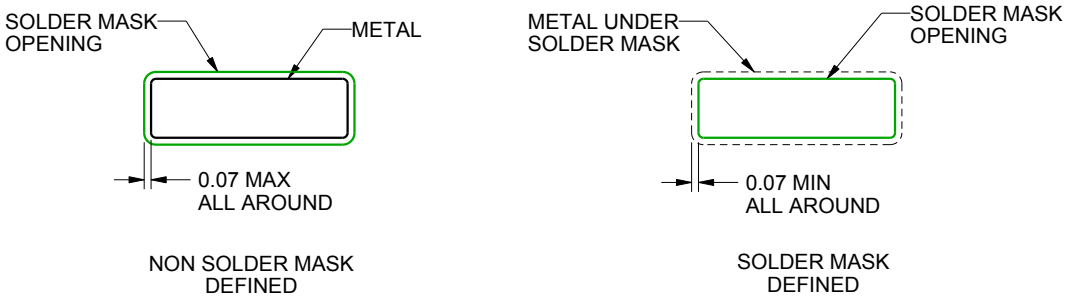


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

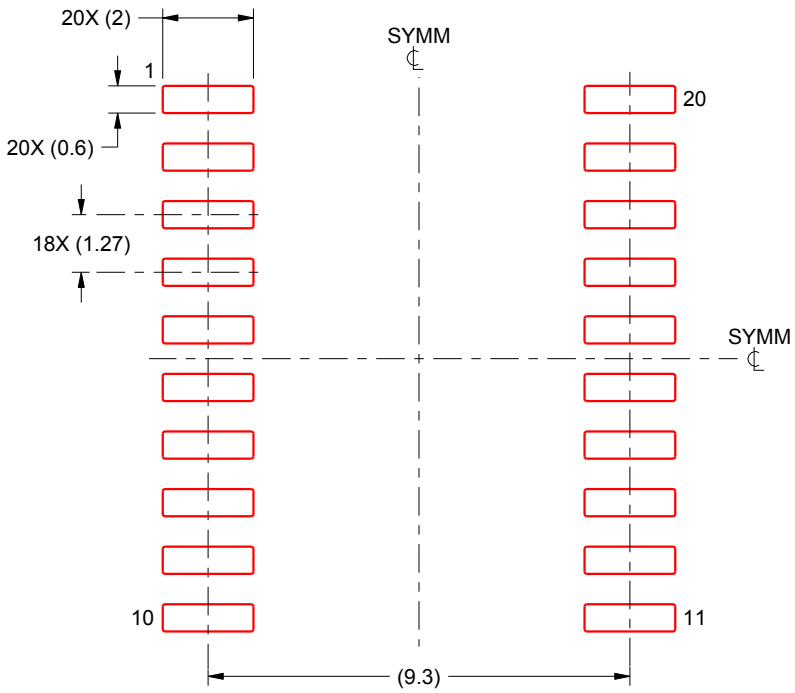


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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