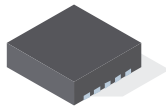




**THE DATASHEET OF
BQ24023DRCR**





SINGLE-CHIP, LI-ION AND LI-POL CHARGER IC WITH AUTONOMOUS USB-PORT AND AC-ADAPTER SUPPLY MANAGEMENT (bqTINY™-II)

FEATURES

- Small 3 mm × 3 mm MLP Package
- Charges and powers Systems from Either AC Adapter or USB With Autonomous power-Source Selection
- Integrated USB Control With Selectable 100 mA and 500 mA Charge Rates
- Ideal for Low-Dropout Charger Designs for Single-Cell Li-Ion or Li-pol Packs in Space Limited portable applications
- Integrated power FET and Current Sensor for Up to 1-A Charge applications From AC Adapter
- Precharge Conditioning With Safety Timer
- power Good (AC Adapter Present) Status Output
- Optional Battery Temperature Monitoring Before and During Charge
- Automatic Sleep Mode for Low-power Consumption

APPLICATIONS

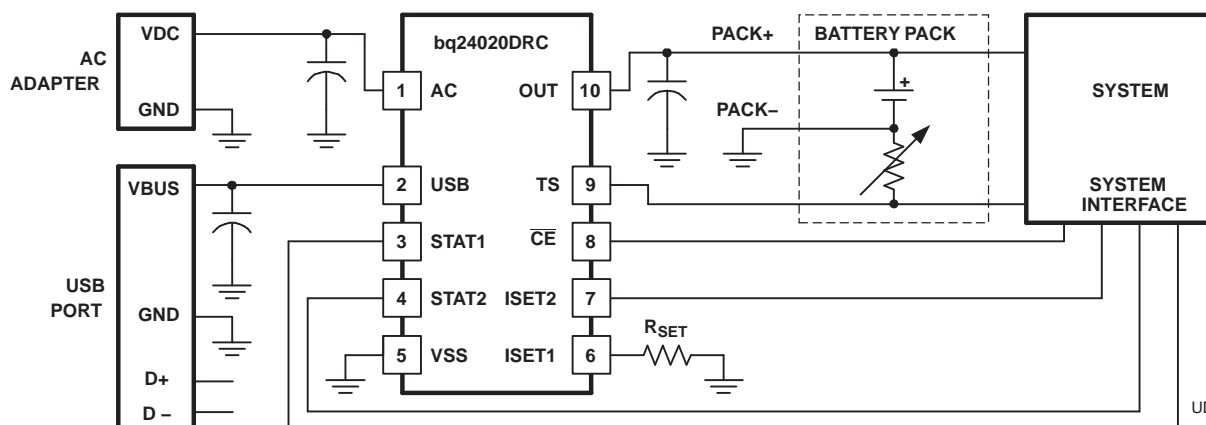
- PDAs, MP3 Players
- Digital Cameras
- Internet appliances
- Smartphones

DESCRIPTION

The bqTINY-II series are highly-integrated, flexible Li-Ion linear charge and system power management devices for space-limited charger applications. In a single monolithic device, the bqTINY-II offers integrated USB-port and ac-adapter supply management with autonomous power-source selection, power-FET and current-sensor interfaces, high-accuracy current and voltage regulation, charge status, and charge termination.

The bqTINY-II automatically selects the USB-port or the ac-adapter as the power source for the system. In the USB configuration, the host can select from two preset charge rates of 100 mA or 500 mA. In the ac-adapter configuration, an external resistor sets the system or charge current.

The bqTINY-II charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety for charge termination. The bqTINY-II automatically restarts the charge if the battery voltage falls below an internal threshold. The bqTINY-II automatically enters sleep mode when both supplies are removed.



UDG-02184



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

bqTINY is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

Different versions of the bqTINY-II offer many additional features. These include a temperature-sensor input for detecting hot or cold battery packs, a power-good output (\overline{PG}) indicating the presence of input power, a TTL-level charge-enable input (\overline{CE}) used to disable or enable the charge process, and a TTL-level timer and taper-detect enable input (\overline{TTE}) used to disable or enable the fast-charge timer and charge termination.

ORDERING INFORMATION

| T _J | CHARGE REGULATION VOLTAGE (V)(1) | OPTIONAL FUNCTIONS ⁽¹⁾ | FAST-CHARGE TIMER (Hours) | TAPER TIMER | USB TAPER THRESHOLD | PART NUMBER(2) | MARKINGS |
|----------------|----------------------------------|--------------------------------------|---------------------------|-------------|---------------------------------|----------------|----------|
| –40°C to 125°C | 4.2 | \overline{CE} and TS | 5 | Yes | 10% of ISET1 Level | bq24020DRRCR | AZS |
| | 4.2 | \overline{PG} and \overline{CE} | 5 | Yes | 10% of ISET1 Level | bq24022DRRCR | AZU |
| | 4.2 | \overline{CE} and \overline{TTE} | 5 | Yes | 10% of ISET1 Level | bq24023DRRCR | AZV |
| | 4.2 | \overline{TTE} and TS | 5 | Yes | 10% of ISET1 Level | bq24024DRRCR | AZW |
| | 4.2 | \overline{CE} and TS | 7 | Yes | 10% of ISET1 Level | bq24025DRRCR | AZX |
| | 4.2 | \overline{TE} and TS | 7 | No | 10% of selected USB charge rate | bq24026DRRCR | ANR |
| | 4.2 | \overline{PG} and \overline{CE} | 7 | No | 10% of selected USB charge rate | bq24027DRRCR | ANS |

(1) The DRC package is available taped and reeled only in quantities of 3,000 devices per reel.

Dissipation Ratings

| PACKAGE | θ_{JA} | T _A < 40°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C |
|--------------------|---------------|------------------------------------|---|
| DRC ⁽¹⁾ | 46.87 °C/W | 1.5 W | 0.021 W/°C |

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2×3 via matrix.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | bq24020, bq24022, bq24023, bq24024, bq24025, bq24026, bq24027 | UNIT |
|--|---|---|------|
| Input voltage ⁽²⁾ | AC, \overline{CE} , ISET1, ISET2, OUT, \overline{PG} , STAT1, STAT2, \overline{TE} , TS, \overline{TTE} , USB | –0.3 to 7.0 | V |
| Output sink/source current | STAT1, STAT2, \overline{PG} | 15 | mA |
| Output current | TS | 200 | μA |
| Output current | OUT | 1.5 | A |
| Operating free-air temperature range, T _A | | –40 to 125 | °C |
| Junction temperature range, T _J | | | |
| Storage temperature, T _{stg} | | | |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|------|-----|-----|------|
| Supply voltage (from AC input), V_{CC} | 4.5 | | 6.5 | V |
| Supply voltage (from USB input), V_{CC} | 4.35 | | 6.5 | V |
| Operating junction temperature range, T_J | -40 | | 125 | °C |

ELECTRICAL CHARACTERISTICS

over $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ and recommended supply voltage, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|---|---|---|-------|-------|---------------|---|
| INPUT CURRENT | | | | | | | |
| $I_{CC}(V_{CC})$ | V_{CC} current | $V_{CC} > V_{CC(\text{min})}$ | | 1.2 | 2.0 | mA | |
| $I_{CC}(\text{SLP})$ | Sleep current | Sum of currents into OUT pin, $V_{CC} < V_{I(\text{SLP})}$ | | 2 | 5 | μA | |
| $I_{CC}(\text{STBY})$ | Standby current | CE = High $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ | | 1 | 150 | | |
| $I_{B(\text{OUT})}$ | Input current on OUT pin | Charge DONE $V_{CC} > V_{CC(\text{MIN})}$ | | | 5 | | |
| $I_{B(\text{CE})}$ | Input current on CE pin | | | | 1 | | |
| $I_{B(\text{TTE})}$ | Input bias current on TTE pin | | | | 1 | | |
| $I_{B(\text{TE})}$ | Input bias current on TE pin | | | | 1 | | |
| VOLTAGE REGULATION $V_{O(\text{REG})} + V_{(\text{DO-MAX})} \leq V_{CC}$, $I_{(\text{TERM})} < I_{O(\text{OUT})} \leq 1 \text{ A}$ | | | | | | | |
| $V_{O(\text{REG})}$ | Output voltage, | | | 4.20 | | V | |
| | Voltage regulation accuracy | $T_A = 25^\circ\text{C}$ | -0.35% | | 0.35% | | |
| | | | -1% | | 1% | | |
| $V_{(\text{DO})}$ | AC dropout voltage ($V_{(\text{AC})} - V_{(\text{OUT})}$) | $V_{O(\text{OUT})} = V_{O(\text{REG})}$ $V_{O(\text{REG})} + V_{(\text{DO-MAX})} \leq V_{CC}$ | $I_{O(\text{OUT})} = 1 \text{ A}$ | 350 | 500 | mV | |
| | | $V_{O(\text{OUT})} = V_{O(\text{REG})}$ $V_{O(\text{REG})} + V_{(\text{DO-MAX})} \leq V_{CC}$ | ISET2 = High | 350 | 500 | | |
| $V_{(\text{DO})}$ | USB dropout voltage ($V_{(\text{USB})} - V_{(\text{OUT})}$) | $V_{O(\text{OUT})} = V_{O(\text{REG})}$ $V_{O(\text{REG})} + V_{(\text{DO-MAX})} \leq V_{CC}$ | ISET2 = Low | 60 | 100 | | |
| CURRENT REGULATION | | | | | | | |
| $I_{O(\text{OUT})}$ | AC output current range ⁽¹⁾ | $V_{I(\text{OUT})} > V_{(\text{LOWV})}$ $V_{I(\text{AC})} - V_{I(\text{OUT})} > V_{(\text{DO-MAX})}$ | $V_{CC} \geq 4.5 \text{ V}$ | 50 | 1000 | mA | |
| | | $V_{CC(\text{MIN})} \geq 4.5 \text{ V}$ $V_{\text{USB}} - V_{I(\text{OUT})} > V_{(\text{DO-MAX})}$ | $V_{I(\text{OUT})} > V_{(\text{LOWV})}$ ISET2 = Low | 80 | 100 | | |
| $I_{O(\text{OUT})}$ | USB output current range | $V_{CC(\text{MIN})} \geq 4.5 \text{ V}$ $V_{\text{USB}} - V_{I(\text{OUT})} > V_{(\text{DO-MAX})}$ | $V_{I(\text{OUT})} > V_{(\text{LOWV})}$ ISET2 = High | 400 | 500 | | |
| $V_{(\text{SET})}$ | Output current set voltage | Voltage on ISET1 pin, $V_{CC} \geq 4.5 \text{ V}$, $V_{\text{IN}} \geq 4.5 \text{ V}$, $V_{I(\text{OUT})} > V_{(\text{LOWV})}$, $V_{\text{IN}} - V_{I(\text{OUT})} > V_{(\text{DO-MAX})}$ | | 2.463 | 2.500 | 2.538 | V |
| $K_{(\text{SET})}$ | Output current set factor | $50 \text{ mA} \leq I_{O(\text{OUT})} \leq 1 \text{ A}$ | | 307 | 322 | 337 | |
| | | $10 \text{ mA} \leq I_{O(\text{OUT})} < 50 \text{ mA}$ | | 296 | 320 | 346 | |
| | | $1 \text{ mA} \leq I_{O(\text{OUT})} < 10 \text{ mA}$ | | 246 | 320 | 416 | |

$$(1) \quad I_{O(\text{OUT})} = \frac{(K_{(\text{SET})} \times V_{(\text{SET})})}{R_{\text{SET}}}$$

ELECTRICAL CHARACTERISTICS (continued)

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|-------|-------|-------|------|
| PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION | | | | | | |
| V _(LOWV) | Precharge to fast-charge transition threshold | Voltage on OUT pin | 2.8 | 3.0 | 3.2 | V |
| | Deglintch time for fast-charge to precharge transition | V _{CC(MIN)} ≥ 4.5 V, t _{FALL} = 100 ns, 10 mV overdrive, V _{I(OUT)} decreasing below threshold | 250 | 375 | 500 | ms |
| I _{O(PRECHG)} | Precharge range ⁽²⁾ | 0 V < V _{I(OUT)} < V _(LOWV) , t < t _(PRECHG) | 5 | | 100 | mA |
| V _(PRECHG) | Precharge set voltage | Voltage on ISET1 pin V _{O(REG)} = 4.2 V 0 V < V _{I(OUT)} > V _(LOWV) , t < t _(PRECHG) | 240 | 255 | 270 | mV |
| CHARGE TAPER AND TERMINATION DETECTION | | | | | | |
| I _(TAPER) | Charge taper detection range ⁽³⁾ | V _{I(OUT)} > V _(RCH) , t < t _(TAPER) | 5 | | 100 | mA |
| | USB-100 charge taper detection level | bq24026 V _{I(OUT)} > V _(RCH) , ISET2 = Low | 6.5 | 9 | 11 | |
| | USB-500 charge taper detection level | bq24026 V _{I(OUT)} > V _(RCH) , ISET2 = High | 32 | 44 | 55 | |
| V _(TAPER) | Charge taper detection set voltage | Voltage on ISET1 pin, V _{O(REG)} = 4.2 V, V _{I(OUT)} > V _(RCH) , t < t _(TAPER) | 235 | 250 | 265 | mV |
| V _(TERM) | Charge termination detection set voltage ⁽⁴⁾ | Voltage on ISET1 pin, V _{O(REG)} = 4.2 V, V _{I(OUT)} > V _(RCH) | 11 | 18 | 25 | |
| t _(TPRDET) | Deglintch time for TAPER detection | V _{CC(MIN)} ≥ 4.5 V, t _{FALL} = 100 ns charging current increasing or decreasing above and below, 10 mV overdrive | 250 | 375 | 500 | ms |
| t _(TRMDET) | Deglintch time for termination detection | V _{CC(MIN)} ≥ 4.5 V, t _{FALL} = 100 ns charging current decreasing below, 10 mV overdrive | 250 | 375 | 500 | |
| TEMPERATURE SENSE COMPARATOR | | | | | | |
| V _(HTF) | High-voltage threshold | PTC thermistor | 2.475 | 2.500 | 2.525 | V |
| V _(LTF) | Low-voltage threshold | PTC thermistor | 0.485 | 0.500 | 0.515 | |
| I _(TS) | Current source | | 96 | 102 | 108 | μA |
| t _(DEGL) | Deglintch time for temperature fault | | 250 | 375 | 500 | ms |

$$(2) \quad I_{O(PRECHG)} = \frac{(K_{(SET)} \times V_{(PRECHG)})}{R_{SET}}$$

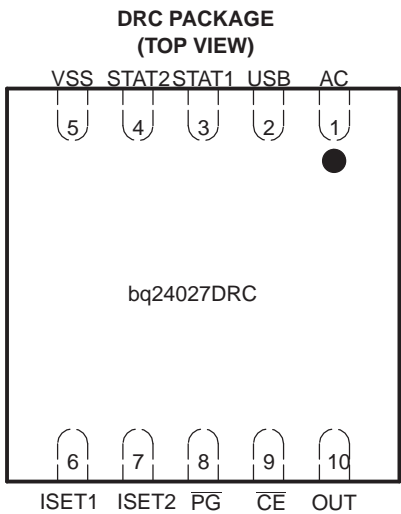
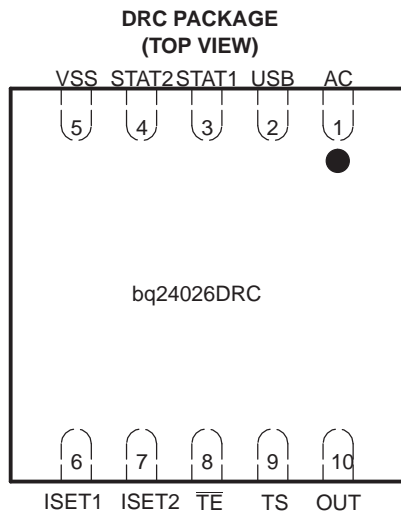
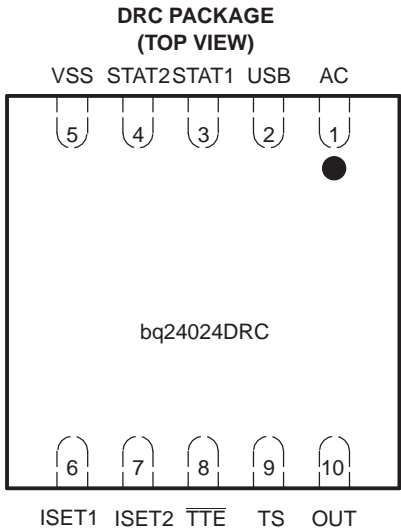
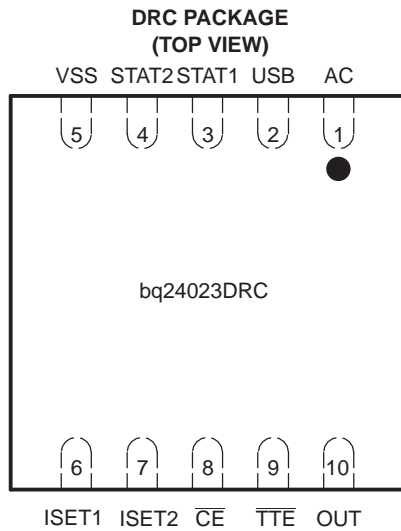
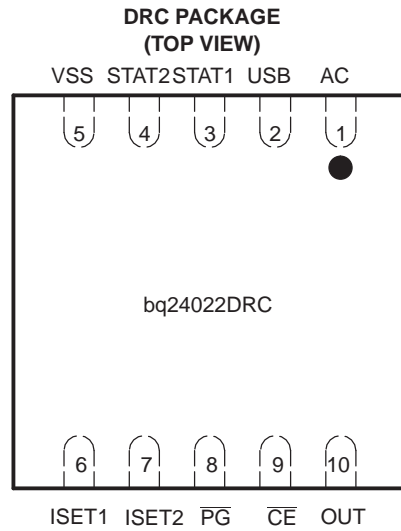
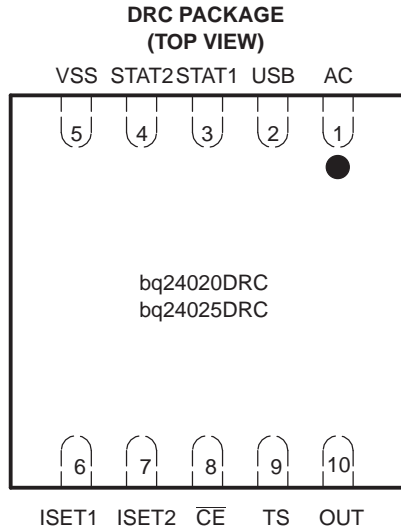
$$(3) \quad I_{O(TAPER)} = \frac{(K_{(SET)} \times V_{(TAPER)})}{R_{SET}}$$

$$(4) \quad I_{O(TERM)} = \frac{(K_{(SET)} \times V_{(TERM)})}{R_{SET}}$$

ELECTRICAL CHARACTERISTICS (continued)

over $0^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ and recommended supply voltage, unless otherwise noted

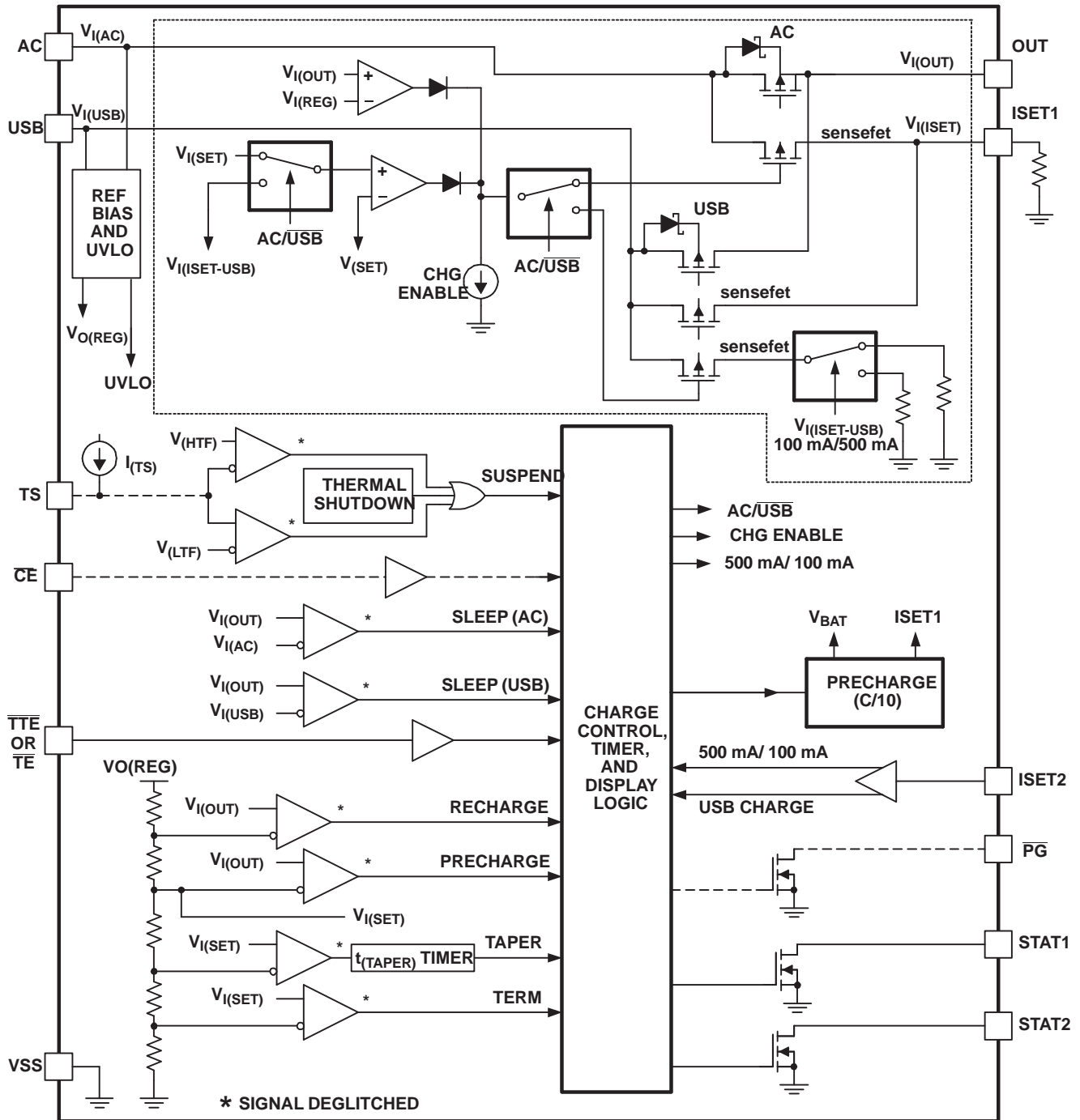
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|-----------------------------|----------------------------|--|--------------------|
| BATTERY RECHARGE THRESHOLD | | | | | | |
| V_{RCH} | Recharge threshold | | $V_{\text{O(REG)}} - 0.115$ | $V_{\text{O(REG)}} - 0.10$ | $V_{\text{O(REG)}} - 0.085$ | V |
| $t_{\text{(DEGL)}}$ | Deglintch time for recharge detect | $V_{\text{CC(MIN)}} \geq 4.5\text{ V}$, $t_{\text{FALL}} = 100\text{ ns}$ decreasing below or increasing above threshold, 10 mV overdrive | 250 | 375 | 500 | ms |
| STAT1, STAT2, and PG OUTPUTS | | | | | | |
| V_{OL} | Low-level output saturation voltage | $I_{\text{O}} = 5\text{ mA}$ | | | 0.25 | V |
| ISET2, CHARGE ENABLE (CE), TIMER AND TERMINATION ENABLE (TTE), AND TIMER ENABLE (TE) INPUTS | | | | | | |
| V_{IL} | Low-level input voltage | $I_{\text{IL}} = 10\text{ }\mu\text{A}$ | 0 | | 0.4 | V |
| V_{IH} | High-level input voltage | $I_{\text{IL}} = 20\text{ }\mu\text{A}$ | 1.4 | | | |
| I_{IL} | CE, TE or TTE low-level input current | | -1 | | | μA |
| I_{IH} | CE, TE or TTE high-level input current | | | | 1 | |
| I_{IL} | ISET2 low-level input current | $I_{\text{ISET2}} = 0$ | -20 | | | |
| I_{IH} | ISET2 high-level input current | $I_{\text{ISET2}} = V_{\text{CC}}$ | | | 40 | |
| I_{IH} | ISET2 high-Z input current | | | | 1 | V |
| TIMERS | | | | | | |
| $t_{\text{(PRECHG)}}$ | Precharge time | | 1,584 | 1,800 | 2,016 | s |
| $t_{\text{(TAPER)}}$ | Taper time | bq24020 bq24022 bq24023 bq24024 bq24025 | 1,584 | 1,800 | 2,016 | |
| $t_{\text{(CHG)}}$ | Charge time | bq24020 bq24022 bq24023 bq24024 | 15,840 | 18,000 | 20,160 | |
| | | bq24025 bq24026 bq24027 | 22,176 | 25,200 | 28,224 | |
| $I_{\text{(FAULT)}}$ | Timer fault recovery current | | | 200 | | |
| SLEEP COMPARATOR | | | | | | |
| $V_{\text{(SLP)}}$ | Sleep-mode entry threshold voltage | $2.3\text{ V} \leq V_{\text{I(OUT)}} \leq V_{\text{O(REG)}}$ | | | $V_{\text{CC}} \leq V_{\text{I(OUT)}} + 80\text{ mV}$ | V |
| $V_{\text{(SLPEXIT)}}$ | Sleep mode exit threshold voltage | $2.3\text{ V} \leq V_{\text{I(OUT)}} \leq V_{\text{O(REG)}}$ | | | $V_{\text{CC}} \geq V_{\text{I(OUT)}} + 190\text{ mV}$ | |
| | Sleep mode deglitch time | AC and USB decreasing below threshold, $t_{\text{FALL}} = 100\text{ ns}$, 10 mV overdrive | 250 | 375 | 500 | ms |
| THERMAL SHUTDOWN THRESHOLDS | | | | | | |
| $T_{\text{(SHTDWN)}}$ | Thermal trip threshold | | | 165 | | $^{\circ}\text{C}$ |
| | Thermal hysteresis | | | 15 | | |
| UNDERVOLTAGE LOCKOUT | | | | | | |
| $V_{\text{(UVLO)}}$ | Undervoltage lockout | Decreasing V_{CC} | 2.4 | 2.5 | 2.6 | V |
| | Hysteresis | | | 27 | | mV |



Terminal Functions

| NAME | TERMINAL | | | | | I/O | DESCRIPTION |
|---------------------|--------------------|--------------------|---------|---------|---------|-----|---|
| | bq24020 bq24025 | bq24022 bq24027 | bq24023 | bq24024 | bq24026 | | |
| AC | 1 | 1 | 1 | 1 | 1 | I | AC charge input voltage |
| \overline{CE} | 8 | 9 | 8 | - | - | I | Charge enable input (active low) |
| ISET1 | 6 | 6 | 6 | 6 | 6 | I | Charge current set point for AC input and precharge and taper set point for both AC and USB |
| ISET2 | 7 | 7 | 7 | 7 | 7 | I | Charge current set point for USB port (high=500 mA, low=100 mA, hi-z = disable USB charge) |
| OUT | 10 | 10 | 10 | 10 | 10 | O | Charge current output |
| \overline{PG} | - | 8 | - | - | - | O | powergood status output (active low) |
| STAT1 | 3 | 3 | 3 | 3 | 3 | O | Charge status output 1 (open-drain) |
| STAT2 | 4 | 4 | 4 | 4 | 4 | O | Charge status output 2 (open-drain) |
| \overline{TE} | - | - | - | - | 8 | I | Timer enable input (active low) |
| TS | 9 | - | - | 9 | 9 | I | Temperature sense input |
| \overline{TTE} | - | - | 9 | 8 | - | I | Timer and termination enable input (active low) |
| USB | 2 | 2 | 2 | 2 | 2 | I | USB charge input voltage |
| VSS | 5 | 5 | 5 | 5 | 5 | - | Ground input |
| Exposed Thermal Pad | pad | pad | pad | pad | pad | - | There is an internal electrical connection between the exposed thermal pad and VSS pin of the device. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times |

FUNCTIONAL BLOCK DIAGRAM



UDG-02185

TYPICAL CHARACTERISTICS
AC DROPOUT VOLTAGE
VS
JUNCTION TEMPERATURE

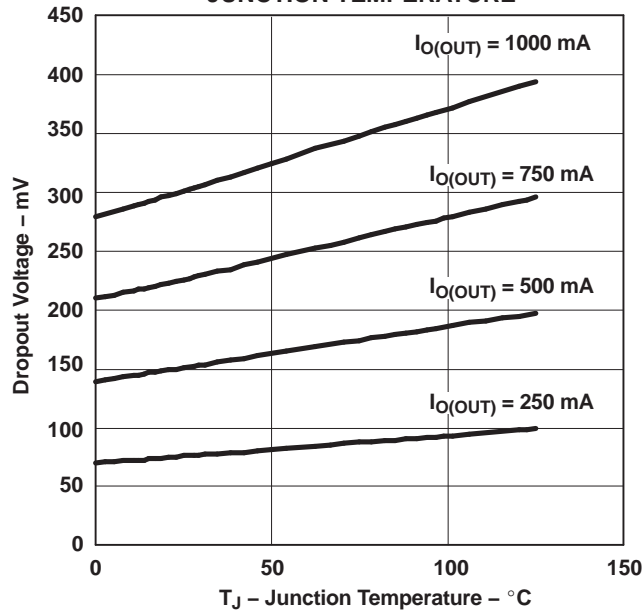


Figure 1.

The bqTINY-II supports a precision Li-Ion, Li-pol charging system suitable for single-cell packs. Figure 3 shows a typical charge profile, application circuit and Figure 4 shows an operational flow chart.

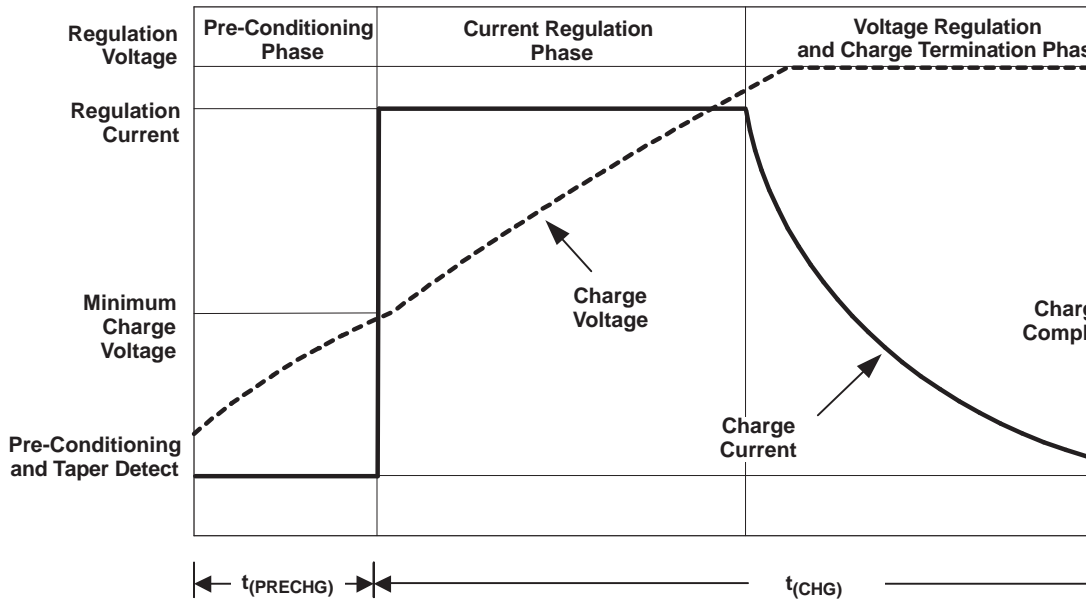
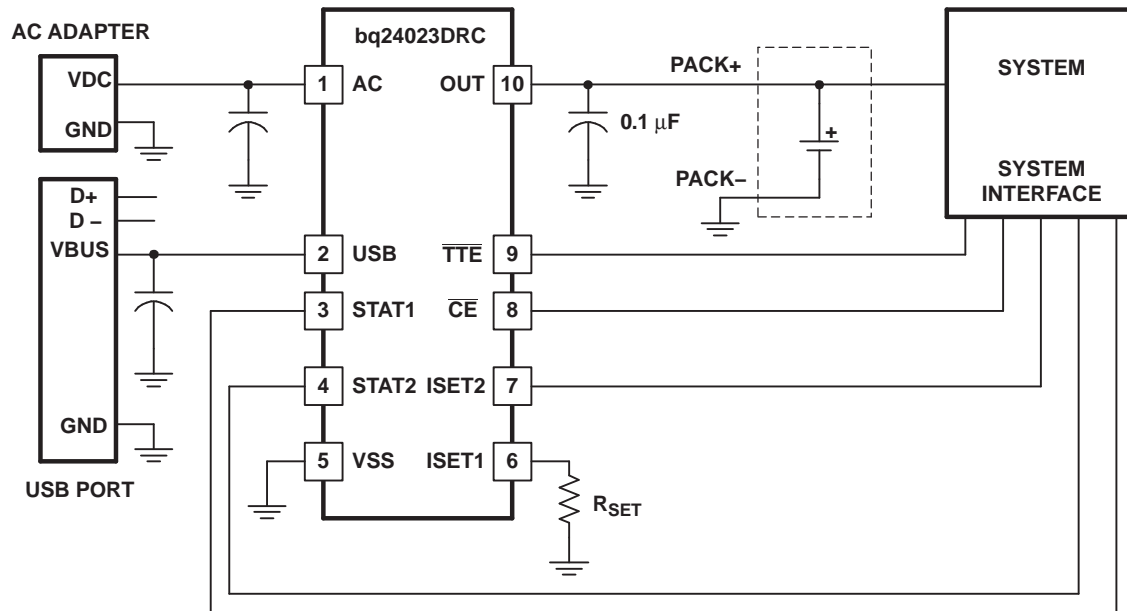


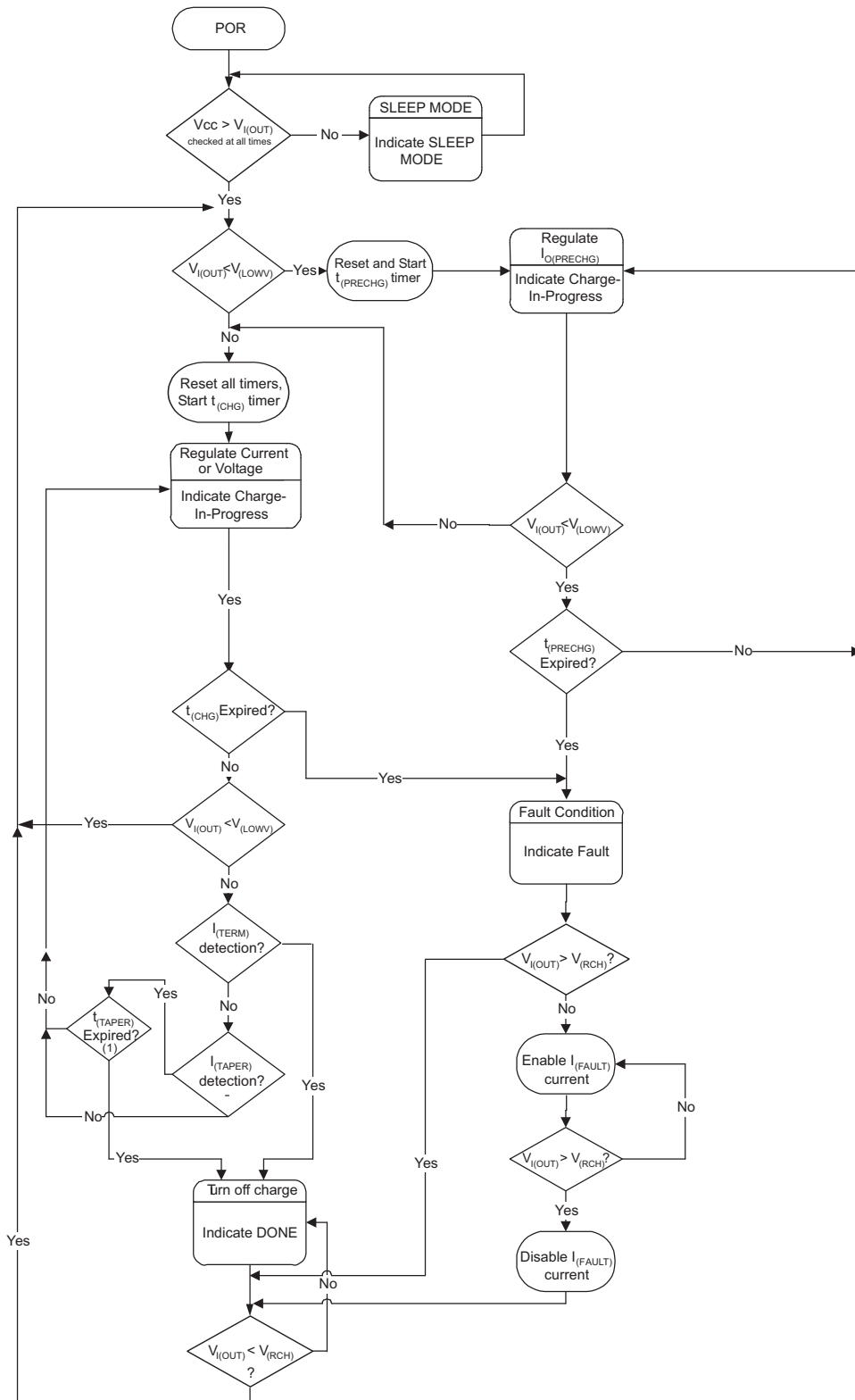
Figure 2. Typical Charging Profile

FUNCTIONAL DESCRIPTION



UDG-02184

Figure 3. Typical Application Circuit

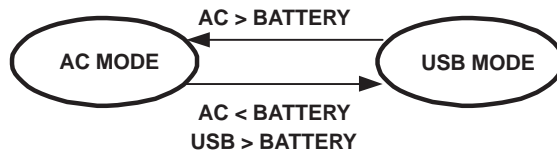


⁽¹⁾ t_{TAPER} does not apply to bq24026/7

Figure 4. Operational Flow Chart

AUTONOMOUS POWER SOURCE SELECTION

As default, the bqTINY-II attempts to charge from the AC input. If AC input is not present, the USB is selected. If both inputs are available, the AC adapter has the priority. See for details.



UDG-02187

Figure 5. Typical Charging Profile

TEMPERATURE QUALIFICATION (bq24020, bq24024, bq24025, and bq24026 only)

The bqTINY-II continuously monitors battery temperature by measuring the voltage between the TS and VSS pins. An internal current source provides the bias for common 10-kΩ negative-temperature coefficient thermistors (NTC) (see Figure 6). The device compares the voltage on the TS pin with the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. If a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected, the device immediately suspends the charge by turning off the power FET and holding the timer value (i.e. timers are NOT reset). Charge is resumed when the temperature returns within the normal range.

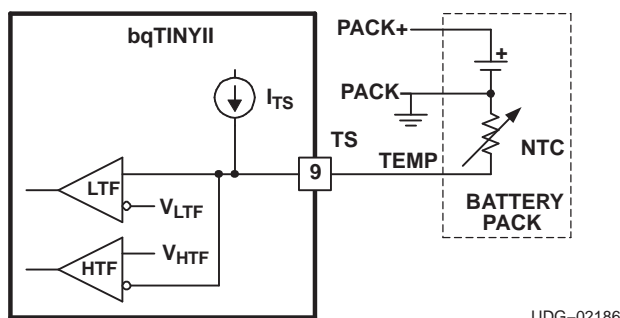
The allowed temperature range for a 103AT-type thermistor is 0°C to 45°C. However the user may modify these thresholds by adding two external resistors. See Figure 7.

BATTERY PRE-CONDITIONING

If the battery voltage falls below the $V_{(LOWV)}$ threshold during a charge cycle, the bqTINY-II applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET1 and V_{SS} , R_{SET} , determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

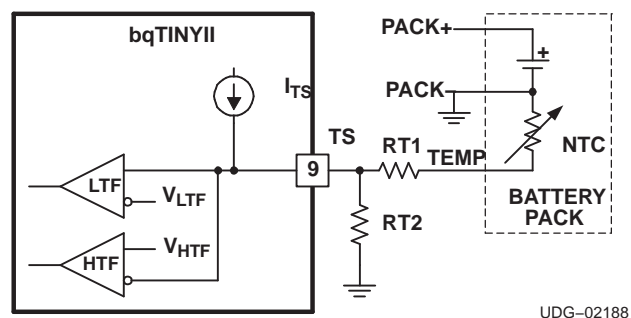
$$I_{O(PRECHG)} = \frac{V_{(PRECHG)} K_{(SET)}}{R_{SET}} \quad (1)$$

The bqTINY-II activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqTINY-II turns off the charger and asserts a FAULT code on the STATx pins. Please refer to the *TIMER FAULT RECOVERY* section for additional details.



UDG-02186

Figure 6. Temperature Sensing Configuration



UDG-02188

Figure 7. Temperature Sensing Thresholds

BATTERY CHARGE CURRENT

The bqTINY-II offers on-chip current regulation with a programmable set point. The resistor connected between the ISET1 and V_{SS} , R_{SET} , determines the AC charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O(OUT)} = \frac{(K_{(SET)} \times V_{(SET)})}{R_{SET}} \quad (2)$$

When charging from a USB port, the host controller has the option of selecting either a 100-mA or a 500-mA charge rate using the ISET2 pin. A low-level signal sets the current at 100 mA, and a high-level signal sets the current at 500 mA. A high-Z input disables USB charging.

BATTERY VOLTAGE REGULATION

The voltage regulation feedback is through the OUT pin. This input is tied directly to the positive side of the battery pack. The bqTINY-II monitors the battery-pack voltage between the OUT and VSS pins. When the battery voltage rises to the $V_{O(REG)}$ threshold, the voltage-regulation phase begins and the charging current begins to taper down.

As a safety backup, the bqTINY-II also monitors the charge time. If the charge is not terminated within the time period specified by $t_{(CHG)}$, the bqTINY-II turns off the charger and asserts a FAULT code on the STATx pins. Please refer to the *TIMER FAULT RECOVERY* section for additional details.

CHARGE TAPER DETECTION, TERMINATION AND RECHARGE

The bqTINY-II monitors the charging current during the voltage-regulation phase. When the taper threshold, $I_{(TAPER)}$, is detected, the bqTINY-II initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The resistor connected between the ISET1 and V_{SS} , R_{SET} , determines the taper detection level. The $V_{(TAPER)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TAPER)} = \frac{V_{(TAPER)} \times K_{(SET)}}{R_{SET}} \quad (3)$$

The bqTINY-II resets the taper timer if the charge current rises above the taper threshold, $I_{(TAPER)}$.

In addition to taper-current detection, the bqTINY-II terminates charge if the charge current falls below the $I_{(TERM)}$ threshold. This feature allows quick recognition of a battery-removal condition, or insertion of a fully charged battery. Note that the charge timer and taper timer are bypassed for this feature. The resistor connected between the ISET1 and V_{SS} , R_{SET} , determines the taper detection level. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \quad (4)$$

After charge termination, the bqTINY-II re-starts the charge when the voltage on the OUT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

Note ON bq24026 AND bq24027

The bq24026 and bq24027 monitor the charging current during the voltage-regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected, the bq24026/27 terminates the charge. There is no taper timer ($t_{(TAPER)}$) for this version.

The resistor connected between the ISET1 and V_{SS} , R_{SET} , determines the taper-detect level for AC input. For USB charge, taper level is fixed at 10% of the 100- or 500-mA charge rate.

Also note that there is $I_{(TERM)}$ detection in the bq24026 and the bq24027.

SLEEP MODE

The bqTINY-II enters low-power sleep mode if both AC and USB are removed from the circuit. This feature prevents draining the battery in the absence of input supply.

CHARGE STATUS OUTPUTS

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in the following table. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

Table 1. Status Pins Summary⁽¹⁾

| CHARGE STATE | STAT1 | STAT2 |
|------------------------------|-------|-------|
| Precharge in progress | ON | ON |
| Fast charge in progress | ON | OFF |
| Charge done | OFF | ON |
| Charge suspend (temperature) | OFF | OFF |
| Timer fault | OFF | OFF |
| Sleep mode | OFF | OFF |

(1) OFF means the open-drain output transistor on the STAT1 and STAT2 pins is in an off state.

\overline{PG} OUTPUT

The open-drain \overline{PG} (power Good) indicates when the AC adapter is present. The output turns ON when a valid voltage is detected. This output is turned off in the sleep mode. The \overline{PG} pin can be used to drive an LED or to communicate to the host processor.

\overline{CE} INPUT (CHARGE ENABLE)

The \overline{CE} digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge. A high-level signal disables the charge, and places the device in a low-power mode. A high-to-low transition on this pin also resets all timers and timer fault conditions. Note that this applies to both AC and USB charging.

\overline{TTE} INPUT (TIMER AND TERMINATION ENABLE)

The \overline{TTE} digital input is used to disable or enable the fast-charge timer and charge-taper detection. A low-level signal on this pin enables the fast-charge timer and taper timer, and a high-level signal disables this feature. Note that this applies to both AC and USB charging.

THERMAL SHUTDOWN AND PROTECTION

The bqTINY-II monitors the junction temperature, T_J , and suspends charging if T_J exceeds $T_{(SHTDWN)}$. Charging resumes when T_J falls approximately 15°C below $T_{(SHTDWN)}$.

\overline{TE} INPUT (TIMER ENABLED)

The \overline{TE} digital input is used to disable or enable the fast-charge timer. A low-level signal on this pin enables the fast-charge timer and a high-level signal disables this feature.

Note that this applies to both AC and USB charging.

TIMER FAULT RECOVERY

As shown in [Figure 4](#), the bqTINY-II provides a recovery method to deal with timer-fault conditions. The following discussion summarizes this method:

Condition #1: The charge voltage is above the recharge threshold ($V_{(RCH)}$), and a timeout fault occurs

Recovery method: bqTINY-II waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. When the battery voltage falls below the recharge threshold, the bqTINY-II clears the fault and starts a new charge cycle. Toggling POR, \overline{CE} , or \overline{TTE} also clears the fault.

Condition #2: The charge voltage is below the recharge threshold ($V_{(RCH)}$), and a timeout fault occurs

Recovery method: In this scenario, the bqTINY-II applies the $I_{(FAULT)}$ current. This small current is used to detect a battery-removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqTINY-II disables the $I_{(FAULT)}$ current and executes the recovery method described for condition #1. When the battery voltage falls below the recharge threshold, the bqTINY-II clears the fault and starts a new charge cycle. Toggling POR, \overline{CE} , or \overline{TTE} also clears the fault.

APPLICATION INFORMATION

THERMAL CONSIDERATIONS

The bqTINY-II is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled, *QFN/SON PCB Attachment Application Note* (TI Literature Number [SLUA271](#)).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad (5)$$

Where:

- T_J = device junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- whether or not the device is board mounted
- trace size, composition, thickness, and geometry
- orientation of the device (horizontal or vertical)
- volume of the ambient air surrounding the device under test and airflow_lus549
- whether other surfaces are in close proximity to the device being tested

The device power dissipation, P , is a function of the charge rate and the voltage drop across the internal power FET. It can be calculated from the following equation:

$$P = (V_{IN} - V_{I(BAT)}) \times I_{O(OUT)} \quad (6)$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See [Figure 2](#).

PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the output filter capacitors from OUT to VSS should be placed as close as possible to the bqTINY, with short trace runs to both signal and V_{SS} pins.
- All low-current V_{SS} connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small-signal ground path and the power-ground path.
- The BAT pin is the voltage feedback to the device. It should be connected with its trace as close to the battery pack as possible.
- The high-current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bqTINY-II is packaged in a thermally-enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (TI Literature No. [SLUA271](#)).

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| BQ24020DRRCR | ACTIVE | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | AZS | Samples |
| BQ24020DRCRG4 | ACTIVE | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | AZS | Samples |
| BQ24022DRRCR | ACTIVE | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | AZU | Samples |
| BQ24022DRCRG4 | ACTIVE | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | AZU | Samples |
| BQ24023DRRCR | NRND | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | AZV | |
| BQ24024DRRCR | ACTIVE | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | AZW | Samples |
| BQ24025DRRCR | NRND | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | AZX | |
| BQ24025DRCRG4 | NRND | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | AZX | |
| BQ24026DRRCR | NRND | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ANR | |
| BQ24027DRRCR | NRND | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ANS | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ24020DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24022DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24023DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |
| BQ24023DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24024DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24025DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24026DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| BQ24027DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

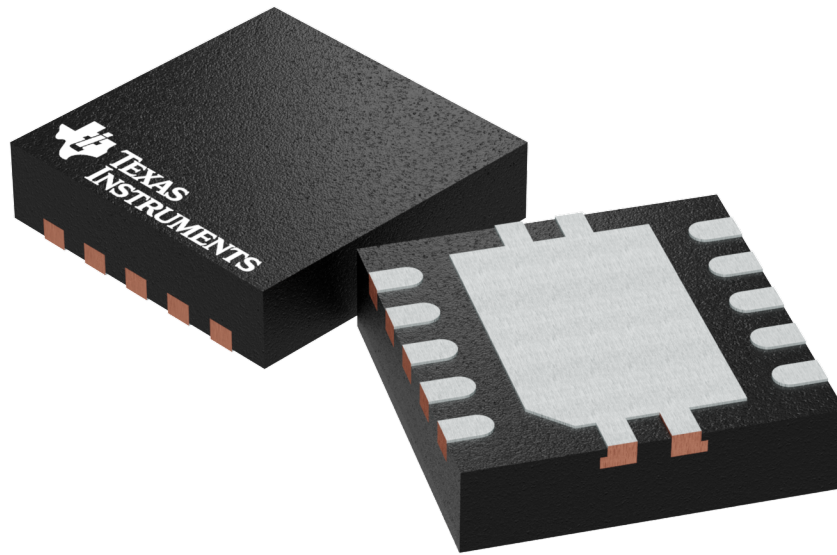
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ24020DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24022DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24023DRCR | VSON | DRC | 10 | 3000 | 370.0 | 355.0 | 55.0 |
| BQ24023DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24024DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24025DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24026DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ24027DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |

GENERIC PACKAGE VIEW

DRC 10

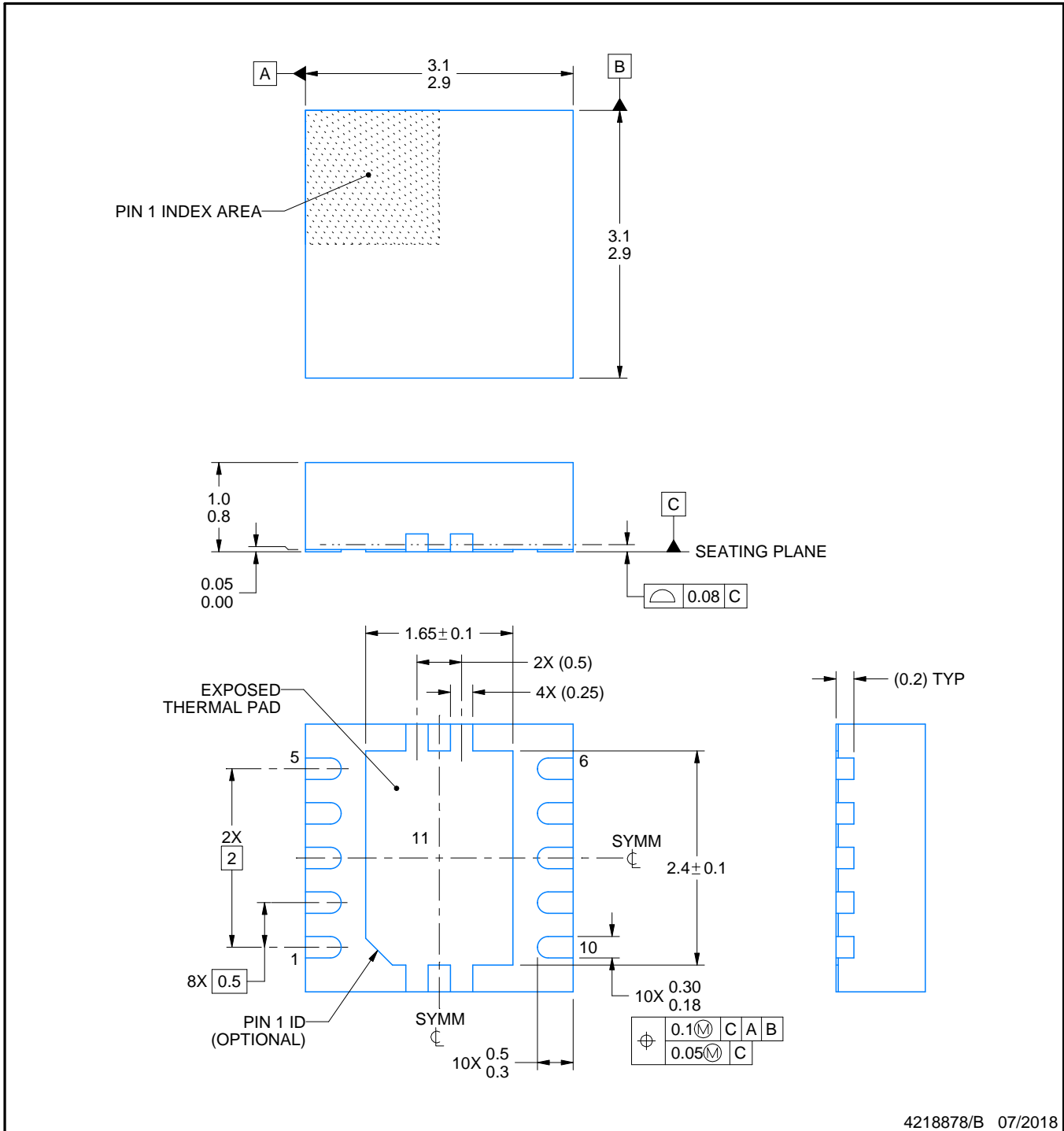
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204102-3/M



4218878/B 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View BQ24023DRCR](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management