



**THE DATASHEET OF
MT18HTF12872PY-667D2**



DDR2 SDRAM Registered DIMM (RDIMM)

MT18HTF6472 – 512MB

MT18HTF12872(P) – 1GB

MT18HTF25672(P) – 2GB

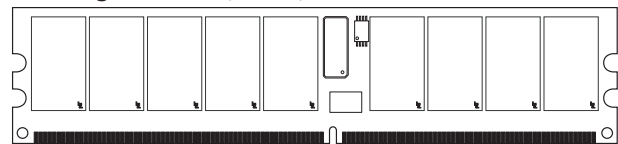
For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 240-pin, registered dual in-line memory module
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- Supports ECC error detection and correction
- VDD = VDDQ = +1.8V
- VDDSPD = +1.7V to +3.6V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Single rank
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 tCK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts

Figure 1: 240-Pin RDIMM (MO-237 R/C C-Non-Parity, R/C H-Parity)

PCB height: 30mm (1.18in)



Options

- Parity³
- Operating temperature¹
 - Commercial (0°C ≤ T_A ≤ +70°C)
 - Industrial (-40°C ≤ T_A ≤ +85°C)
- Package
 - 240-pin DIMM (Pb-free)
- Frequency/CAS latency²
 - 2.5ns @ CL = 5 (DDR2-800)³
 - 2.5ns @ CL = 6 (DDR2-800)³
 - 3.0ns @ CL = 5 (DDR2-667)³
 - 3.75ns @ CL = 4 (DDR2-533)
 - 5.0ns @ CL = 3 (DDR2-400)
- PCB height
 - 30mm (1.18in)

Marking

P
None
I
Y
-80E
-800
-667
-53E
-40E

- Notes: 1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
3. Not available in 512MB density.

Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | | t _{RCD} (ns) | t _{RP} (ns) | t _{RC} (ns) |
|-------------|-----------------------|------------------|--------|--------|--------|-----------------------|----------------------|----------------------|
| | | CL = 6 | CL = 5 | CL = 4 | CL = 3 | | | |
| -80E | PC2-6400 | – | 800 | 533 | – | 12.5 | 12.5 | 55 |
| -800 | PC2-6400 | 800 | 667 | 533 | – | 15 | 15 | 55 |
| -667 | PC2-5300 | – | 667 | 533 | 400 | 15 | 15 | 55 |
| -53E | PC2-4200 | – | – | 533 | 400 | 15 | 15 | 55 |
| -40E | PC2-3200 | – | – | 400 | 400 | 15 | 15 | 55 |



Table 2: Addressing

| | 512MB | 1GB | 2GB |
|---------------------------|--------------------|---------------------|-------------------|
| Refresh count | 8K | 8K | 8K |
| Row address | 8K (A0–A12) | 16K (A0–A13) | 16K (A0–A13) |
| Device bank address | 4 (BA0, BA1) | 4 (BA0, BA1) | 8 (BA0, BA1, BA2) |
| Device page size per bank | 1KB | 1KB | 1KB |
| Device configuration | 256Mb (64 Meg x 4) | 512Mb (128 Meg x 4) | 1Gb (256 Meg x 4) |
| Column address | 2K (A0–A9, A11) | 2K (A0–A9, A11) | 2K (A0–A9, A11) |
| Module rank address | 1 (S0#) | 1 (S0#) | 1 (S0#) |

Table 3: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT47H64M4,¹ 256Mb DDR2 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Latency (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|--|
| MT18HTF6472Y-53E__ | 512MB | 64 Meg x 72 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT18HTF6472Y-40E__ | 512MB | 64 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |

Table 4: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H128M4,¹ 512Mb DDR2 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Latency (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|--|
| MT18HTF12872(P)Y-80E__ | 1GB | 128 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT18HTF12872(P)Y-800__ | 1GB | 128 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT18HTF12872(P)Y-667__ | 1GB | 128 Meg x 72 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT18HTF12872(P)Y-53E__ | 1GB | 128 Meg x 72 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT18HTF12872(P)Y-40E__ | 1GB | 128 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |

Table 5: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT47H256M4,¹ 1Gb DDR2 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Latency (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|--|
| MT18HTF25672(P)Y-80E__ | 2GB | 256 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT18HTF25672(P)Y-800__ | 2GB | 256 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT18HTF25672(P)Y-667__ | 2GB | 256 Meg x 72 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |
| MT18HTF25672(P)Y-53E__ | 2GB | 256 Meg x 72 | 4.3 GB/s | 3.75ns/533 MT/s | 4-4-4 |
| MT18HTF25672(P)Y-40E__ | 2GB | 256 Meg x 72 | 3.2 GB/s | 5.0ns/400 MT/s | 3-3-3 |

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18HTF6472Y-667D2.



Pin Assignments and Descriptions

Table 6: Pin Assignments

| 240-Pin RDIMM Front | | | | | | | |
|---------------------|--------|-----------------|----------------|-----------------|---------------|-----|--------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | VREF | 31 | DQ19 | 61 | A4 | 91 | Vss |
| 2 | Vss | 32 | Vss | 62 | VDDQ | 92 | DQS5# |
| 3 | DQ0 | 33 | DQ24 | 63 | A2 | 93 | DQS5 |
| 4 | DQ1 | 34 | DQ25 | 64 | VDD | 94 | Vss |
| 5 | Vss | 35 | Vss | 65 | Vss | 95 | DQ42 |
| 6 | DQS0# | 36 | DQS3# | 66 | Vss | 96 | DQ43 |
| 7 | DQS0 | 37 | DQS3 | 67 | VDD | 97 | Vss |
| 8 | Vss | 38 | Vss | 68 ³ | NC/ PAR_IN | 98 | DQ48 |
| 9 | DQ2 | 39 | DQ26 | 69 | VDD | 99 | DQ49 |
| 10 | DQ3 | 40 | DQ27 | 70 | A10 | 100 | Vss |
| 11 | Vss | 41 | Vss | 71 | BA0 | 101 | SA2 |
| 12 | DQ8 | 42 | CB0 | 72 | VDDQ | 102 | NC |
| 13 | DQ9 | 43 | CB1 | 73 | WE# | 103 | Vss |
| 14 | Vss | 44 | Vss | 74 | CAS# | 104 | DQS6# |
| 15 | DQS1# | 45 | DQS8# | 75 | VDDQ | 105 | DQS6 |
| 16 | DQS1 | 46 | DQS8 | 76 | S1# | 106 | Vss |
| 17 | Vss | 47 | Vss | 77 | ODT1 | 107 | DQ50 |
| 18 | RESET# | 48 | CB2 | 78 | VDDQ | 108 | DQ51 |
| 19 | NC | 49 | CB3 | 79 | Vss | 109 | Vss |
| 20 | Vss | 50 | Vss | 80 | DQ32 | 110 | DQ56 |
| 21 | DQ10 | 51 | VDDQ | 81 | DQ33 | 111 | DQ57 |
| 22 | DQ11 | 52 | CKE0 | 82 | Vss | 112 | Vss |
| 23 | Vss | 53 | VDD | 83 | DQS4# | 113 | DQS7# |
| 24 | DQ16 | 54 ¹ | NC/BA2 | 84 | DQS4 | 114 | DQS7 |
| 25 | DQ17 | 55 ² | NC/ ERR_OUT | 85 | Vss | 115 | Vss |
| 26 | Vss | 56 | VDDQ | 86 | DQ34 | 116 | DQ58 |
| 27 | DQS2# | 57 | A11 | 87 | DQ35 | 117 | DQ59 |
| 28 | DQS2 | 58 | A7 | 88 | Vss | 118 | Vss |
| 29 | Vss | 59 | VDD | 89 | DQ40 | 119 | SDA |
| 30 | DQ18 | 60 | A5 | 90 | DQ41 | 120 | SCL |

| 240-Pin RDIMM Back | | | | | | | |
|--------------------|--------|-----|--------|------------------|--------|-----|--------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 121 | Vss | 151 | Vss | 181 | VDDQ | 211 | DQS14 |
| 122 | DQ4 | 152 | DQ28 | 182 | A3 | 212 | DQS14# |
| 123 | DQ5 | 153 | DQ29 | 183 | A1 | 213 | Vss |
| 124 | Vss | 154 | Vss | 184 | VDD | 214 | DQ46 |
| 125 | DQS9 | 155 | DQS12 | 185 | CK0 | 215 | DQ47 |
| 126 | DQS9# | 156 | DQS12# | 186 | CK0# | 216 | Vss |
| 127 | Vss | 157 | Vss | 187 | VDD | 217 | DQ52 |
| 128 | DQ6 | 158 | DQ30 | 188 | A0 | 218 | DQ53 |
| 129 | DQ7 | 159 | DQ31 | 189 | VDD | 219 | Vss |
| 130 | Vss | 160 | Vss | 190 | BA1 | 220 | RFU |
| 131 | DQ12 | 161 | CB4 | 191 | VDDQ | 221 | RFU |
| 132 | DQ13 | 162 | CB5 | 192 | RAS# | 222 | Vss |
| 133 | Vss | 163 | Vss | 193 | S0# | 223 | DQS15 |
| 134 | DQS10 | 164 | DQS17 | 194 | VDDQ | 224 | DQS15# |
| 135 | DQS10# | 165 | DQS17# | 195 | ODT0 | 225 | Vss |
| 136 | Vss | 166 | Vss | 196 ⁴ | NC/A13 | 226 | DQ54 |
| 137 | RFU | 167 | CB6 | 197 | VDD | 227 | DQ55 |
| 138 | RFU | 168 | CB7 | 198 | Vss | 228 | Vss |
| 139 | Vss | 169 | Vss | 199 | DQ36 | 229 | DQ60 |
| 140 | DQ14 | 170 | VDDQ | 200 | DQ37 | 230 | DQ61 |
| 141 | DQ15 | 171 | CKE1 | 201 | Vss | 231 | Vss |
| 142 | Vss | 172 | VDD | 202 | DQS13 | 232 | DQS16 |
| 143 | DQ20 | 173 | NC | 203 | DQS13# | 233 | DQS16# |
| 144 | DQ21 | 174 | NC | 204 | Vss | 234 | Vss |
| 145 | Vss | 175 | VDDQ | 205 | DQ38 | 235 | DQ62 |
| 146 | DQS11 | 176 | A12 | 206 | DQ39 | 236 | DQ63 |
| 147 | DQS11# | 177 | A9 | 207 | Vss | 237 | Vss |
| 148 | Vss | 178 | VDD | 208 | DQ44 | 238 | VDDSPD |
| 149 | DQ22 | 179 | A8 | 209 | DQ45 | 239 | SA0 |
| 150 | DQ23 | 180 | A6 | 210 | Vss | 240 | SA1 |

- Notes:
1. Pin 54 is NC for 512MB and 1GB or BA2 for 2GB.
 2. Pin 55 is NC for non-parity and ERR_OUT for parity.
 3. Pin 68 is NC for non-parity and PAR_IN for parity.
 4. Pin 196 is NC for 512MB or A13 for 1GB and 2GB.



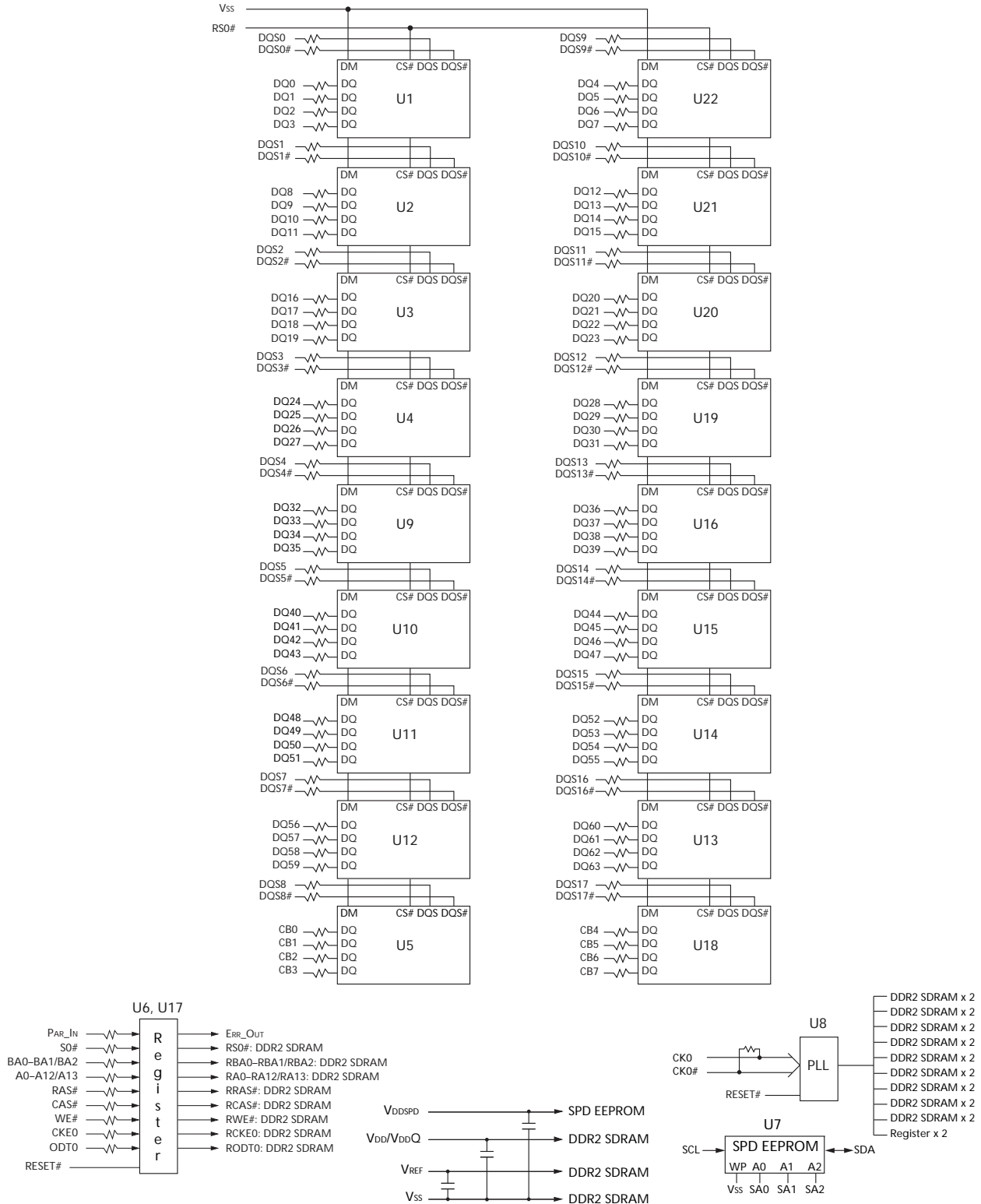
512MB, 1GB, 2GB (x72, ECC, SR) 240-Pin DDR2 SDRAM RDIMM Pin Assignments and Descriptions

Table 7: Pin Descriptions

| Symbol | Type | Description |
|--|---------------------|---|
| ODT0 | Input (SSTL_18) | On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and CB. The ODT input will be ignored if disabled via the LOAD MODE command. |
| CK0, CK0# | Input (SSTL_18) | Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#. |
| CKE0 | Input (SSTL_18) | Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. |
| S0# | Input (SSTL_18) | Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. |
| RAS#, CAS#, WE# | Input (SSTL_18) | Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| BA0, BA1 (512MB, 1GB) BA0, BA1, BA2 (2GB) | Input (SSTL_18) | Bank address inputs: BA0–BA1/BA2 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. |
| A0–A12 (512MB) A0–A13 (1GB, 2GB) | Input (SSTL_18) | Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. |
| PAR_IN | Input (SSTL_18) | Parity bit for the address and control bus. |
| SCL | Input | Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module. |
| SA0–SA2 | Input | Presence-detect address inputs: These pins are used to configure the presence-detect device. |
| RESET# | Input (LVCMOS) | Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQs are High-Z. |
| DQS0–DQS17, DQS0#–DQS17# | I/O (SSTL_18) | Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. |
| DQ0–DQ63 | I/O (SSTL_18) | Data input/output: Bidirectional data bus. |
| CB0–CB7 | I/O (SSTL_18) | Check bits. |
| SDA | I/O | Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. |
| ERR_OUT | Output (open drain) | Parity error found on the address and control bus. |
| VDD/VDDQ | Supply | Power supply: 1.8V ±0.1V. |
| VREF | Supply | SSTL_18 reference voltage. |
| VSS | Supply | Ground. |
| VDDSPD | Supply | Serial EEPROM positive power supply: +1.7V to +3.6V. |
| NC | – | No connect: These pins should be left unconnected. |
| DNU | – | Do not use. |

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT18HTF6472, MT18HTF12872(P), and MT18HTF25672(P) DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 512MB, 1GB, and 2GB memory modules organized in a x72 configuration. These DDR2 SDRAM modules use internally configured 4-bank (256Mb, 512Mb) or 8-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to VSS on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | |
|-----------------|---|------------|------|---------|-------------|
| VDD/VDDQ | VDD supply voltage relative to VSS | -0.5 | +2.3 | V | |
| VIN, VOUT | Voltage on any pin relative to VSS | -0.5 | +2.3 | V | |
| II | Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; VREF input $0V \leq V_{IN} \leq 0.95V$; (All other pins not under test = 0V) | -5 | +5 | μA | |
| | Command/address, RAS#, CAS#, WE#, S#, CKE, ODT, BA CK, CK# | -250 | +250 | | |
| IOZ | Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQs and ODT are disabled | -5 | +5 | μA | |
| IVREF | VREF leakage current; VREF = valid VREF level | -36 | +36 | μA | |
| TA | Module ambient operating temperature | Commercial | 0 | +70 | $^{\circ}C$ |
| | | Industrial | -40 | +85 | $^{\circ}C$ |
| TC ¹ | DDR2 SDRAM component case operating temperature ² | Commercial | 0 | +85 | $^{\circ}C$ |
| | | Industrial | -40 | +85 | $^{\circ}C$ |

- Notes: 1. The refresh rate is required to double when $85^{\circ}C < T_C \leq 95^{\circ}C$.
2. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades as shown in Table 9.

Table 9: Module and Component Speed Grades

| Module Speed Grade | Component Speed Grade |
|--------------------|-----------------------|
| -80E | -25E |
| -800 | -25 |
| -667 | -3 |
| -53E | -37E |
| -40E | -5E |

IDD Specifications

Table 10: DDR2 IDD Specifications and Conditions – 512MB

Values shown for MT47H64M4 DDR2 SDRAM only and are computed from values specified in the 256Mb (64 Meg x 4) component data sheet

| Parameter/Condition | Symbol | -53E | -40E | Units |
|---|-----------------------------|-----------------------------|-------|-------|
| Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} MIN (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD0 | 1,440 | 1,350 | mA |
| Operating one bank active-read-precharge current: $I_{OUT} = 0mA$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} MIN (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W | IDD1 | 1,620 | 1,530 | mA |
| Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | IDD2P | 90 | 90 | mA |
| Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | IDD2Q | 630 | 450 | mA |
| Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | IDD2N | 630 | 540 | mA |
| Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | 450 | 360 | mA |
| | | Slow PDN exit MR[12] = 1 | 108 | 108 |
| Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | IDD3N | 720 | 540 | mA |
| Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD4W | 2,880 | 2,250 | mA |
| Operating burst read current: All device banks open; Continuous burst reads; $I_{OUT} = 0mA$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD4R | 2,700 | 2,070 | mA |
| Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | IDD5 | 3,060 | 2,970 | mA |
| Self refresh current: CK and CK# at 0V; $CKE \leq 0.2V$; Other control and address bus inputs are floating; Data bus inputs are floating | IDD6 | 90 | 90 | mA |
| Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0mA$; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | IDD7 | 4,320 | 4,140 | mA |



Table 11: DDR2 IDD Specifications and Conditions – 1GB

Values shown for MT47H128M4 DDR2 SDRAM only and are computed from values specified in the 512Mb (128 Meg x 4) component data sheet

| Parameter/Condition | Symbol | -80E/ -800 | -667 | -53E | -40E | Units | |
|--|-----------------------------|-----------------------------|-------|-------|-------|-------|----|
| Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD0 | 1,800 | 1,620 | 1,440 | 1,440 | mA | |
| Operating one bank active-read-precharge current: $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W | IDD1 | 2,070 | 1,890 | 1,710 | 1,620 | mA | |
| Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | IDD2P | 126 | 126 | 126 | 126 | mA | |
| Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | IDD2Q | 900 | 810 | 720 | 630 | mA | |
| Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | IDD2N | 990 | 900 | 810 | 720 | mA | |
| Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | IDD3P | 720 | 630 | 540 | 450 | mA |
| | | Slow PDN exit MR[12] = 1 | 216 | 216 | 216 | 216 | mA |
| Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | IDD3N | 1,260 | 1,170 | 990 | 810 | mA | |
| Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD4W | 3,510 | 3,060 | 2,520 | 2,070 | mA | |
| Operating burst read current: All device banks open; Continuous burst reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD4R | 3,690 | 3,240 | 2,610 | 2,070 | mA | |
| Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | IDD5 | 4,140 | 3,240 | 3,060 | 2,970 | mA | |
| Self refresh current: CK and CK# at 0V; CKE $\leq 0.2\text{V}$; Other control and address bus inputs are floating; Data bus inputs are floating | IDD6 | 126 | 126 | 126 | 126 | mA | |
| Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | IDD7 | 5,400 | 4,320 | 4,050 | 3,960 | mA | |

Table 12: DDR2 IDD Specifications and Conditions (Die Revision A) – 2GB

Values shown for MT47H256M4 DDR2 SDRAM only and are computed from values specified in the 1Gb (256 Meg x 4) component data sheet

| Parameter/Condition | Symbol | -667 | -53E | -40E | Units |
|--|-----------------------------|-----------------------------|-------|-------|-------|
| Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD0 | 1,620 | 1,440 | 1,260 | mA |
| Operating one bank active-read-precharge current: $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W | IDD1 | 1,800 | 1,710 | 1,440 | mA |
| Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | IDD2P | 126 | 126 | 126 | mA |
| Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | IDD2Q | 990 | 738 | 630 | mA |
| Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | IDD2N | 1,080 | 810 | 720 | mA |
| Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | 720 | 540 | 450 | mA |
| | | Slow PDN exit MR[12] = 1 | 180 | 180 | 180 |
| Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | IDD3N | 1,260 | 990 | 810 | mA |
| Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD4W | 2,880 | 2,340 | 1,980 | mA |
| Operating burst read current: All device banks open; Continuous burst reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD4R | 2,880 | 2,610 | 1,980 | mA |
| Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | IDD5 | 4,680 | 4,500 | 3,960 | mA |
| Self refresh current: CK and CK# at 0V; CKE $\leq 0.2\text{V}$; Other control and address bus inputs are floating; Data bus inputs are floating | IDD6 | 126 | 126 | 126 | mA |
| Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | IDD7 | 5,400 | 5,220 | 4,680 | mA |



Table 13: DDR2 IDD Specifications and Conditions (Die Revision E) – 2GB

Values shown for MT47H256M4 DDR2 SDRAM only and are computed from values specified in the 1Gb (256 Meg x 4) component data sheet

| Parameter/Condition | Symbol | -80E/ -800 | -667 | -53E | -40E | Units | |
|--|-----------------------------|-----------------------------|-------|-------|-------|-------|----|
| Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD0 | 1,620 | 1,530 | 1,260 | 1,260 | mA | |
| Operating one bank active-read-precharge current: $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W | IDD1 | 1,980 | 1,800 | 1,710 | 1,620 | mA | |
| Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | IDD2P | 126 | 126 | 126 | 126 | mA | |
| Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | IDD2Q | 900 | 720 | 720 | 630 | mA | |
| Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | IDD2N | 900 | 720 | 720 | 630 | mA | |
| Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | IDD3P | 720 | 540 | 540 | 540 | mA |
| | | Slow PDN exit MR[12] = 1 | 180 | 180 | 180 | 180 | mA |
| Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | IDD3N | 1,080 | 990 | 810 | 720 | mA | |
| Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD4W | 2,880 | 2,430 | 2,250 | 1,890 | mA | |
| Operating burst read current: All device banks open; Continuous burst reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | IDD4R | 2,880 | 2,430 | 2,250 | 1,890 | mA | |
| Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | IDD5 | 4,230 | 3,870 | 3,780 | 3,690 | mA | |
| Self refresh current: CK and CK# at 0V; CKE $\leq 0.2\text{V}$; Other control and address bus inputs are floating; Data bus inputs are floating | IDD6 | 126 | 126 | 126 | 126 | mA | |
| Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | IDD7 | 6,030 | 5,040 | 4,860 | 4,680 | mA | |



Register and PLL Specifications

Table 14: Register Specifications
SSTU32866 devices or equivalent JESD82-16

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---|---------------------|---------------------------|---|----------------------------|----------------------------|-------|
| DC high-level input voltage | V _{IH(DC)} | Address, control, command | SSTL_18 | V _{REF(DC)} + 125 | V _{DDQ} + 250 | V |
| DC low-level input voltage | V _{IL(DC)} | Address, control, command | SSTL_18 | 0 | V _{REF(DC)} - 125 | V |
| AC high-level input voltage | V _{IH(AC)} | Address, control, command | SSTL_18 | V _{REF(DC)} + 250 | V _{DD} | V |
| AC low-level input voltage | V _{IL(AC)} | Address, control, command | SSTL_18 | 0 | V _{REF(DC)} - 250 | V |
| Output high voltage | V _{OH} | Parity output | LVC MOS | 1.2 | – | V |
| Output low voltage | V _{OL} | Parity output | LVC MOS | – | 0.5 | V |
| Input current | I _I | All pins | V _I = V _{DDQ} or V _{SSQ} | –5 | 5 | μA |
| Static standby | I _{DD} | All pins | RESET# = V _{SSQ} (I _O = 0) | – | 100 | μA |
| Static operating | I _{DD} | All pins | RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)} I _O = 0 | – | 40 | mA |
| Dynamic operating (clock tree) | I _{DDD} | n/a | RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _O = 0; CK and CK# switching 50% duty cycle | – | Varies by manufacturer | μA |
| Dynamic operating (per each input) | I _{DDD} | n/a | RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _O = 0; CK and CK# switching 50% duty cycle; One data input switching at ^t CK/2, 50% duty cycle | – | Varies by manufacturer | μA |
| Input capacitance (per device, per pin) | C _I | All inputs except RESET# | V _I = V _{REF} ±250mV; V _{DDQ} = 1.8V | 2.5 | 3.5 | pF |
| Input capacitance (per device, per pin) | C _I | RESET# | V _I = V _{DDQ} or V _{SSQ} | – | Varies by manufacturer | pF |

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

Table 15: PLL Specifications
CU877 device or equivalent JESD82-8.01

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---------------------------------------|---------------------|-----------------|---|------------------------------|------------------------------|-------|
| DC high-level input voltage | V _{IH} | RESET# | LVC MOS | 0.65 × V _{DD} | – | V |
| DC low-level input voltage | V _{IL} | RESET# | LVC MOS | – | 0.35 × V _{DD} | V |
| Input voltage (limits) | V _{IN} | RESET#, CK, CK# | | –0.3 | V _{DDQ} + 0.3 | V |
| DC high-level input voltage | V _{IH} | CK, CK# | Differential input | 0.65 × V _{DD} | – | V |
| DC low-level input voltage | V _{IL} | CK, CK# | Differential input | – | 0.35 × V _{DD} | mV |
| Input differential-pair cross voltage | V _{IX} | CK, CK# | Differential input | (V _{DDQ} /2) - 0.15 | (V _{DDQ} /2) + 0.15 | V |
| Input differential voltage | V _{ID(DC)} | CK, CK# | Differential input | 0.3 | V _{DDQ} + 0.4 | V |
| Input differential voltage | V _{ID(AC)} | CK, CK# | Differential input | 0.6 | V _{DDQ} + 0.4 | V |
| Input current | I _I | RESET# | V _I = V _{DDQ} or V _{SSQ} | –10 | 10 | μA |
| | | CK, CK# | V _I = V _{DDQ} or V _{SSQ} | –250 | 250 | μA |
| Output disabled current | I _{ODL} | | RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)} | 100 | – | μA |
| Static supply current | I _{DDLD} | | CK = CK# = LOW | – | 500 | μA |
| Dynamic supply | I _{DD} | n/a | CK, CK# = 270 MHz, all outputs open (not connected to PCB) | – | 300 | mA |
| Input capacitance | C _{IN} | Each input | V _I = V _{DDQ} or V _{SSQ} | 2 | 3 | pF |

Table 16: PLL Clock Driver Timing Requirements and Switching Characteristics

| Parameter | Symbol | Min | Max | Units |
|---|------------------|-----|-------|-------|
| Stabilization time | t _L | – | 15 | μs |
| Input clock slew rate | t _{LS1} | 1.0 | 4 | V/ns |
| SSC modulation frequency | | 30 | 33 | kHz |
| SSC clock input frequency deviation | | 0.0 | –0.50 | % |
| PLL loop bandwidth (–3dB from unity gain) | | 2.0 | – | MHz |

- Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Serial Presence-Detect

Table 17: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

| Parameter/Condition | Symbol | Min | Max | Units |
|---|--------------------|--------------------------|--------------------------|-------|
| Supply voltage | V _{DDSPD} | 1.7 | 3.6 | V |
| Input high voltage: Logic 1; All inputs | V _{IH} | V _{DDSPD} × 0.7 | V _{DDSPD} + 0.5 | V |
| Input low voltage: Logic 0; All inputs | V _{IL} | -0.6 | V _{DDSPD} × 0.3 | V |
| Output low voltage: I _{OUT} = 3mA | V _{OL} | - | 0.4 | V |
| Input leakage current: V _{IN} = GND to V _{DD} | I _{LI} | 0.10 | 3 | μA |
| Output leakage current: V _{OUT} = GND to V _{DD} | I _{LO} | 0.05 | 3 | μA |
| Standby current | I _{SB} | 1.6 | 4 | μA |
| Power supply current, READ: SCL clock frequency = 100 kHz | I _{CCR} | 0.4 | 1 | mA |
| Power supply current, WRITE: SCL clock frequency = 100 kHz | I _{CCW} | 2 | 3 | mA |

Table 18: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

| Parameter/Condition | Symbol | Min | Max | Units | Notes |
|---|---------------------|-----|-----|-------|-------|
| SCL LOW to SDA data-out valid | t ^{AA} | 0.2 | 0.9 | μs | 1 |
| Time the bus must be free before a new transition can start | t ^{BUF} | 1.3 | - | μs | |
| Data-out hold time | t ^{DH} | 200 | - | ns | |
| SDA and SCL fall time | t ^F | - | 300 | ns | 2 |
| Data-in hold time | t ^{HD:DAT} | 0 | - | μs | |
| Start condition hold time | t ^{HD:STA} | 0.6 | - | μs | |
| Clock HIGH period | t ^{HIGH} | 0.6 | - | μs | |
| Noise suppression time constant at SCL, SDA inputs | t ^I | - | 50 | ns | |
| Clock LOW period | t ^{LOW} | 1.3 | - | μs | |
| SDA and SCL rise time | t ^R | - | 0.3 | μs | 2 |
| SCL clock frequency | f ^{SCL} | - | 400 | kHz | |
| Data-in setup time | t ^{SU:DAT} | 100 | - | ns | |
| Start condition setup time | t ^{SU:STA} | 0.6 | - | μs | 3 |
| Stop condition setup time | t ^{SU:STO} | 0.6 | - | μs | |
| WRITE cycle time | t ^{WRC} | - | 10 | ms | 4 |

- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition, or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t^{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.



Table 19: Serial Presence-Detect Matrix

| Byte | Description | Entry (Version) | 512MB ¹ | 1GB | 2GB |
|------|--|---|-------------------------|----------------------------|----------------------------|
| 0 | Number of SPD bytes used by Micron | 128 | 80 | 80 | 80 |
| 1 | Total number of bytes in SPD device | 256 | 08 | 08 | 08 |
| 2 | Fundamental memory type | DDR2 SDRAM | 08 | 08 | 08 |
| 3 | Number of row addresses on SDRAM | 13, 14 | 0D | 0E | 0E |
| 4 | Number of column addresses on SDRAM | 10 | 0B | 0B | 0B |
| 5 | DIMM height and module ranks | 30mm, single rank | 60 | 60 | 60 |
| 6 | Module data width | 72 | 48 | 48 | 48 |
| 7 | Reserved | 0 | 00 | 00 | 00 |
| 8 | Module voltage interface levels | SSTL 1.8V | 05 | 05 | 05 |
| 9 | SDRAM cycle time, ^t CK (CL = MAX value, see byte 18) | -80E -800 -667 -53E -40E | - - - 3D 50 | 25 25 30 3D 50 | 25 25 30 3D 50 |
| 10 | SDRAM access from clock, ^t AC (CL = MAX value, see byte 18) | -80E/-800 -667 -53E -40E | - - 50 60 | 40 45 50 60 | 40 45 50 60 |
| 11 | Module configuration type | ECC ECC and parity | 02 06 | 02 06 | 02 06 |
| 12 | Refresh rate/type | 7.81µs/SELF | 82 | 82 | 82 |
| 13 | SDRAM device width (primary SDRAM) | 4 | 04 | 04 | 04 |
| 14 | Error-checking SDRAM data width | 4 | 04 | 04 | 04 |
| 15 | Reserved | 0 | 00 | 00 | 00 |
| 16 | Burst lengths supported | 4, 8 | 0C | 0C | 0C |
| 17 | Number of banks on SDRAM device | 4 or 8 | 04 | 04 | 08 |
| 18 | CAS latencies supported | -80E (5, 4) -800 (6, 5, 4) -667 (5, 4, 3) -53E/-40E (4, 3) | - - - 18 | 30 70 38 18 | 30 70 38 18 |
| 19 | Module thickness | | 01 | 01 | 01 |
| 20 | DDR2 DIMM type | Registered DIMM | 01 | 01 | 01 |
| 21 | SDRAM module attributes | 1 PLL, 2 Reg | 05 | 05 | 05 |
| 22 | SDRAM device attributes: weak driver (01), or weak driver and 50Ω ODT (03) | -80E/-800/-667 -53E/-40E | - 01 | 03 01 | 03 01 |
| 23 | SDRAM cycle time, ^t CK, MAX CL - 1 | -80E/-667 -800 -53E/-40E | - - 50 | 3D 30 50 | 3D 30 50 |
| 24 | SDRAM access from CK, ^t AC, MAX CL - 1 | -80E/-800 -667 -53E -40E | - - 50 60 | 40 45 50 60 | 40 45 50 60 |
| 25 | SDRAM cycle time, ^t CK, MAX CL - 2 | -80E/-800 -667 -53E/-40E | - - 00 | 3D/00 50 00 | 3D/00 50 00 |
| 26 | SDRAM access from CK, ^t AC, MAX CL - 2 | -80E/-800 -667 -53E/-40E | - - 00 | 40/00 45 00 | 40/00 45 00 |



Table 19: Serial Presence-Detect Matrix (continued)

| Byte | Description | Entry (Version) | 512MB ¹ | 1GB | 2GB |
|------|--|-----------------------------------|--------------------|----------------------|----------------------|
| 27 | MIN row precharge time, ^t RP | -80E -800/-667 -53E/-40E | - - 3C | 32 3C 3C | 32 3C 3C |
| 28 | MIN row active-to-row active, ^t RRD | - | 1E | 1E | 1E |
| 29 | MIN RAS#-to-CAS# delay, ^t RCD | -80E -800/-667 -53E/-40E | - - 3C | 32 3C 3C | 32 3C 3C |
| 30 | MIN active-to-precharge, ^t RAS | -80E/-800 -667/-53E -40E | - -2D 28 | 2D 2D 28 | 2D 2D 28 |
| 31 | Module rank density | 512MB, 1GB, 2GB | 80 | 01 | 02 |
| 32 | Address and command setup time, ^t IS _b | -80E/-800 -667 -53E -40E | - - 25 35 | 17 20 25 35 | 17 20 25 35 |
| 33 | Address and command hold time, ^t IH _b | -80E/-800 -667 -53E -40E | - - 37 47 | 25 27 37 47 | 25 27 37 47 |
| 34 | Data/data mask input setup time, ^t DS _b | -80E/-800 -667/-53E -40E | - -10 15 | 05 10 15 | 05 10 15 |
| 35 | Data/data mask input hold time, ^t DH _b | -80E/-800 -667 -53E -40E | - - 22 27 | 12 17 22 27 | 12 17 22 27 |
| 36 | Write recovery time, ^t WR | - | 3C | 3C | 3C |
| 37 | WRITE-to-READ command delay, ^t WTR | -80E/-667/-53E -800/-40E | -/-1E 28 | 1E 28 | 1E 28 |
| 38 | READ-to-PRECHARGE command delay, ^t RTP | - | 1E | 1E | 1E |
| 39 | Memory analysis probe | - | 00 | 00 | 00 |
| 40 | Extension for bytes 41 and 42 | -80E -800/-667 -53E/-40E | - 00 00 | 30 00 00 | 36 06 06 |
| 41 | MIN active-to-active/refresh time, ^t RC ² | -80E -800/-667/-53E -40E | - -/-3C 37 | 39 3C 37 | 39 3C 37 |
| 42 | MIN AUTO REFRESH-to-ACTIVE/ AUTO REFRESH command period, ^t RFC | | 4B | 69 | 7F |
| 43 | SDRAM device MAX cycle time, ^t CK (MAX) | | 80 | 80 | 80 |
| 44 | SDRAM device MAX DQS-DQ skew time, ^t DQSQ | -80E/-800 -667 -53E -40E | - - 1E 23 | 14 18 1E 23 | 14 18 1E 23 |
| 45 | SDRAM device MAX read data hold skew factor, ^t QHS | -80E/-800 -667 -53E -40E | - - 28 2D | 1E 22 28 2D | 1E 22 28 2D |
| 46 | PLL relock time | | 0F | 0F | 0F |



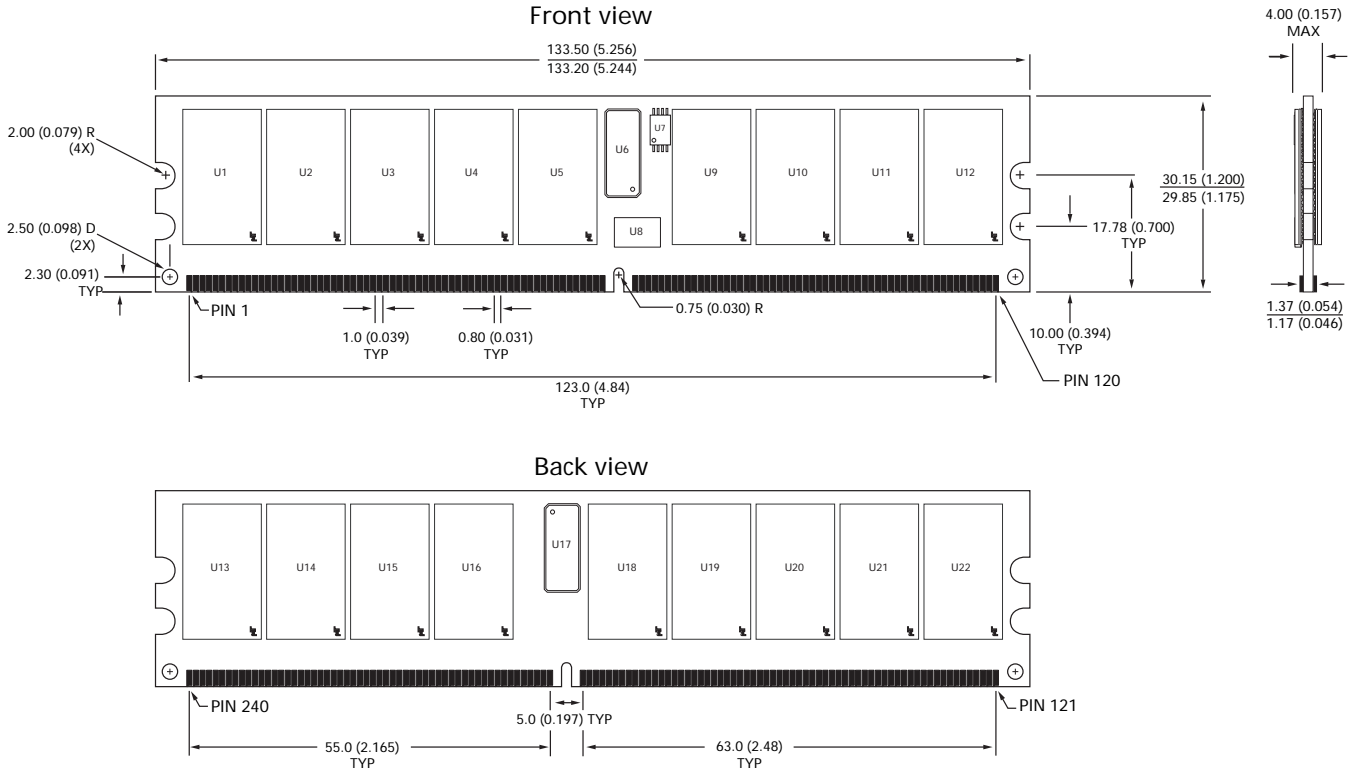
Table 19: Serial Presence-Detect Matrix (continued)

| Byte | Description | Entry (Version) | 512MB ¹ | 1GB | 2GB |
|---------|---|--------------------------------------|-------------------------------|---|--|
| 47–61 | Optional features, not supported | | 00 | 00 | 00 |
| 62 | SPD revision | Release 1.2 | 12 | 12 | 12 |
| 63 | Checksum for bytes 0–62 ECC/ECC and parity | -80E -800 -667 -53E -40E | - - - F5/F9 5C/60 | 2E/32 CF/D3 EA/EE 95/99 FC/00 | 4F/53 F0/F4/ 0B/0F B6/BA 1D/21 |
| 64 | Manufacturer's JEDEC ID code | MICRON | 2C | 2C | 2C |
| 65–71 | Manufacturer's JEDEC ID code | (continued) | FF | FF | FF |
| 72 | Manufacturing location | 1–12 | 01–0C | 01–0C | 01–0C |
| 73–90 | Module part number (ASCII) | – | Variable data | Variable data | Variable data |
| 91 | PCB identification code | 1–9 | 01–09 | 01–09 | 01–09 |
| 92 | Identification code (continued) | 0 | 00 | 00 | 00 |
| 93 | Year of manufacture in BCD | – | Variable data | Variable data | Variable data |
| 94 | Week of manufacture in BCD | – | Variable data | Variable data | Variable data |
| 95–98 | Module serial number | – | Variable data | Variable data | Variable data |
| 99–127 | Reserved for manufacturer-specific data | | 00 | 00 | 00 |
| 128–255 | Reserved for customer-specific data | | FF | FF | FF |

- Notes: 1. The 512MB module is not available in -80E, -800, or -667 speed grades.
2. The ^tRC SPD values shown are JEDEC DDR2 device specification values. The actual Micron DDR2 device specification is ^tRC = 55ns for all speed grades.

Module Dimensions

Figure 3: 240-Pin DDR2 RDIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.



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